CMOS Digital Integrated Circuits Silicon Monolithic

74HC4053D

1. Functional Description

• Triple 2-Channel Analog Multiplexer/Demultiplexer

2. General

The 74HC4053D are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC4053D has a 2 channel \times 3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal (V_{CC} - V_{EE}) can then be switched by the small logical amplitude (V_{CC} - GND) control signal.

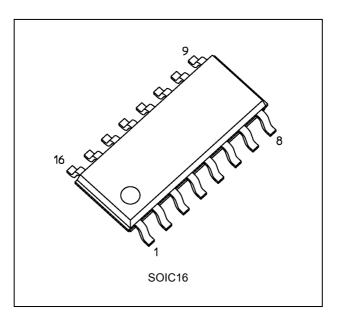
For example, in the case of V_{CC} = 5 V, GND = 0 V, V_{EE} = -5 V, signals between -5 V and +5 V can be switched from the logical circuit with a single power supply of 5 V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

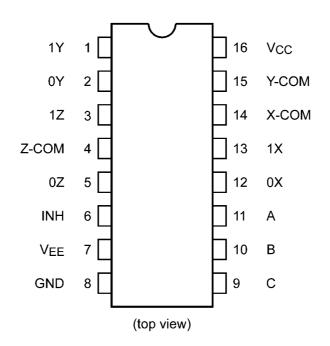
- (1) Low power dissipation: I_{CC} = 4.0 μ A (max) (V_{CC} = 6.0 V, V_{EE} = GND, T_a = 25 °C)
- (2) High noise immunity: $V_{\rm NIH} = V_{\rm NIL} = 28\% V_{\rm CC}$ (min)
- (3) Low ON-resistance: R_{ON} = 50 Ω (typ.) at V_{CC} V_{EE} = 9 V
- (4) High noise immunity: THD = 0.020 % (typ.) at V_{CC} V_{EE} = 9 V
- (5) Pin and function compatible with 4053B

4. Packaging

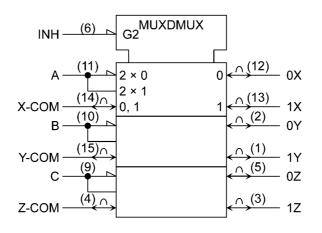


5. Pin Assignment

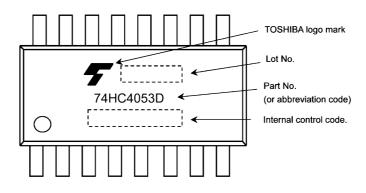
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6. IEC Logic Symbol

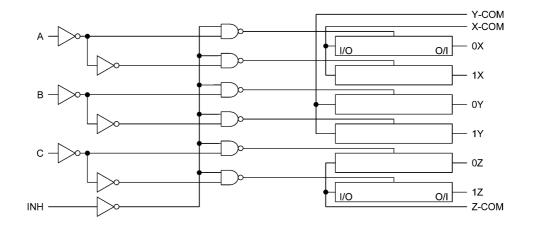


7. Marking



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8. System Diagram



9. Truth Table

Input Inhibit	Input C	Input B	Input A	ON Channel
L	L	L	L	0X, 0Y, 0Z
L	L	L	Н	1X, 0Y, 0Z
L	L	Н	L	0X, 1Y, 0Z
L	L	Н	Н	1X, 1Y, 0Z
L	н	L	L	0X, 0Y, 1Z
L	н	L	Н	1X, 0Y, 1Z
L	Н	Н	L	0X, 1Y, 1Z
L	н	н	Н	1X, 1Y, 1Z
Н	х	х	х	None

X: Don't care

10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to 7.0	V
	V _{EE}	-7.0 to 0	
	V _{CC} -V _{EE}	-0.5 to 13.0	
Input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
Switch I/O voltage	V _{I/O}	V _{EE} - 0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
I/O diode current	I _{I/OK}	±20	mA
Switch through current	Ι _Τ	±25	mA
V _{CC} /ground current	I _{CC}	±50	mA
Power dissipation	PD	500	mW
Storage temperature	T _{stg}	-65 to 150	C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

11. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 6.0	V
	V _{EE}	-6.0 to 0	
	V _{CC} -V _{EE}	2.0 to 12.0	
Input voltage	V _{IN}	0 to V _{CC}	V
Switch I/O voltage	V _{I/O}	V _{EE} to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall times	t _r ,t _f	0 to 50	μS

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

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12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition	V _{EE} (V)	V _{CC} (V)	Min	Тур.	Max	Unit
High-level input voltage	VIH	—		2.0	1.50	_	_	V
				4.5	3.15		—	
				6.0	4.20	—	_	
Low-level input voltage	V _{IL}	—		2.0	_		0.50	V
				4.5		—	1.35	
				6.0		_	1.80	
ON-resistance	R _{ON}		GND	4.5		85	180	Ω
			-4.5	4.5		55	120	
			-6.0	6.0		50	100	
		$\label{eq:VIN} \begin{array}{l} V_{IN} = V_{IH} \mbox{ or } V_{IL} \\ V_{I/O} = V_{CC} \mbox{ or } V_{EE} \\ I_{I/O} \leq 2 \mbox{ mA} \end{array}$	GND	2.0	_	150	_	
			GND	4.5	_	70	150	
			-4.5	4.5	_	50	100	
			-6.0	6.0	_	45	80	
Difference of ON-resistance	ΔR _{ON}		GND	4.5	_	10	30	Ω
between switches			-4.5	4.5	_	5	12	
			-6.0	6.0	_	5	10	
Input/Output leakage current	I _{OFF}	$V_{OS} = V_{CC}$ or GND	GND	6.0	_		±0.06	μA
(Switch OFF)		V_{IS} = GND or V_{CC} V_{IN} = V_{IH} or V_{IL}	-6.0	6.0		_	±0.1	
Input/Output leakage current	I _{I/O}	V _{OS} = V _{CC} or GND	GND	6.0	_	—	±0.06	μA
(Switch ON)		$V_{IN} = V_{IH} \text{ or } V_{IL}$	-6.0	6.0	_	—	±0.1	
Control input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	GND	6.0	_	_	±0.1	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	GND	6.0	_		4.0	μA
			-6.0	6.0			8.0	

12.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition	V _{EE} (V)	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	—	·	2.0	1.50	_	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V _{IL}	—		2.0		0.50	
				4.5		1.35	
				6.0		1.80	
ON-resistance	R _{ON}		GND	4.5		225	Ω
			-4.5	4.5		150	
			-6.0	6.0	_	125]
		$\label{eq:VIN} \begin{array}{l} V_{IN} = V_{IH} \text{ or } V_{IL} \\ V_{I/O} = V_{CC} \text{ or } V_{EE} \\ I_{I/O} \leq 2 \ mA \end{array}$	GND	2.0	_	—	
			GND	4.5	_	190	
			-4.5	4.5	_	125	
			-6.0	6.0	_	100	
Difference of ON-resistance	ΔR_{ON}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{I/O} = V_{CC} \text{ to } V_{EE}$ $I_{I/O} \le 2 \text{ mA}$	GND	4.5		35	Ω
between switches			-4.5	4.5		15	
		1∥0 ≤ 2 mA	-6.0	6.0	_	12	
Input/Output leakage current	I _{OFF}	$V_{OS} = V_{CC} \text{ or GND}$ $V_{IS} = GND \text{ or } V_{CC}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	GND	6.0	_	±0.6	μA
(Switch OFF)			-6.0	6.0	_	±1.0	
Input/Output leakage current	I _{I/O}	V _{OS} = V _{CC} or GND	GND	6.0		±0.6	μA
(Switch ON)		$V_{IN} = V_{IH} \text{ or } V_{IL}$	-6.0	6.0		±1.0	
Control input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	GND	6.0		±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	GND	6.0	_	40.0	μA
			-6.0	6.0	_	80.0	

12.3. AC Characteristics (Unless otherwise specified, $C_L = 50 \text{ pF}$, $T_a = 25 \text{ °C}$, Input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	V _{EE} (V)	V _{CC} (V)	Min	Тур.	Max	Unit
Phase difference between input	Φι/Ο	—	GND	2.0		25	60	ns
to output			GND	4.5		6	12	
			GND	6.0		5	10	
			-4.5	4.5	_	4	_	
Output enable time	t _{PZL} ,t _{PZH}	R _L = 1 kΩ Figure 1	GND	2.0	_	50	225	ns
			GND	4.5	_	14	45	
			GND	6.0	_	12	38	
			-4.5	4.5	_	14	_	
Output disable time	t _{PLZ} ,t _{PHZ}	$R_L = 1 k\Omega$ Figure 1	GND	2.0	_	95	225	ns
			GND	4.5	_	30	45	
			GND	6.0	_	26	38	
			-4.5	4.5	_	26	_	
Control input capacitance	C _{IN}	_	_	_	_	5	10	pF
Common terminal capacitance	C _{IS}	Figure 2	-5.0	5.0	_	11	20	pF
Switch terminal capacitance	C _{OS}	Figure 2	-5.0	5.0	_	7	15	pF
Feedthrough capacitance	C _{IOS}	Figure 2	-5.0	5.0	_	0.75	2	pF
Power dissipation capacitance	C _{PD}	Figure 2 (Note 1)	GND	5.0	_	10	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

12.4. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = -40 to 85 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{EE} (V)	V _{CC} (V)	Min	Max	Unit
Phase difference between input to	φι/ο	—	GND	2.0	_	75	ns
output			GND	4.5	_	15	
			GND	6.0	_	13	
			-4.5	4.5	_	_	
Output enable time	t _{PZL} ,t _{PZH}	R _L = 1 kΩ Figure 1	GND	2.0	_	280	ns
			GND	4.5	_	56	
			GND	6.0	_	48	
			-4.5	4.5	_	_	
Output disable time	t _{PLZ} ,t _{PHZ}	R _L = 1 kΩ Figure 1	GND	2.0	_	280	ns
			GND	4.5	_	56	
			GND	6.0	_	48	
			-4.5	4.5	_	_	
Control input capacitance	C _{IN}	_	_	_	_	10	pF
Common terminal capacitance	CIS	Figure 2	-5.0	5.0	_	20	pF
Switch terminal capacitance	C _{OS}	Figure 2	-5.0	5.0	_	15	pF
Feedthrough capacitance	C _{IOS}	Figure 2	-5.0	5.0	—	2	pF

12.5. Analog Switch Characteristics (T_a = 25 °C) (Note)

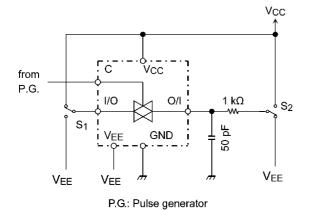
Characteristics	Symbol	Test Condition		V _{EE} (V)	V _{CC} (V)	Тур.	Unit
Sine Wave Distortion	THD	R_L = 10 kΩ, C_L = 50 pF	V _{IN} = 4.0 V _{p-p}	-2.25	2.25	0.025	%
		f _{IN} = 1 kHz	V _{IN} = 8.0 V _{p-p}	-4.5	4.5	0.020	
			V _{IN} = 11.0 V _{p-p}	-6.0	6.0	0.018	
Maximum frequency	f _{MAX(I/O)}	(I/O) Adjust f _{IN} voltage to obtain 0 dBm ((Note 1)	-2.25	2.25	120	MHz
response		at V _{OS} Increase f _{IN} frequency until dB	(Note 2)			95	
	meter reads -3 dB $R_L = 50 \Omega$, $C_L = 10 pF$ $f_{ N} = 1 MHz$, sine wave Figure 3	(Note 1)	-4.5	4.5	190		
			(Note 2)			150	
		(Note 1)	-6.0	6.0	200		
		ş	(Note 2)			190	
Feed through attenuation	FTH	V_{IN} is centered at ($V_{CC} - V_{EE}$)/2		-2.25	2.25	-50	dB
(switch OFF)		Adjust input for 0 dBm. $R_L = 600 \Omega$, $C_L = 50 pF$,		-4.5	4.5	-50	
		f _{IN} = 1 MHz, sine wave Figure 4		-6.0	6.0	-50	
Crosstalk (control input to	X _{talk}	R _L = 600 Ω, C _L = 50 pF,		-2.25	2.25	60	mV
signal output)		$f_{IN} = 1 \text{ MHz},$ square wave ($t_r = t_f = 6 \text{ ns}$)		-4.5	4.5	140	
		Figure 5		-6.0	6.0	200	
Crosstalk (between any switches)	X _{talk}	Adjust V _{IN} to obtain 0 dBm at		-2.25	2.25	-50	dB
switches)		input. R _L = 600 Ω, C _L = 50 pF,		-4.5	4.5	-50	
		f _{IN} = 1 MHz, sine wave Figure 6		-6.0	6.0	-50	

Note: These characteristics are determined by design of devices.

Note 1: Input COMMON terminal, and measured at SWITCH terminal.

Note 2: Input SWITCH terminal, and measured at COMMON terminal.

13. AC Test Circuit



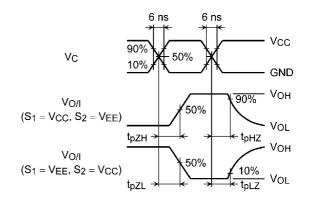


Figure 1 tPLZ, tPHZ, tPZL, tPZH

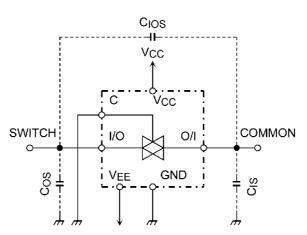


Figure 2 C_{IOS}, C_{IS}, C_{OS}

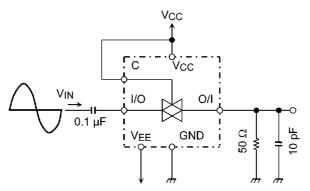


Figure 3 Frequency Response

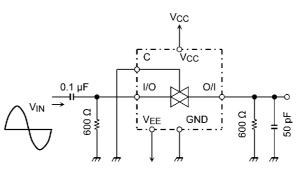
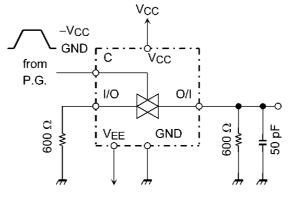


Figure 4 Feedthrough Attenuation



P.G.: Pulse generator

Figure 5 Cross Talk (control input to output signal)

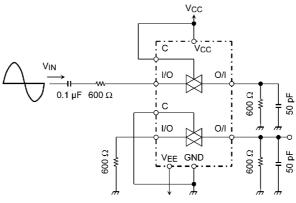


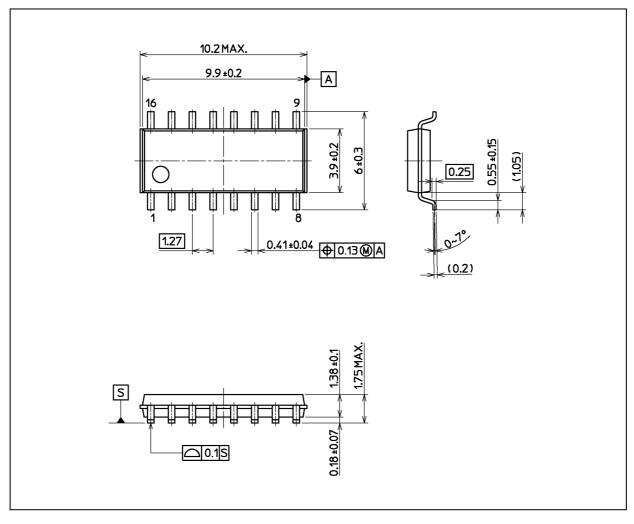
Figure 6 Cross Talk (between any two switches)



Package Dimensions

74HC4053D

Unit: mm



Weight: 0.15 g (typ.)

Package Name(s)
Nickname: SOIC16

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