



PCF85063A

Tiny Real-Time Clock/calendar with alarm function and I²C-bus

Rev. 7 — 30 March 2018

Product data sheet

1. General description

The PCF85063A is a CMOS¹ Real-Time Clock (RTC) and calendar optimized for low power consumption. An offset register allows fine-tuning of the clock. All addresses and data are transferred serially via the two-line bidirectional I²C-bus. Maximum data rate is 400 kbit/s. The register address is incremented automatically after each written or read data byte.

For a selection of NXP Real-Time Clocks, see [Table 45 on page 56](#)

2. Features and benefits

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Clock operating voltage: 0.9 V to 5.5 V
- Low current; typical 0.22 μ A at $V_{DD} = 3.3$ V and $T_{amb} = 25$ °C
- 400 kHz two-line I²C-bus interface (at $V_{DD} = 1.8$ V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Selectable integrated oscillator load capacitors for $C_L = 7$ pF or $C_L = 12.5$ pF
- Alarm function
- Countdown timer
- Minute and half minute interrupt
- Oscillator stop detection function
- Internal Power-On Reset (POR)
- Programmable offset register for frequency adjustment

3. Applications

- Digital still camera
- Digital video camera
- Printers
- Copy machines
- Mobile equipment
- Battery powered devices

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 21](#).



4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|------------|--|-----------|
| | Name | Description | Version |
| PCF85063AT | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| PCF85063ATL | DFN2626-10 | plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 × 2.6 × 0.5 mm | SOT1197-1 |
| PCF85063ATT | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |

4.1 Ordering options

Table 2. Ordering options

| Product type number | Orderable part number | Sales item (12NC) | Delivery form | IC revision |
|---------------------|-----------------------|-------------------|----------------------------------|-------------|
| PCF85063AT/A | PCF85063AT/AY | 935303639518 | tape and reel, 13 inch, dry pack | 1 |
| | PCF85063AT/AAZ | 935303639515 | tape and reel, 7 inch, dry pack | 1 |
| PCF85063ATL/1 | PCF85063ATL/1,118 | 935299022118 | tape and reel, 7 inch | 1 |
| PCF85063ATT/A | PCF85063ATT/AJ | 935304639118 | tape and reel, 13 inch | 1 |

5. Marking

Table 3. Marking codes

| Product type number | Marking code |
|---------------------|--------------|
| PCF85063AT/A | 85063A |
| PCF85063ATL/1 | 063A |
| PCF85063ATT/A | 063A |

6. Block diagram

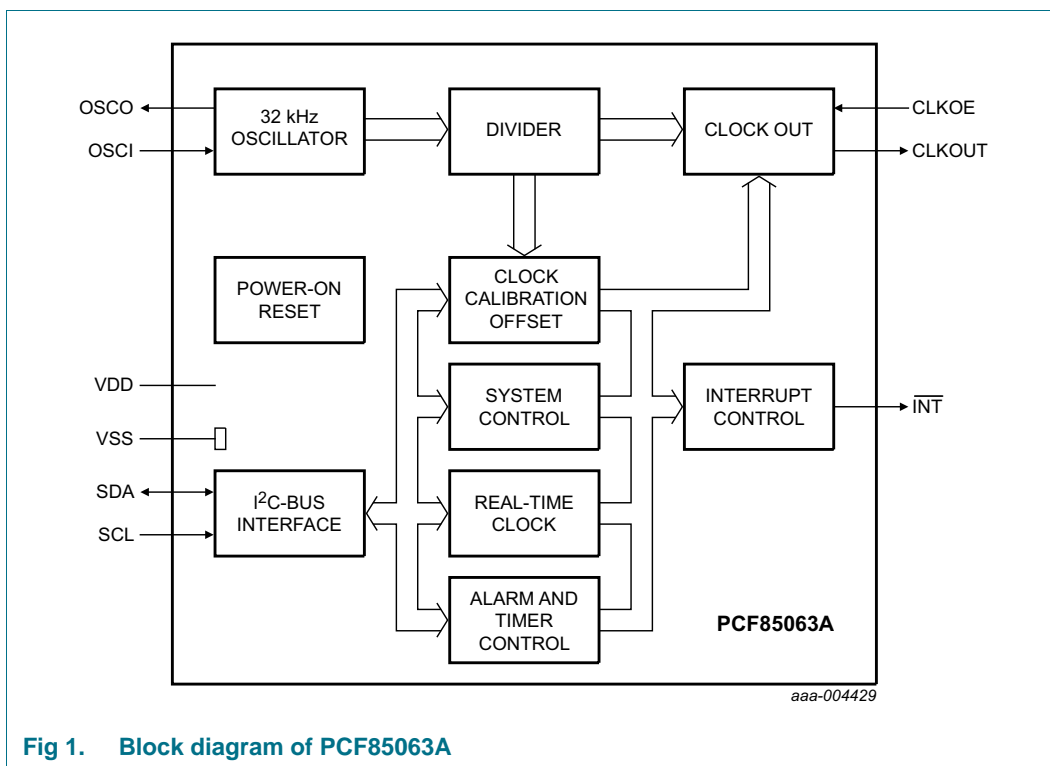
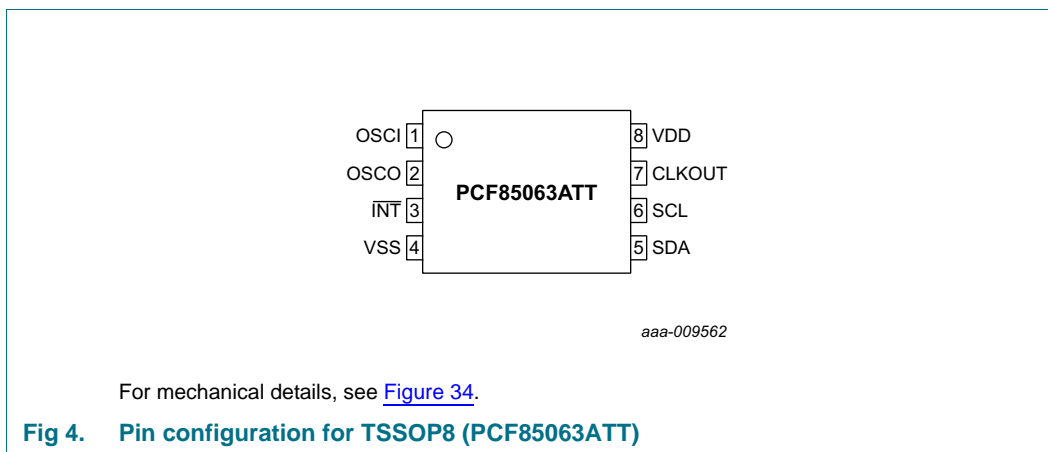
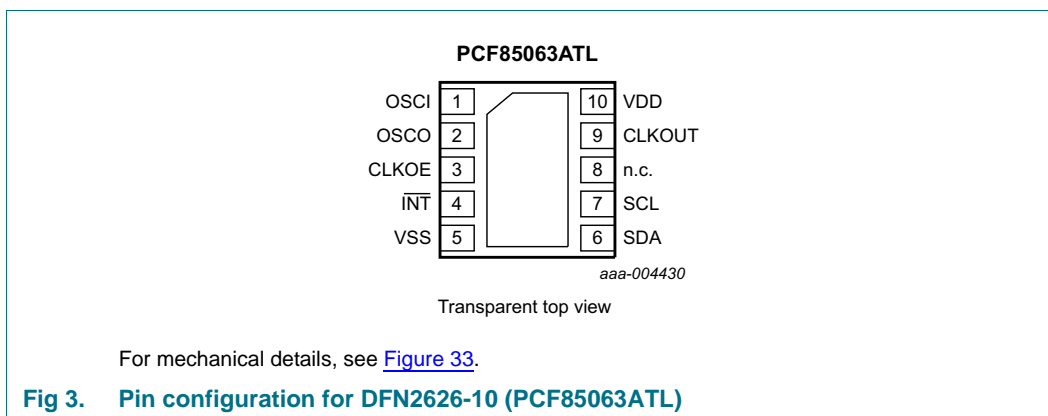
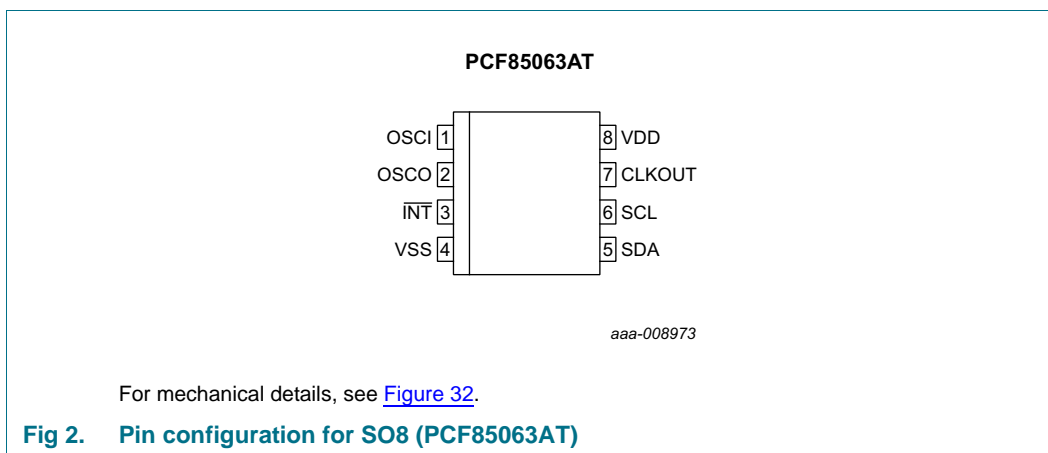


Fig 1. Block diagram of PCF85063A

7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

| Symbol | Pin | | | Type | Description |
|--|------------|------------------|-------------|--------------|---|
| | PCF85063AT | PCF85063ATL | PCF85063ATT | | |
| OSCI | 1 | 1 | 1 | input | oscillator input |
| OSCO | 2 | 2 | 2 | output | oscillator output |
| CLKOE ^[2] | - | 3 | - | input | CLKOUT enable or disable pin; enable is active HIGH |
| $\overline{\text{INT}}$ ^[2] | 3 | 4 | 3 | output | interrupt output (open-drain) |
| VSS | 4 | 5 ^[1] | 4 | supply | ground supply voltage |
| SDA ^[2] | 5 | 6 | 5 | input/output | serial data line |
| SCL ^[2] | 6 | 7 | 6 | input | serial clock input |
| n.c. | - | 8 | - | - | not connected |
| CLKOUT | 7 | 9 | 7 | output | clock output (push-pull) |
| VDD | 8 | 10 | 8 | supply | supply voltage |

- [1] The die paddle (exposed pad) is connected to V_{SS} through high ohmic (non-conductive) silicon attach and should be electrically isolated. It is good engineering practice to solder the exposed pad to an electrically isolated PCB copper pad as shown in [Figure 37](#) "Footprint information for reflow soldering of SOT1197-1 (DFN2626-10) of PCF85063ATL" for better heat transfer but it is not required as the RTC doesn't consume much power. In no case should traces be run under the package exposed pad.
- [2] NXP recommends tying VDD of the device and VDD of all the external pull-up resistors to the same Power Supply.

8. Functional description

The PCF85063A contains 18 8-bit registers with an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calendar, and an I²C-bus interface with a maximum data rate of 400 kbit/s.

The built-in address register will increment automatically after each read or write of a data byte up to the register 11h. After register 11h, the auto-incrementing will wrap around to address 00h (see [Figure 5](#)).

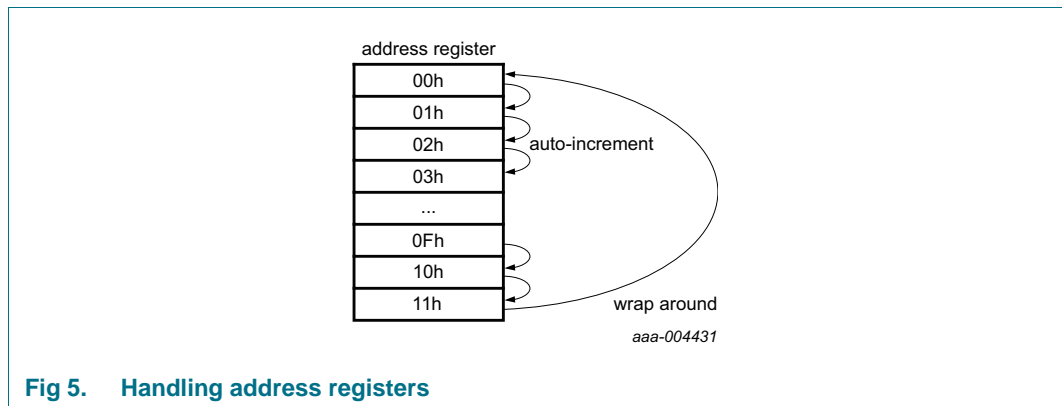


Fig 5. Handling address registers

All registers (see [Table 5](#)) are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and status register. The register at address 02h is an offset register allowing the fine-tuning of the clock; and at 03h is a free RAM byte. The addresses 04h through 0Ah are used as counters for the clock function (seconds up to years counters). Address locations 0Bh through 0Fh contain alarm registers which define the conditions for an alarm. The registers at 10h and 11h are for the timer function.

The Seconds, Minutes, Hours, Days, Months, and Years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all time counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented. For details on maximum access time, see [Section 8.4 on page 25](#).

8.1 Registers organization

Table 5. Registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to [Table 8 on page 12](#).

| Address | Register name | Bit | | | | | | | | Reference | |
|------------------------------|---------------|-----------------|------------------------|--------------------------------------|--------------------------------------|----|------------------------|-------|---------|-------------------------------|-------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Control and status registers | | | | | | | | | | | |
| 00h | Control_1 | EXT_TEST | - | STOP | SR | - | CIE | 12_24 | CAP_SEL | Section 8.2.1 | |
| 01h | Control_2 | AIE | AF | MI | HMI | TF | COF[2:0] | | | Section 8.2.2 | |
| 02h | Offset | MODE | OFFSET[6:0] | | | | | | | | Section 8.2.3 |
| 03h | RAM_byte | B[7:0] | | | | | | | | Section 8.2.4 | |
| Time and date registers | | | | | | | | | | | |
| 04h | Seconds | OS | SECONDS (0 to 59) | | | | | | | | Section 8.3.1 |
| 05h | Minutes | - | MINUTES (0 to 59) | | | | | | | | Section 8.3.2 |
| 06h | Hours | - | - | AMPM | HOURS (1 to 12) in 12-hour mode | | | | | Section 8.3.3 | |
| | | | | HOURS (0 to 23) in 24-hour mode | | | | | | | |
| 07h | Days | - | - | DAYS (1 to 31) | | | | | | Section 8.3.4 | |
| 08h | Weekdays | - | - | - | - | - | WEEKDAYS (0 to 6) | | | Section 8.3.5 | |
| 09h | Months | - | - | - | MONTHS (1 to 12) | | | | | | Section 8.3.6 |
| 0Ah | Years | YEARS (0 to 99) | | | | | | | | Section 8.3.7 | |
| Alarm registers | | | | | | | | | | | |
| 0Bh | Second_alarm | AEN_S | SECOND_ALARM (0 to 59) | | | | | | | | Section 8.5.1 |
| 0Ch | Minute_alarm | AEN_M | MINUTE_ALARM (0 to 59) | | | | | | | | Section 8.5.2 |
| 0Dh | Hour_alarm | AEN_H | - | AMPM | HOUR_ALARM (1 to 12) in 12-hour mode | | | | | Section 8.5.3 | |
| | | | | HOUR_ALARM (0 to 23) in 24-hour mode | | | | | | | |
| 0Eh | Day_alarm | AEN_D | - | DAY_ALARM (1 to 31) | | | | | | Section 8.5.4 | |
| 0Fh | Weekday_alarm | AEN_W | - | - | - | - | WEEKDAY_ALARM (0 to 6) | | | Section 8.5.5 | |
| Timer registers | | | | | | | | | | | |
| 10h | Timer_value | T[7:0] | | | | | | | | Section 8.6.1 | |
| 11h | Timer_mode | - | - | - | TCF[1:0] | | TE | TIE | TI_TP | Section 8.6.2 | |

8.2 Control registers

To ensure that all control registers will be set to their default values, the V_{DD} level must be at zero volts at initial power-up. If this is not possible, a reset must be initiated with the software reset command when power is stable. Refer to [Section 8.2.1.3](#) for details.

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

| Bit | Symbol | Value | Description | Reference |
|-----|----------|------------------|--|--|
| 7 | EXT_TEST | | external clock test mode | Section 8.2.1.1 |
| | | 0 ^[1] | normal mode | |
| | | 1 | external clock test mode | |
| 6 | - | 0 | unused | - |
| 5 | STOP | | STOP bit | Section 8.2.1.2 |
| | | 0 ^[1] | RTC clock runs | |
| | | 1 | RTC clock is stopped; all RTC divider chain flip-flops are asynchronously set logic 0 | |
| 4 | SR | | software reset | Section 8.2.1.3 |
| | | 0 ^[1] | no software reset | |
| | | 1 | initiate software reset ^[2] ; this bit always returns a 0 when read | |
| 3 | - | 0 | unused | - |
| 2 | CIE | | correction interrupt enable | Section 8.2.3 |
| | | 0 ^[1] | no correction interrupt generated | |
| | | 1 | interrupt pulses are generated at every correction cycle | |
| 1 | 12_24 | | 12 or 24-hour mode | Section 8.3.3 Section 8.5.3 |
| | | 0 ^[1] | 24-hour mode is selected | |
| | | 1 | 12-hour mode is selected | |
| 0 | CAP_SEL | | internal oscillator capacitor selection for quartz crystals with a corresponding load capacitance | - |
| | | 0 ^[1] | 7 pF | |
| | | 1 | 12.5 pF | |

[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see [Section 8.2.1.3](#)).

8.2.1.1 EXT_TEST: external clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1 000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2⁶ divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.2.1.2 STOP: STOP bit function

The function of the STOP bit (see [Figure 6](#)) is to allow for accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. It also stops the output of clock frequencies below 8 kHz on pin CLKOUT.

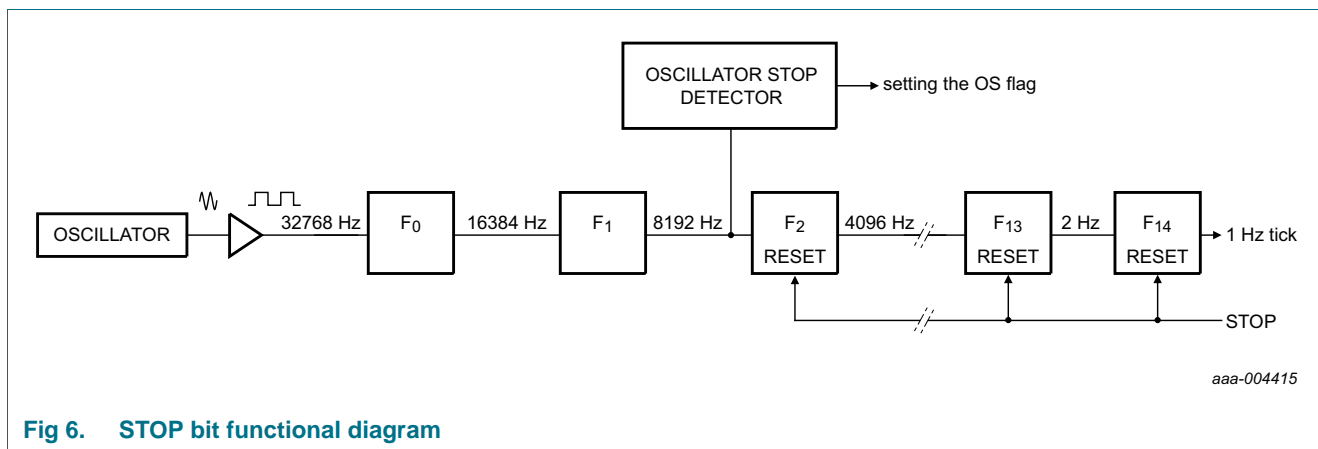


Fig 6. STOP bit functional diagram

The time circuits can then be set and do not increment until the STOP bit is released (see [Figure 7](#) and [Table 7](#)).

Table 7. First increment of time circuits after STOP bit release

| Bit | Prescaler bits | [1] 1 Hz tick | Time | Comment |
|--|--|---------------|----------|---|
| STOP | F ₀ F ₁ -F ₂ to F ₁₄ | | hh:mm:ss | |
| Clock is running normally | | | | |
| 0 | 01-0 0001 1101 0100 | | 12:45:12 | prescaler counting normally |
| STOP bit is activated by user. F₀F₁ are not reset and values cannot be predicted externally | | | | |
| 1 | XX-0 0000 0000 0000 | | 12:45:12 | prescaler is reset; time circuits are frozen |
| New time is set by user | | | | |
| 1 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is reset; time circuits are frozen |
| STOP bit is released by user | | | | |
| 0 | XX-0 0000 0000 0000 | | 08:00:00 | prescaler is now running |
| | XX-1 0000 0000 0000 | | 08:00:00 | - |
| | XX-0 1000 0000 0000 | | 08:00:00 | - |
| | XX-1 1000 0000 0000 | | 08:00:00 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:00 | - |
| | 00-0 0000 0000 0001 | | 08:00:01 | 0 to 1 transition of F ₁₄ increments the time circuits |
| | 10-0 0000 0000 0001 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1111 | | 08:00:01 | - |
| | 00-0 0000 0000 0000 | | 08:00:01 | - |
| | 10-0 0000 0000 0000 | | 08:00:01 | - |
| | : | | : | : |
| | 11-1 1111 1111 1110 | | 08:00:01 | - |
| | 00-0 0000 0000 0001 | | 08:00:02 | 0 to 1 transition of F ₁₄ increments the time circuits |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

[1] F₀ is clocked at 32.768 kHz.

The lower two stages of the prescaler (F₀ and F₁) are not reset. And because the I²C-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see [Figure 7](#)).

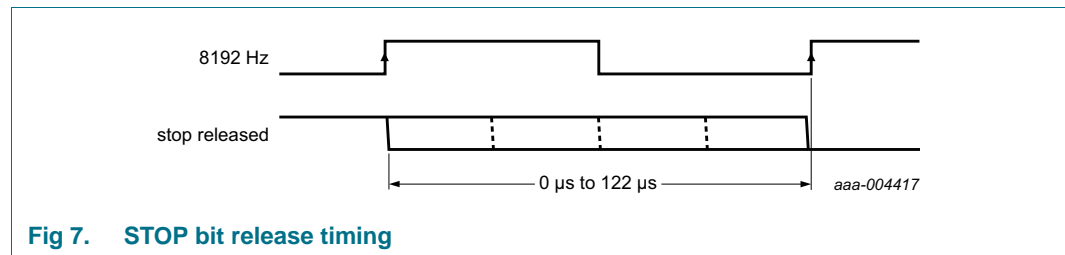
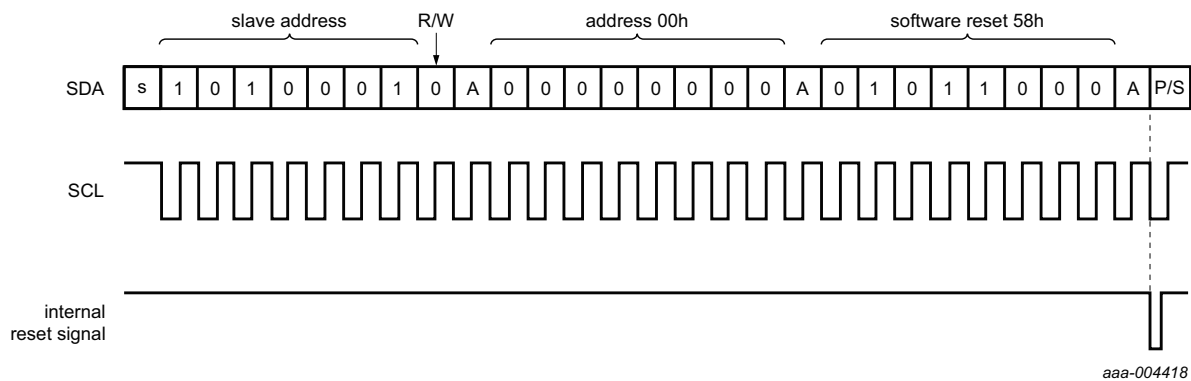


Fig 7. STOP bit release timing

The first increment of the time circuits is between 0.507813 s and 0.507935 s after STOP bit is released. The uncertainty is caused by the prescaler bits F₀ and F₁ not being reset (see [Table 7](#)) and the unknown state of the 32 kHz clock.

8.2.1.3 Software reset

A reset is automatically generated at power-on. There is a low probability that some devices will have corruption of the registers after the automatic power-on reset if the device is powered up with a residual V_{DD} level. It is required that the V_{DD} starts at zero volts at power up or upon power cycling to ensure that there is no corruption of the registers. If this is not possible, a reset must be initiated after power-up (i.e. when power is stable) with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control_1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see [Figure 8](#).



After sending the software reset command, it is recommended to re-initialize the interface by a STOP and START.

Fig 8. Software reset command

In reset state, all registers are set according to [Table 8](#) and the address pointer returns to address 00h.

Table 8. Registers reset values

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h | Control_1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01h | Control_2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | Offset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | RAM_byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | Seconds | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | Minutes | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06h | Hours | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07h | Days | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 08h | Weekdays | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 09h | Months | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0Ah | Years | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Bh | Second_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ch | Minute_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Dh | Hour_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Eh | Day_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 8. Registers reset values ...continued

| Address | Register name | Bit | | | | | | | |
|---------|---------------|-----|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0Fh | Weekday_alarm | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10h | Timer_value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11h | Timer_mode | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

The PCF85063A resets to:

Time — 00:00:00

Date — 20000101

Weekday — Saturday

8.2.2 Register Control_2

Table 9. Control_2 - control and status register 2 (address 01h) bit description

| Bit | Symbol | Value | Description | Reference |
|--------|----------|------------------------------|---|---|
| 7 | AIE | | alarm interrupt | Section 8.2.2.1 Section 8.5.6 |
| | | 0[1] | disabled | |
| | | 1 | enabled | |
| 6 | AF | | alarm flag | Section 8.2.2.1 Section 8.5.6 |
| | | 0[1] | read: alarm flag inactive | |
| | | | write: alarm flag is cleared | |
| | | 1 | read: alarm flag active | |
| | | | write: alarm flag remains unchanged | |
| 5 | MI | | minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0[1] | disabled | |
| | | 1 | enabled | |
| 4 | HMI | | half minute interrupt | Section 8.2.2.2 Section 8.2.2.3 |
| | | 0[1] | disabled | |
| | | 1 | enabled | |
| 3 | TF | | timer flag | Section 8.2.2.1 Section 8.2.2.3 Section 8.6.3 |
| | | 0[1] | no timer interrupt generated | |
| | | 1 | flag set when timer interrupt generated | |
| 2 to 0 | COF[2:0] | see Table 11 | CLKOUT control | Section 8.2.2.4 |

[1] Default value.

8.2.2.1 Alarm interrupt

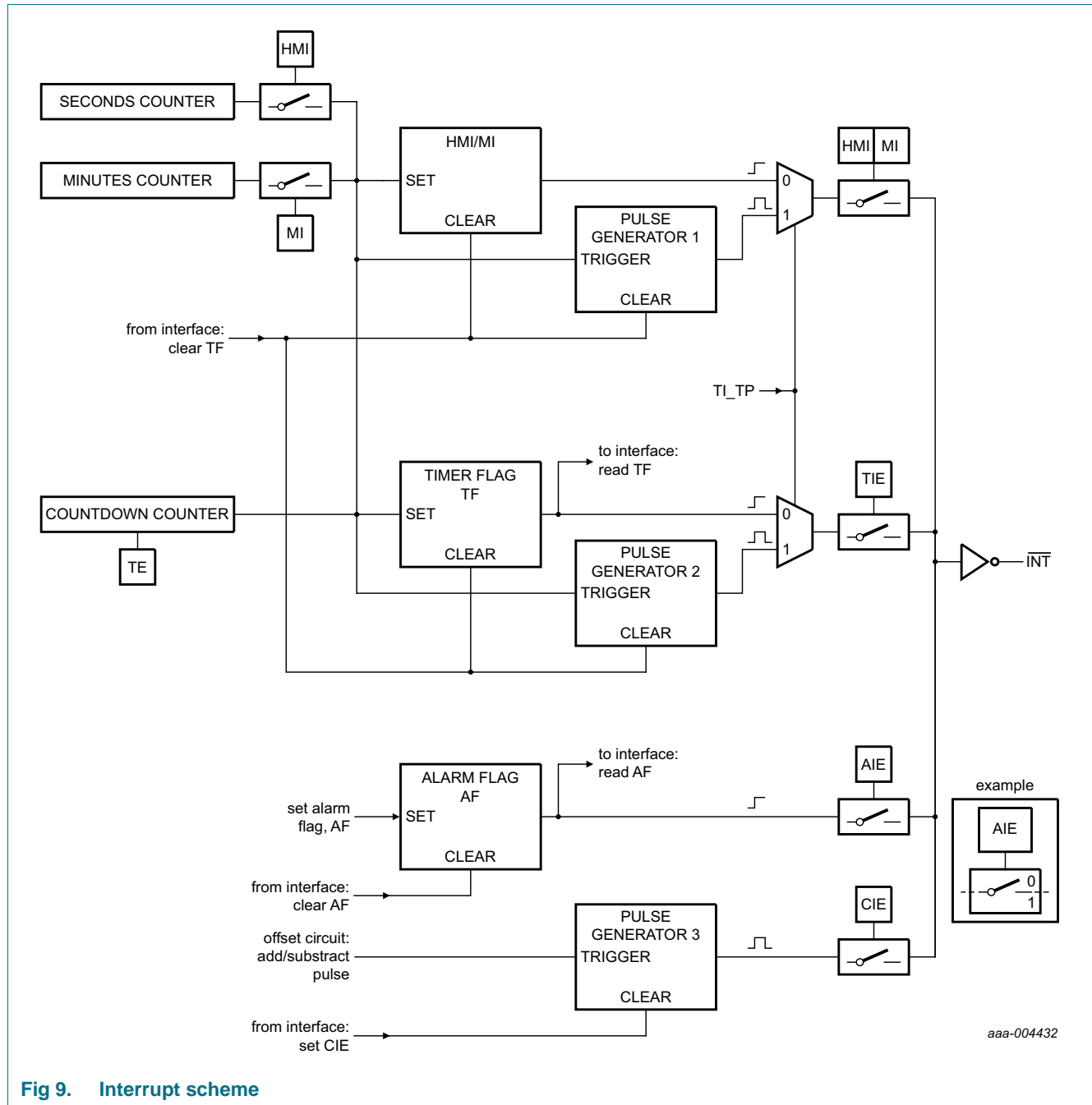


Fig 9. Interrupt scheme

AIE: This bit activates or deactivates the generation of an interrupt when AF is asserted, respectively.

AF: When an alarm occurs, AF is set logic 1. This bit maintains its value until overwritten by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access.

8.2.2.2 MI and HMI: minute and half minute interrupt

The minute interrupt (bit MI) and half minute interrupt (bit HMI) are pre-defined timers for generating interrupt pulses on pin $\overline{\text{INT}}$; see [Figure 10](#). The timers are running in sync with the seconds counter (see [Table 19 on page 21](#)).

The minute and half minute interrupts must only be used when the frequency offset is set to normal mode (MODE = 0), see [Section 8.2.3](#). In normal mode, the interrupt pulses on pin $\overline{\text{INT}}$ are $\frac{1}{64}$ s wide.

When starting MI, the first interrupt will be generated after 1 second to 59 seconds. When starting HMI, the first interrupt will be generated after 1 second to 29 seconds. Subsequent periods do not have such a delay. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a half minute interrupt is not distinguishable.

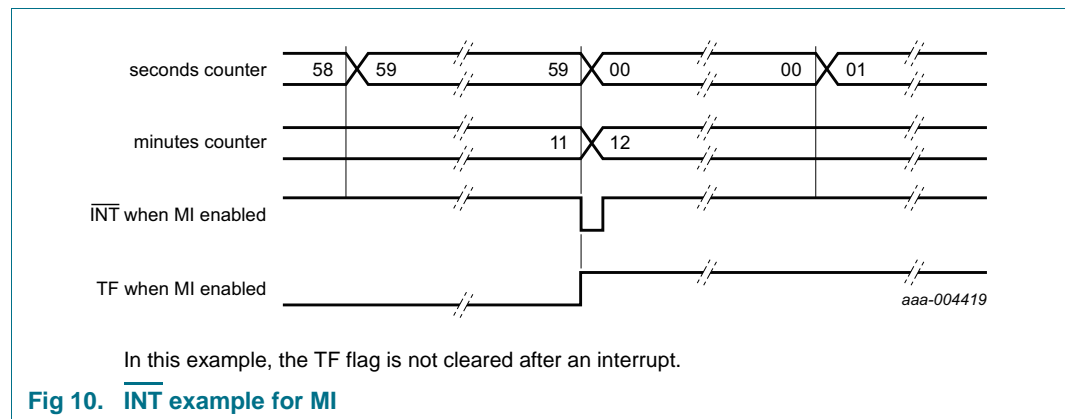


Table 10. Effect of bits MI and HMI on $\overline{\text{INT}}$ generation

| Minute interrupt (bit MI) | Half minute interrupt (bit HMI) | Result |
|---------------------------|---------------------------------|---------------------------|
| 0 | 0 | no interrupt generated |
| 1 | 0 | an interrupt every minute |
| 0 | 1 | an interrupt every 30 s |
| 1 | 1 | an interrupt every 30 s |

The duration of the timer is affected by the register Offset (see [Section 8.2.3](#)). Only when OFFSET[6:0] has the value 00h the periods are consistent.

8.2.2.3 TF: timer flag

The timer flag (bit TF) is set logic 1 on the first trigger of MI, HMI, or the countdown timer. The purpose of the flag is to allow the controlling system to interrogate what caused the interrupt: timer or alarm. The flag can be read and cleared by command.

The status of the timer flag TF can affect the $\overline{\text{INT}}$ pulse generation depending on the setting of TI_TP (see [Section 8.6.2 "Register Timer_mode" on page 30](#)):

- When TI_TP is set logic 1
 - an $\overline{\text{INT}}$ pulse is generated independent of the status of the timer flag TF
 - TF stays set until it is cleared
 - TF does not affect $\overline{\text{INT}}$

- the countdown timer runs in a repetitive loop and keeps generating timed periods
- When TI_TP is set logic 0
 - the $\overline{\text{INT}}$ generation follows the TF flag
 - TF stays set until it is cleared
 - If TF is not cleared before the next coming interrupt, no $\overline{\text{INT}}$ is generated
 - the countdown timer stops after the first countdown

8.2.2.4 COF[2:0]: Clock output frequency

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Control_2. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is a push-pull output and enabled at power-on. CLKOUT can be disabled by setting COF[2:0] to 111 or by setting CLKOE LOW (PCF85063ATL only). When disabled, the CLKOUT is LOW. If CLKOE is HIGH and COF[2:0]=111 there will be no clock and CLKOUT will be LOW.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function, see [Section 8.2.1.2](#).

Table 11. CLKOUT frequency selection

| COF[2:0] | CLKOUT frequency (Hz) | Typical duty cycle ^[1] | Effect of STOP bit |
|--------------------|-----------------------|-----------------------------------|--------------------|
| 000 ^[2] | 32768 | 60 : 40 to 40 : 60 | no effect |
| 001 | 16384 | 50 : 50 | no effect |
| 010 | 8192 | 50 : 50 | no effect |
| 011 | 4096 | 50 : 50 | CLKOUT = LOW |
| 100 | 2048 | 50 : 50 | CLKOUT = LOW |
| 101 | 1024 | 50 : 50 | CLKOUT = LOW |
| 110 | 1 ^[3] | 50 : 50 | CLKOUT = LOW |
| 111 | CLKOUT = LOW | - | - |

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default values: The duty cycle of the CLKOUT when outputting 32,768 Hz could change from 60:40 to 40:60 depending on the detector since the 32,768 Hz is derived from the oscillator output which is not perfect. It could change from device to device and it depends on the silicon diffusion. There is nothing that can be done from outside the chip to influence the duty cycle.

[3] 1 Hz clock pulses are affected by offset correction pulses.

8.2.3 Register Offset

The PCF85063A incorporates an offset register (address 02h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Table 12. Offset - offset register (address 02h) bit description

| Bit | Symbol | Value | Description |
|--------|-------------|------------------------------|--|
| 7 | MODE | | offset mode |
| | | 0 ^[1] | normal mode: offset is made once every two hours |
| | | 1 | course mode: offset is made every 4 minutes |
| 6 to 0 | OFFSET[6:0] | see Table 13 | offset value |

[1] Default value.

For MODE = 0, each LSB introduces an offset of 4.34 ppm. For MODE = 1, each LSB introduces an offset of 4.069 ppm. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

Table 13. Offset values

| OFFSET[6:0] | Offset value in decimal | Offset value in ppm | |
|------------------------|-------------------------|-------------------------|-----------------------|
| | | Normal mode MODE = 0 | Fast mode MODE = 1 |
| 0111111 | +63 | +273.420 | +256.347 |
| 0111110 | +62 | +269.080 | +252.278 |
| : | : | : | : |
| 0000010 | +2 | +8.680 | +8.138 |
| 0000001 | +1 | +4.340 | +4.069 |
| 0000000 ^[1] | 0 | 0 ^[1] | 0 ^[1] |
| 1111111 | -1 | -4.340 | -4.069 |
| 1111110 | -2 | -8.680 | -8.138 |
| : | : | : | : |
| 1000001 | -63 | -273.420 | -256.347 |
| 1000000 | -64 | -277.760 | -260.416 |

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (register Control_1) has to be set logic 1. At every correction cycle, a pulse is generated on pin INT. The pulse width depends on the correction mode. If multiple correction pulses are applied, an interrupt pulse is generated for each correction pulse applied.

8.2.3.1 Correction when MODE = 0

The correction is triggered once every two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 14. Correction pulses for MODE = 0

| Correction value | Update every n th hour | Minute | Correction pulses on INT per minute ^[1] |
|------------------|-----------------------------------|--------------------|--|
| +1 or –1 | 2 | 00 | 1 |
| +2 or –2 | 2 | 00 and 01 | 1 |
| +3 or –3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or –59 | 2 | 00 to 58 | 1 |
| +60 or –60 | 2 | 00 to 59 | 1 |
| +61 or –61 | 2 | 00 to 59 | 1 |
| | 2nd and next hour | 00 | 1 |
| +62 or –62 | 2 | 00 to 59 | 1 |
| | 2nd and next hour | 00 and 01 | 1 |
| +63 or –63 | 02 | 00 to 59 | 1 |
| | 2nd and next hour | 00, 01, and 02 | 1 |
| –64 | 02 | 00 to 59 | 1 |
| | 2nd and next hour | 00, 01, 02, and 03 | 1 |

[1] The correction pulses on pin $\overline{\text{INT}}$ are $\frac{1}{64}$ s wide.

In MODE = 0, any timer or clock output using a frequency below 64 Hz is affected by the clock correction (see [Table 15](#)).

Table 15. Effect of correction pulses on frequencies for MODE = 0

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | no effect |
| 1 | affected |
| $\frac{1}{60}$ | affected |

8.2.3.2 Correction when MODE = 1

The correction is triggered once every four minutes and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 16. Correction pulses for MODE = 1

| Correction value | Update every n th minute | Second | Correction pulses on INT per second ^[1] |
|------------------|-------------------------------------|----------------|--|
| +1 or –1 | 2 | 00 | 1 |
| +2 or –2 | 2 | 00 and 01 | 1 |
| +3 or –3 | 2 | 00, 01, and 02 | 1 |
| : | : | : | : |
| +59 or –59 | 2 | 00 to 58 | 1 |
| +60 or –60 | 2 | 00 to 59 | 1 |
| +61 or –61 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 2 |
| +62 or –62 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 3 |
| +63 or –63 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 4 |
| –64 | 2 | 00 to 58 | 1 |
| | 2 | 59 | 5 |

[1] The correction pulses on pin $\overline{\text{INT}}$ are $\frac{1}{1024}$ s wide. For multiple pulses, they are repeated at an interval of $\frac{1}{512}$ s.

In MODE = 1, any timer source clock using a frequency below 1.024 kHz is also affected by the clock correction (see [Table 17](#)).

Table 17. Effect of correction pulses on frequencies for MODE = 1

| Frequency (Hz) | Effect of correction |
|---------------------------|----------------------|
| CLKOUT | |
| 32768 | no effect |
| 16384 | no effect |
| 8192 | no effect |
| 4096 | no effect |
| 2048 | no effect |
| 1024 | no effect |
| 1 | affected |
| Timer source clock | |
| 4096 | no effect |
| 64 | affected |
| 1 | affected |
| $\frac{1}{60}$ | affected |

8.2.3.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. [Figure 11](#) shows the workflow how the offset register values can be calculated:

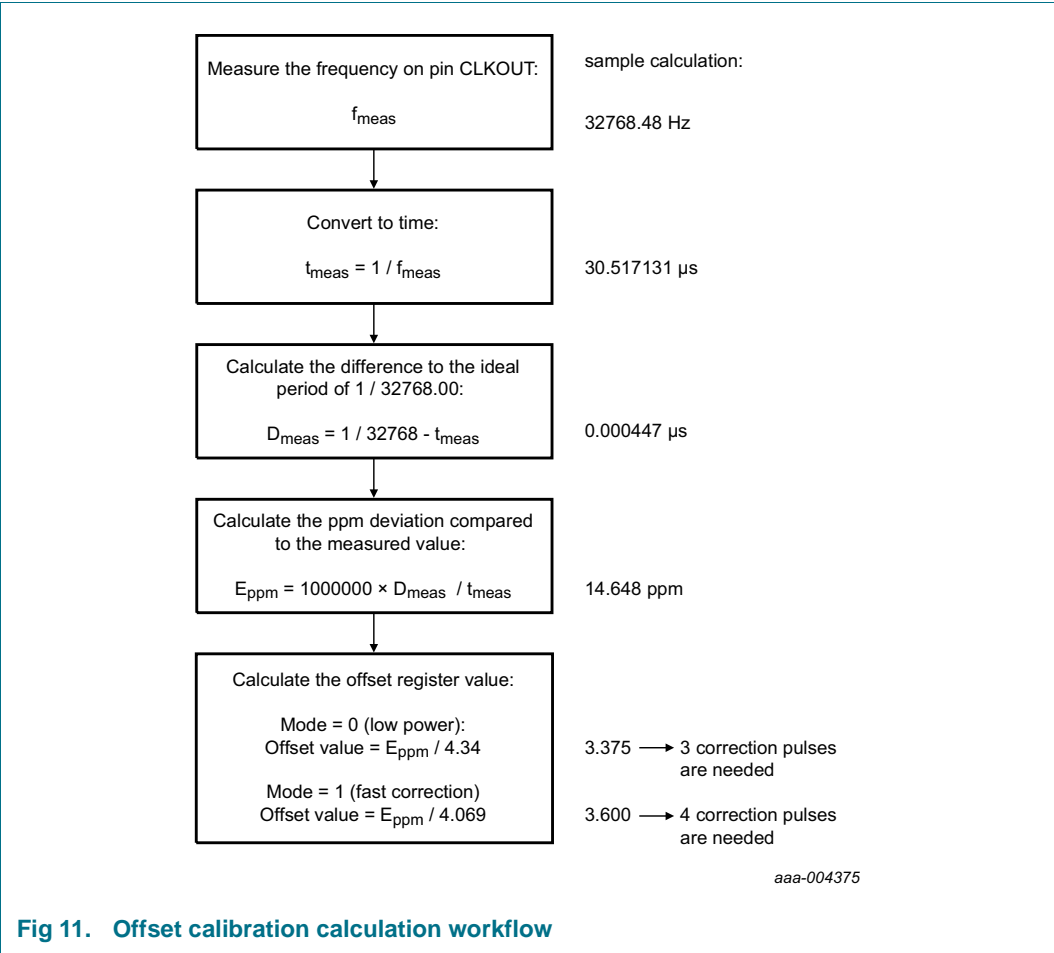
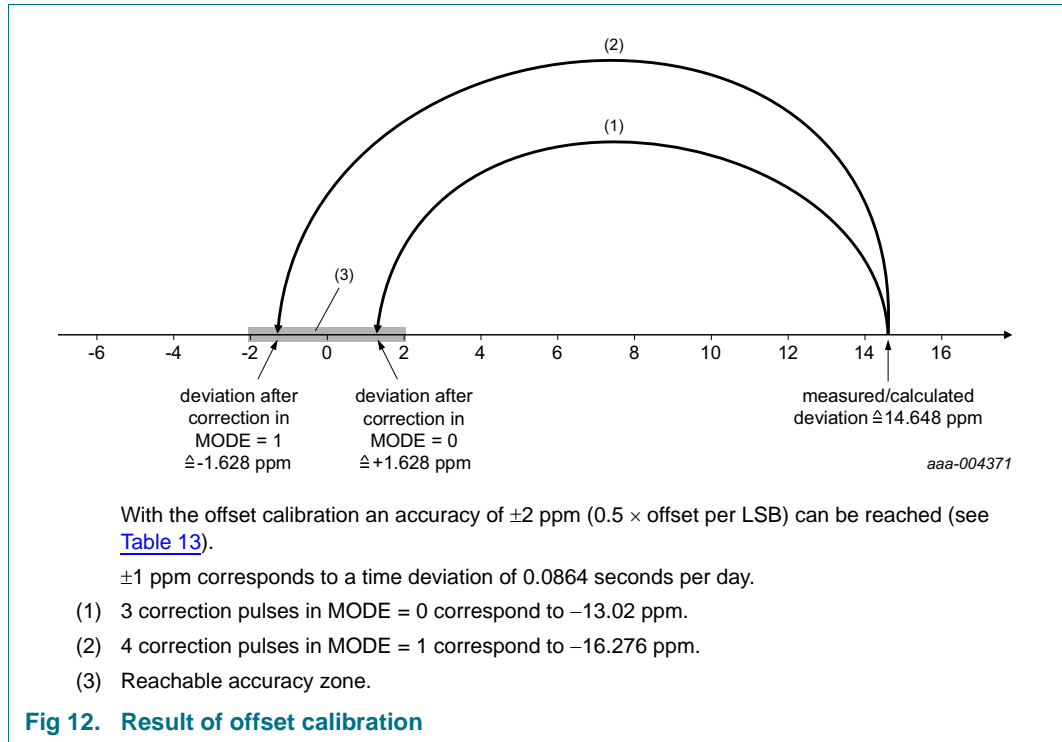


Fig 11. Offset calibration calculation workflow



8.2.4 Register RAM_byte

The PCF85063A provides a free RAM byte, which can be used for any purpose, for example, status byte of the system.

Table 18. RAM_byte - 8-bit RAM register (address 03h) bit description

| Bit | Symbol | Value | Description |
|--------|--------|-------------------------------------|-------------|
| 7 to 0 | B[7:0] | 00000000 ^[1] to 11111111 | RAM content |

[1] Default value.

8.3 Time and date registers

Most of the registers are coded in the BCD format to simplify application use.

8.3.1 Register Seconds

Table 19. Seconds - seconds register (address 04h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | OS | | | oscillator stop |
| | | 0 | - | clock integrity is guaranteed |
| | | 1 ^[1] | - | clock integrity is not guaranteed; oscillator has stopped or has been interrupted |
| 6 to 4 | SECONDS | 0 ^[1] to 5 | ten's place | actual seconds coded in BCD format, see Table 20 |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

Table 20. Seconds coded in BCD format

| Seconds value in decimal | Upper-digit (ten's place) | | | Digit (unit place) | | | |
|--------------------------|---------------------------|-------|-------|--------------------|-------|-------|-------|
| | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 00 ^[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| : | : | : | : | : | : | : | : |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| : | : | : | : | : | : | : | : |
| 58 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 59 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

[1] Default value.

8.3.1.1 OS: Oscillator stop

When the oscillator of the PCF85063A is stopped, the OS flag is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSC1 or OSC0 to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The flag remains set until cleared by command (see [Figure 13](#)). If the flag cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

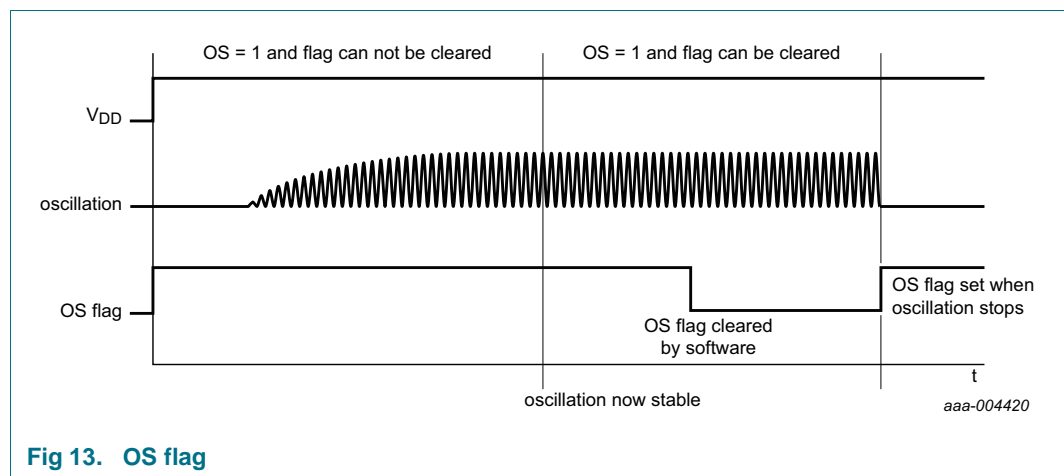


Fig 13. OS flag

8.3.2 Register Minutes

Table 21. Minutes - minutes register (address 05h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------|-----------------------|-------------|---|
| 7 | - | 0 | - | unused |
| 6 to 4 | MINUTES | 0 ^[1] to 5 | ten's place | actual minutes coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.3.3 Register Hours

Table 22. Hours - hours register (address 06h) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------|--------|-----------------------|-------------|---|
| 7 to 6 | - | 00 | - | unused |
| 12-hour mode ^[1] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[2] | - | AM |
| | | 1 | - | PM |
| 4 | HOURS | 0 ^[2] to 1 | ten's place | actual hours in 12-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |
| 24-hour mode ^[1] | | | | |
| 5 to 4 | HOURS | 0 ^[2] to 2 | ten's place | actual hours in 24-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[2] to 9 | unit place | |

[1] Hour mode is set by the 12_24 bit in register Control_1.

[2] Default value.

8.3.4 Register Days

Table 23. Days - days register (address 07h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|---------------------|-----------------------|-------------|---------------------------------------|
| 7 to 6 | - | 00 | - | unused |
| 5 to 4 | DAYS ^[1] | 0 ^[2] to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 | | 0 ^[3] to 9 | unit place | |

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the PCF85063A compensates for leap years by adding a 29th day to February.

[2] Default value.

[3] Default value is 1.

8.3.5 Register Weekdays

Table 24. Weekdays - weekdays register (address 08h) bit description

| Bit | Symbol | Value | Description |
|--------|----------|--------|--|
| 7 to 3 | - | 00000 | unused |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday values, see Table 25 |

Table 25. Weekday assignments

| Day ^[1] | Bit | | |
|-------------------------|-----|---|---|
| | 2 | 1 | 0 |
| Sunday | 0 | 0 | 0 |
| Monday | 0 | 0 | 1 |
| Tuesday | 0 | 1 | 0 |
| Wednesday | 0 | 1 | 1 |
| Thursday | 1 | 0 | 0 |
| Friday | 1 | 0 | 1 |
| Saturday ^[2] | 1 | 1 | 0 |

[1] Definition may be reassigned by the user.

[2] Default value.

8.3.6 Register Months

Table 26. Months - months register (address 09h) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|--------|-------------|---|
| 7 to 5 | - | 000 | - | unused |
| 4 | MONTHS | 0 to 1 | ten's place | actual month coded in BCD format, see Table 27 |
| 3 to 0 | | 0 to 9 | unit place | |

Table 27. Month assignments in BCD format

| Month | Upper-digit (ten's place) | Digit (unit place) | | | |
|------------------------|------------------------------|--------------------|-------|-------|-------|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January ^[1] | 0 | 0 | 0 | 0 | 1 |
| February | 0 | 0 | 0 | 1 | 0 |
| March | 0 | 0 | 0 | 1 | 1 |
| April | 0 | 0 | 1 | 0 | 0 |
| May | 0 | 0 | 1 | 0 | 1 |
| June | 0 | 0 | 1 | 1 | 0 |
| July | 0 | 0 | 1 | 1 | 1 |
| August | 0 | 1 | 0 | 0 | 0 |
| September | 0 | 1 | 0 | 0 | 1 |
| October | 1 | 0 | 0 | 0 | 0 |
| November | 1 | 0 | 0 | 0 | 1 |
| December | 1 | 0 | 0 | 1 | 0 |

[1] Default value.

8.3.7 Register Years

Table 28. Years - years register (0Ah) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------|-----------|-------------|--|
| 7 to 4 | YEARS | 0[1] to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 | | 0[1] to 9 | unit place | |

[1] Default value.

8.4 Setting and reading the time

Figure 14 shows the data flow and data dependencies starting from the 1 Hz clock tick.

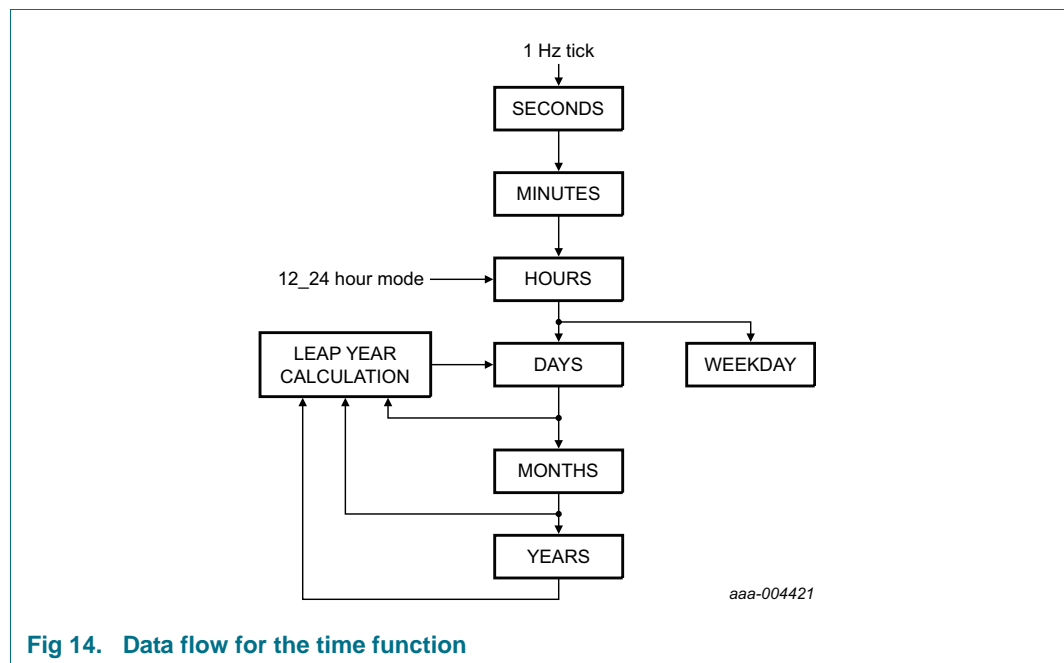


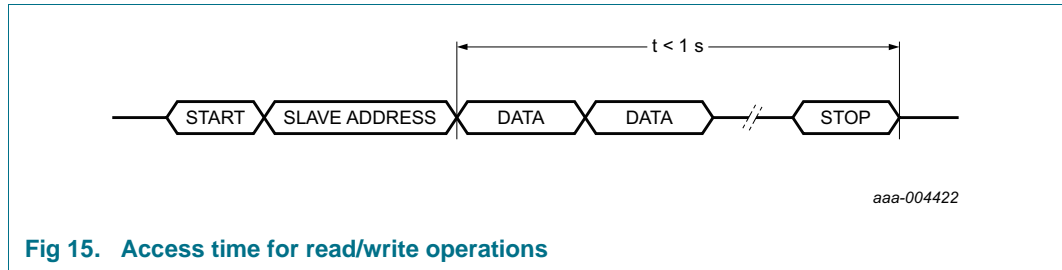
Fig 14. Data flow for the time function

During read/write operations, the time counting circuits (memory locations 04h through 0Ah) are blocked.

The blocking prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 15).



Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Recommended method for reading the time:

1. Send a START condition and the slave address (see [Table 39 on page 35](#)) for write (A2h)
2. Set the address pointer to 4 (Seconds) by sending 04h
3. Send a RESTART condition or STOP followed by START
4. Send the slave address for read (A3h)
5. Read Seconds
6. Read Minutes
7. Read Hours
8. Read Days
9. Read Weekdays
10. Read Months
11. Read Years
12. Send a STOP condition

8.5 Alarm registers

8.5.1 Register Second_alarm

Table 29. Second_alarm - second alarm register (address 0Bh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|--|
| 7 | AEN_S | | | second alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | SECOND_ALARM | 0 ^[1] to 5 | ten's place | second alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.2 Register Minute_alarm

Table 30. Minute_alarm - minute alarm register (address 0Ch) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|--------------|-----------------------|-------------|---|
| 7 | AEN_M | | | minute alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 to 4 | MINUTE_ALARM | 0 ^[1] to 5 | ten's place | minute alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.3 Register Hour_alarm

Table 31. Hour_alarm - hour alarm register (address 0Dh) bit description

| Bit | Symbol | Value | Place value | Description |
|-----------------------------|------------|-----------------------|-------------|---|
| 7 | AEN_H | | | hour alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 12-hour mode ^[2] | | | | |
| 5 | AMPM | | | AM/PM indicator |
| | | 0 ^[1] | - | AM |
| | | 1 | - | PM |
| 4 | HOUR_ALARM | 0 ^[1] to 1 | ten's place | hour alarm information in 12-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |
| 24-hour mode ^[2] | | | | |
| 5 to 4 | HOUR_ALARM | 0 ^[1] to 2 | ten's place | hour alarm information in 24-hour mode coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

[2] Hour mode is set by the 12_24 bit in register Control_1.

8.5.4 Register Day_alarm

Table 32. Day_alarm - day alarm register (address 0Eh) bit description

| Bit | Symbol | Value | Place value | Description |
|--------|-----------|-----------------------|-------------|--|
| 7 | AEN_D | | | day alarm |
| | | 0 | - | enabled |
| | | 1 ^[1] | - | disabled |
| 6 | - | 0 | - | unused |
| 5 to 4 | DAY_ALARM | 0 ^[1] to 3 | ten's place | day alarm information coded in BCD format |
| 3 to 0 | | 0 ^[1] to 9 | unit place | |

[1] Default value.

8.5.5 Register Weekday_alarm

Table 33. Weekday_alarm - weekday alarm register (address 0Fh) bit description

| Bit | Symbol | Value | Description |
|--------|---------------|-----------------------|--|
| 7 | AEN_W | | weekday alarm |
| | | 0 | enabled |
| | | 1 ^[1] | disabled |
| 6 to 3 | - | 0 | unused |
| 2 to 0 | WEEKDAY_ALARM | 0 ^[1] to 6 | weekday alarm information coded in BCD format |

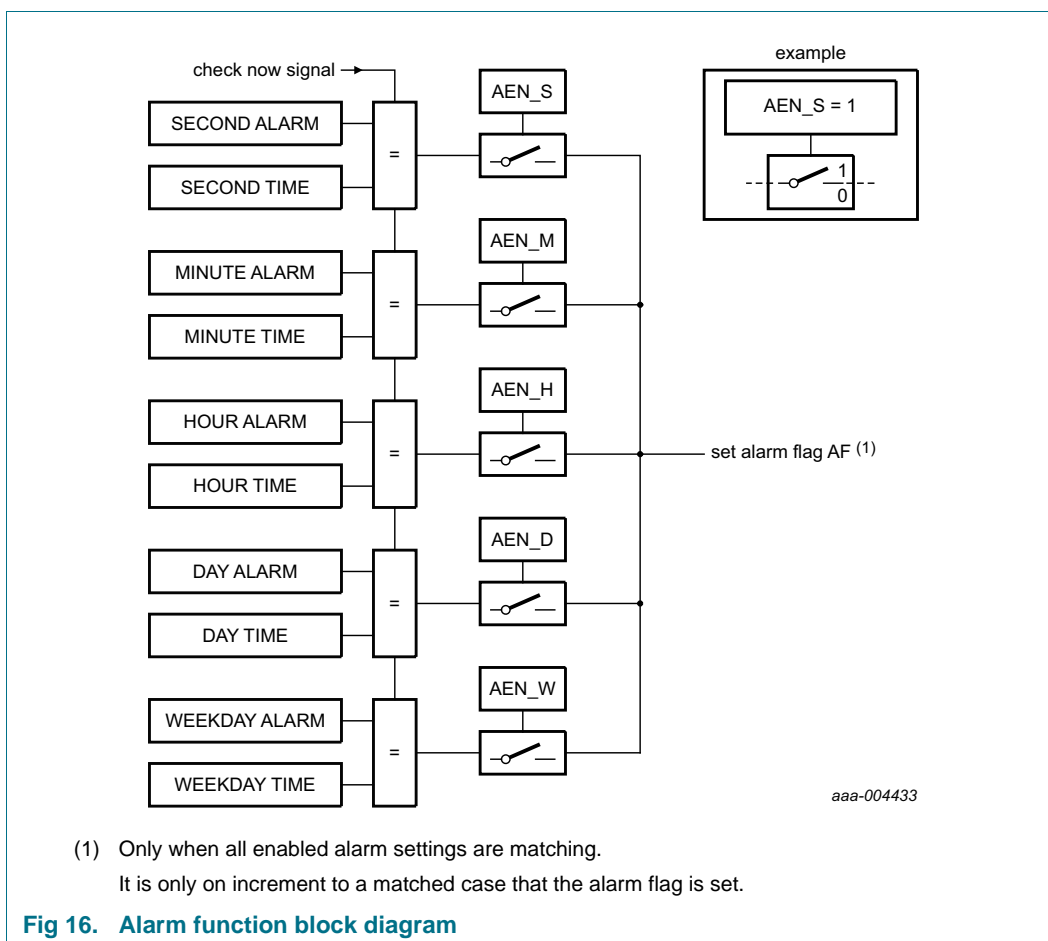
[1] Default value.

8.5.6 Alarm function

By clearing the alarm enable bit (AEN_x) of one or more of the alarm registers, the corresponding alarm condition(s) are active. When an alarm occurs, AF is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{\text{INT}}$). The AF is cleared by command.

The registers at addresses 0Bh through 0Fh contain alarm information. When one or more of these registers is loaded with second, minute, hour, day or weekday, and its corresponding AEN_x is logic 0, then that information is compared with the current second, minute, hour, day, and weekday. When all enabled comparisons first match, the alarm flag (AF in register Control_2) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{\text{INT}}$ pin follows the condition of bit AF. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_x bit at logic 1 are ignored.



8.6 Timer registers

The 8-bit countdown timer at address 10h is controlled by the register `Timer_mode` at address 11h.

8.6.1 Register `Timer_value`

Table 34. `Timer_value` - timer value register (address 10h) bit description

| Bit | Symbol | Value | Description |
|--------|--------|--------------------------|--------------------------------------|
| 7 to 0 | T[7:0] | 0h ^[1] to FFh | countdown timer value ^[2] |

[1] Default value.

[2] Countdown period in seconds: $CountdownPeriod = \frac{T}{SourceClockFrequency}$ where T is the countdown value.

8.6.2 Register Timer_mode

Table 35. Timer_mode - timer control register (address 11h) bit description

| Bit | Symbol | Value | Description |
|--------|----------------------|-------------------|--------------------------------------|
| 7 to 5 | - | 000 | unused |
| 4 to 3 | TCF[1:0] | | timer clock frequency |
| | | 00 | 4.096 kHz timer source clock |
| | | 01 | 64 Hz timer source clock |
| | | 10 | 1 Hz timer source clock |
| | | 11 ^[1] | $\frac{1}{60}$ Hz timer source clock |
| 2 | TE | | timer enable |
| | | 0 ^[1] | timer is disabled |
| | | 1 | timer is enabled |
| 1 | TIE | | timer interrupt enable |
| | | 0 ^[1] | no interrupt generated from timer |
| | | 1 | interrupt generated from timer |
| 0 | TI_TP ^[2] | | timer interrupt mode |
| | | 0 ^[1] | interrupt follows timer flag |
| | | 1 | interrupt generates a pulse |

[1] Default value.

[2] How the setting of TI_TP and the timer flag TF can affect the $\overline{\text{INT}}$ pulse generation is explained in [Section 8.2.2.3 on page 15](#).

8.6.3 Timer functions

The timer has four selectable source clocks allowing for countdown periods in the range from 244 μs to 4 hours 15 min. For periods longer than 4 hours, the alarm function can be used.

Table 36. Timer clock frequency and timer durations

| TCF[1:0] | Timer source clock frequency ^[1] | Delay | |
|----------|---|---------------------------------|-----------------------------------|
| | | Minimum timer duration T = 1 | Maximum timer duration T = 255 |
| 00 | 4.096 kHz | 244 μs | 62.256 ms |
| 01 | 64 Hz | 15.625 ms | 3.984 s |
| 10 | 1 Hz ^[2] | 1 s | 255 s |
| 11 | $\frac{1}{60}$ Hz ^[2] | 60 s | 4 hours 15 min |

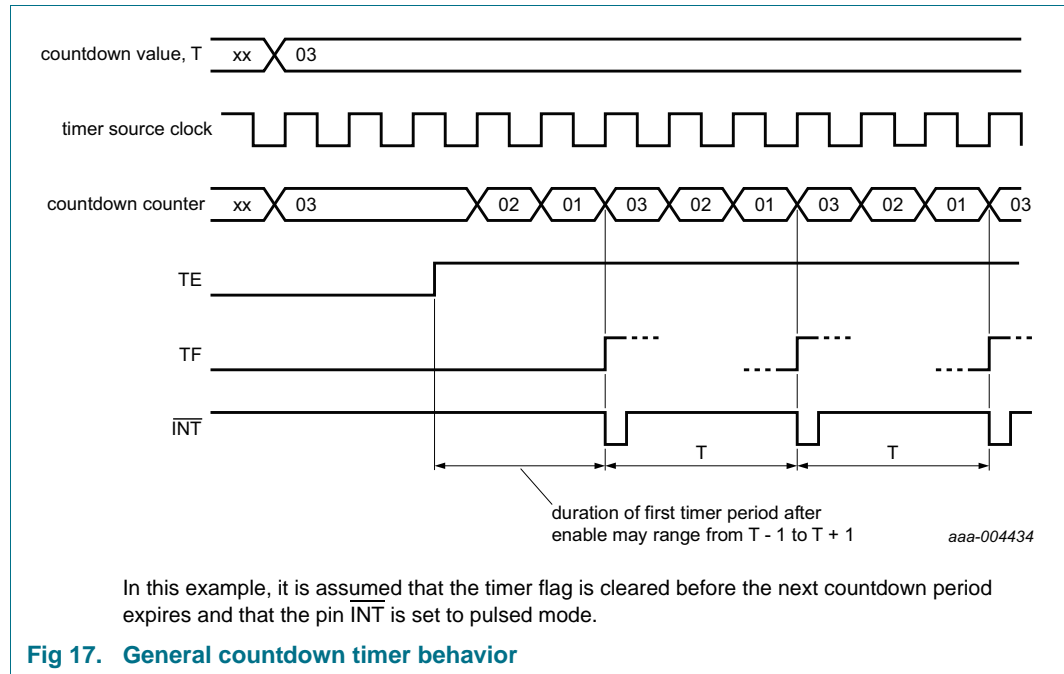
[1] When not in use, TCF[1:0] must be set to $\frac{1}{60}$ Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, T[7:0], in register Timer_value. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid.

When the counter decrements from 1, the timer flag (bit TF in register Control_2) is set and the counter automatically re-loads and starts the next timer period.



If a new value of T is written before the end of the current timer period, then this value takes immediate effect. NXP does not recommend changing T without first disabling the counter by setting bit TE logic 0. The update of T is asynchronous to the timer clock. Therefore changing it without setting bit TE logic 0 may result in a corrupted value loaded into the countdown counter. This results in an undetermined countdown period for the first period. The countdown value T will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the TIE flag is set, an interrupt signal on INT is generated if this mode is enabled. See [Section 8.2.2](#) for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty. The uncertainty is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods do not have such delay. The amount of delay for the first timer period depends on the chosen source clock, see [Table 37](#).

Table 37. First period delay for timer counter value T

| Timer source clock | Minimum timer period | Maximum timer period |
|---------------------------|-------------------------------------|-------------------------------|
| 4.096 kHz | T | T + 1 |
| 64 Hz | T | T + 1 |
| 1 Hz | $(T - 1) + \frac{1}{64 \text{ Hz}}$ | $T + \frac{1}{64 \text{ Hz}}$ |
| $\frac{1}{60} \text{ Hz}$ | $(T - 1) + \frac{1}{64 \text{ Hz}}$ | $T + \frac{1}{64 \text{ Hz}}$ |

At the end of every countdown, the timer sets the countdown timer flag (bit TF in register Control_2). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt at pin INT. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see [Table 35](#) and [Figure 17](#).

When reading the timer, the current countdown value is returned and **not** the initial value T. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and 1/60 Hz is affected by the Offset register. The duration of a program period varies according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefore be longer or shorter depending on the setting of the Offset register. See [Section 8.2.3](#) to understand the operation of the Offset register.

8.6.3.1 Countdown timer interrupts

The pulse generator for the countdown timer interrupt uses an internal clock and is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies (see [Table 38](#)).

Table 38. $\overline{\text{INT}}$ operation

TF and $\overline{\text{INT}}$ become active simultaneously.

| Source clock (Hz) | INT period (s) | |
|-------------------|----------------------|----------------------|
| | T = 1 ^[1] | T > 1 ^[1] |
| 4096 | 1/8192 | 1/4096 |
| 64 | 1/128 | 1/64 |
| 1 | 1/64 | 1/64 |
| 1/60 | 1/64 | 1/64 |

[1] T = loaded countdown value. Timer stops when T = 0.

9. Characteristics of the I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signal (see [Figure 18](#)).

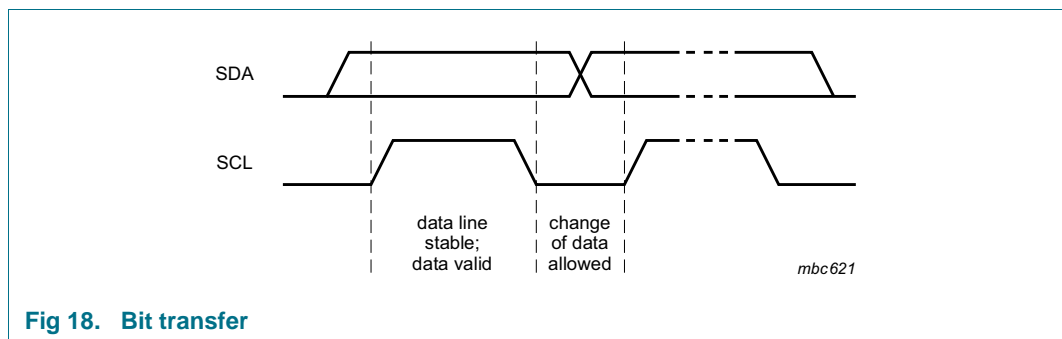


Fig 18. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see [Figure 19](#)).

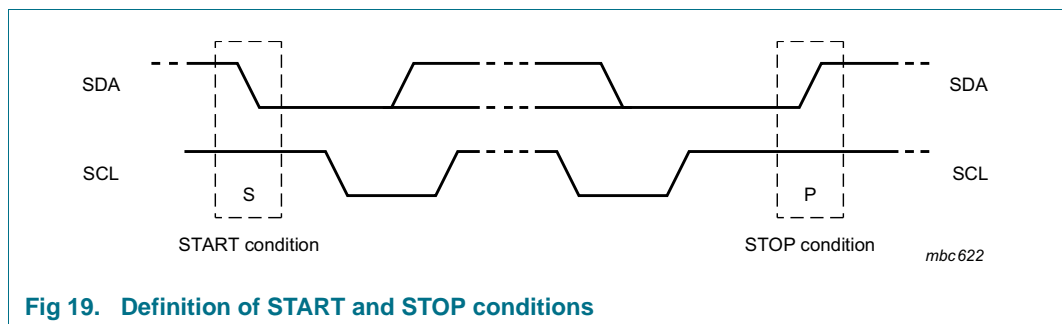
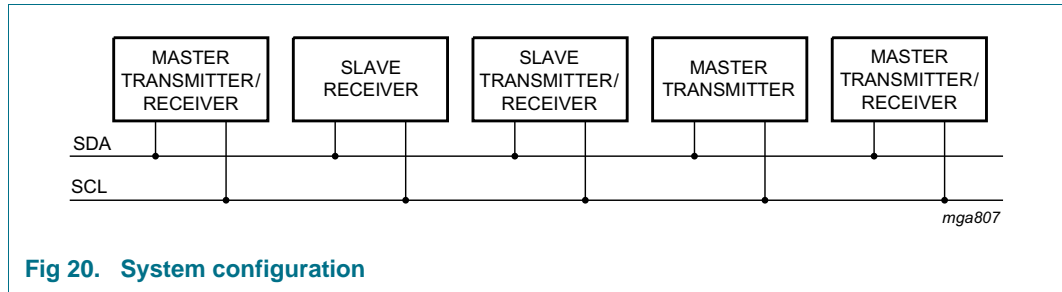


Fig 19. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see [Figure 20](#)).

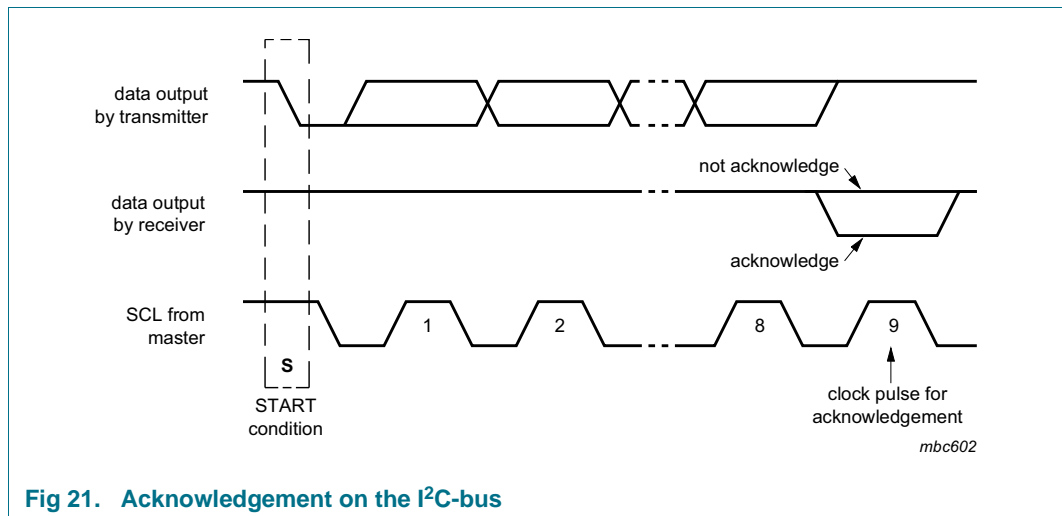


9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I²C-bus is shown in [Figure 21](#).



9.5 I²C-bus protocol

9.5.1 Addressing

One I²C-bus slave address (1010001) is reserved for the PCF85063A. The entire I²C-bus slave address byte is shown in [Table 39](#).

Table 39. I²C slave address byte

| Bit | Slave address | | | | | | | |
|-----|---------------|---|---|---|---|---|---|-----|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | MSB | | | | | | | LSB |
| | 1 | 0 | 1 | 0 | 0 | 0 | 1 | R/W |

After a START condition, the I²C slave address has to be sent to the PCF85063A device.

The R/W bit defines the direction of the following single or multiple byte data transfer (R/W = 0 for writing, R/W = 1 for reading). For the format and the timing of the START condition (S), the STOP condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics (see [Ref. 16 "UM10204"](#)). In the write mode, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

9.5.2 Clock and calendar READ or WRITE cycles

The I²C-bus configuration for the different PCF85063A READ and WRITE cycles is shown in [Figure 22](#) and [Figure 23](#). The register address is a 5-bit value that defines which register is to be accessed next. The upper 3 bits of the register address are not used.

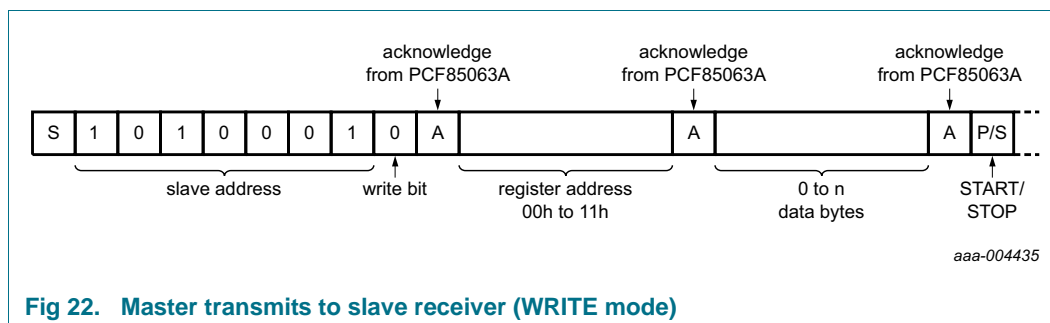
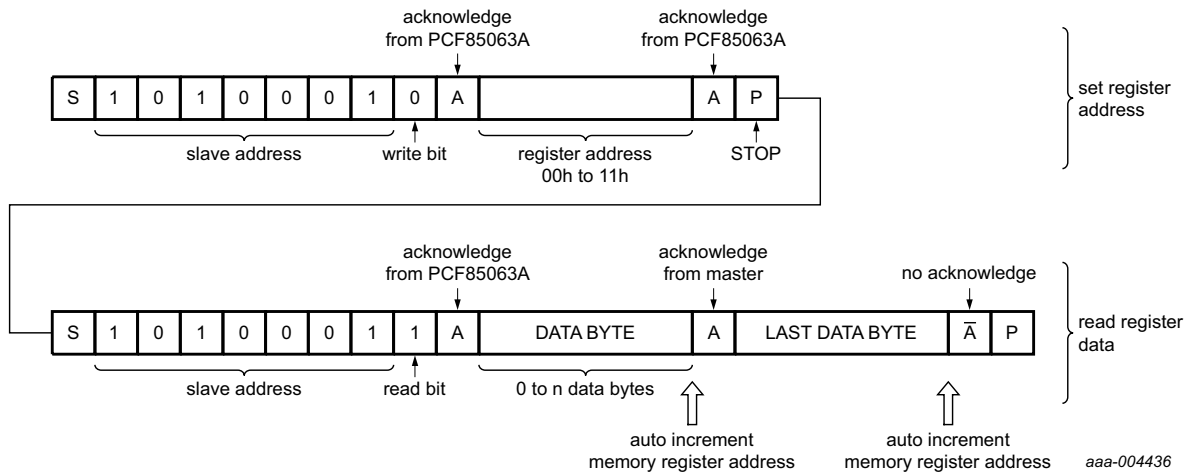


Fig 22. Master transmits to slave receiver (WRITE mode)



For multimaster configurations and to fasten the communication, the STOP-START sequence can be replaced by a repeated START (Sr).

Fig 23. Master reads after setting register address (write register address; READ data)

9.5.2.1 I²C-bus error recovery technique

Slave devices like the PCF85063A use a state machine to implement the I²C protocol and expect a certain sequence of events to occur to function properly. Unexpected events at the I²C master can wreak havoc with the slaves connected on the bus. However, it is usually possible to recover deterministically to a known bus state with careful protocol manipulation.

A deterministic method to clear this situation if SDA is stuck LOW (it effectively blocks any other I²C-bus transaction, once the master recognizes a 'stuck bus' state), is for the master to blindly transmit nine clocks on SCL. If the slave was transmitting data or acknowledging, nine or more clocks ensures the slave state machine returns to a known, idle state since the protocol calls for eight data bits and one ACK bit. It does not matter when the slave state machine finishes its transmission; extra clocks are recognized as STOP conditions.

With careful design of the bus master error recovery firmware, many I²C-bus protocol problems can be avoided.

S/W considerations: NXP recommends customers allow for S/W reset capability to enable the bus error recovery technique. The 9-clock pulse method as described above involves a bus-master capable of providing such a signal.

Further comments/additional information are available in [Ref. 17 "UM10301"](#) and [Ref. 16 "UM10204"](#).

10. Internal circuitry

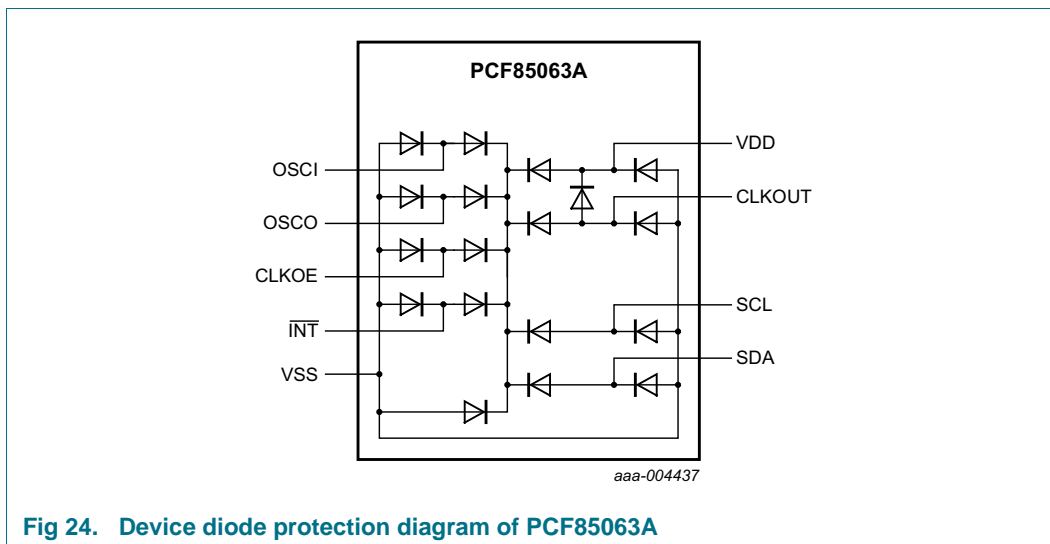


Fig 24. Device diode protection diagram of PCF85063A

11. Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

12. Limiting values

Table 40. Limiting values^[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------------|-------------------------------|------|-------|------|
| V _{DD} | supply voltage | | −0.5 | +6.5 | V |
| I _{DD} | supply current | | −50 | +50 | mA |
| V _I | input voltage | on pins SCL, SDA, OSCI, CLKOE | −0.5 | +6.5 | V |
| V _O | output voltage | | −0.5 | +6.5 | V |
| I _I | input current | at any input | −10 | +10 | mA |
| I _O | output current | at any output | −10 | +10 | mA |
| P _{tot} | total power dissipation | | - | 300 | mW |
| V _{ESD} | electrostatic discharge voltage | HBM ^[2] | - | ±5000 | V |
| | | CDM ^[3] | | | |
| | | PCF85063ATL | - | ±1750 | V |
| | | PCF85063AT | - | ±2000 | V |
| | | PCF85063ATT | - | ±2000 | V |
| I _{IU} | latch-up current | ^[4] | - | 200 | mA |
| T _{stg} | storage temperature | ^[5] | −65 | +150 | °C |
| T _{amb} | ambient temperature | operating device | −40 | +85 | °C |

[1] Remark: The PCF85063A part is not guaranteed (nor characterized) above the operating range as denoted in the datasheet. NXP recommends not to bias the PCF85063A device during reflow (e.g. if utilizing a 'coin' type battery in the assembly). If customer so chooses to continue to use this assembly method, there must be the allowance for a full '0 V' level Power supply 'reset' to re-enable the device. Without a proper POR, the device may remain in an indeterminate state.

[2] Pass level; Human Body Model (HBM) according to [Ref. 7 "JESD22-A114"](#).

[3] Pass level; Charged-Device Model (CDM), according to [Ref. 8 "JESD22-C101"](#).

[4] Pass level; latch-up testing, according to [Ref. 9 "JESD78"](#) at maximum ambient temperature (T_{amb(max)}).

[5] According to the store and transport requirements (see [Ref. 18 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

13. Characteristics

Table 41. Static characteristics

$V_{DD} = 0.9\text{ V}$ to 5.5 V ; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 60\text{ k}\Omega$; $C_L = 7\text{ pF}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---------------------------|---|--------------------|-----|---------------------|------|
| Supplies | | | | | | |
| V _{DD} | supply voltage | interface inactive; [1] f _{SCL} = 0 Hz | 0.9 | - | 5.5 | V |
| | | interface active; [2] f _{SCL} = 400 kHz | 1.8 | - | 5.5 | V |
| I _{DD} | supply current | CLKOUT disabled; [3] V _{DD} = 3.3 V | | | | |
| | | interface inactive; f _{SCL} = 0 Hz | | | | |
| | | T _{amb} = 25 °C | - | 220 | 450 | nA |
| | | T _{amb} = 50 °C [4] | - | 250 | 500 | nA |
| | | T _{amb} = 85 °C | - | 470 | 600 | nA |
| | | interface active; f _{SCL} = 400 kHz | - | 18 | 50 | μA |
| Inputs [5] | | | | | | |
| V _I | input voltage | | −0.5 | - | +5.5 | V |
| V _{IL} | LOW-level input voltage | | −0.5 | - | +0.3V _{DD} | V |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DD} | - | 5.5 | V |
| I _{LI} | input leakage current | V _I = V _{SS} or V _{DD} | - | 0 | - | μA |
| | | post ESD event | −0.15 | - | +0.15 | μA |
| C _i | input capacitance | [6] | - | - | 7 | pF |
| Outputs | | | | | | |
| V _{OH} | HIGH-level output voltage | on pin CLKOUT | 0.8V _{DD} | - | V _{DD} | V |
| V _{OL} | LOW-level output voltage | on pins SDA, $\overline{\text{INT}}$, CLKOUT | V _{SS} | - | 0.2V _{DD} | V |
| I _{OH} | HIGH-level output current | output source current; V _{OH} = 2.9 V; V _{DD} = 3.3 V; on pin CLKOUT | 1 | 3 | - | mA |
| I _{OL} | LOW-level output current | output sink current; V _{OL} = 0.4 V; V _{DD} = 3.3 V | | | | |
| | | on pin SDA | 3 | 8.5 | - | mA |
| | | on pin $\overline{\text{INT}}$ | 2 | 6 | - | mA |
| | | on pin CLKOUT | 1 | 3 | - | mA |

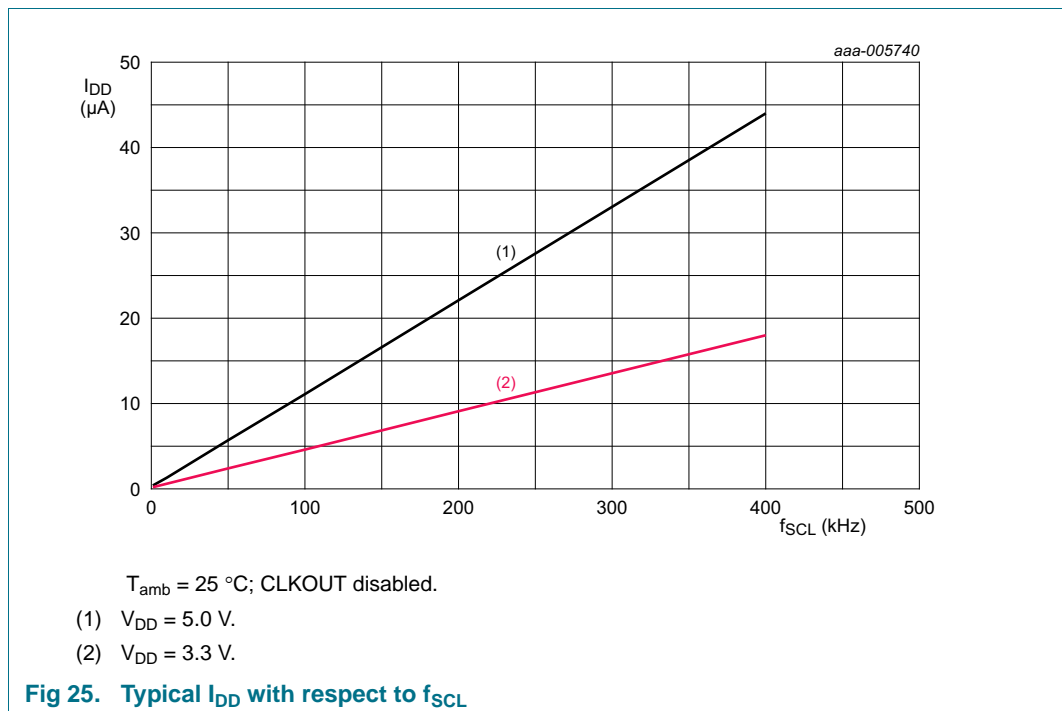
Table 41. Static characteristics ...continued

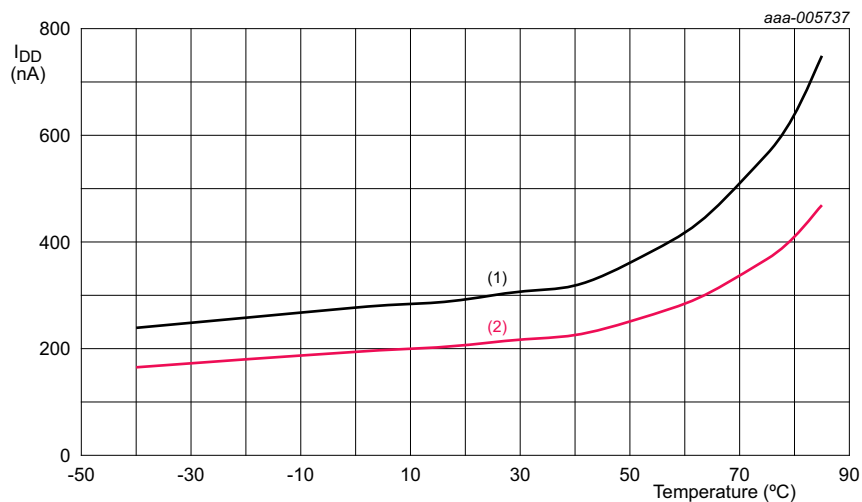
$V_{DD} = 0.9 \text{ V to } 5.5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$; $f_{osc} = 32.768 \text{ kHz}$; quartz $R_s = 60 \text{ k}\Omega$; $C_L = 7 \text{ pF}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|---|---|-----|-------|------|------------|
| Oscillator | | | | | | |
| $\Delta f_{osc}/f_{osc}$ | relative oscillator frequency variation | $\Delta V_{DD} = 200 \text{ mV}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$ | - | 0.075 | - | ppm |
| $C_{L(itg)}$ | integrated load capacitance | on pins OSC0, OSC1 [7] | | | | |
| | | $C_L = 7 \text{ pF}$ | 4.2 | 7 | 9.8 | pF |
| | | $C_L = 12.5 \text{ pF}$ | 7.5 | 12.5 | 17.5 | pF |
| R_s | series resistance | | - | - | 100 | k Ω |

- [1] For reliable oscillator start-up at power-on use V_{DD} greater than 1.2 V. If powered up at 0.9 V the oscillator will start but it might be a bit slow, especially if at high temperature. Normally the power supply is not 0.9 V at start-up and only comes at the end of battery discharge. V_{DD} min of 0.9 V is specified so that the customer can calculate how large a battery or capacitor they need for their application. V_{DD} min of 1.2 V or greater is needed to ensure speedy oscillator start-up time. For a restart condition, NXP recommends a full '0 V' V_{DD} value upon re-biasing.
- [2] 400 kHz I2C operation is production tested at 1.8 V. Design methodology allows I2C operation at 1.8 V – 5 % (1.71 V) which has been verified during product characterization on a limited number of devices.
- [3] Timer source clock = $\frac{1}{60}$ Hz, level of pins SCL and SDA is V_{DD} or V_{SS} .
- [4] Tested on sample basis.
- [5] The I²C-bus interface of PCF85063A is 5 V tolerant.
- [6] Implicit by design.

- [7] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

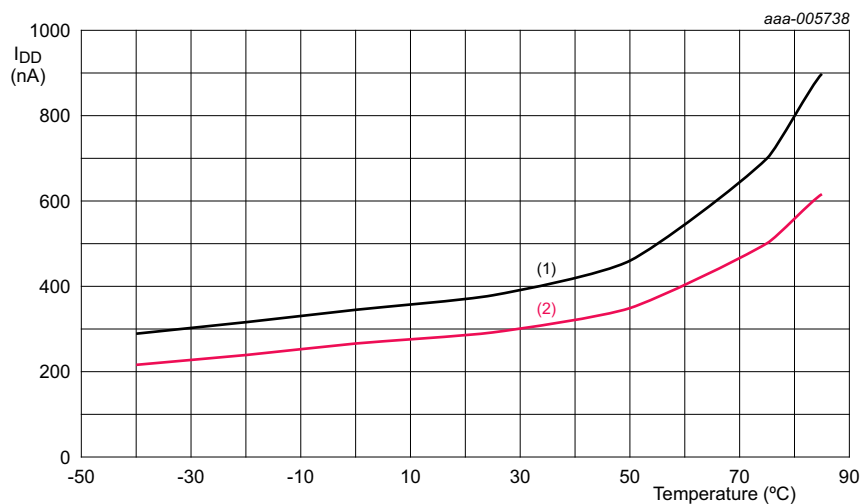




$C_{L(itg)} = 7 \text{ pF}$; CLKOUT disabled.

(1) $V_{DD} = 5.5 \text{ V}$.

(2) $V_{DD} = 3.3 \text{ V}$.

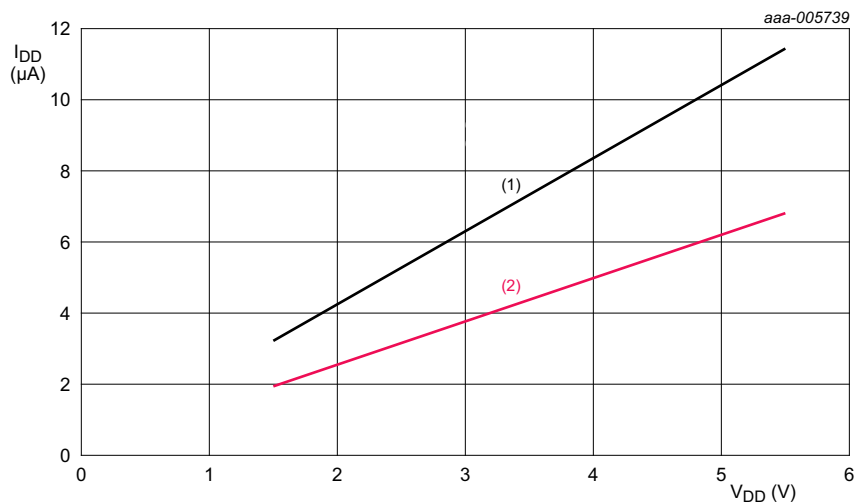


$C_{L(itg)} = 12.5 \text{ pF}$; CLKOUT disabled.

(1) $V_{DD} = 5.5 \text{ V}$.

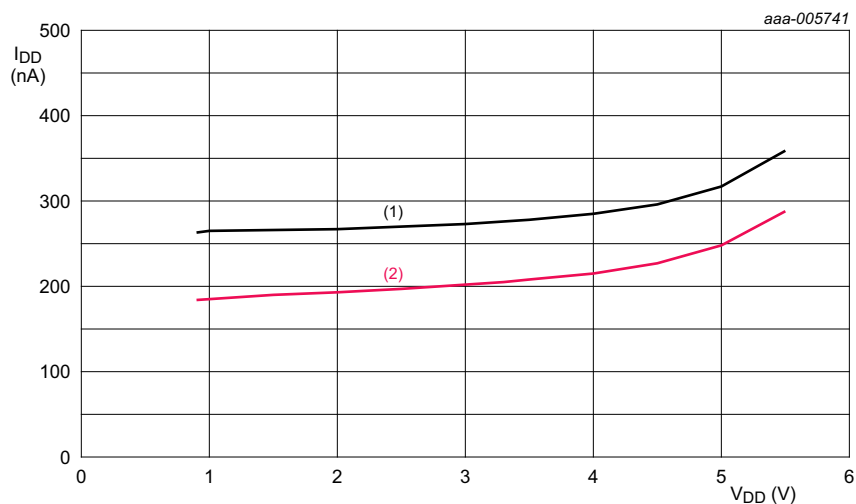
(2) $V_{DD} = 3.3 \text{ V}$.

Fig 26. Typical I_{DD} as a function of temperature



$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $f_{\text{CLKOUT}} = 32768\text{ Hz}$.

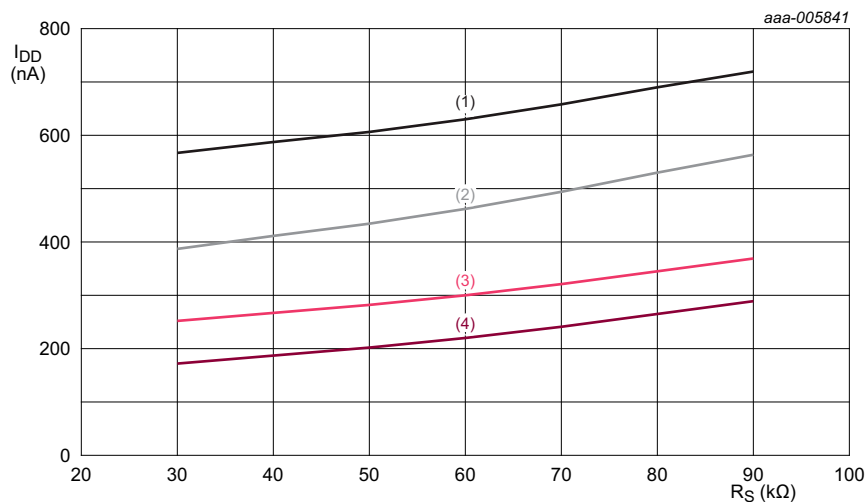
- (1) 47 pF CLKOUT load.
- (2) 22 pF CLKOUT load.



$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; CLKOUT disabled.

- (1) $C_{L(\text{itg})} = 12.5\text{ pF}$.
- (2) $C_{L(\text{itg})} = 7\text{ pF}$.

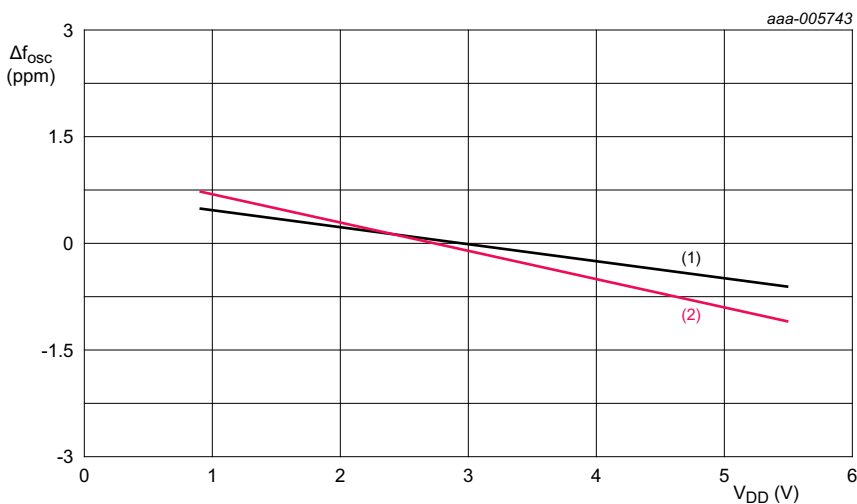
Fig 27. Typical I_{DD} with respect to V_{DD}



$V_{DD} = 3.3$ V; CLKOUT disabled.

- (1) $C_{L(itg)} = 12.5$ pF; 50 °C; maximum value.
- (2) $C_{L(itg)} = 7$ pF; 50 °C; maximum value.
- (3) $C_{L(itg)} = 12.5$ pF; 25 °C; typical value.
- (4) $C_{L(itg)} = 7$ pF; 25 °C; typical value.

Fig 28. I_{DD} with respect to quartz R_S



$T_{amb} = 25$ °C.

- (1) $C_{L(itg)} = 7$ pF.
- (2) $C_{L(itg)} = 12.5$ pF.

Fig 29. Oscillator frequency variation with respect to V_{DD}

Table 42. I²C-bus characteristics

$V_{DD} = 1.8 \text{ V to } 5.5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$; $f_{osc} = 32.768 \text{ kHz}$; quartz $R_s = 60 \text{ k}\Omega$; $C_L = 7 \text{ pF}$; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} ^[1].

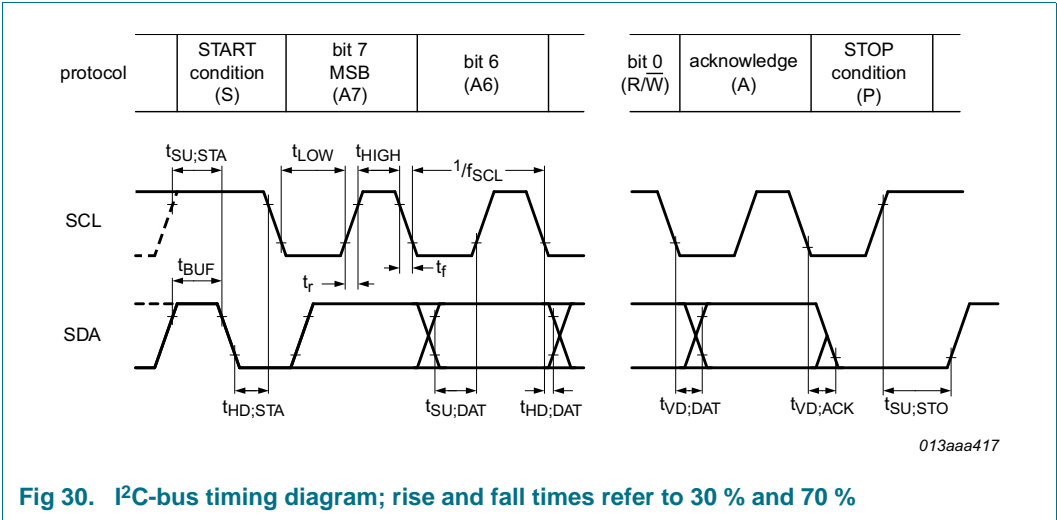
| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|---|------------|--------------------------------------|-----|---------------|
| C_b | capacitive load for each bus line | | - | 400 | pF |
| f_{SCL} | SCL clock frequency | [2] | 0 | 400 | kHz |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 0.6 | - | μs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 0.6 | - | μs |
| t_{LOW} | LOW period of the SCL clock | | 1.3 | - | μs |
| t_{HIGH} | HIGH period of the SCL clock | | 0.6 | - | μs |
| t_r | rise time of both SDA and SCL signals | | 20 | 300 | ns |
| t_f | fall time of both SDA and SCL signals | [3][4] | $20 \times (V_{DD} / 5.5 \text{ V})$ | 300 | ns |
| t_{BUF} | bus free time between a STOP and START condition | | 1.3 | - | μs |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | 0.6 | - | μs |
| $t_{VD;DAT}$ | data valid time | | 0 | 0.9 | μs |
| $t_{VD;ACK}$ | data valid acknowledge time | | 0 | 0.9 | μs |
| t_{SP} | pulse width of spikes that must be suppressed by the input filter | | 0 | 50 | ns |

[1] A detailed description of the I²C-bus specification is given in [Ref. 16 "UM10204"](#).

[2] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

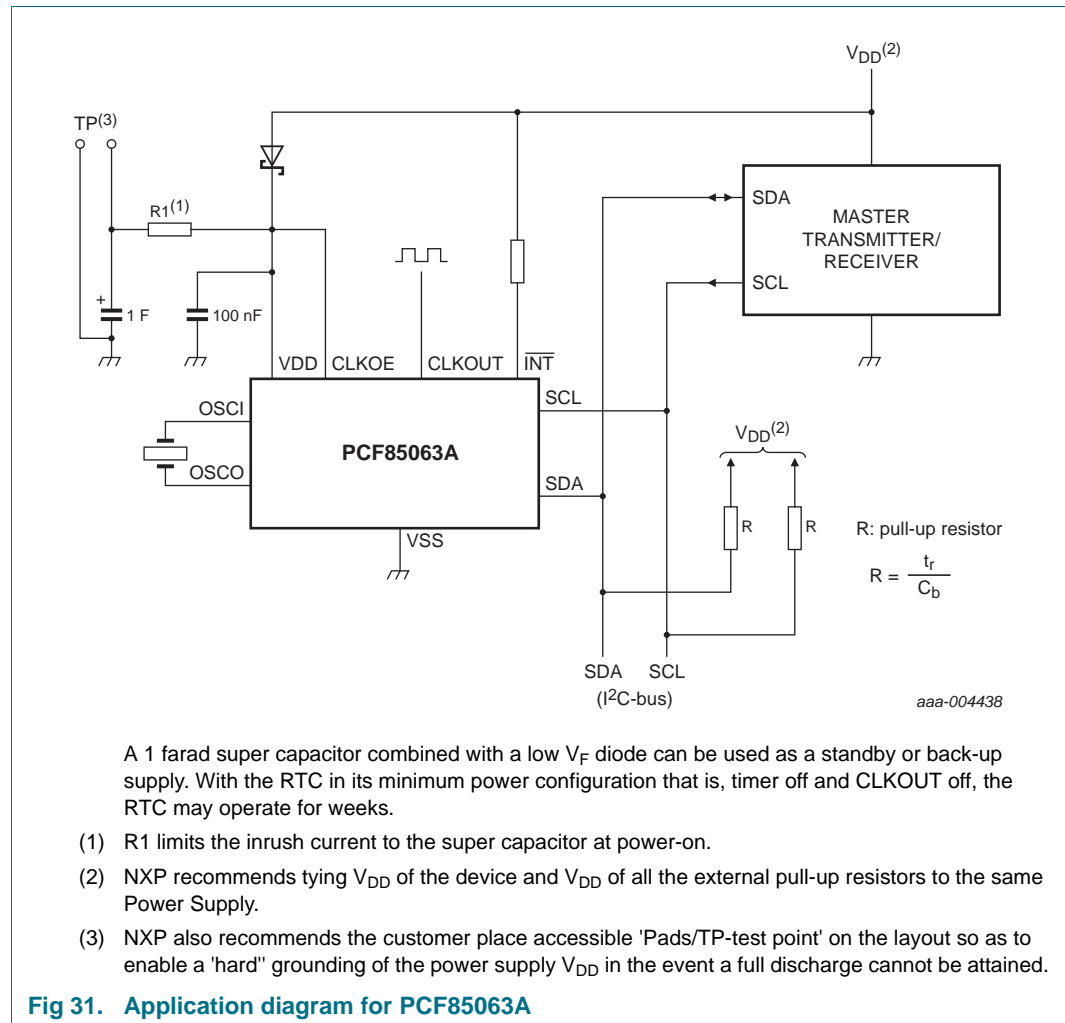
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .



14. Application information

The data sheet values were obtained using a crystal with an ESR of 60 kΩ. If a crystal with an ESR of 70 kΩ is used then the power consumption would increase by a few nA and the start-up time will increase slightly.



15. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

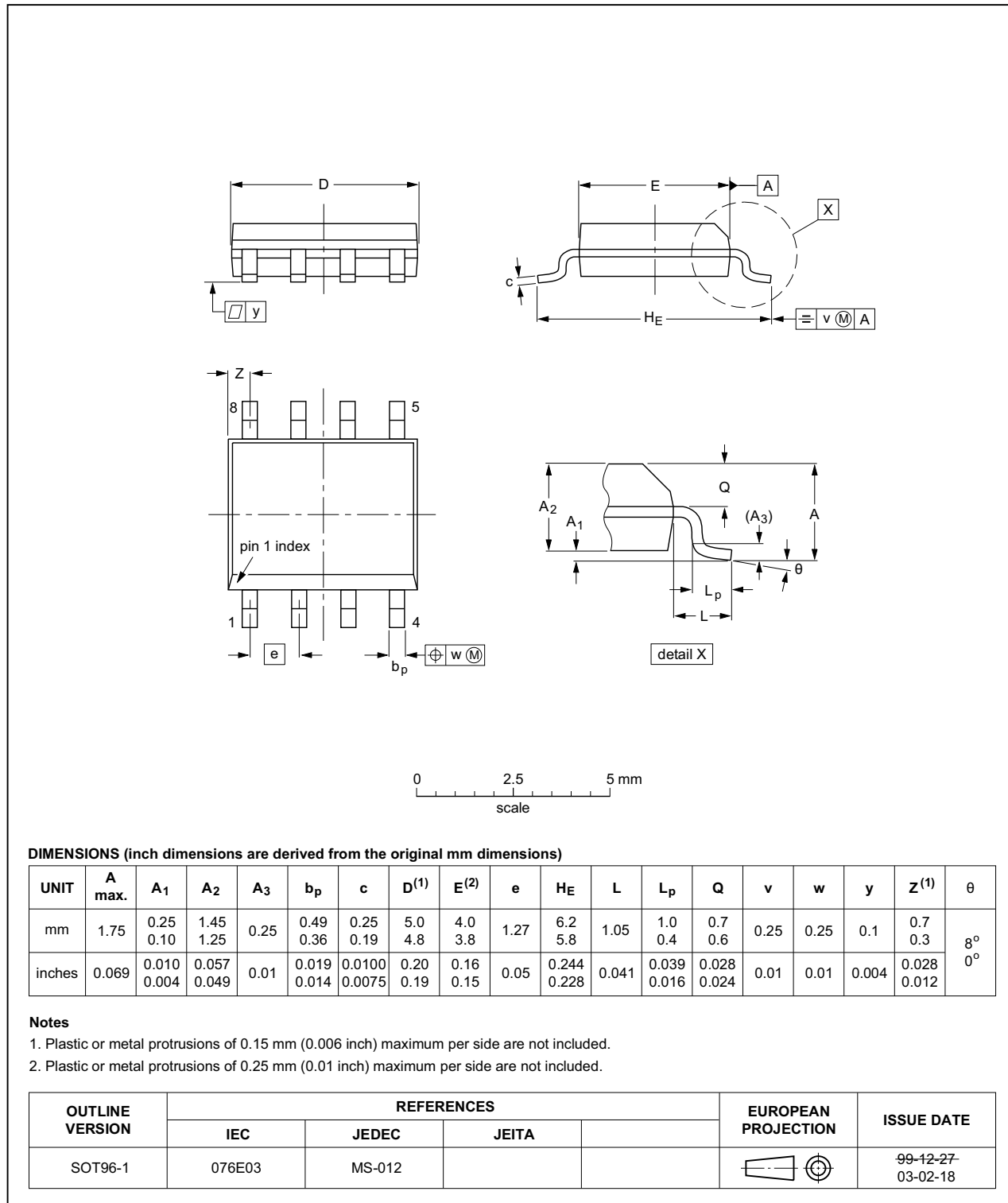


Fig 32. Package outline SOT96-1 (SO8) of PCF85063AT

DFN2626-10: plastic thermal enhanced extremely thin small outline package; no leads;
10 terminals; body 2.6 x 2.6 x 0.5 mm

SOT1197-1

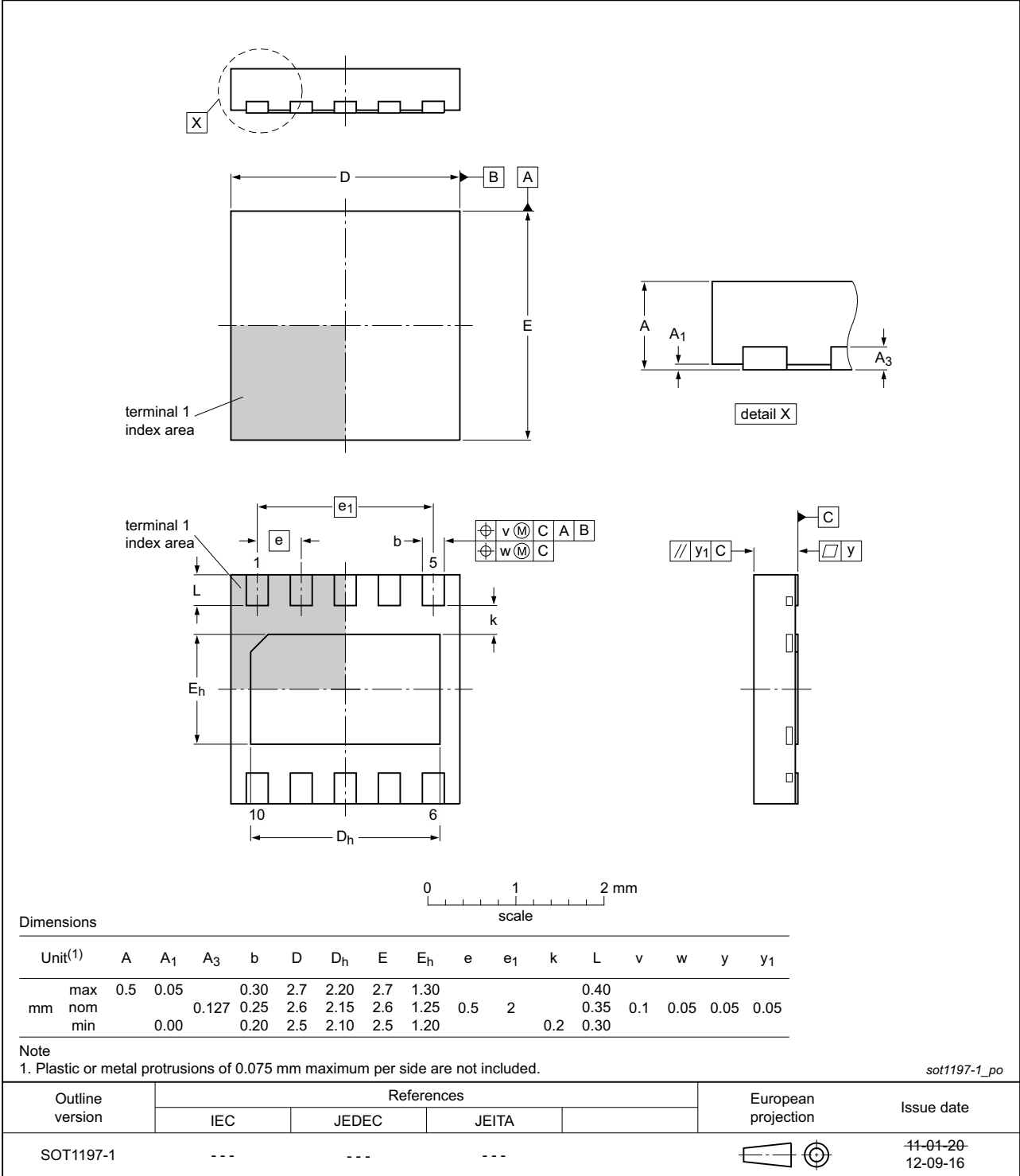


Fig 33. Package outline SOT1197-1 (DFN2626-10) of PCF85063ATL

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

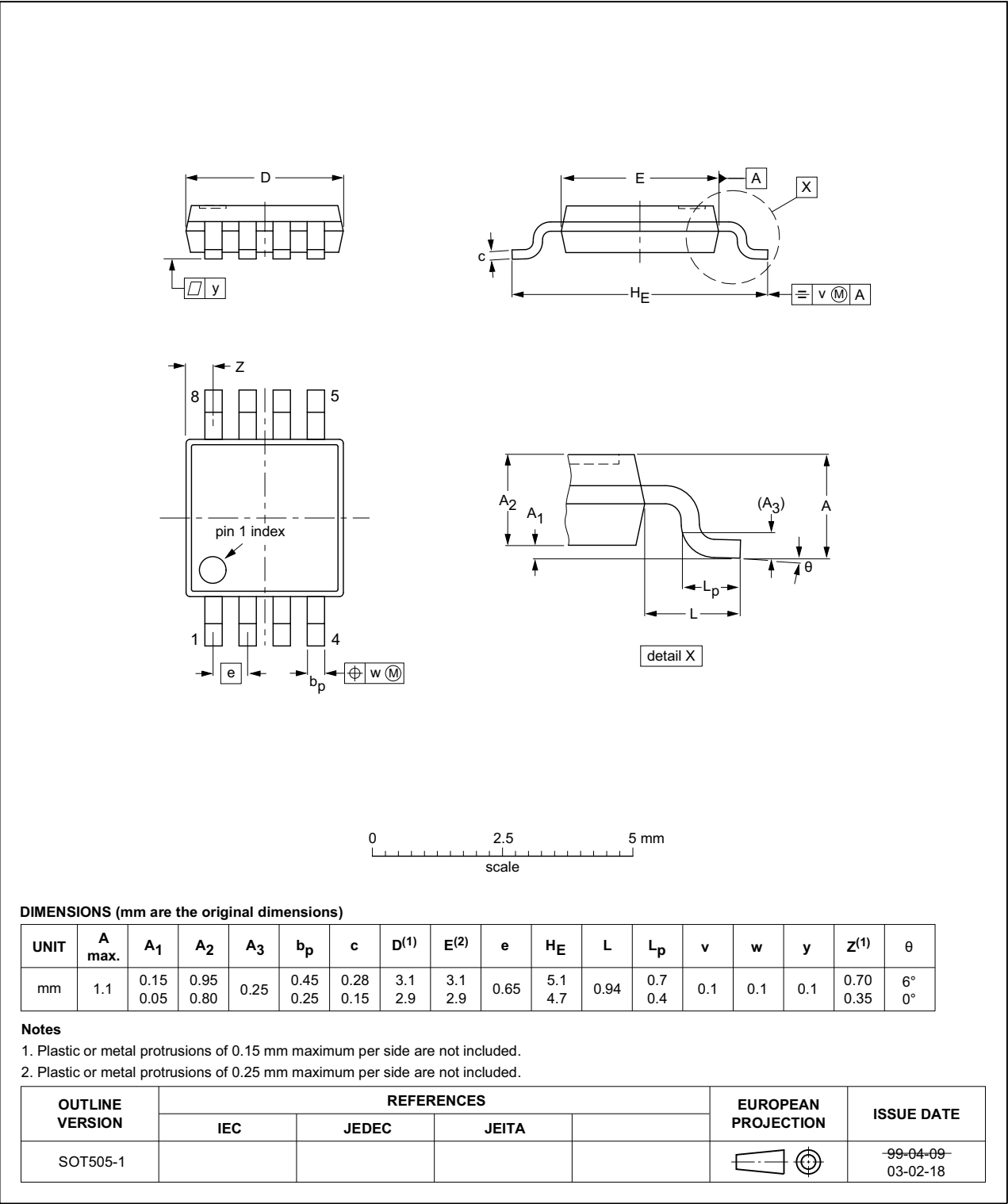


Fig 34. Package outline SOT505-1 (TSSOP8) of PCF85063ATT

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tape and reel information

For tape and reel packing information, please see for

PCF85063AT — [Ref. 12 "SOT96-1_515"](#) and [Ref. 13 "SOT96-1_518"](#)

PCF85063ATL — [Ref. 15 "SOT1197-1_115"](#)

PCF85063ATT — [Ref. 14 "SOT505-1_118"](#)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 35](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 43](#) and [44](#)

Table 43. SnPb eutectic process (from J-STD-020D)

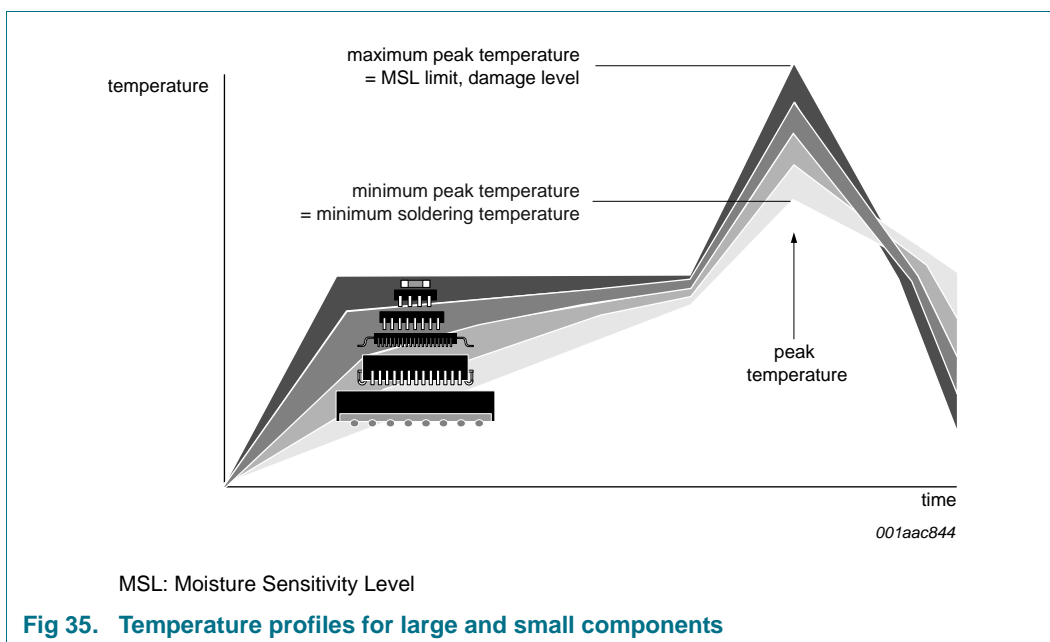
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 44. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

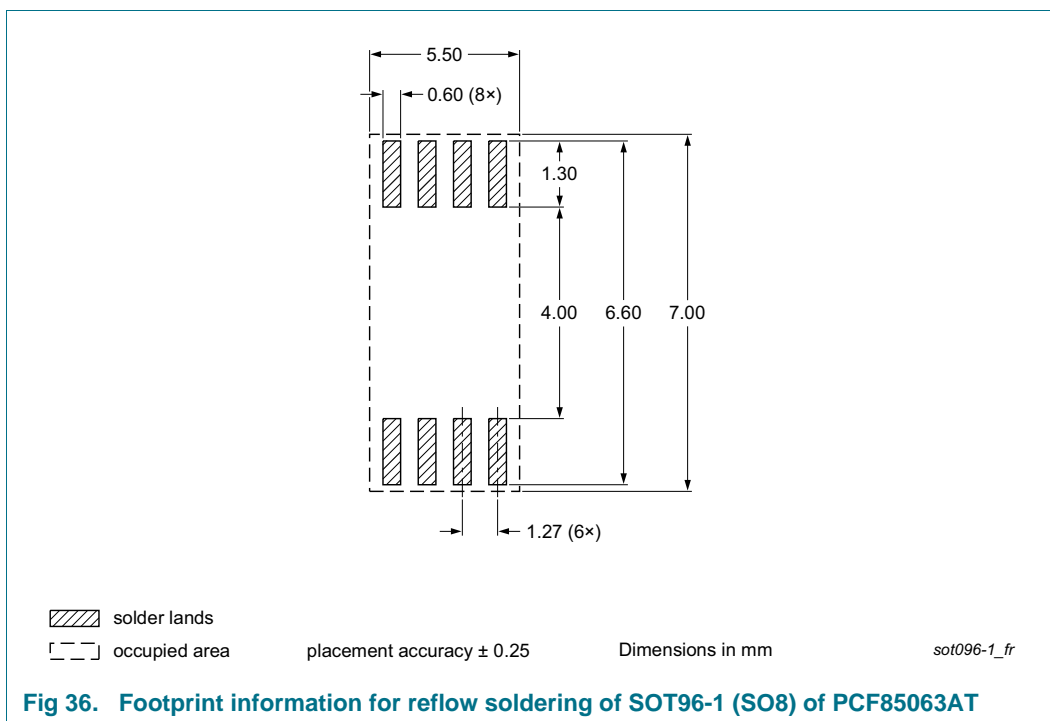
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 35](#).



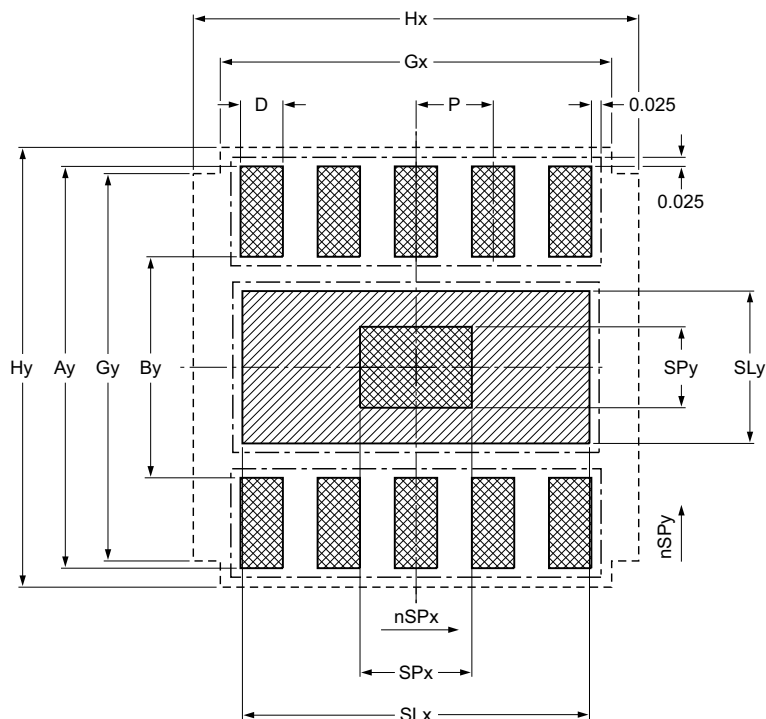
For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

19. Footprint information






Footprint information for reflow soldering of DFN2626-10 package

SOT1197-1



Generic footprint pattern
Refer to the package outline drawing for actual layout

-  solder land
-  solder paste deposit
-  solder land plus solder paste
- occupied area
- solder resist

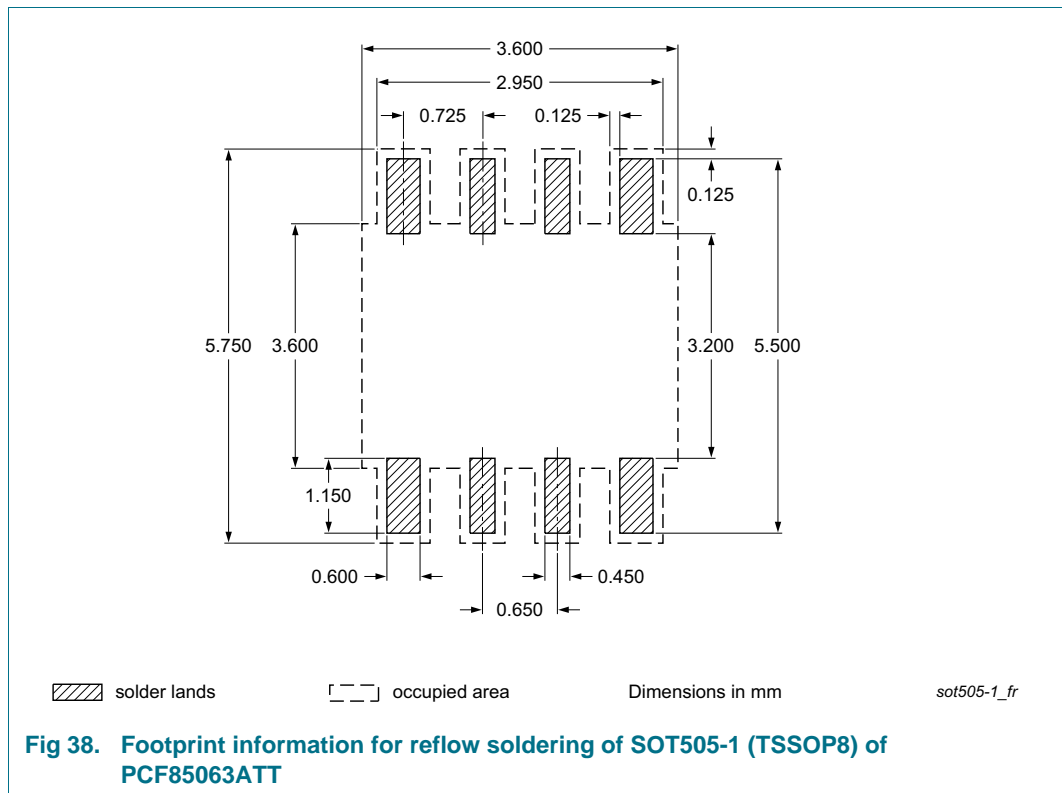
DIMENSIONS in mm

| P | Ay | By | D | SLx | SLy | SPx | SPy | Gx | Gy | Hx | Hy |
|-----|------|-----|------|-----|-----|-----|-----|-----|------|------|-----|
| 0.5 | 3.05 | 1.9 | 0.25 | 2.2 | 1.3 | 0.8 | 0.4 | 2.5 | 2.85 | 2.85 | 3.3 |

Issue date ~~11-07-27~~
12-09-16

sot1197-1_fr

Fig 37. Footprint information for reflow soldering of SOT1197-1 (DFN2626-10) of PCF85063ATL



20. Appendix

20.1 Real-Time Clock selection

Table 45. Selection of Real-Time Clocks

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface | I _{DD} , typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features | Packages |
|------------|------------------------|------------------|------------------|--------------------------------|----------------|-------------------------|--------------------|---|----------------------------------|
| PCF85063TP | - | 1 | I ² C | 220 | - | - | - | basic functions only, no alarm | HXSON8 |
| PCF85063A | X | 1 | I ² C | 220 | - | - | - | tiny package | SO8, DFN2626-10, TSSOP8 |
| PCF85063B | X | 1 | SPI | 220 | - | - | - | tiny package | DFN2626-10 |
| PCF85263A | X | 2 | I ² C | 230 | X | X | - | time stamp, battery backup, stopwatch 1/100 s | SO8, TSSOP10, TSSOP8, DFN2626-10 |
| PCF85263B | X | 2 | SPI | 230 | X | X | - | time stamp, battery backup, stopwatch 1/100s | TSSOP10, DFN2626-10 |
| PCF85363A | X | 2 | I ² C | 230 | X | X | - | time stamp, battery backup, stopwatch 1/100s, 64 Byte RAM | TSSOP10, TSSOP8, DFN2626-10 |
| PCF85363B | X | 2 | SPI | 230 | X | X | - | time stamp, battery backup, stopwatch 1/100s, 64 Byte RAM | TSSOP10, DFN2626-10 |
| PCF2123 | X | 1 | SPI | 100 | - | - | - | lowest power 100 nA in operation | TSSOP14, HVQFN16 |
| PCF8523 | X | 2 | I ² C | 150 | X | - | - | lowest power 150 nA in operation, FM+ 1 MHz | SO8, HVSON8, TSSOP14, WLCSP |
| PCF8563 | X | 1 | I ² C | 250 | - | - | - | - | SO8, TSSOP8, HVSON10 |
| PCA8565 | X | 1 | I ² C | 600 | - | - | grade 1 | high robustness, T _{amb} = -40 °C to 125 °C | TSSOP8, HVSON10 |
| PCA8565A | X | 1 | I ² C | 600 | - | - | - | integrated oscillator caps, T _{amb} = -40 °C to 125 °C | WLCSP |
| PCF8564A | X | 1 | I ² C | 250 | - | - | - | integrated oscillator caps | WLCSP |

Table 45. Selection of Real-Time Clocks ...continued

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface | I _{DD} , typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features | Packages |
|-----------|------------------------|------------------|--------------------------|--------------------------------|----------------|-------------------------|--------------------|--|----------|
| PCF2127 | X | 1 | I ² C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO16 |
| PCF2127A | X | 1 | I ² C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO20 |
| PCF2129 | X | 1 | I ² C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated | SO16 |
| PCF2129A | X | 1 | I ² C and SPI | 500 | X | X | - | temperature compensated, quartz built in, calibrated | SO20 |
| PCA2129 | X | 1 | I ² C and SPI | 500 | X | X | grade 3 | temperature compensated, quartz built in, calibrated | SO16 |
| PCA21125 | X | 1 | SPI | 820 | - | - | grade 1 | high robustness, T _{amb} = -40 °C to 125 °C | TSSOP14 |

21. Abbreviations

Table 46. Abbreviations

| Acronym | Description |
|------------------|---|
| BCD | Binary Coded Decimal |
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I ² C | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| RTC | Real-Time Clock |
| SCL | Serial CLock line |
| SDA | Serial DATa line |
| SMD | Surface Mount Device |

22. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10366** — HVQFN application information
- [3] **AN11247** — Improved timekeeping accuracy with PCF85063, PCF8523 and PCF2123 using an external temperature sensor
- [4] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [5] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [6] **IPC/JEDEC J-STD-020** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [7] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [8] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [9] **JESD78** — IC Latch-Up Test
- [10] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [11] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [12] **SOT96-1_515** — SO8; Reel pack; SMD, 7", packing information
- [13] **SOT96-1_518** — SO8; Reel pack; SMD, 13", packing information
- [14] **SOT505-1_118** — TSSOP8; Reel pack; SMD, 13", packing information
- [15] **SOT1197-1_115** — DFN2626-10; Reel pack; SMD, 7", packing information
- [16] **UM10204** — I²C-bus specification and user manual
- [17] **UM10301** — User Manual for NXP Real Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125
- [18] **UM10569** — Store and transport requirements
- [19] **UM10788** — User manual for I²C-bus RTC demo board OM13515

23. Revision history

Table 47. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|---|--------------------|---------------|-----------------|
| PCF85063A v.7 | 20180330 | Product data sheet | 201801014IU01 | PCF85063A v.6 |
| Modifications: | <ul style="list-style-type: none"> • Table 4 "Pin description": Added Table note 2 to INT, SDA, and SCL • Added Section 9.5.2.1 "I²C-bus error recovery technique" • Table 41 "Static characteristics": Updated Table note 1 • Updated Figure 31 "Application diagram for PCF85063A"; added Figure note 2 and Figure note 3 • Table 40 "Limiting values[1]": Added Table note 1 • Clarified reset information in Section 8.2 and Section 8.2.1.3. | | | |
| PCF85063A v.6 | 20151118 | Product data sheet | - | PCF85063A v.5 |
| Modifications: | <ul style="list-style-type: none"> • Updated Table 4 "Pin description" Table note 1 • Adjusted Section 8.2.2.4 paragraph 2 • Updated Table 11 "CLKOUT frequency selection" Table note 2 • Table 41 "Static characteristics": <ul style="list-style-type: none"> – Corrected V_I min from V_{SS} to -0.5 V – Corrected V_{IL} min from V_{SS} to -0.5 V – Corrected V_{IH} max from V_{DD} to 5.5 V – Corrected Table note 1 – Added Table note 2 • Added text to Section 14 "Application information" | | | |
| PCF85063A v.5 | 20150506 | Product data sheet | - | PCF85063A v.4 |
| Modifications: | <ul style="list-style-type: none"> • Added the 7" reel delivery form for PCF85063AT • Adjusted Section 8.2.2.2 | | | |
| PCF85063A v.4 | 20141124 | Product data sheet | - | PCF85063A v.3 |
| PCF85063A v.3 | 20140604 | Product data sheet | - | PCF85063A v.2 |
| PCF85063ATL v.2 | 20130415 | Product data sheet | - | PCF85063ATL v.1 |
| PCF85063ATL v.1 | 20130225 | Product data sheet | - | - |

24. Legal information

24.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

24.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

24.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

24.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

25. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

26. Tables

| | | | | | |
|-----------|--|----|-----------|--|----|
| Table 1. | Ordering information | 2 | Table 37. | First period delay for timer counter value T | 31 |
| Table 2. | Ordering options | 2 | Table 38. | INT operation | 32 |
| Table 3. | Marking codes | 2 | Table 39. | I ² C slave address byte | 35 |
| Table 4. | Pin description | 5 | Table 40. | Limiting values | 38 |
| Table 5. | Registers overview | 7 | Table 41. | Static characteristics | 39 |
| Table 6. | Control_1 - control and status register 1 (address 00h) bit description | 8 | Table 42. | I ² C-bus characteristics | 44 |
| Table 7. | First increment of time circuits after STOP bit release | 11 | Table 43. | SnPb eutectic process (from J-STD-020D) | 52 |
| Table 8. | Registers reset values | 12 | Table 44. | Lead-free process (from J-STD-020D) | 52 |
| Table 9. | Control_2 - control and status register 2 (address 01h) bit description | 13 | Table 45. | Selection of Real-Time Clocks | 56 |
| Table 10. | Effect of bits MI and HMI on INT generation | 15 | Table 46. | Abbreviations | 58 |
| Table 11. | CLKOUT frequency selection | 16 | Table 47. | Revision history | 60 |
| Table 12. | Offset - offset register (address 02h) bit description | 17 | | | |
| Table 13. | Offset values | 17 | | | |
| Table 14. | Correction pulses for MODE = 0 | 18 | | | |
| Table 15. | Effect of correction pulses on frequencies for MODE = 0 | 18 | | | |
| Table 16. | Correction pulses for MODE = 1 | 19 | | | |
| Table 17. | Effect of correction pulses on frequencies for MODE = 1 | 19 | | | |
| Table 18. | RAM_byte - 8-bit RAM register (address 03h) bit description | 21 | | | |
| Table 19. | Seconds - seconds register (address 04h) bit description | 21 | | | |
| Table 20. | Seconds coded in BCD format | 22 | | | |
| Table 21. | Minutes - minutes register (address 05h) bit description | 23 | | | |
| Table 22. | Hours - hours register (address 06h) bit description | 23 | | | |
| Table 23. | Days - days register (address 07h) bit description | 23 | | | |
| Table 24. | Weekdays - weekdays register (address 08h) bit description | 23 | | | |
| Table 25. | Weekday assignments | 24 | | | |
| Table 26. | Months - months register (address 09h) bit description | 24 | | | |
| Table 27. | Month assignments in BCD format | 24 | | | |
| Table 28. | Years - years register (0Ah) bit description | 25 | | | |
| Table 29. | Second_alarm - second alarm register (address 0Bh) bit description | 26 | | | |
| Table 30. | Minute_alarm - minute alarm register (address 0Ch) bit description | 27 | | | |
| Table 31. | Hour_alarm - hour alarm register (address 0Dh) bit description | 27 | | | |
| Table 32. | Day_alarm - day alarm register (address 0Eh) bit description | 27 | | | |
| Table 33. | Weekday_alarm - weekday alarm register (address 0Fh) bit description | 28 | | | |
| Table 34. | Timer_value - timer value register (address 10h) bit description | 29 | | | |
| Table 35. | Timer_mode - timer control register (address 11h) bit description | 30 | | | |
| Table 36. | Timer clock frequency and timer durations | 30 | | | |

27. Figures

| | | |
|---------|---|----|
| Fig 1. | Block diagram of PCF85063A | 3 |
| Fig 2. | Pin configuration for SO8 (PCF85063AT) | 4 |
| Fig 3. | Pin configuration for DFN2626-10 (PCF85063ATL) | 4 |
| Fig 4. | Pin configuration for TSSOP8 (PCF85063ATT) | 4 |
| Fig 5. | Handling address registers | 6 |
| Fig 6. | STOP bit functional diagram | 10 |
| Fig 7. | STOP bit release timing | 11 |
| Fig 8. | Software reset command | 12 |
| Fig 9. | Interrupt scheme | 14 |
| Fig 10. | INT example for MI | 15 |
| Fig 11. | Offset calibration calculation workflow | 20 |
| Fig 12. | Result of offset calibration | 21 |
| Fig 13. | OS flag | 22 |
| Fig 14. | Data flow for the time function | 25 |
| Fig 15. | Access time for read/write operations | 26 |
| Fig 16. | Alarm function block diagram | 29 |
| Fig 17. | General countdown timer behavior | 31 |
| Fig 18. | Bit transfer | 33 |
| Fig 19. | Definition of START and STOP conditions | 33 |
| Fig 20. | System configuration | 34 |
| Fig 21. | Acknowledgement on the I ² C-bus | 34 |
| Fig 22. | Master transmits to slave receiver (WRITE mode) | 35 |
| Fig 23. | Master reads after setting register address (write register address; READ data) | 36 |
| Fig 24. | Device diode protection diagram of PCF85063A | 37 |
| Fig 25. | Typical I _{DD} with respect to f _{SCL} | 40 |
| Fig 26. | Typical I _{DD} as a function of temperature | 41 |
| Fig 27. | Typical I _{DD} with respect to V _{DD} | 42 |
| Fig 28. | I _{DD} with respect to quartz R _S | 43 |
| Fig 29. | Oscillator frequency variation with respect to V _{DD} | 43 |
| Fig 30. | I ² C-bus timing diagram; rise and fall times refer to 30 % and 70 % | 45 |
| Fig 31. | Application diagram for PCF85063A | 46 |
| Fig 32. | Package outline SOT96-1 (SO8) of PCF85063AT | 47 |
| Fig 33. | Package outline SOT1197-1 (DFN2626-10) of PCF85063ATL | 48 |
| Fig 34. | Package outline SOT505-1 (TSSOP8) of PCF85063ATT | 49 |
| Fig 35. | Temperature profiles for large and small components | 53 |
| Fig 36. | Footprint information for reflow soldering of SOT96-1 (SO8) of PCF85063AT | 53 |
| Fig 37. | Footprint information for reflow soldering of SOT1197-1 (DFN2626-10) of PCF85063ATL | 54 |
| Fig 38. | Footprint information for reflow soldering of SOT505-1 (TSSOP8) of PCF85063ATT | 55 |

28. Contents

| | | | | | |
|----------|---|----------|-----------|--|-----------|
| 1 | General description | 1 | 8.6.2 | Register Timer_mode | 30 |
| 2 | Features and benefits | 1 | 8.6.3 | Timer functions | 30 |
| 3 | Applications | 1 | 8.6.3.1 | Countdown timer interrupts | 32 |
| 4 | Ordering information | 2 | 9 | Characteristics of the I²C-bus interface | 33 |
| 4.1 | Ordering options | 2 | 9.1 | Bit transfer | 33 |
| 5 | Marking | 2 | 9.2 | START and STOP conditions | 33 |
| 6 | Block diagram | 3 | 9.3 | System configuration | 33 |
| 7 | Pinning information | 4 | 9.4 | Acknowledge | 34 |
| 7.1 | Pinning | 4 | 9.5 | I ² C-bus protocol | 35 |
| 7.2 | Pin description | 5 | 9.5.1 | Addressing | 35 |
| 8 | Functional description | 6 | 9.5.2 | Clock and calendar READ or WRITE cycles . | 35 |
| 8.1 | Registers organization | 7 | 10 | Internal circuitry | 37 |
| 8.2 | Control registers | 8 | 11 | Safety notes | 37 |
| 8.2.1 | Register Control_1 | 8 | 12 | Limiting values | 38 |
| 8.2.1.1 | EXT_TEST: external clock test mode | 9 | 13 | Characteristics | 39 |
| 8.2.1.2 | STOP: STOP bit function | 10 | 14 | Application information | 46 |
| 8.2.1.3 | Software reset | 12 | 15 | Package outline | 47 |
| 8.2.2 | Register Control_2 | 13 | 16 | Handling information | 50 |
| 8.2.2.1 | Alarm interrupt | 14 | 17 | Packing information | 50 |
| 8.2.2.2 | MI and HMI: minute and half minute interrupt. | 15 | 17.1 | Tape and reel information | 50 |
| 8.2.2.3 | TF: timer flag | 15 | 18 | Soldering of SMD packages | 51 |
| 8.2.2.4 | COF[2:0]: Clock output frequency | 16 | 18.1 | Introduction to soldering | 51 |
| 8.2.3 | Register Offset | 17 | 18.2 | Wave and reflow soldering | 51 |
| 8.2.3.1 | Correction when MODE = 0 | 18 | 18.3 | Wave soldering | 51 |
| 8.2.3.2 | Correction when MODE = 1 | 19 | 18.4 | Reflow soldering | 52 |
| 8.2.3.3 | Offset calibration workflow | 20 | 19 | Footprint information | 53 |
| 8.2.4 | Register RAM_byte | 21 | 20 | Appendix | 56 |
| 8.3 | Time and date registers | 21 | 20.1 | Real-Time Clock selection | 56 |
| 8.3.1 | Register Seconds | 21 | 21 | Abbreviations | 58 |
| 8.3.1.1 | OS: Oscillator stop | 22 | 22 | References | 59 |
| 8.3.2 | Register Minutes | 23 | 23 | Revision history | 60 |
| 8.3.3 | Register Hours | 23 | 24 | Legal information | 61 |
| 8.3.4 | Register Days | 23 | 24.1 | Data sheet status | 61 |
| 8.3.5 | Register Weekdays | 23 | 24.2 | Definitions | 61 |
| 8.3.6 | Register Months | 24 | 24.3 | Disclaimers | 61 |
| 8.3.7 | Register Years | 25 | 24.4 | Trademarks | 62 |
| 8.4 | Setting and reading the time | 25 | 25 | Contact information | 62 |
| 8.5 | Alarm registers | 26 | 26 | Tables | 63 |
| 8.5.1 | Register Second_alarm | 26 | 27 | Figures | 64 |
| 8.5.2 | Register Minute_alarm | 27 | 28 | Contents | 65 |
| 8.5.3 | Register Hour_alarm | 27 | | | |
| 8.5.4 | Register Day_alarm | 27 | | | |
| 8.5.5 | Register Weekday_alarm | 28 | | | |
| 8.5.6 | Alarm function | 28 | | | |
| 8.6 | Timer registers | 29 | | | |
| 8.6.1 | Register Timer_value | 29 | | | |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9