Title	***Engineering Prototype Report for EP-71 – 6.6 W DC-DC Converter Using DPA-Switch™ (DPA423G)***
Specification	36-72 VDC Input, 3.3 V, 2 A Output
Application	Standby Supply for Distributed Power Architectures
Author	Power Integrations Applications Department
Document Number	EPR-71
Date	19-Jul-2005
Revision	1.2

Summary and Features

- High efficiency, low cost, low component count solution
- Ideally suited as a standby supply in a larger 48 V input system
- The *DPA-Switch* IC integrates
  - PWM controller and 220 V MOSFET switching device
  - Accurate 400 kHz trimmed internal oscillator
  - Accurate OV/UV protection
  - Hysteretic thermal shutdown
  - Overload, open loop and short-circuit protection
  - Cycle skipping for regulation at no-load without a minimum load
- Small footprint 1.85" × 1", low overall height 0.9", two-layer PCB
- 100% surface mount construction

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at *www.powerint.comT*.

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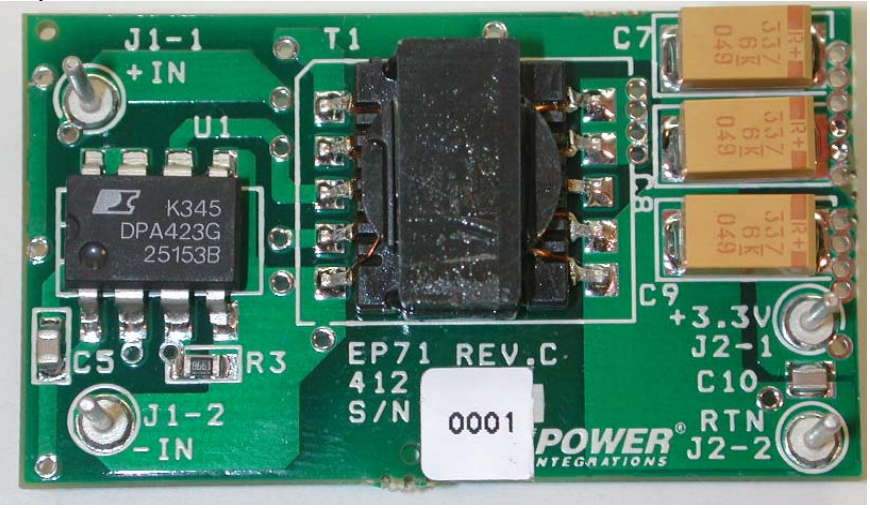
Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

1 Introduction

This document is an engineering report describing an isolated 3.3 V, 2 A (6.6 W) DC-DC converter utilizing a DPA423G. This design is intended as an evaluation platform for *DPA-Switch* devices in the 8-pin DIP, low cost surface-mount package. High operating efficiency, low parts count and small footprint make this circuit an ideal choice for standby supplies or other low power applications operating from telecom input voltages.

This report contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit board layout, and performance data.

Top Side



Bottom Side

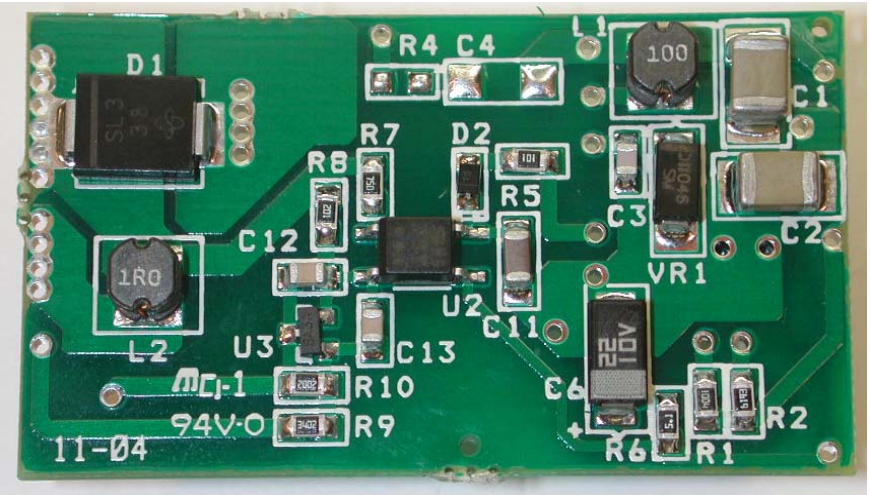


Figure 1 - EP-71 Populated Circuit Board Photograph.

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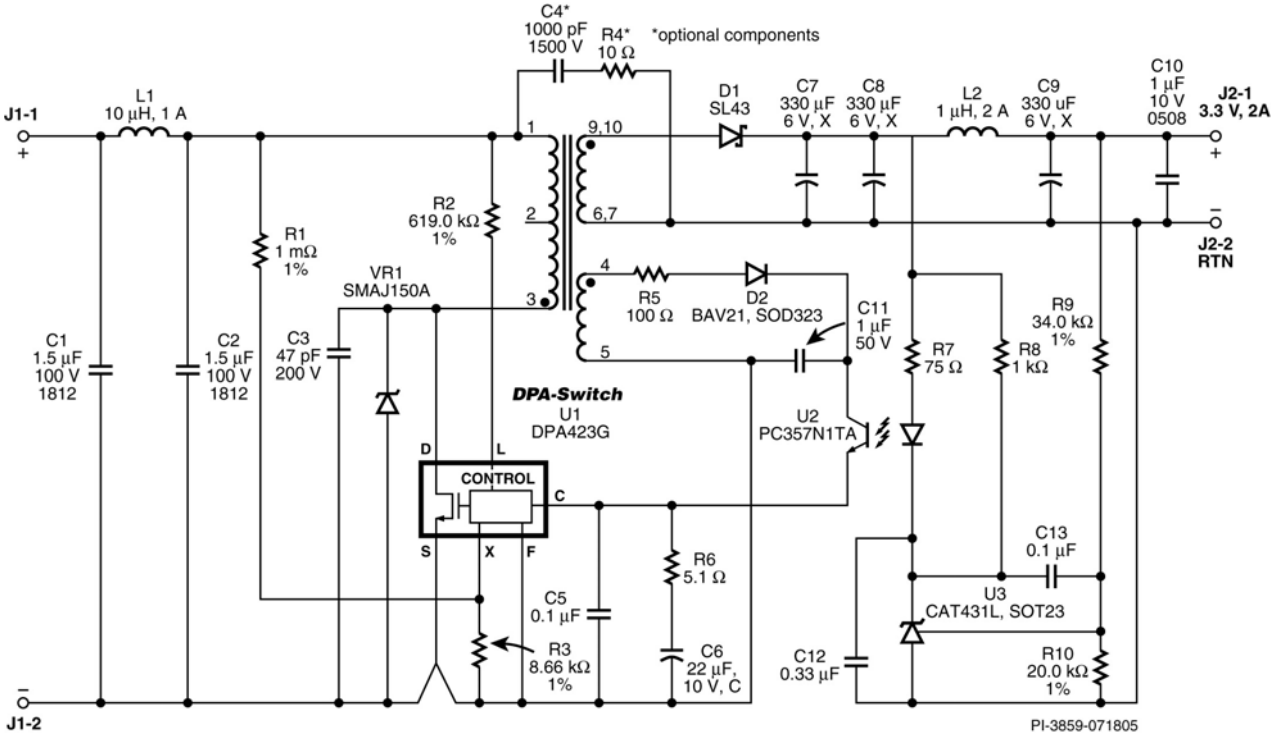
2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	36		72	VDC	OV shutdown at 90 V typ.
Output						
Output Voltage	V_{OUT1}	3.20	3.30	3.40	V	±3% including setpoint, line/load regulation
Output Ripple Voltage	$V_{RIPPLE1}$		35	50	mVpp	20 MHz bandwidth
Continuous Output Current	I_{OUT}	0		2.0	A	
Peak Output Current	I_{OUT}	2.0	2.5		A	
Total Output Power						
Continuous Output Power	P_{OUT}			6.6	W	
Peak Output Power	P_{OUT_PEAK}		8.25		W	
Efficiency	η	78	79		%	Measured at 48 V, P_{OUT} (6.6 W), 25 °C
Environmental						
Safety Isolation		1500			VDC	1 min.
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

3 Schematic



*All resistors and capacitors 0805 size unless specified otherwise

Figure 2 - EP-71 Schematic.

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4 Circuit Description

The schematic in Figure 2 shows a DC input flyback converter using the DPA423G device operating at 400 kHz. The circuit is designed for the standard nominal 48 V telecom input voltage range of 36-72 VDC. Using the Flyback topology, circuit board size, parts count and cost are minimized, while attaining excellent operating efficiency across the input voltage range.

4.1 Input Filtering

An input pi filter formed by C1, L1 and C2 reduces the input ripple current and high frequency noise. However additional external filtering may be required depending on applicable standards and specific application.

4.2 DPA-Switch Primary

The DPA423G IC (U1) provides startup, PWM control, under-voltage lock out, overvoltage shutdown and over-temperature protection functions. The integrated 220 V MOSFET has excellent switching characteristics at the selected 400 kHz operating frequency. This together with the minimal power consumption of the control enables a typical operating efficiency of 75% to 80% across the operating input voltage range (see Figure 7).

The DC input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. Zener diode VR1 and C3 clamp leakage spikes generated when the MOSFET in U1 turns off. Under normal operation, VR1 does not conduct but limits the maximum drain voltage under input overvoltage and output overload conditions.

Resistor R5 programs the typical input under-voltage on-threshold to 33 VDC and the protective overvoltage shutdown to 90 VDC. Resistors R4 and R6 program the internal device current limit to reduce with increasing input voltage. Maximum output (overload) current varies less than 5% across the operating voltage range. The reduction in overload output current reduces secondary transformer leakage spikes and allows the use of a 30 V Schottky diode for the output rectifier D1.

The primary bias winding provides CONTROL pin current after start-up. Diode D2 rectifies the bias winding, while components R5 and C11 reduce the high frequency switching noise and reduce peak charging of the bias voltage.

The DPA423G operates well within the recommended junction temperature limits (110 °C) at an elevated ambient of 50 °C, in a free-convection cooled environment (see Section 10).

4.3 Output Rectification

Schottky output diode D1 enables low loss rectification of the secondary winding voltage. Low ESR tantalum output capacitors, C7 to C9, reduce switching ripple and minimize

losses. Secondary output choke L2 and ceramic output capacitor C10 reduce high frequency noise and ripple at the output.

4.4 Output Feedback

The output voltage is sensed via the resistor divider formed by R9 and R10 and fed into the reference pin of the low voltage reference, U3. Feedback compensation components R7, R8, and C13 ensure stable operation and optimum line and load transient response. Capacitor C12 provides a soft-finish characteristic, preventing output voltage overshoot during startup of the converter.

5 PCB Layout

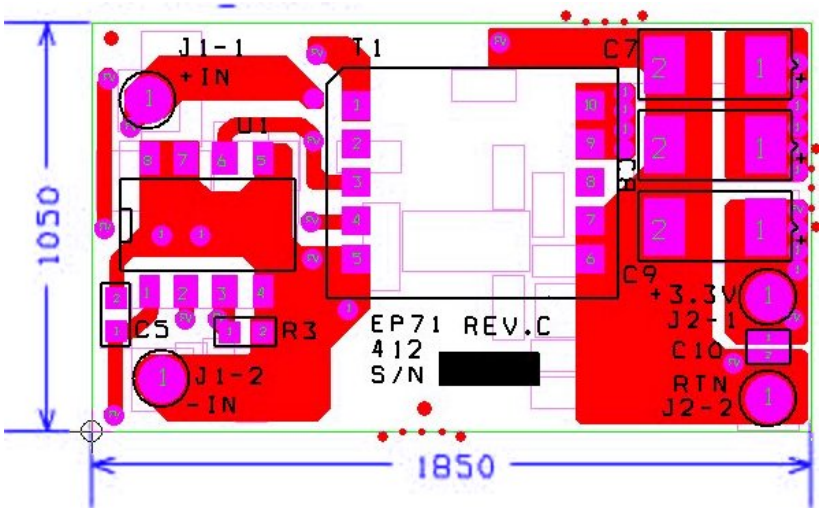

Figure 3 - Top Side, SMT Printed Circuit Layout (Top View).

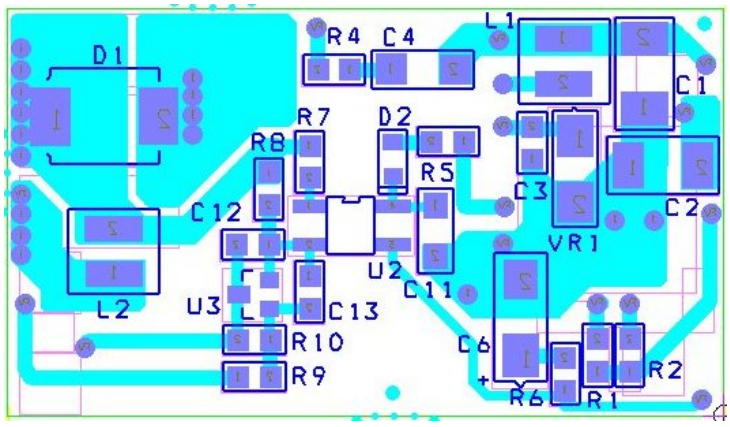

Figure 4 - Bottom Side, SMT Printed Circuit Layout (Top View).

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6 Bill of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	1	U1	*DPA-Switch*	DPA423G	Power Integrations
2	1	U2	Optocoupler, 80-160% graded CTR	PC357N1TA	Sharp
3	1	U3	Low voltage shunt regulator, SOT23	CAT431L	Catalyst Semiconductor
4	1	C1, C2	1.5 µF, 100 V, 1812	THCS50E2A155ZT	UCC
5	1	C3	47 pF, 200 V	ECJ-2VC2D470J	Panasonic
6	1	C4 *	1000 pF, 1500 V, 1808	1808SC102KAT1A	AVX
7	2	C5, C13	0.1 µF, 50 V	ECJ-2YB1H104K	Panasonic
8	1	C6	22 µF, 10 V, tantalum, C size	ECST1AC226R	Panasonic
9	3	C7-9	330 µF, 6.3 V, tantalum, X size	T495X337K006AS	Kemet
10	1	C10	1 µF, 10 V, 0508 alternative geometry	ECY-29RA105KV	Panasonic
11	1	C11	1 µF, 50 V, 1206	ECJ-3FF1H105Z	Panasonic
12	1	C12	0.33 µF, 50 V	ECJ-2YB1C334K	Panasonic
13	1	D1	30 V, 4 A Schottky	SL43	Vishay
14	1	D2	200 V, 200 mA	BAV21	generic
15	4	J1-1,2 J2-1,2	Pin, surface mount, 0.040 x 0.375”	4531051-0000	Zierick
16	1	L1	10 µH, 1 A	SCD-0403-100MT	Chilisin
17	1	L2	1 µH, 2 A	SCD-0403-1R0M	Chilisin
18	1	R1	1.00 MΩ, 1%	ERJ-6ENF1004V	Panasonic
19	1	R2	619 kΩ, 1%	ERJ-6ENF6193V	Panasonic
20	1	R3	8.66 kΩ, 1%	ERJ-6ENF8661V	Panasonic
21	1	R4 *	10 Ω	ERJ-6GEYJ100V	Panasonic
22	1	R5	100 Ω	ERJ-6GEYJ101V	Panasonic
23	1	R6	5.1 Ω	ERJ-6GEYJ5R1V	Panasonic
24	1	R7	75 Ω	ERJ-6GEYJ750V	Panasonic
25	1	R8	1 kΩ	ERJ-6GEYJ102V	Panasonic
26	1	R9	34.0 kΩ, 1%	ERJ-6ENF3402V	Panasonic
27	1	R10	20.0 kΩ, 1%	ERJ-6ENF2002V	Panasonic
28	1	T1	ER14.5 Transformer	LSTA30825 SIL6029 IM 040 202 31	L.S.E. HiCal Vogt
29	1	VR1	150 V TVS	SMAJ150A	Generic

Resistors and capacitors size 0805, unless specified otherwise.

* Optional components C4 and R4 may be included for improved EMI performance. Recommended values are shown.

7 Transformer Specification

7.1 Electrical Diagram

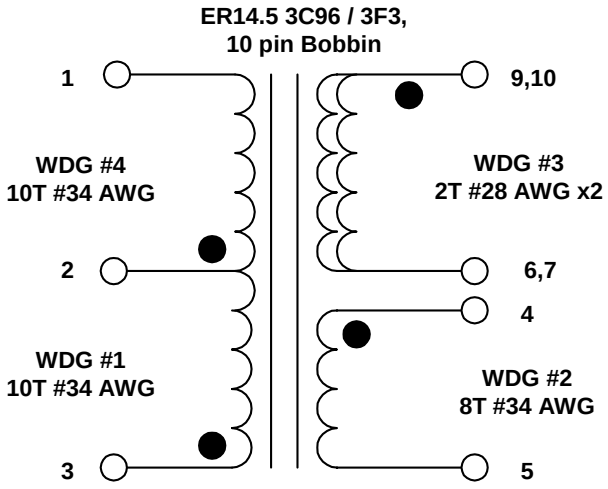

Figure 5 - Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10	1500 VDC
Primary Inductance	pins 1-3, all other windings open	120 µH, +/-10%
Resonant Frequency	Pins 1-3, all other windings open	7.5 MHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 6/7-9/10 shorted	3.0 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: ER14.5, Ferroxcube 3C96, 3F3 (or equivalent), A_{LG} = 312 nH/T^2
[2]	Bobbin: ER14.5, 10 pin
[3]	Magnet wire: #34 AWG, double coated (heavy nyleze)
[4]	Magnet wire: #28 AWG, double coated (heavy nyleze)
[5]	Tape: 3M 1298 polyester film (or equivalent), 1.8 mm wide
[6]	Core clamp ER14.5 Ferroxcube CLM14.5 (optional)
[7]	Varnish (DIPPED ONLY, NOT IMPREGNATED)

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7.4 Transformer Build Diagram

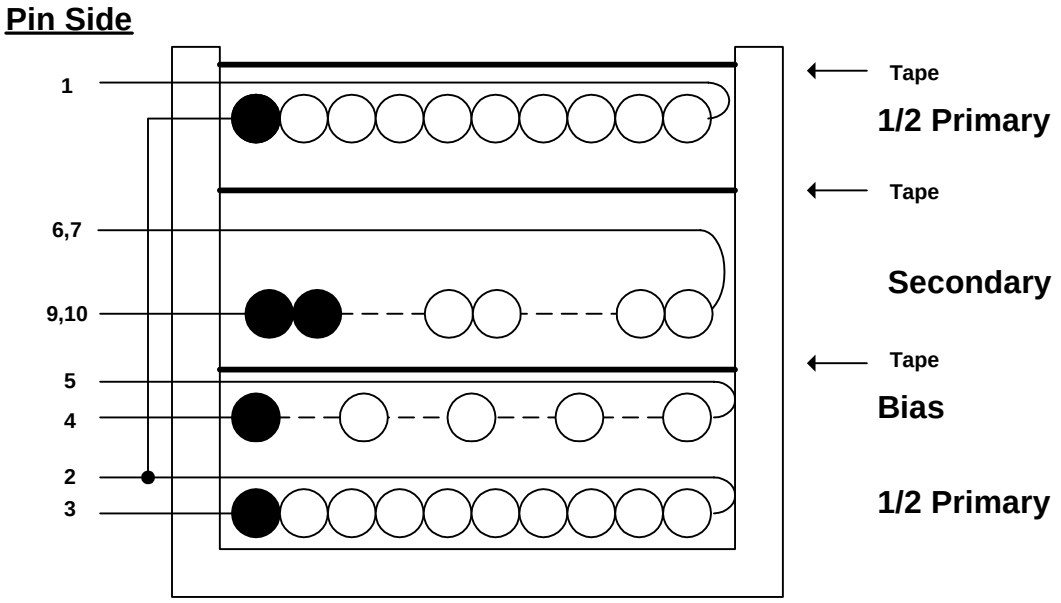

Figure 6 - Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Arrange bobbin & rotation such that primary start/finish wires do not overlap.
½ Primary	Start at pin 3. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on pin 2.
Bias Winding	Starting at pin 4, wind 8 turns of item [3]. Spread turns evenly across bobbin in a single layer. Bring finish lead back and terminate on pin 5.
Basic Insulation	Use one layer of item [5] for basic insulation.
Secondary Winding	Start at pins 9 and 10. Wind 2 turns of bifilar item [4] in 1 layer. Bring finish lead back and terminate on pins 6 and 7.
Basic Insulation	Use one layer of item [5] for basic insulation.
½ Primary	Continue from pin 2. Wind 10 turns of item [3] in 1 layer. Bring finish lead back and terminate on pin 1.
Outer Insulation	Use one layer of item [5] for basic insulation.
Final Assembly	Assemble and secure (glue or clamp, item [6]) core halves. Dip varnish item [7] and cure.

8 Transformer Spreadsheets

DCDC_DPASwitch_Flyback_010704_Revision1H. Copyright Power Integrations 2004	INPUT	INFO	OUTPUT	UNITS	DPASwitch_Flyback_010704 - Continuous/Discontinuous mode Spreadsheet. Copyright 2004 Power Integrations
ENTER APPLICATION VARIABLES					EP71 Power Supply
VDCMIN	36			Volts	Minimum DC Input Voltage
VDCMAX	72			Volts	Maximum DC Input Voltage
VO	3.3			Volts	Output Voltage
PO	6.6	Comment		Watts	Verify temperature rise for continuous power. P and G packages may be thermally limited
n	0.8				Efficiency Estimate
Z			0.7		Loss Allocation Factor, (0.7 Recommended)
VB	14			Volts	Bias Voltage (Recommended between 12V and 18V)
UV AND OV PARAMETERS					
		min	max		
VUVOFF		30.0	33.1	Volts	Minimum undervoltage On-Off threshold
VUVON		32.2	34.7	Volts	Maximum undervoltage Off-On threshold (turn-on)
VOVON		74.9	-	Volts	Minimum overvoltage Off-On threshold
VOVOFF			94.7	Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			619.0	k-Ohms	
ENTER DPASWITCH VARIABLES					
DPASWITCH	DPA423G			*16VDC*	*36VDC*
Chosen Device	*DPA423G*		*Power Ou*	*6W*	*13W*
ILIMITMAX	*1.16*	*1.34*		Amps	From DPASWITCH Data Sheet
Frequency	F				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
fS	375000			Hertz	DPASWITCH Switching Frequency
VOR	38		38	Volts	Reflected Output Voltage
KI	0.70		0.7		Current Limit Reduction Factor
ILIMITEXT			0.812	Amps	Minimum External Current limit
RX			11.0	k-Ohms	Resistor from X pin to source to set external current limit
VDS	1			Volts	DPASWITCH on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	0.62				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	ER14.5				
Core Manuf					
Bobbin Manuf					
Core		*ER14.5*		*P/N:*	*ER14.5-3F3-S*
Bobbin		*ER14.5_Bob*		*P/N:*	*CPVS-ER14.5-1S-10F*
AE			0.176	cm^2	Core Effective Cross Sectional Area
LE			1.9	cm	Core Effective Path Length
AL			1400	nH/T^2	Ungapped Core Effective Inductance
BW			1.9	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2				Number of Primary Layers
NS	2				Number of Secondary Turns
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Maximum Duty Cycle
IAVG			0.23	Amps	Average Primary Current
IP			0.64	Amps	Peak Primary Current
IR			0.39	Amps	Primary Ripple Current
IRMS			0.33	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			120	uHenries	Primary Inductance
NP			20		Primary Winding Number of Turns
NB			8		Bias Winding Number of Turns
ALG			300	nH/T^2	Gapped Core Effective Inductance
BP			2768	Gauss	Peak Flux density during transients (Limit to 3000 Gauss)
BM			2168	Gauss	Maximum Flux Density
BAC			667	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1203		Relative Permeability of Ungapped Core
LG			0.06	mm	Gap Length (Lg >> 0.051 mm)
BWE			3.8	mm	Effective Bobbin Width
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			6.36	Amps	Peak Secondary Current
ISRMS			3.15	Amps	Secondary RMS Current
IO			2.00	Amps	Power Supply Output Current
IRIPPLE			2.43	Amps	Output Capacitor RMS Ripple Current
VOLTAGE STRESS PARAMETERS					
VDRAIN			172	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
PIVS			11	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			42	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2				Volts	Auxiliary Output Voltage
VD_OUT2				Volts	Auxiliary Diode Forward Voltage Drop
N_OUT2			0.00		Auxiliary Number of Turns
PIV_OUT2			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
V_OUT3				Volts	Auxiliary Output Voltage
VD_OUT3				Volts	Auxiliary Diode Forward Voltage Drop
N_OUT3			0.00		Auxiliary Number of Turns
PIV_OUT3			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage

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TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			6.36	Amps	Peak Secondary Current
ISRMS			3.15	Amps	Secondary RMS Current
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VDRAIN			**172**	**Volts**	**Maximum Drain Voltage (Includes Effect of Leakage Inductance)**
PIVS			11	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			42	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2				Volts	Auxiliary Output Voltage
VD_OUT2				Volts	Auxiliary Diode Forward Voltage Drop
N_OUT2			0.00		Auxiliary Number of Turns
PIV_OUT2			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
V_OUT3				Volts	Auxiliary Output Voltage
VD_OUT3				Volts	Auxiliary Diode Forward Voltage Drop
N_OUT3			0.00		Auxiliary Number of Turns
PIV_OUT3			0	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage

9 Performance Data

All measurements were performed at room temperature utilizing a DC input source and DC dynamic loads. Input and output voltages and current were measured with dedicated DVMs.

9.1 Efficiency

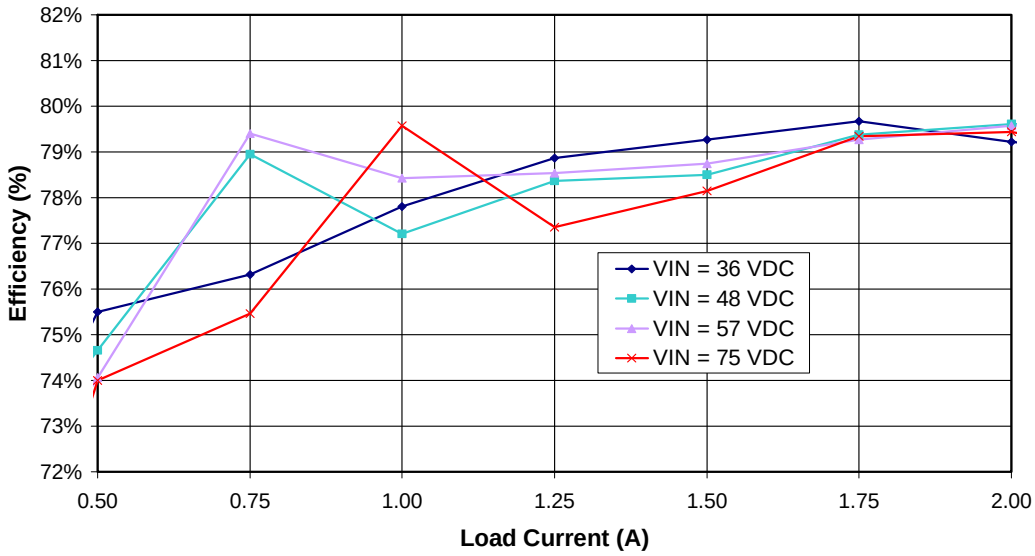

Figure 7 - Efficiency vs. Output Load, Room Temperature.

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9.2 Regulation

9.2.1 Load

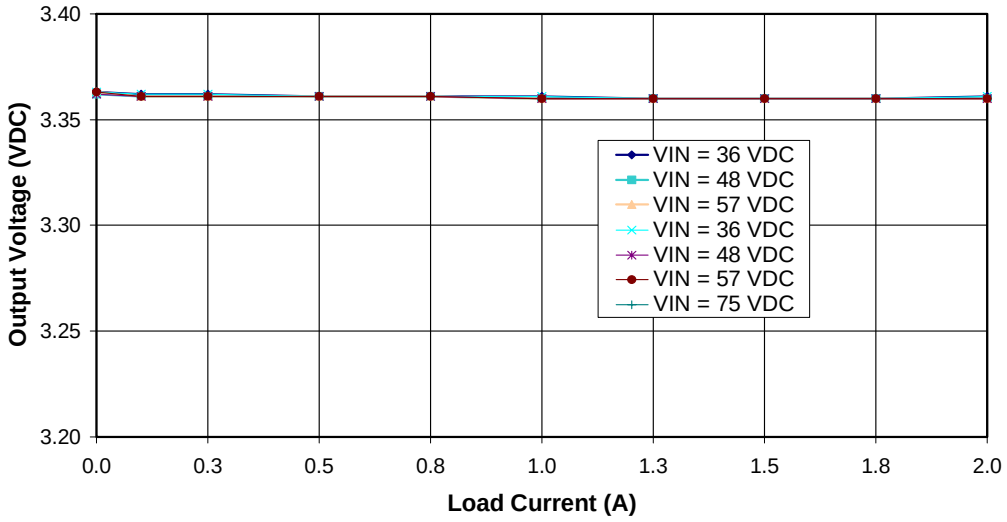

Figure 8 - Load Regulation, Room Temperature.

9.2.2 Line

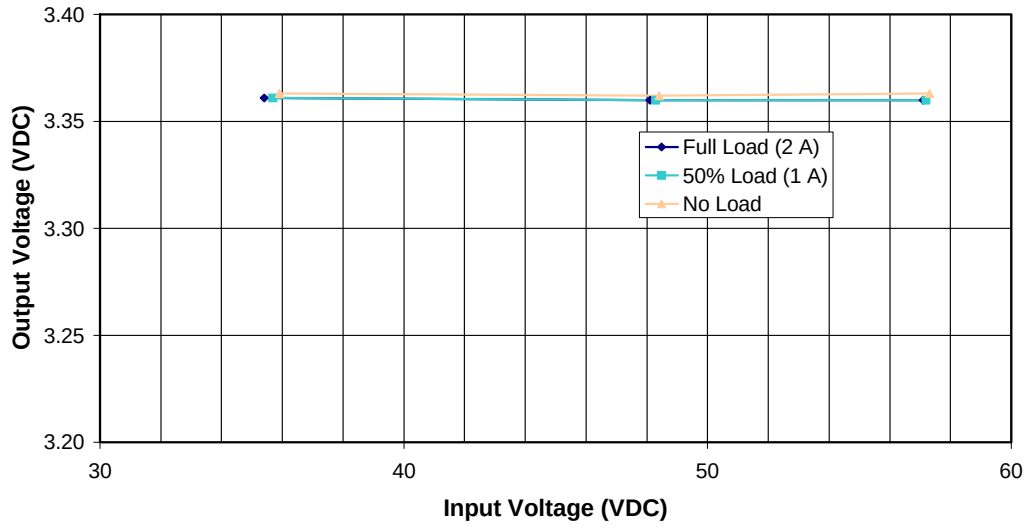

Figure 9 - Line Regulation, Room Temperature.

9.3 Peak Power

The DC output load current was recorded just prior to the auto-restart operation.

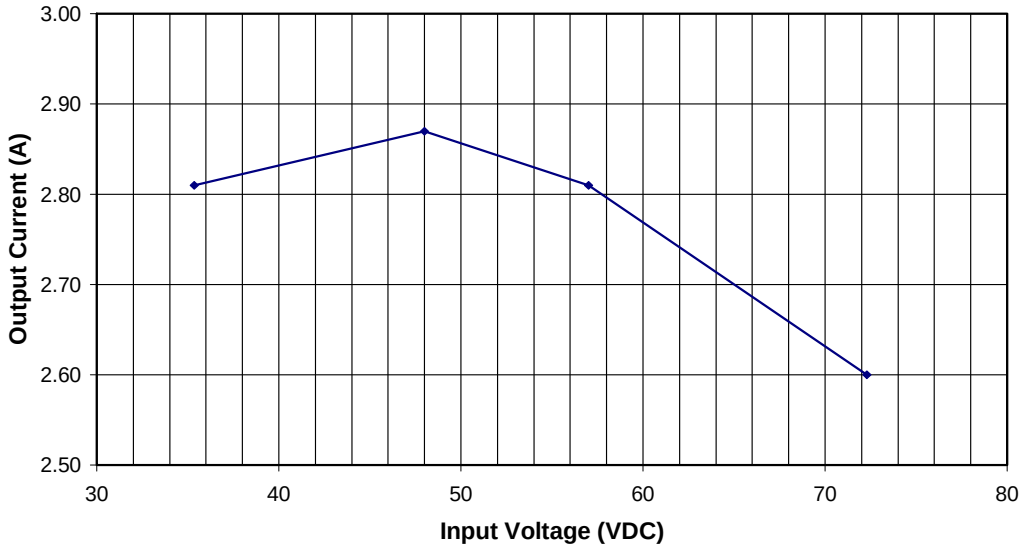

Figure 10 - Maximum Output Overload Current, Room Temperature.

10 Waveforms

10.1 Drain Voltage and Current, Full Load Operation

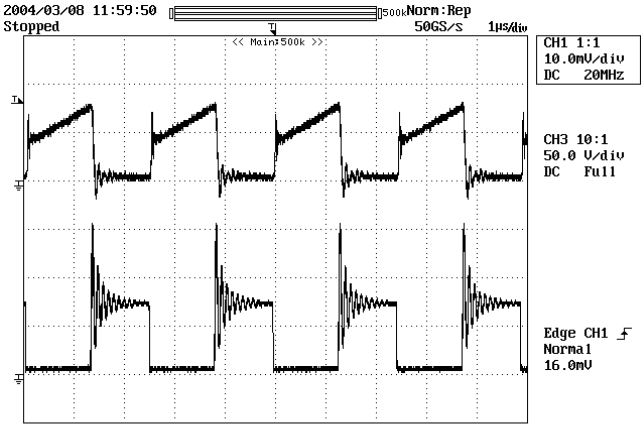

Figure 11 – 36 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

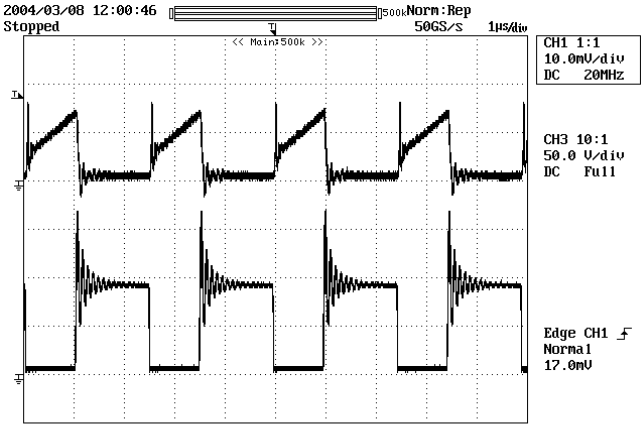

Figure 12 – 57 VDC, Full Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 50 V, 1 µs / div.

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10.2 Output Voltage Start-Up Profile

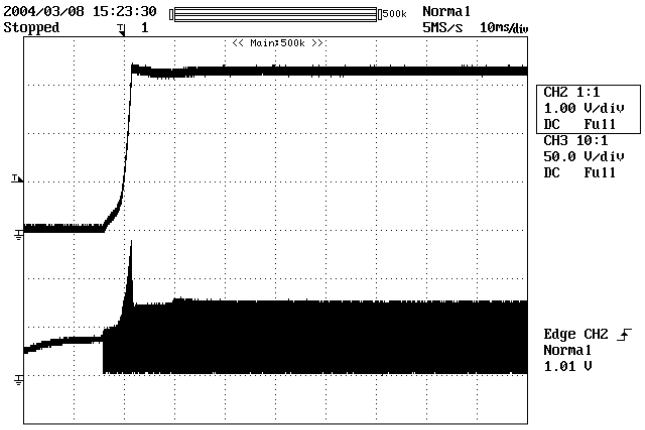

Figure 13 - Start-up Profile, 36 VDC, No Load (Worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 10 ms / div.

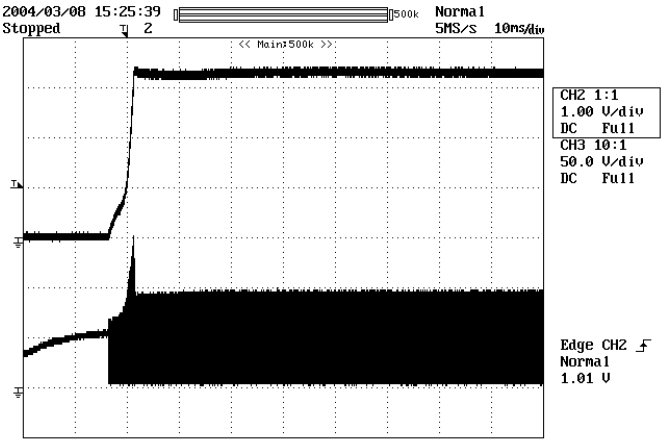

Figure 14 - Start-up Profile, 57 VDC, No Load (Worst-case).
Upper: V_{OUT}, 1 V / div.
Lower: V_{DRAIN}, 50 V, 10 ms / div.

10.3 Drain Voltage and Current Start-Up Profile

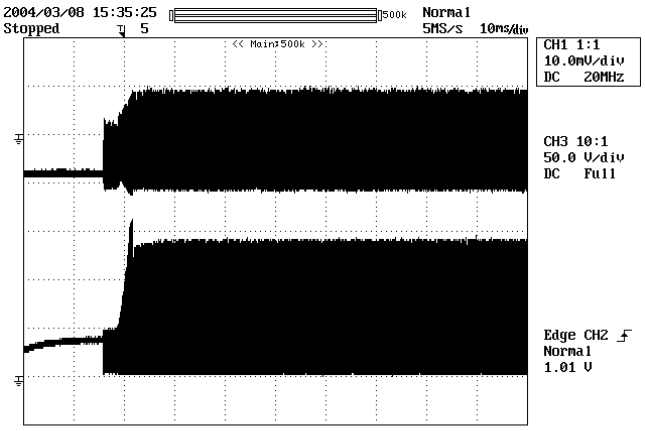

Figure 15 – 36 VDC Input, 2 A Resistive Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 10 ms / div.

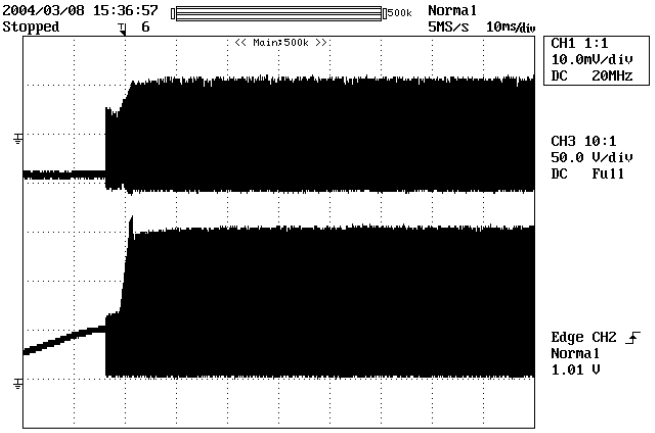

Figure 16 – 57 VDC Input, 2 A Resistive Load.
Upper: I_{DRAIN}, 0.5 A / div.
Lower: V_{DRAIN}, 100 V, 10 ms / div.

10.4 Load Transient Response (75% to 100% Load Step)

In the following two oscilloscope screen shots (Figure 17 and 18), signal averaging was used to more clearly capture the output voltage response to a load transient. Averaging minimizes the appearance of the 400 kHz switching ripple in the output voltage scope plot. The load current step was used to trigger the horizontal sweep of the oscilloscope.

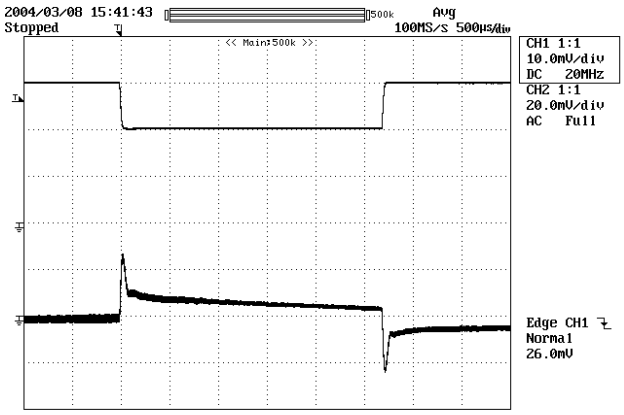

Figure 17 - Transient Response,
36 VDC, 75-100-75% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage,
20 mV, 500 µs / div.

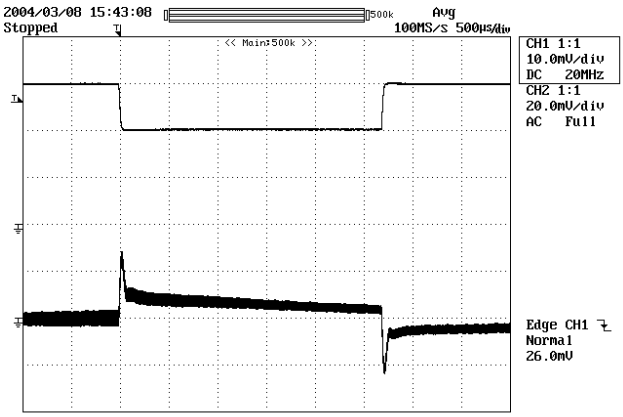

Figure 18 - Transient Response,
57 VDC, 75-100-75% Load Step.
Upper: Load Current, 1 A / div.
Lower: Output Voltage,
20 mV, 500 µs / div.

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10.5 Output Ripple Measurements

10.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figures 19 and 20.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

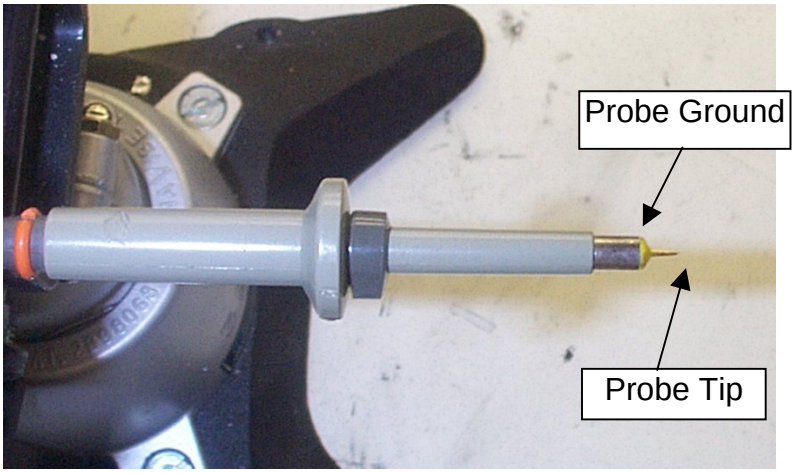

Figure 19 - Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

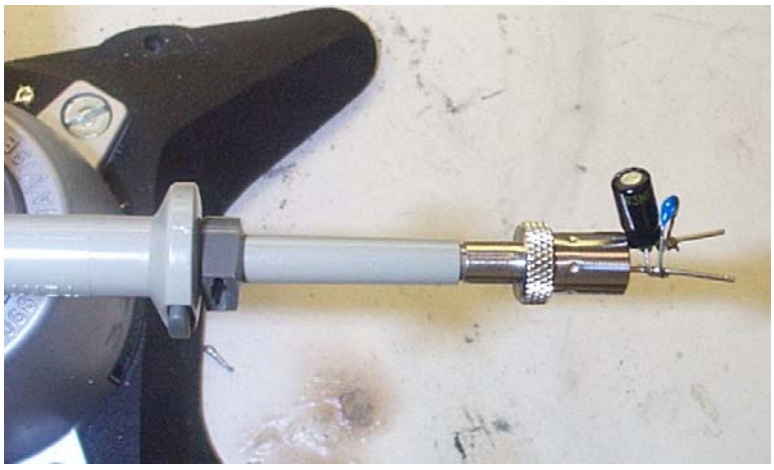

Figure 20 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple Measurement, and Two Parallel Decoupling Capacitors Added).

10.5.2 Output Ripple Measurements

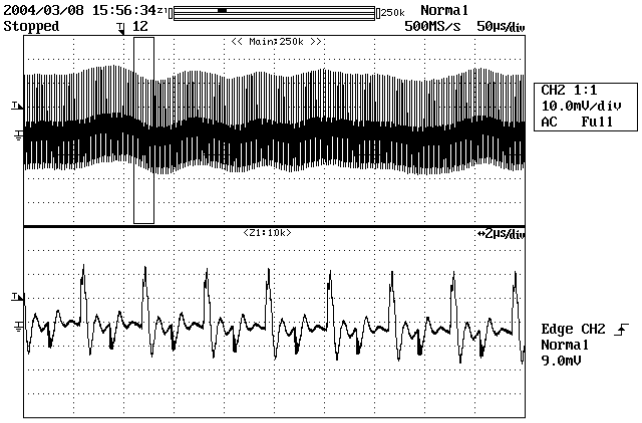

Figure 21 - Ripple, 36 VDC, Full Load.
Upper: 50 µs / div, 10 mV / div.
Lower: 2 µs / div, 10 mV / div.

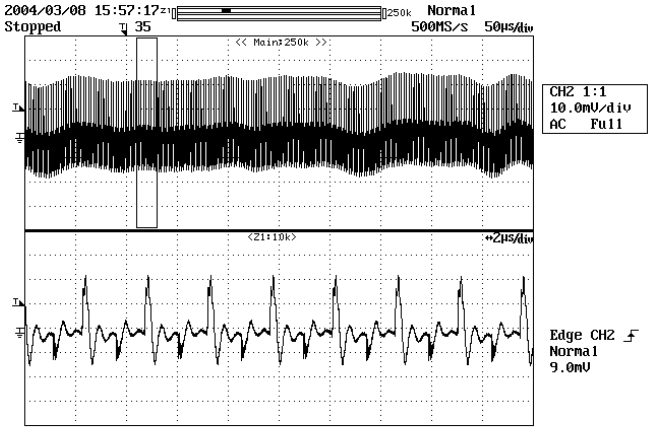

Figure 22 - Ripple, 48 VDC, Full Load.
Upper: 50 µs / div, 10 mV / div.
Lower: 2 µs / div, 10 mV / div.

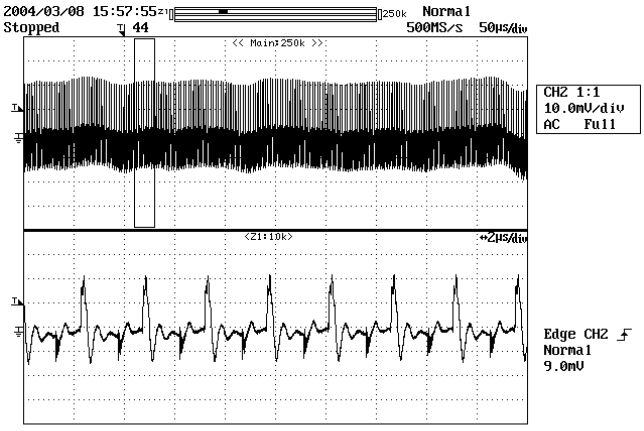

Figure 23 - Ripple, 57 VDC, Full Load.
Upper: 50 µs / div, 10 mV / div.
Lower: 2 µs / div, 10 mV / div.

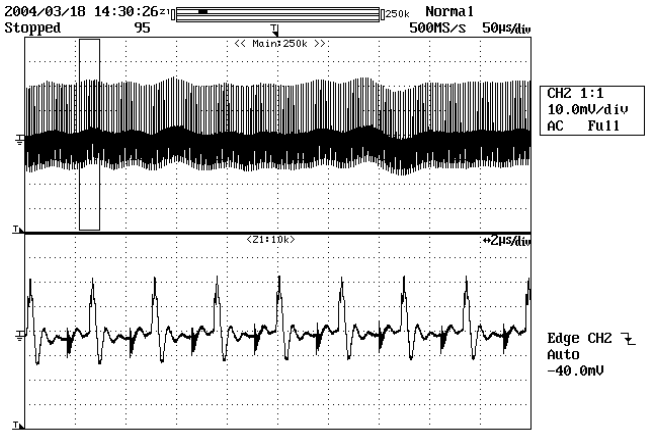

Figure 24 – Ripple, 75 VDC, Full Load.
Upper: 50 µs / div, 10 mV / div.
Lower: 2 µs / div, 10 mV / div.

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11 Thermal Performance

The temperatures of key components were recorded using T-type thermocouples. Two of the four thermocouples were soldered, one directly to a SOURCE pin of the DPA423G (U1) and the other to the cathode of the output rectifier (D1). The other two thermocouples were glued, one to the transformer (T1) core on the center leg, and the other to the case of the first of the two high-ripple output capacitors (C7).

The unit was operated at full load, at 36 VDC, 48 VDC and 57 VDC in free convection within a small enclosure to prevent external air currents affecting the measurements.

The results show adequate thermal margin, considering an additional ambient rise of +29 °C. At 36 VDC, full load, within an enclosure at elevated 50 °C ambient, this equates to a DPA423G case temperature of 79 °C. This is well below the recommended maximum case temperature of 100 °C.

An infrared measurement taken at nominal-line (48 VDC) is provided.

Measured Temperature (°C)			
Item	**36 VDC**	**48 VDC**	**57 VDC**
Ambient	21	21	21
DPA423G (U1)	50	49	49
Transformer core (T1)	75	74	74
Output Rectifier (D1)	66	64	64
Output Capacitor (C7)	42	41	42

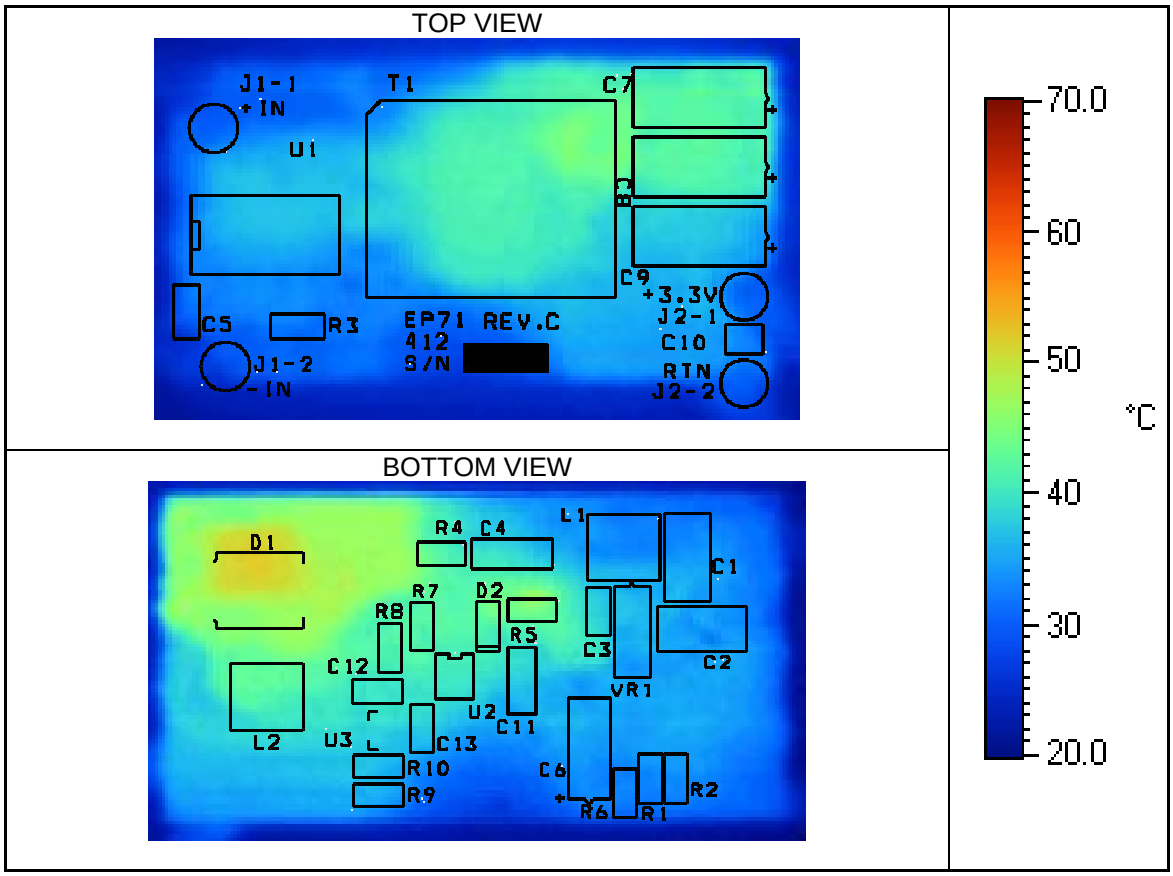

Figure 25- Infrared Thermograph of Top of EP-71 Board, 48 VDC, Full Load, Room Ambient.

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12 Control Loop Measurements

12.1 36 VDC Maximum and Nominal Load

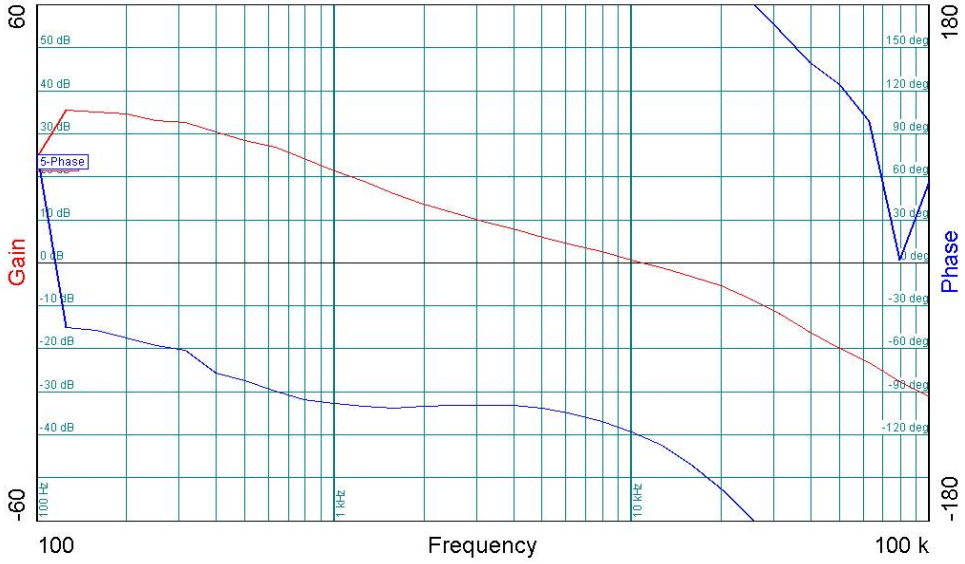

Figure 26 - Gain-Phase Plot, 36 VDC, Maximum Load (2 A).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 10.0 kHz, Phase Margin = 60°

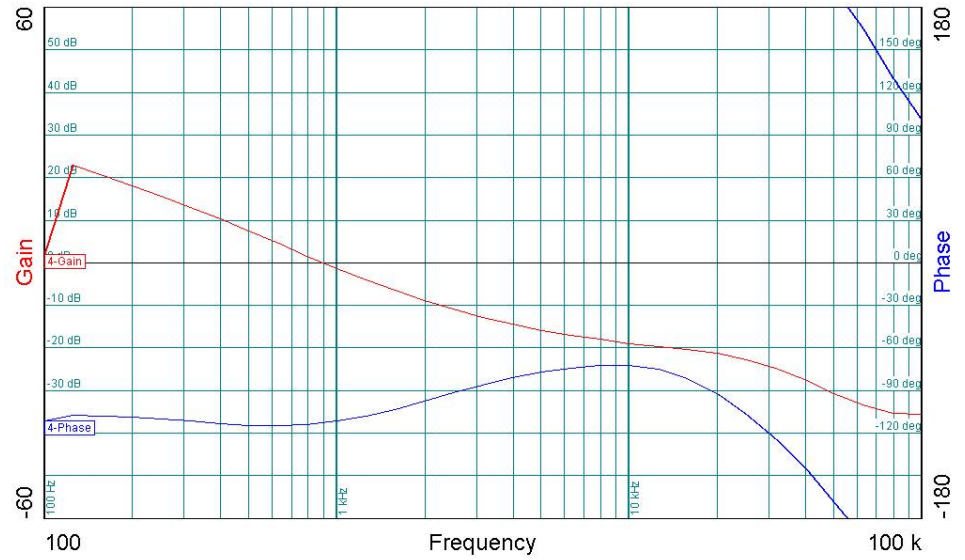

Figure 27 - Gain-Phase Plot, 36 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 0.9 kHz, Phase Margin = 65°

12.2 57 VDC Maximum Load

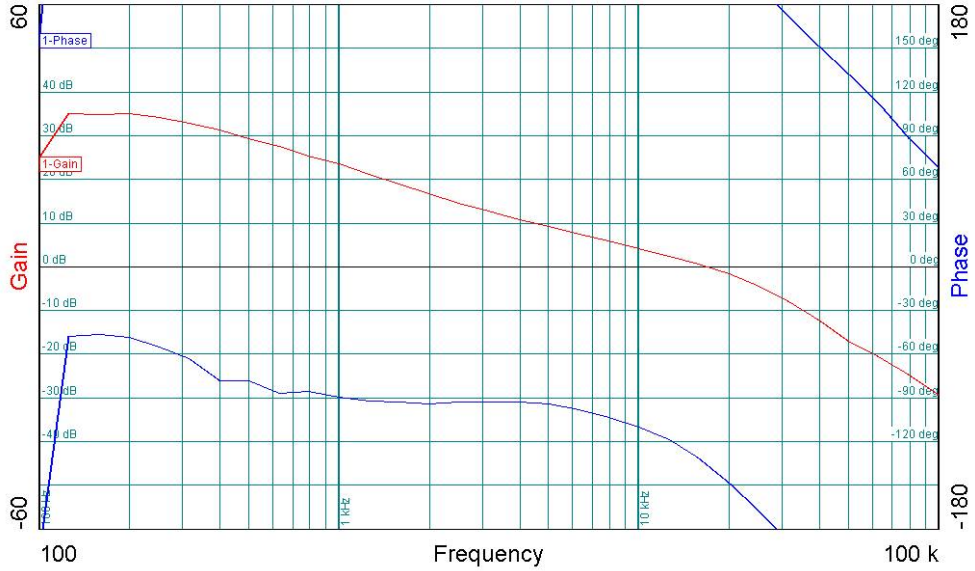

Figure 28 - Gain-Phase Plot, 57 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 10.8 kHz, Phase Margin = 40°

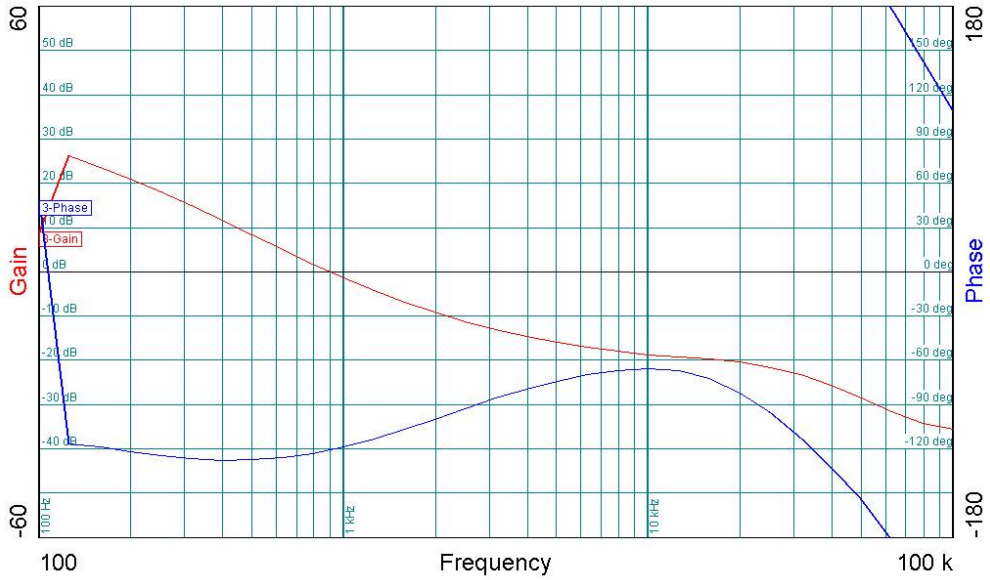

Figure 29 - Gain-Phase Plot, 57 VDC, Light Load (100 mA).
Vertical Scale: Gain = 10 dB / div, Phase = 30° / div.
Crossover Frequency = 0.9 kHz, Phase Margin = 60°

The results indicate adequate loop bandwidth and significant gain and phase margin.

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13 Revision History

Date	Author	Revision	Description & changes
11-Mar-04	SH	0.1	First draft
16-Mar-04	PV	0.2	Minor text edits
22-Mar-04	PV	1.0	Insert board photograph
02-Apr-04	KM	1.1	Added vendor name to Bill of Materials
19-Jul-05	PV	1.2	Fixed schematic and bill of materials (BOM)

Notes

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