NOT RECOMMENDED FOR NEW DESIGN

The EY1501DI-ADJ is a low voltage, high current, single output LDO specified at 1A output current. This LDO operates from input voltages from 2.2V to 6V, and is capable of providing output voltages from 0.8V to 5V. The EY1501DI-ADJ features an adjustable output.

A sub-micron BiCMOS process is utilized to deliver the best in class analog performance and overall value. This CMOS LDO will consume significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. State of the art internal compensation achieves a very fast load transient response. An external capacitor on the soft-start pin provides an adjustable soft-starting ramp. The EN feature allows the part to be placed into a low quiescent current shutdown mode. A Power OK logic output signals a fault condition.

Table 1 shows the EY1501DI-ADJ features.

TABLE 1. EY1501DI-ADJ Features

PART NUMBER	PROGRAMMABLE I_{LIMIT}	I_{LIMIT} (DEFAULT)	V_{OUT}
EY1501DI-ADJ	No	1.75A	ADJ

Features

- ±0.2% initial V_{OUT} Accuracy
- ±1.8% V_{OUT} Accuracy Guaranteed Over Line, Load and T_J = -40°C to +125°C
- Very Low 130mV Dropout Voltage at V_{OUT} = 2.5V
- Very Fast Transient Response
- Programmable Soft-starting
- Power OK Output
- Excellent 58dB PSRR at 1kHz
- Current Limit Protection
- Thermal Shutdown Function
- Available in a 10 Ld DFN Package
- Pb-Free (RoHS Compliant)

Applications

- DSP, FPGA and µP Core Power Supplies
- Noise-Sensitive Instrumentation Systems
- Post Regulation of Switched Mode Power Supplies
- Industrial Systems
- Medical Equipment
- Telecommunications and Networking Equipment
- Servers
- Hard Disk Drives (HD/HDD)

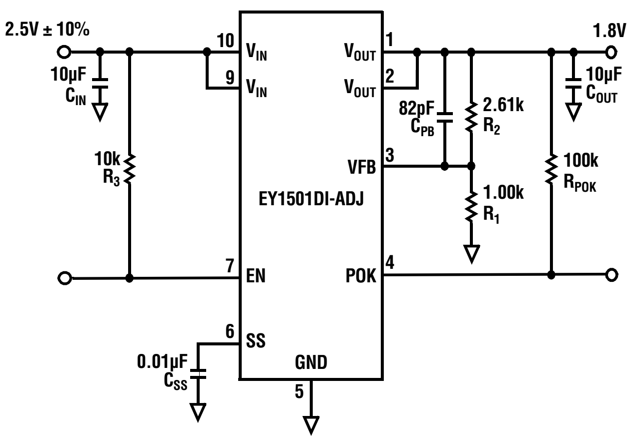

FIGURE 1. TYPICAL APPLICATION CIRCUIT

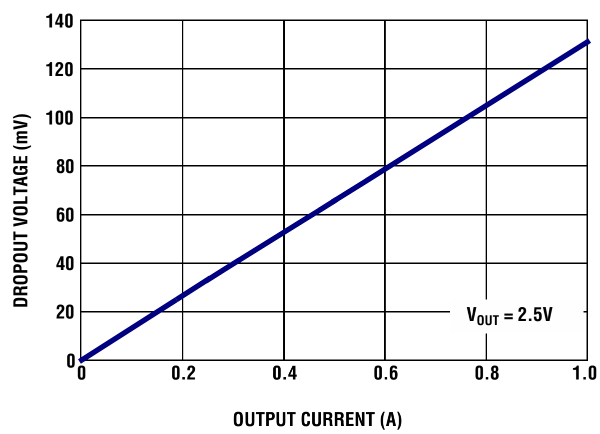

FIGURE 2. DROPOUT vs LOAD CURRENT

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www.altera.com

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Ordering Information

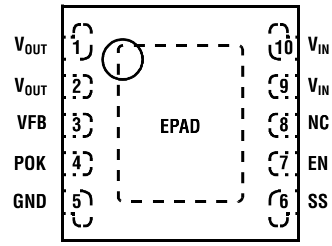
PART NUMBER (Note 3)	PART MARKING	V_{OUT} VOLTAGE (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
EY1501DI-ADJ (Note 1)	1501	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
2. For other output voltages, contact Altera Enpirion Marketing.
3. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

EY1501DI-ADJ
(10 LD 3x3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Regulated output voltage. A minimum 10µF X5R/X7R output capacitor is required for stability. See “External Capacitor Requirements” on page 9 for more details.
3	VFB	This pin is connected to the feedback resistor divider and provides voltage feedback signals for the LDO to set the output voltage. In addition, the Power OK circuit uses this input to monitor the output voltage status.
4	POK	This is an open drain logic output used to indicate the status of the output voltage. Logic low indicates V_{OUT} is not in regulation. Must be grounded if not used.
5	GND	Ground.
6	SS	External capacitor on this pin adjusts startup ramp and controls inrush current.
7	EN	V_{IN} independent chip EN. TTL and CMOS compatible.
8	NC	No connection. Leave floating.
9, 10	V_{IN}	Input supply. A minimum of 10µF X5R/X7R input capacitor is required for proper operation. See “External Capacitor Requirements” on page 9 for more details.
-	EPAD	EPAD at ground potential. It is recommended to solder the EPAD to the ground plane.

Absolute Maximum Ratings

V_{IN} Relative to GND (Note 4). . . . . -0.3V to +6.5V
V_{OUT} Relative to GND (Note 4) . . . . -0.3V to +6.5V
POK, EN, VFB, SS
Relative to GND (Note 4) . . . . -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JESD22 A114F) 2.5kV
Machine Model (Tested per JESD22 A115C) 250V
Latch Up (Tested per JESD78C, Class 2, Level A)±100mA at +85°C

Recommended Operating Conditions (Notes 7, 8)

Junction Temperature Range (TJ) (Note 7) . . . .-40°C to +125°C
V_{IN} Relative to GND . . . . .2.2V to 6V
V_{OUT} Range . . . . 800mV to 5V
POK, EN, VFB, SS relative to GND . . . . 0V to 6V
POK Sink Current . . . . <10mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W) θ_{JC} (°C/W)
10 Ld DFN Package (Notes 5, 6). 48 7
Storage Temperature Range . . . .-65°C to +150°C
Junction Temperature. . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. ABS max voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
8. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 2.2µF$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
DC CHARACTERISTICS						
Feedback Pin (VFB Option Only)	V_{VFB}	$2.2V \le V_{IN} \le 6V$, $0A < I_{LOAD} < 1A$	**491**	500	**509**	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.5V < V_{IN} < 5V$			1	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$0A < I_{LOAD} < 1A$, All voltage options	**-1**			%
Feedback Input Current		$V_{VFB} = 0.5V$		0.01	**1**	µA
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		3	**5**	mA
		$I_{LOAD} = 1A$, $2.2V < V_{IN} < 6V$		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	EN Pin = 0.2V, $V_{IN} = 6V$		0.2	**12**	µA
Dropout Voltage (Note 10)	V_{DO}	$I_{LOAD} = 1A$, $V_{OUT} = 2.5V$		130	**212**	mV
Output Short Circuit Current	OCP	$V_{OUT} = 0V$, $2.2V < V_{IN} < 6V$		1.75		A
Thermal Shutdown Temperature	TSD	$2.2V < V_{IN} < 6V$		160		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$2.2V < V_{IN} < 6V$		30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		58		dB
		f = 120Hz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		72		dB
Output Noise Voltage		$I_{LOAD} = 1A$, BW = 10Hz < f < 100kHz		63		$µV_{RMS}$

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
EN PIN CHARACTERISTICS						
Turn-on Threshold		$2.2V < V_{IN} < 6V$	**0.3**	0.8	**1**	V
Hysteresis (Rising Threshold)		$2.2V < V_{OUT} + 0.4V < 6V$	**10**	80	**200**	mV
EN Pin Turn-on Delay		$C_{OUT} = 10\mu F$, $I_{LOAD} = 1A$		100		µs
EN Pin Leakage Current		$V_{IN} = 6V$, EN = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
SS Pin Currents (Note 11)	IPD	$V_{IN} = 3.5V$, EN = 0V, SS = 1V	**0.5**	1	**1.3**	mA
	ICHG		**-3.3**	-2	**-0.8**	µA
POK PIN CHARACTERISTICS						
V_{OUT} POK Flag Threshold			**75**	85	**92**	$\%V_{OUT}$
V_{OUT} POK Flag Hysteresis				4		%
POK Flag Low Voltage		$V_{IN} = 2.5V$, $I_{SINK} = 500\mu A$			**100**	mV
POK Flag Leakage Current		$V_{IN} = 6V$, POK = 6V			**1**	µA

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Dropout is defined as the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal voltage.
11. I_{PD} is the internal pull down current that discharges the external SS capacitor on disable. I_{CHG} is the current from the SS pin that charges the external SS capacitor during start-up.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

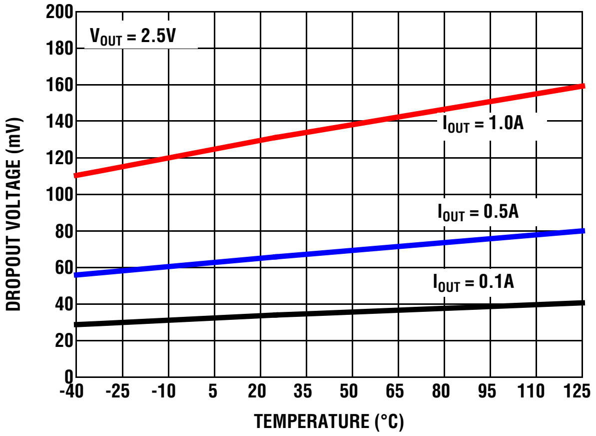


FIGURE 3. DROPOUT vs TEMPERATURE

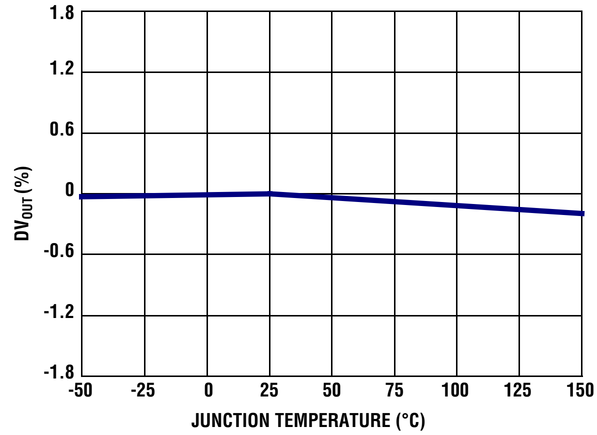


FIGURE 4. V_{OUT} vs TEMPERATURE

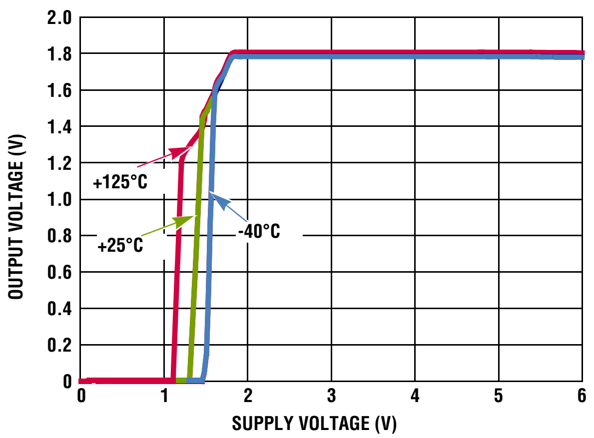


FIGURE 5. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

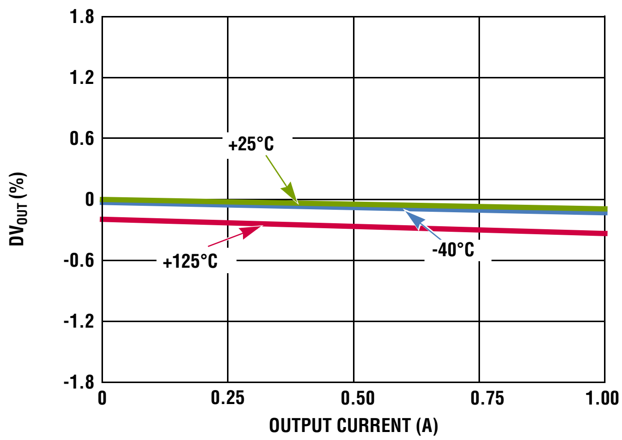


FIGURE 6. OUTPUT VOLTAGE vs OUTPUT CURRENT

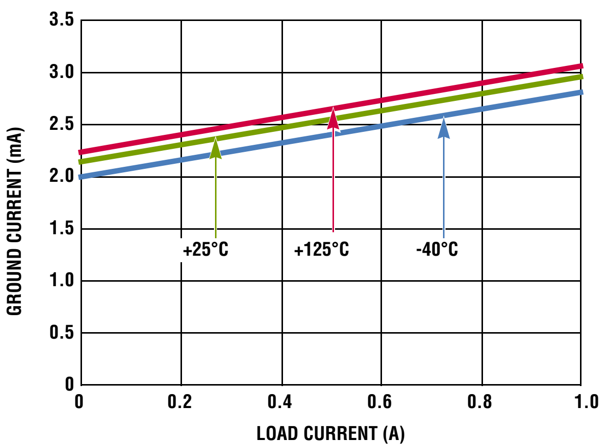


FIGURE 7. GROUND CURRENT vs LOAD CURRENT

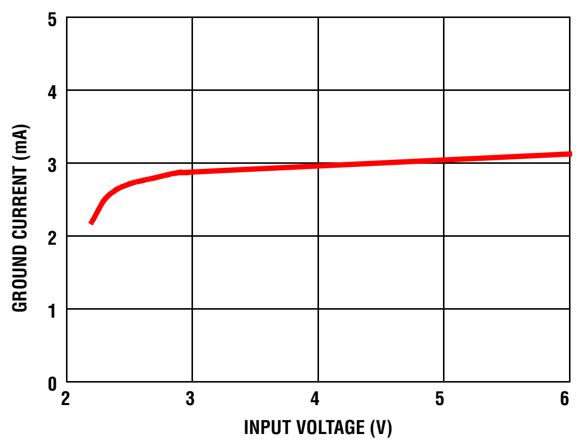


FIGURE 8. GROUND CURRENT vs SUPPLY VOLTAGE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

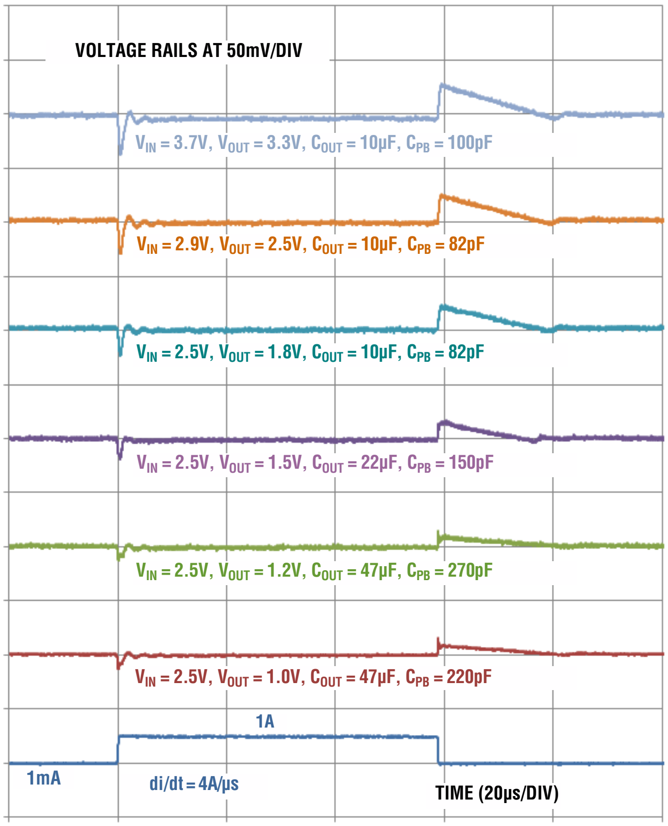


FIGURE 9. LOAD TRANSIENT RESPONSE

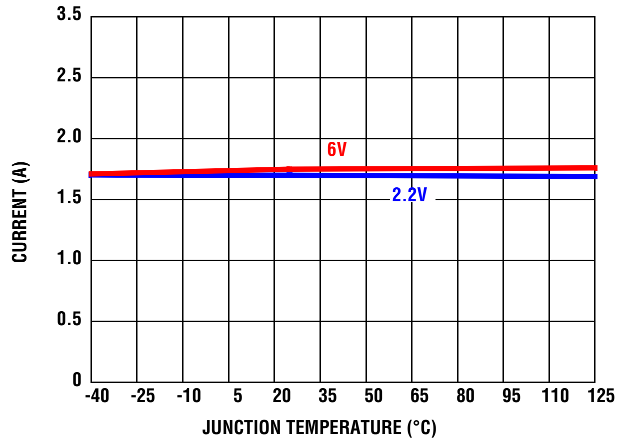


FIGURE 10. CURRENT LIMIT vs TEMPERATURE (V_{OUT} = 0V)

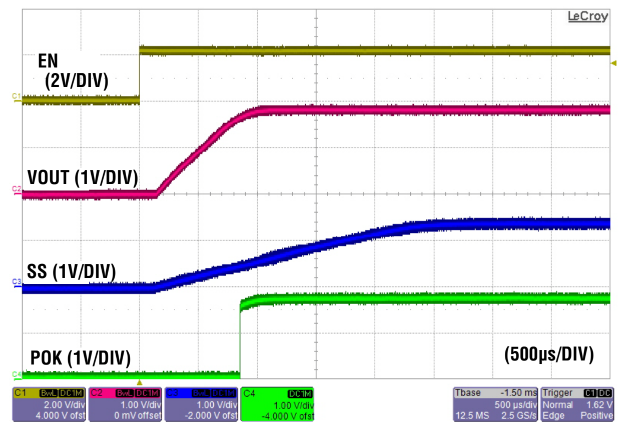


FIGURE 11. EN START-UP (Css = 2.2nF)

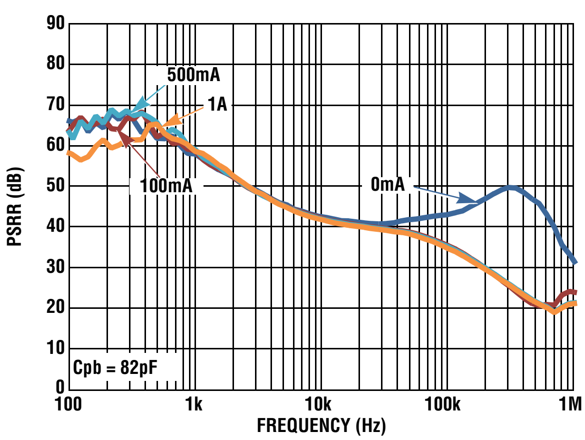


FIGURE 12. PSRR vs FREQUENCY AND LOAD CURRENT

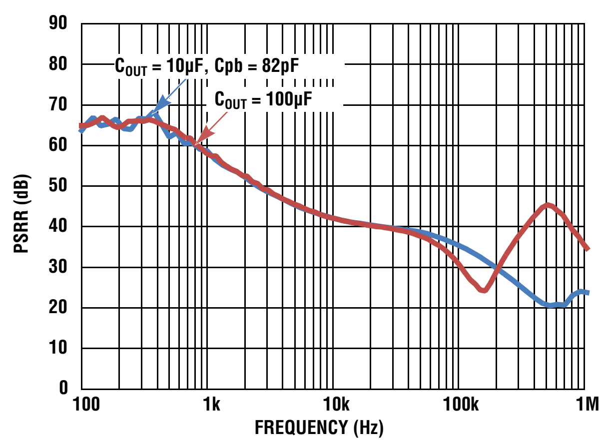


FIGURE 13. PSRR VS FREQUENCY AND OUTPUT CAPACITANCE (I_{OUT} = 100MA)

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

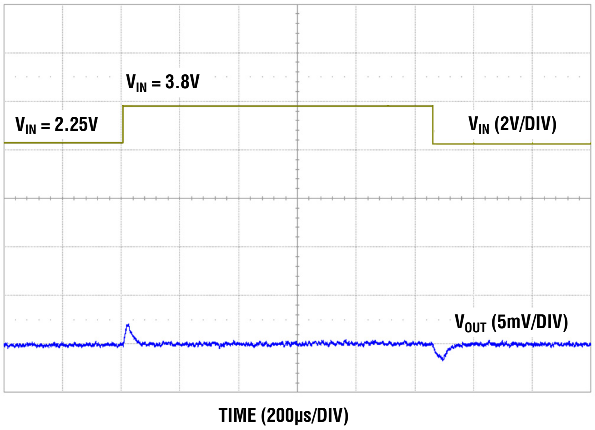


FIGURE 14. LINE TRANSIENT RESPONSE

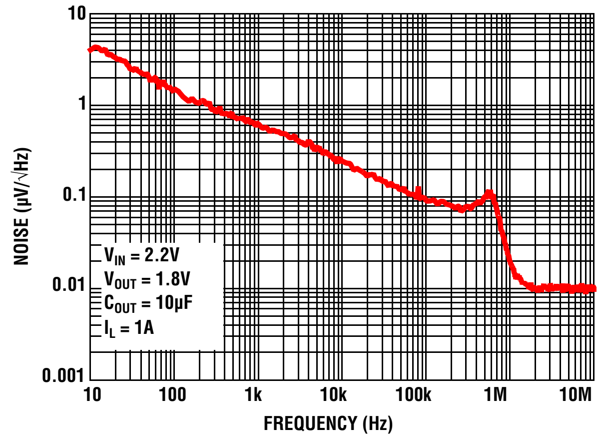
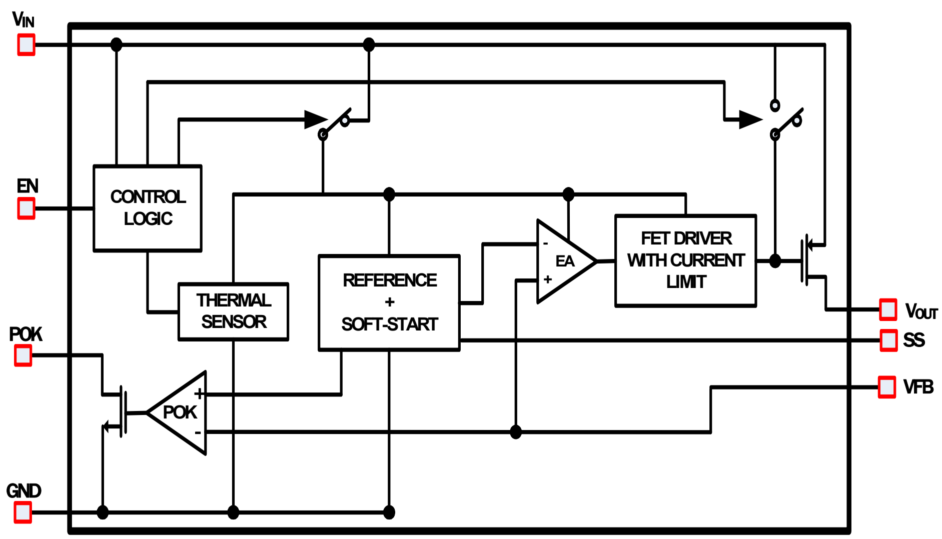


FIGURE 15. OUTPUT NOISE SPECTRAL DENSITY

Block Diagram



Applications Information

Input Voltage Requirements

EY1501DI-ADJ is capable of delivering output voltages from 0.8V to 5.0V. Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The very low dropout specification allows applications to design for a level of efficiency that can accommodate profiles smaller than the TO220/263.

EN Operation

The EN turn-on threshold is typically 800mV with 80mV of hysteresis. This pin must not be left floating, and should be tied to V_{IN} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the EN pin. An internal pull-up or pull-down resistor to change these values is available upon request. The EN pin may be connected directly to V_{IN} for applications with outputs that are always on.

Power OK Operation

POK is a logic output that indicates the status of V_{OUT}. The POK flag is an open-drain NMOS that can sink up to 10mA. It requires an external pull-up resistor typically connected to the V_{OUT} pin. The POK pin should not be pulled up to a voltage source greater than V_{IN}. POK goes low when the output voltage drops below 84% of the nominal output voltage or if the part is disabled. The POK comparator functions during current limit and thermal shutdown. For applications not using this feature, connect this pin to ground.

Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up this C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 1.

$$T_{start} = \frac{C_{SS} x 0.5}{2\mu A} \quad \text{(EQ. 1)}$$

Equation 2 determines the C_{SS} required for a specific start-up in-rush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired in-rush current.

$$C_{SS} = \frac{V_{OUT} x C_{OUT} x 2\mu A}{I_{INRUSH} x 0.5V} \quad \text{(EQ. 2)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

Output Voltage Selection

An external resistor divider, R1 and R2 as referenced in Figure 1 on page 1, is used to scale the output voltage relative to the internal reference voltage. The output voltage can be programmed to any level between 0.8V and 5V. The recommended value for R2 is 500Ω to 5kΩ R1 is then chosen to satisfy Equation 3.

$$V_{OUT} = 0.5V \times \left(\frac{R_2}{R_1} + 1\right) \quad \text{(EQ. 3)}$$

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The EY1501DI-ADJ applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming the minimum recommended ceramic capacitor is used for local bypass on V_{OUT}. There is a growing trend to use very-low ESR multilayer ceramic capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age, and temperature. X7R and X5R dieletric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances. The use of Cpb (see following section) is recommended when only the minimum recommended ceramic capacitor is used on the output. Please refer to Table 2 for these minimum conditions for various output voltages.

Phase Boost Capacitor

A small phase boost capacitor, Cpb, can be placed across the top resistor, R_2, in the feedback resistor divider network in order to place a zero at:

$$F_Z = \frac{1}{2\pi x R_2 x C_{PB}} \quad \text{(EQ. 4)}$$

This zero increases the crossover frequency of the LDO and provides additional phase resulting in faster load transient response.

It is important to note that LDO stability and load transient performance are affected by the type of output capacitor used. For optimal result, empirical tuning of C_{PB} is suggested for each specific application. It is recommended to not use C_{PB} when high ESR capacitors such as Aluminum Electrolytic or Tantalum are used on the output.

Table 2 shows the recommended minimum ceramic C_{OUT} and corresponding C_{PB}, R_2 and R_1 for different output voltages.

TABLE 2. RECOMMENDED C_{PB} FOR DIFFERENT V_{OUT} AND C_{OUT}

V_{OUT} (V)	R_2 (kΩ)	R_1 (kΩ)	C_{OUT} (µF)	C_{PB} (pF)
5.0	2.61	0.287	10	100
3.3	2.61	0.464	10	100
2.5	2.61	0.649	10	82
1.8	2.61	1.0	10	82
1.5	2.61	1.3	10	68
1.5	2.61	1.3	22	150
1.2	2.61	1.87	22	120
1.2	2.61	1.87	47	270
1.0	2.61	2.61	47	220
0.8	2.61	4.32	47	220

INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the “Recommended Operating Conditions (Notes 7, 8)” on page 4. The power dissipation can be calculated by using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 5)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 6:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad \text{(EQ. 6)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, enure that the power dissipation P_D, calculated from Equation 5, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 16 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

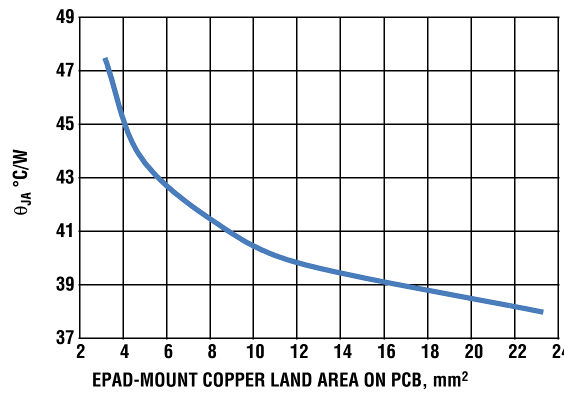


FIGURE 16. 3MMX3MM-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} VS EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

The power level and the thermal impedance of the package (+45°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

Current Limit Protection

The EY1501DI-ADJ LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the “Electrical Specifications” table on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage regulation mode. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition and subsequently cooling down after the power device is turned off.

Revision History

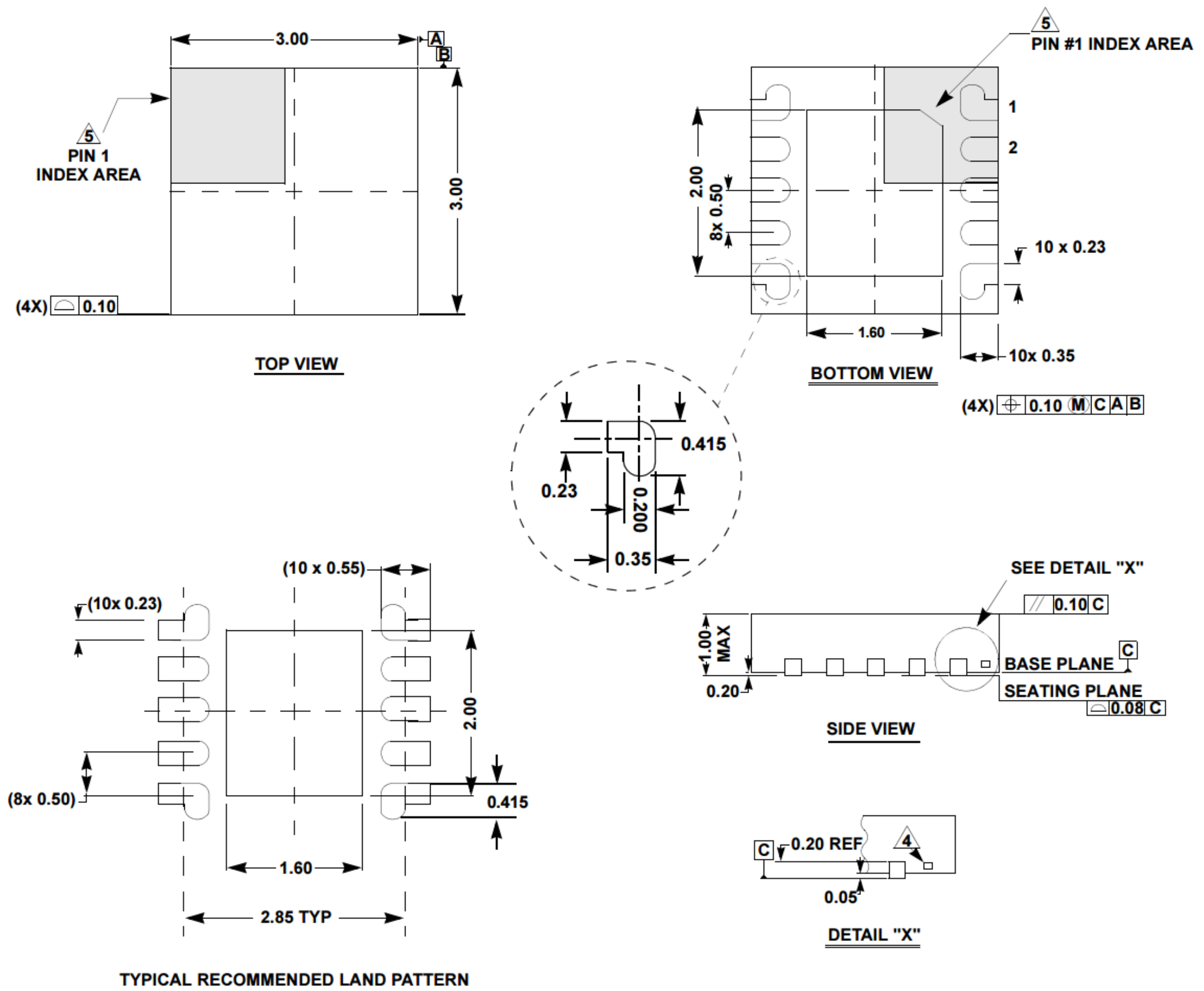
The table lists the revision history for this document.

DATE	REVISION	CHANGE
May, 2014	A	Initial Release.
Jan, 2017	B	Modified Package Diagram

Package Outline Drawing

L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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