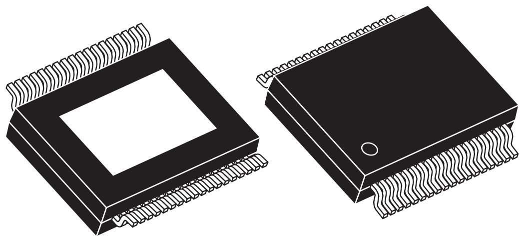
STA533WF

18-volt, 3-amp, quad power half-bridge

Features

- Multipower BCD technology
- Low input/output pulse width distortion
- 200-mΩ R_{dsON} complementary DMOS output stage
- CMOS-compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- Short-circuit protection



PowerSSO36 package
with exposed pad down

Description

The STA533WF is a monolithic quad half-bridge stage in multipower BCD technology. The device can be used as a dual bridge or reconfigured, by connecting pin CONFIG to pins VDD, as a single bridge with double-current capability.

The device is designed for the output stage of a stereo Full Flexible Amplifier (FFX™). It is capable of delivering 10 W x 4 channels into 4-Ω loads with 10% THD at V_{CC} = 18 V in single-ended configuration.

It can also deliver 20 W + 20 W into 8-Ω loads with 10% THD at V_{CC} = 18 V in BTL configuration or, in single parallel BTL configuration, 40 W into a 4-Ω load with 10% THD at V_{CC} = 18 V.

The input pins have a threshold proportional to the voltage on pin VL.

The STA533WF comes in a 36-pin PowerSSO package with exposed pad down (EPD).

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STA533WF	0 to 70 °C	PowerSSO36 EPD	Tube
STA533WF13TR	0 to 70 °C	PowerSSO36 EPD	Tape and reel

1 Pin description

Figure 1. Pin out

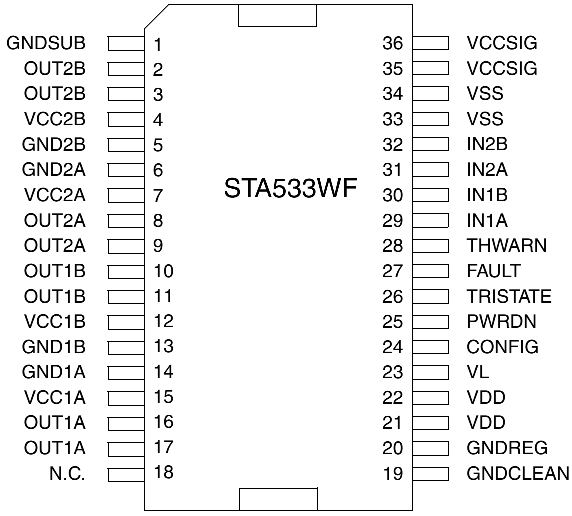


Table 2. Pin list

Pin	Name	Type	Description
1	GNDSUB	PWR	Substrate ground
2, 3	OUT2B	O	Output half-bridge 2B
4	VCC2B	PWR	Positive supply
5	GND2B	PWR	Negative supply
6	GND2A	PWR	Negative supply
7	VCC2A	PWR	Positive supply
8, 9	OUT2A	O	Output half-bridge 2A
10, 11	OUT1B	O	Output half-bridge 1B
12	VCC1B	PWR	Positive supply
13	GND1B	PWR	Negative supply
14	GND1A	PWR	Negative supply
15	VCC1A	PWR	Positive supply
16, 17	OUT1A	O	Output half-bridge 1A
18	N.C.	-	No internal connection
19	GNDCLEAN	PWR	Logical ground
20	GNDREG	PWR	Filtering for regulator; this is an internally generated ground for V_{DD}
21, 22	VDD	PWR	5-V regulator referred to ground
23	VL	PWR	High logical state setting voltage, V_L

Table 2. Pin list (continued)

Pin	Name	Type	Description
24	CONFIG	I	Configuration pin: 0: normal operation 1: bridges in parallel, see *Parallel-output and high-current operation on page 8*
25	PWRDN	I	Stand-by pin: 0: low-power mode 1: normal operation
26	TRISTATE	I	Hi-Z pin: 0: all power amplifier outputs in high-impedance state 1: normal operation
27	FAULT	O	Fault pin advisor (open-drain device, needs pull-up resistor): 0: fault detected (short circuit or thermal, for example) 1: normal operation
28	THWARN	O	Thermal-warning advisor (open-drain device, needs pull-up resistor): 0: temperature of the IC >130 ^{o}C 1: normal operation
29	IN1A	I	Input of half-bridge 1A
30	IN1B	I	Input of half-bridge 1B
31	IN2A	I	Input of half-bridge 2A
32	IN2B	I	Input of half-bridge 2B
33, 34	VSS	PWR	5-V regulator referred to +V_{CC}
35, 36	VCCSIG	PWR	Filtering for regulator, this is an internally generated supply for V_{SS}

2 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Pins 4, 7, 12, 15)	23	V
V_{Lmax}	Voltage on pin 23	4.0	V
V_{inputs}	Voltage on pins 25, 26, 29 to 32	-0.3 to V_L + 0.3	V
V_{config}	Voltage on pins 24	-0.3 to V_{DD} + 0.3	V
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	DC supply voltage (Pins 4, 7, 12, 15)	5.0	-	18	V
V_L	Input logic reference	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	0	-	70	°C

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	-	1.5	°C/W
T_{jSD}	Thermal shut-down junction temperature	-	150	-	°C
T_{warn}	Thermal warning temperature	-	130	-	°C
t_{hSD}	Thermal shut-down hysteresis	-	25	-	°C

Unless otherwise stated, the test conditions for *Table 6* below are V_L = 3.3 V, V_{CC} = 18 V, R_L = 8 Ω, f_{SW} = 384 kHz and T_{amb} = 25 °C.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
P_{OUT}	Output power in BTL mode	THD+N > 10%	-	20	-	W
R_{dsON}	Power P-channel/N-channel MOSFET on resistance	I_{dd} = 1 A	-	180	230	mΩ
I_{dss}	Power P-channel/N-channel leakage	-	-	-	10	µA
g_N	Power P-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
g_P	Power N-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	see *Figure 2*	-	5	10	ns

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Dt_d	High current dead time (dynamic)	L = 22 μH, C = 470 nF R_L = 8 Ω, I_{dd} = 2.0 A see *Figure 3*	-	10	20	ns
t_{d_ON}	Turn-on delay time	Resistive load	-	40	60	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	40	60	ns
t_r	Rise time	Resistive load see *Figure 2*	-	8	10	ns
t_f	Fall time	Resistive load see *Figure 2*	-	8	10	ns
$V_{IN\text{-}Low}$	Half-bridge input, low-level voltage	-	-	-	V_L / 2 - 300 mV	V
$V_{IN\text{-}High}$	Half-bridge input, high-level voltage	-	V_L / 2 + 300 mV	-	-	V
$I_{IN\text{-}H}$	High-level input current	$V_{IN} = V_L$	-	1	-	μA
$I_{IN\text{-}L}$	Low-level input current	V_{IN} = 0.3 V	-	1	-	μA
$I_{PWRDN\text{-}H}$	High level PWRDN pin input current	V_L = 3.3 V	-	35	-	μA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE)	V_L = 3.3 V	-	-	0.8	V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE)	V_L = 3.3 V	1.7	-	-	V
$I_{VCC\text{-}PWRDN}$	Supply current from V_{CC} in power down mode	V_{PWRDN} = 0 V	-	-	10	μA
I_{FAULT}	Output current on pins FAULT, THWARN with fault condition	V_{pin} = 3.3 V	-	1	-	mA
$I_{VCC\text{-}HiZ}$	Supply current from V_{CC} in 3-state	$V_{TRISTATE}$ = 0 V	-	22	-	mA
I_{VCC}	Supply current from V_{CC} in operation (both channels switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	50	-	mA
I_{OCP}	Overcurrent protection threshold (short-circuit current limit)	-	3.0	4.0	-	A
V_{UVP}	Undervoltage protection threshold	-	-	3.5	4.3	V
t_{pw_min}	Output minimum pulse width	No load	70	-	150	ns

Table 7. **Logic truth table**

Pin PWRDN	Pin TRISTATE	Inputs as per *Figure 3*		Transistors as per *Figure 3*				Output mode
		INxA	INxB	Q1	Q2	Q3	Q4	
0	0	x	x	Off	Off	Off	Off	Hi Z
1	1	0	0	Off	Off	On	On	Dump
1	1	0	1	Off	On	On	Off	Negative
1	1	1	0	On	Off	Off	On	Positive
1	1	1	1	On	On	Off	Off	Not used

Test circuits

Figure 2. **Test circuit**

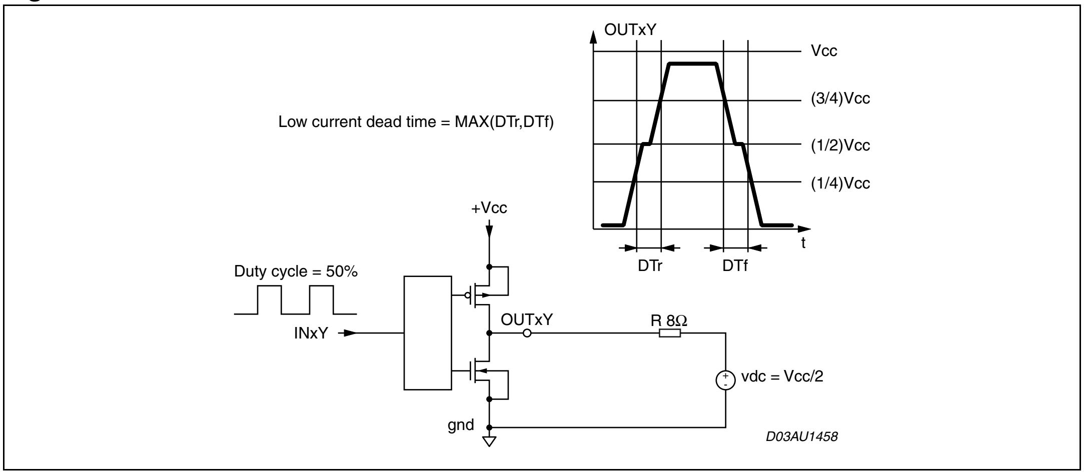
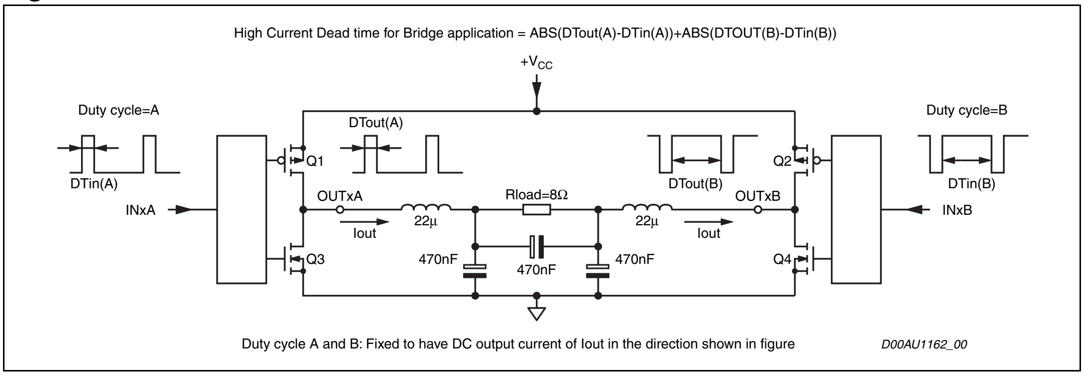


Figure 3. **Current dead time test circuit**



3 Applications information

The STA533WF is a dual-channel H-bridge audio power amplifier that can deliver 20 W per channel into 8 Ω with 10% THD at V_{CC} = 18 V with high efficiency.

The STA533WF converts both FFX and binary-logic-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high-efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In FFX mode, two logic-level signals per channel are used to control the high-speed MOSFET switches which drive the speaker load in a bridge configuration, according to the damped ternary modulation operation.

In binary mode, both full-bridge and half-bridge modes are supported.

The STA533WF includes overcurrent and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 4. Block diagram for FFX or binary modes

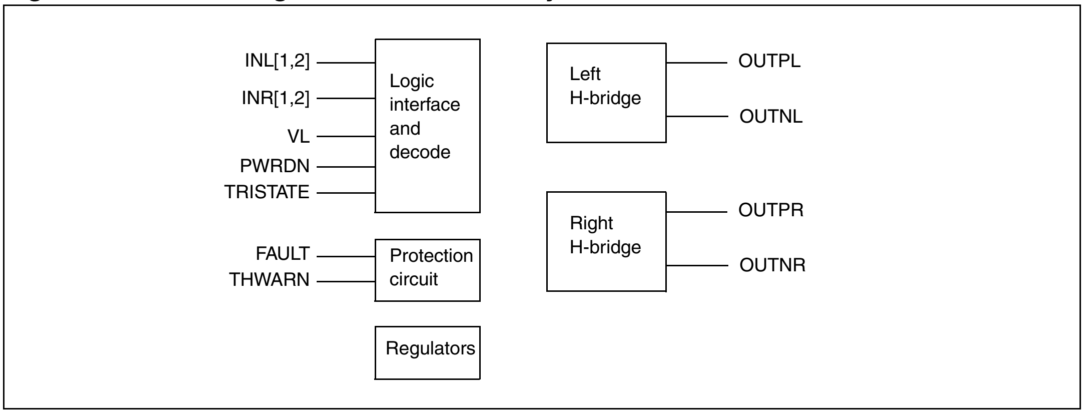
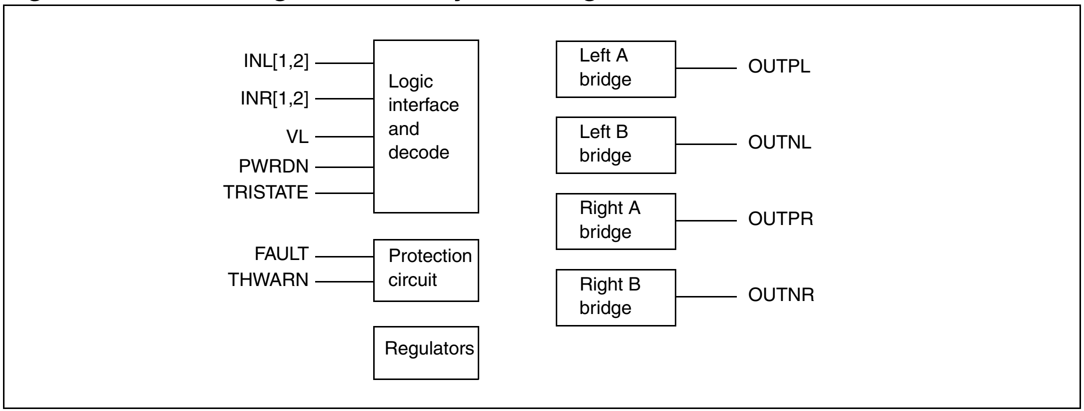


Figure 5. Block diagram for binary half-bridge mode



Logic interface and decode

The STA533WF power outputs are controlled using one or two logic-level timing signals. In order to provide a proper logic interface, pin VL must have the same voltage as the PWM input signal.

Protection circuits

The STA533WF includes protection circuitry for overcurrent and thermal overload conditions. A thermal warning pin (THWARN) is activated low (open-drain MOSFET) when the IC temperature exceeds 130 °C, which is in advance of the thermal shutdown protection. When a fault condition is detected an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-bridges in the high-impedance state. At the same time an open-drain MOSFET connected to pin FAULT is switched on.

There are two possible modes subsequent to activating a fault:

- Shutdown mode:
  with pins FAULT (with pull-up resistor) and TRISTATE independent, an activated fault disables the device, signalling low at pin FAULT.
  The device may subsequently be reset to normal operation by toggling pin TRISTATE from high to low and back to high using an external logic signal.
- Automatic recovery mode:
  This is shown in the applications circuit in *Figure 6* and *Figure 7 on page 10*.
  Pins FAULT and TRISTATE are shorted together and connected to a time constant circuit comprising R59 and C58.
  An activated fault forces a reset on pin TRISTATE causing normal operation to resume following a delay determined by the time constant of the circuit.
  If the fault condition is still present this operation continues to repeat until the fault condition is removed.
  An increase in the time constant of the circuit produces a longer recovery interval.

Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

Power outputs

The STA533WF power and output pins are duplicated to provide a low-impedance path for the device bridged outputs. All duplicated power, ground and output pins must be connected for reliable operation.

Pins PWRDN or TRISTATE should be used to set all MOSFETS to the high-impedance state during power-up and until the logic power supply on pin VL has settled.

Parallel-output and high-current operation

When using FFX mode, the STA533WF outputs can be connected in parallel to increase the output current capability. In this configuration the device can provide 40 W into 4 Ω.

This mode of operation is enabled with pin CONFIG connected to V_{DD}. The inputs must be combined to give INLA = INLB and INRA = INRB, then the corresponding outputs can be shorted together to give OUTLA = OUTLB and OUTRA = OUTRB.

The snubber RC network shown in the applications figures must be placed as close as possible to the output pins. This reduces ringing, over- and undervoltage effects, and improves the audio quality and EMI performance.

Supply decoupling capacitors

To meet the performance figures given in this datasheet the STA533WF power supply must be adequately filtered.

For this purpose capacitors connected from pins VCC1 to GND1 and from VCC2 to GND2 must be placed as close as possible to the related IC pins.

For reliability and optimum performance the following capacitors are suggested:

- 100-nF ceramic capacitor with lead length less than 2 mm, connected to the ground plane and as close as possible to the GND pin
- 1-uF X7R (low ESR) capacitors.

Pin GNDREG is used to filter the internal reference voltage V_{DD}; This pin must not be connected to other ground pins, it is an internally generated supply.

Pin VCCSIG is used to filter the internal reference voltage V_{SS}; This pin must not be connected to other supply pins, it is an internally generated supply.

Output filter

A passive 2nd-order filter is used on the STA533WF power outputs to reconstruct an analog audio signal. The system performance can be significantly affected by the output filter design and choice of passive components.

Filter designs for 4-Ω and 8-Ω loads are shown in the applications circuits below.

Applications circuits

Figure 6 shows a typical full-bridge circuit for supplying 20 W + 20 W into 8-Ω speakers with 10% THD when V_{CC} = 18 V.

Figure 7 shows a single-BTL configuration capable of supplying 40 W into a 4-Ω load at 10% THD when V_{CC} = 19 V. This result was obtained with peak power for <1 s using the STA309A + STA533WF demo board.

For both applications circuits a PWM modulator is required as driver.

Figure 6. Applications circuit for stereo full-bridge configuration

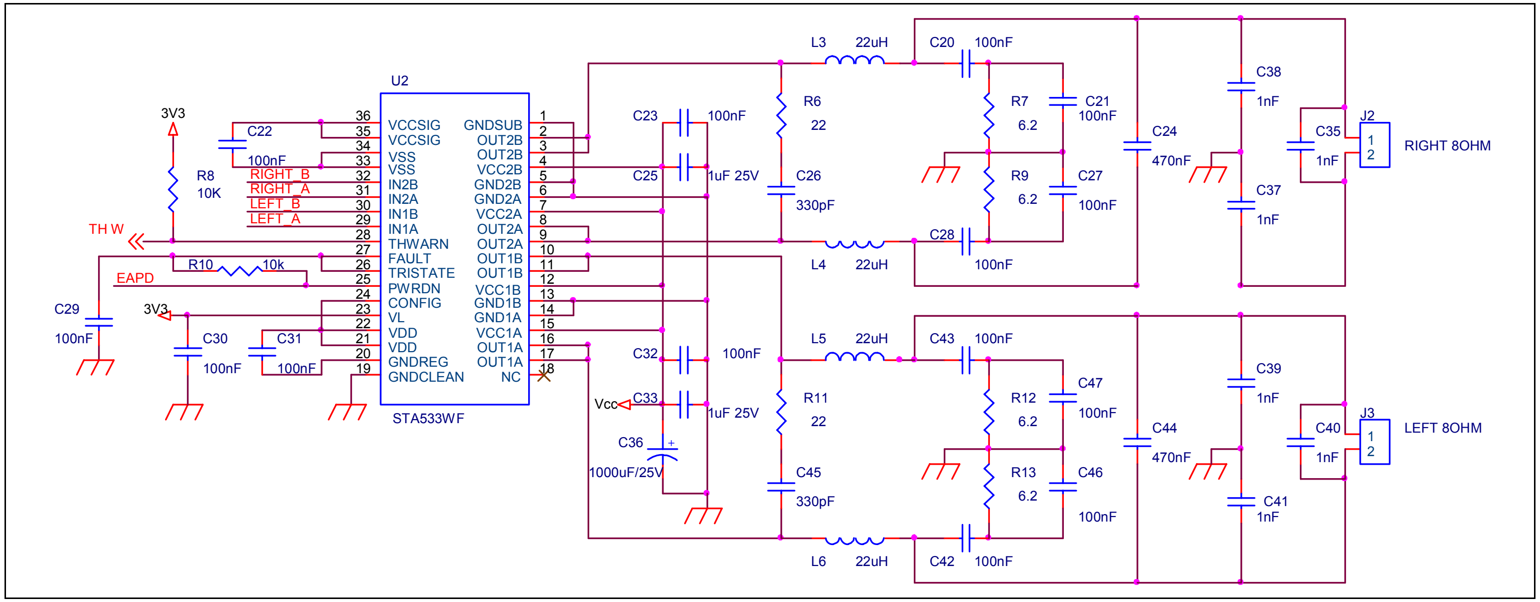
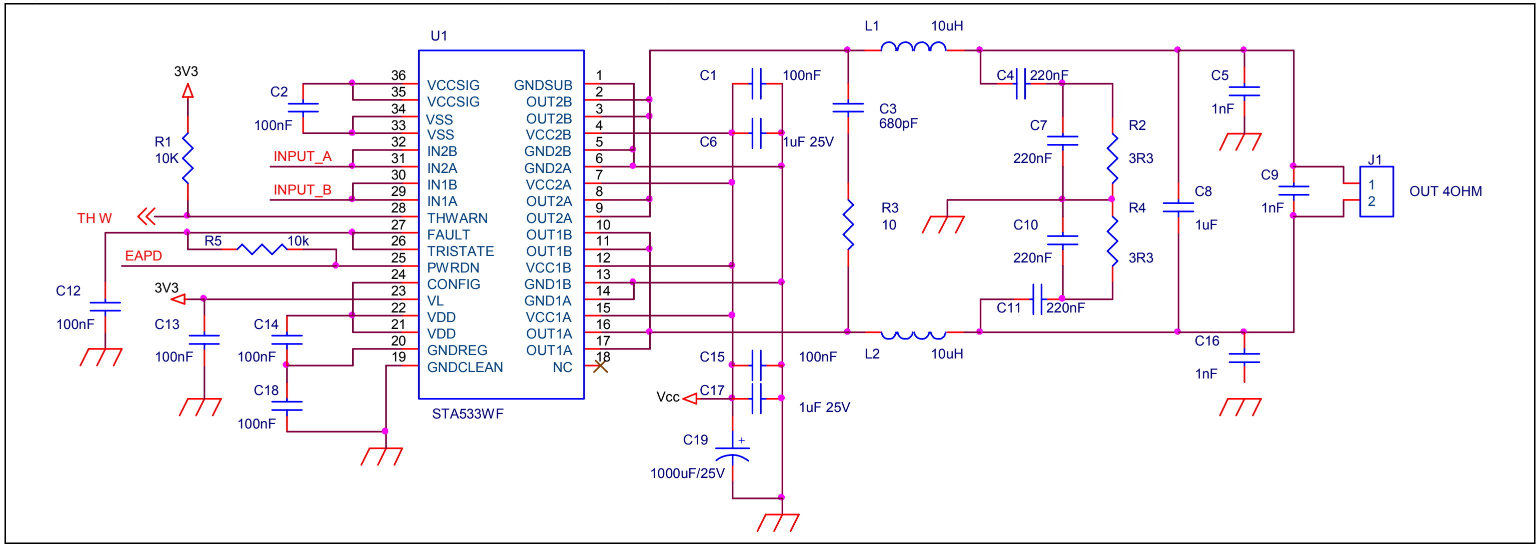


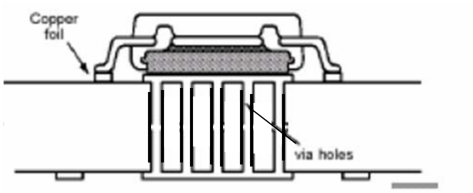
Figure 7. Applications circuit for single-BTL configuration



4 Heatsink requirements

Using the STA533WF mounted on a double-layer PCB having 2 copper ground areas of 3 x 3 cm^2 and with 16 via holes the junction to ambient thermal resistance is approximately 24 °C/W in natural air convection.

Figure 8. Double-layer PCB with copper ground areas and 16 via holes



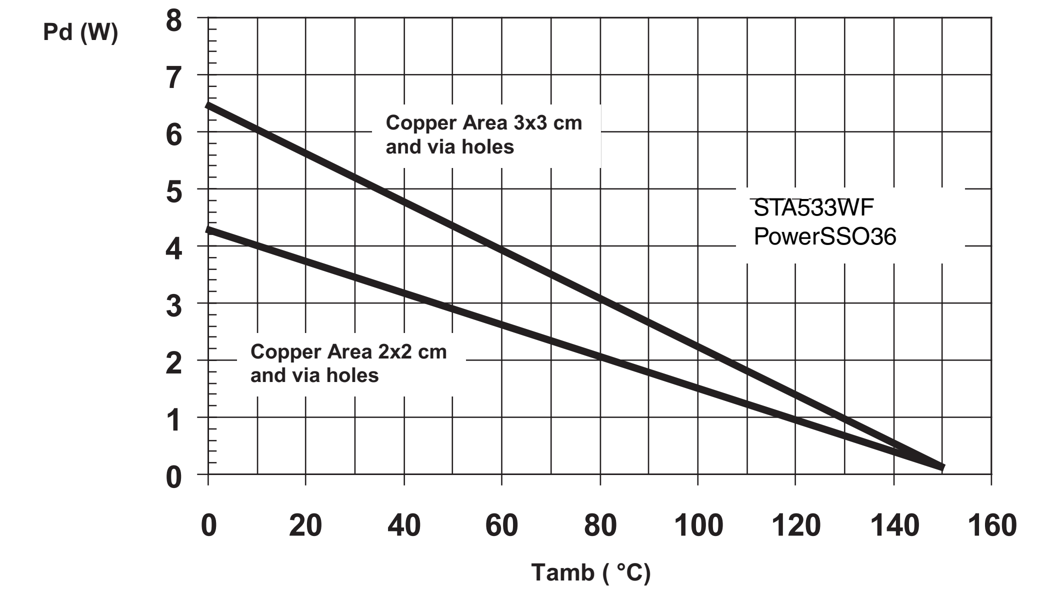
With the dissipated power within the device depending primarily on the supply voltage, the load impedance and the output modulation level, the maximum estimated dissipated power, Pdmax, for the STA533WF is:

4 W for 2 x 20 W into 8 Ω at 18 V

< 5 W for 2 x 10 W into 8 Ω + 1 x 20 W into 4 Ω at 18 V.

The figure below shows the power derating curve for the PowerSSO36 EPD package on PCBs with copper areas of 2 x 2 cm^2 and 3 x 3 cm^2.

Figure 9. Power derating curves for PCB used as heatsink



5 Package mechanical data

The STA533WF comes in a 36-pin PowerSSO package with exposed pad down (EPD).

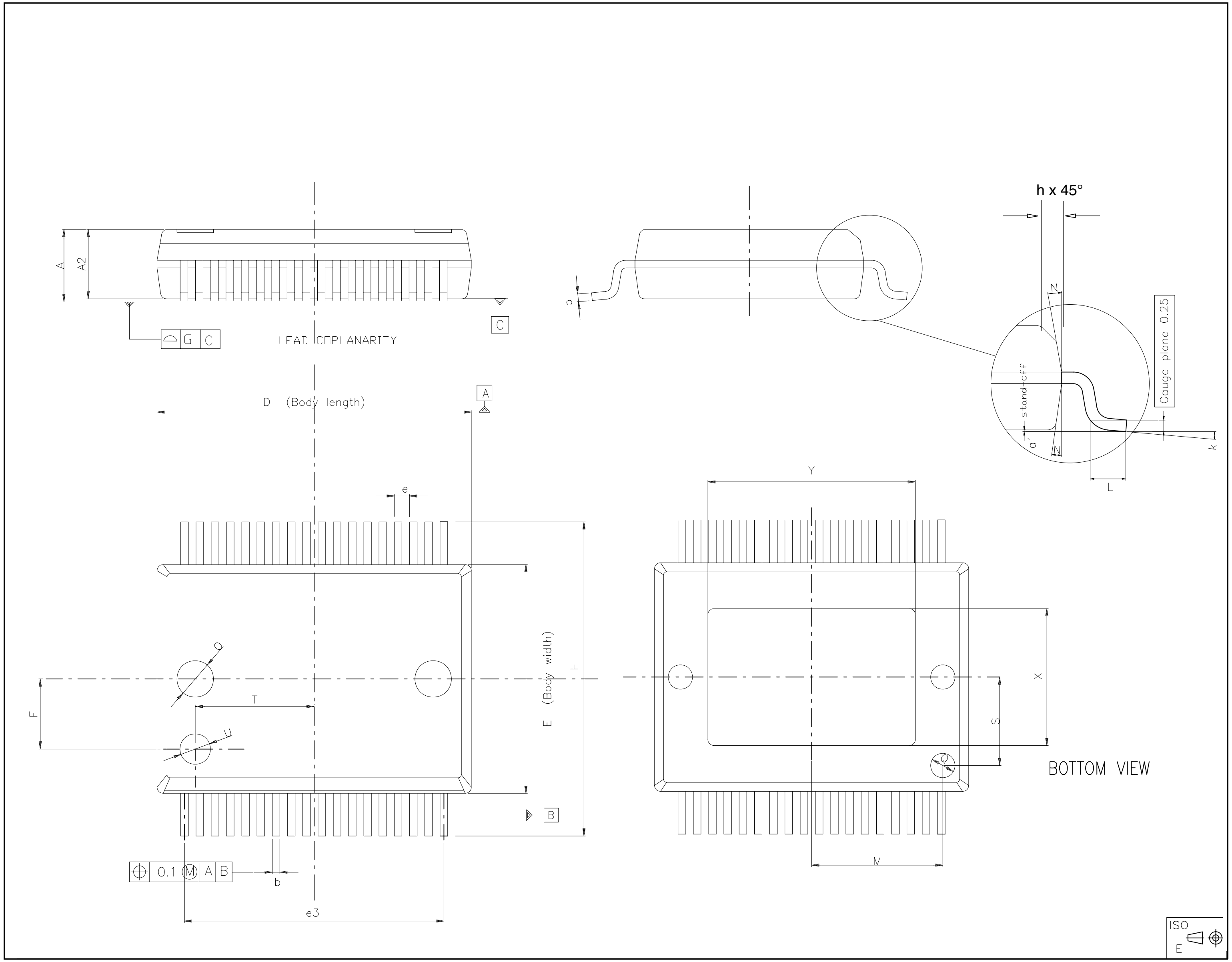
Figure 10 below shows the package outline and *Table 8* gives the dimensions.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerSSO36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.000	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	6.50	-	7.10	0.256	-	0.280

Figure 10. PowerSSO36 EPD outline drawing



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Jul-2010	1	Initial release.
22-Jun-2011	2	Updated *Applications circuits on page 9*

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