I²C-bus Serial Interface Real Time Clock (8pin SSOP)

RS5C372B

■ OUTLINE

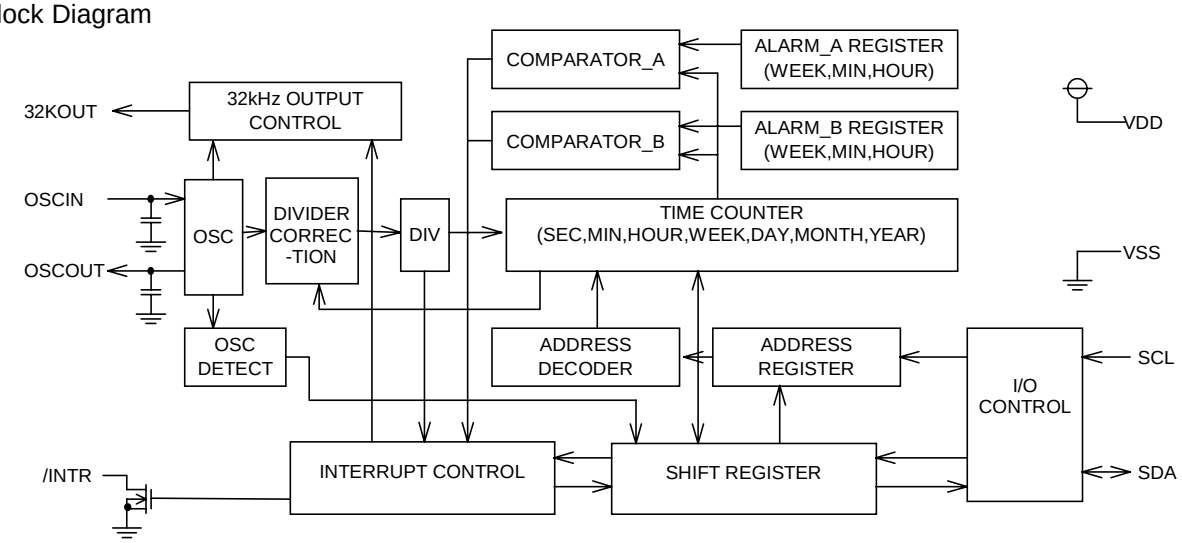
The RS5C372B is a CMOS type real-time clock which is connected to the CPU via 2-wire and capable of serial transmission of clock and calendar data to the CPU. The RS5C372B can generate various periodic interrupt clock pulses lasting for long period (one month), and alarm interrupt can be made by days of the week, hours, and minutes by two incorporated systems. Since an oscillation circuit is driven at a constant voltage, it undergoes fluctuations of few voltage and consequently offers low current consumption (0.5µA at 3V). It also provides an oscillator halt sensing function applicable for data validation at power-on and other occasions and 32kHz clock output (CMOS output) for an external micro computer. The product also incorporates a time trimming circuit that adjusts the clock with higher precision by adjusting any errors in crystal oscillator frequencies based on signals from the CPU. The crystal oscillator may be selected between 32.768kHz or 32.000kHz types. Integrated into an ultra compact and ultra thin 8 pin SSOP package, the RS5C372B is the optimum choice for equipment requiring small sized and low power consuming products.

■ Features

- ● Time keeping voltage 1.45V to 6.0V
- ● Lowest supply current 0.5µA TYP (0.9µA MAX) at 3V(25°C)
  (0.9µA MAX) at 3V(-40 to +85°C)
- ● Connected to the CPU via only 2-wire (I²C-bus interface, max.400KHz, address 7bits)
- ● A clock counter (hours, minutes, and seconds) and a calendar counter (leap years, years, months, days, and days of the week) in BCD codes
- ● Interrupt to the CPU (period of one month to half second, with interrupt flag, interrupt halt function) (/INTR)
- ● Two systems of alarm functions (days of the week, hours, and minutes) (/INTR)
- ● Oscillation halt sensing to judge internal data validity
- ● Clock output of 32.768kHz(32.000kHz) (output controllable via a register) (32KOUT:CMOS push-pull output)
- ● Second digit adjustment by ±30 seconds
- ● Automatic leap year recognition up to the year 2099
- ● 12-hour or 24-hour time display selectable
- ● Oscillation stabilizing capacity (CG, CD) incorporated
- ● High precision clock error adjustment circuit
- ● Oscillator of 32.768kHz or 32.000kHz may be used
- ● CMOS logic
- ● Package:8pin SSOP

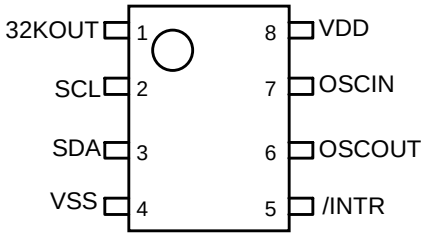
*) I²C-bus is a trademark of PHILIPS ELECTRONICS N.V.

■ Block Diagram



■ Pin Configuration

RS5C372B (8PIN SSOP)



TOP VIEW

■ Pin Description

Symbol	Pin Name	Description
SCL	Shift clock input	This pin is used to input shift clock pulses to synchronize data input/output to and from the SDA pin with this clock. Up to 6V beyond VDD may be input.
SDA	Serial input output	This pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCL pin. Up to 6V beyond VDD may be input. This pin functions as an Nch open drain output.
/INTR	Interrupt output	This pin outputs periodic interrupt pulses and alarm interrupt (ALARM_A, ALARM_B) to the CPU. This pin is off when power is activated from 0V. This pin functions as an Nch open drain output.
32KOUT	32K Clock Output	This pin outputs 32.768kHz pulses (when 32.768kHz crystal is used), It outputs 32.768kHz when power source is activated from 0V. This pin functions as an CMOS push-pull output.
OSCIN OSCOUT	Oscillator circuit input/output	These pins configure an oscillator circuit by connecting a 32.768kHz or 32.000kHz crystal oscillator between the OSCIN–OSCOUT pins. (Any other oscillator circuit components are built into the RS5C372B.)
VDD VSS	Positive power supply input Negative power supply input	The VDD pin is connected to the positive power supply and Vss to the ground.

■ Absolute Maximum Ratings

(VSS=0V)

Symbol	Item	Conditions	Ratings	Unit
VDD	Supply Voltage		-0.3 to +7.0	V
VI	Input Voltage	SCL, SDA	-0.3 to +7.0	V
VO	Output Voltage 1	SDA	-0.3 to +7.0	V
	Output Voltage 2	/INTR	-0.3 to +12.0	
	Output Voltage 3	32KOUT	-0.3 to VDD+0.3	
PD	Power Dissipation	Topt=25°C	300	mW
Topt	Operating Temperature		-40 to +85	°C
Tstg	Storage Temperature		-55 to +125	°C

■ Recommended Operating Conditions

(VSS=0V, Topt=-40 to +85°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
VDD	Operating Voltage		2.0		6.0	V
VCLK	Time Keeping Voltage		1.45		6.0	V
FXT	Oscillation Frequency			32.768 or 32.000		kHz
VPUP1	Pull up Voltage 1	SCL, SDA			6.0	V
VPUP2	Pull up Voltage 2	/INTR			10.0	V

■ DC Characteristics

Unless otherwise specified: VSS=0V, VDD=3V, Topt=-40 to +85°C, Oscillation Frequency=32.768kHz or 32.000KHz(R1=30kΩ)

Symbol	Item	Pin Name	Conditions	MIN.	TYP.	MAX.	Unit
VIH	"H" input Voltage	SCL, SDA		0.8VDD		6.0	V
VIL	"L" input voltage	SCL, SDA		-0.3		0.2VDD	V
IOH	"H" output current	32KOUT	VOH=VDD-0.5V			-0.5	mA
IOL1	"L" output current	/INTR, 32KOUT	VOL1=0.4V	1			mA
IOL2		SDA	VOL2=0.6V	6			
IILK	Input leakage current	SCL	VI=6V or VSS VDD=6V	-1		1	µA
IOZ	Output off state leakage current	SDA, /INTR, 32KOUT	VO=6V or VSS VDD=6V	-1		1	µA
IDD1	Standby current	VDD	VDD=3V, Topt=25°C SCL,SDA=3V Output=OPEN *)		0.5	0.9	µA
IDD2		VDD	VDD=3V, Topt=-40 to +85°C SCL,SDA=3V Output=OPEN *)			1.0	µA
IDD3		VDD	VDD=6V SCL,SDA=6V Output=OPEN *)		0.8	2.0	µA
CG	Internal oscillation capacitance 1	OSCIN			10		pF
CD	Internal oscillation capacitance 2	OSCOUT			10		pF

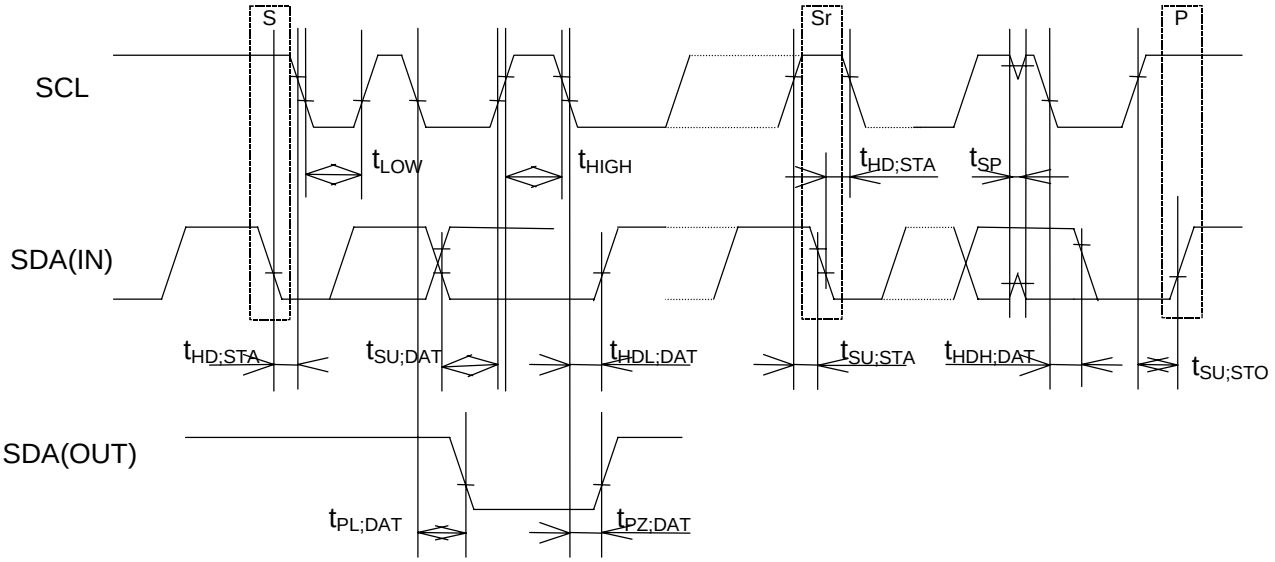
*) The mode outputs no clock pulses and output is open (output off state).
For consumption current (output: no load) when 32kHz pulses are output from 32KOUT, see "Typical Characteristics Measurement ".

■ AC Characteristics

Unless otherwise specified: VSS=0V,Topt=-40 to +85°C

I/O Conditions: VIH=0.8×VDD,VIL=0.2×VDD,VOL=0.2×VDD,CL=50pF

Symbol	Item	Condi-tions	VDD≥2.0V			VDD≥2.5V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
t_{LOW}	SCL clock "L" time		4.7			1.3			µs
t_{HIGH}	SCL clock "H" time		4.0			0.6			µs
$t_{HD;STA}$	Hold time for a (repeated) start condition		4.0			0.6			µs
$t_{SU;STO}$	Set-up time for a stop condition		4.0			0.6			µs
$t_{SU;STA}$	Set-up time for a repeated start condition		4.7			0.6			µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
$t_{HDH;DAT}$	"H" Data hold time		0			0			ns
$t_{HDL;DAT}$	"L" Data hold time		35			35			ns
$t_{PL;DAT}$	SDA low stable time after falling of SCL				2.0			0.9	µs
$t_{PZ;DAT}$	SDA off stable time after falling of SCL				2.0			0.9	µs
t_R	Rising time of SCL and SDA (input)				1000			300	ns
t_F	Falling time of SCL and SDA (input)				300			300	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input Filter				50			50	ns



S Start Condition

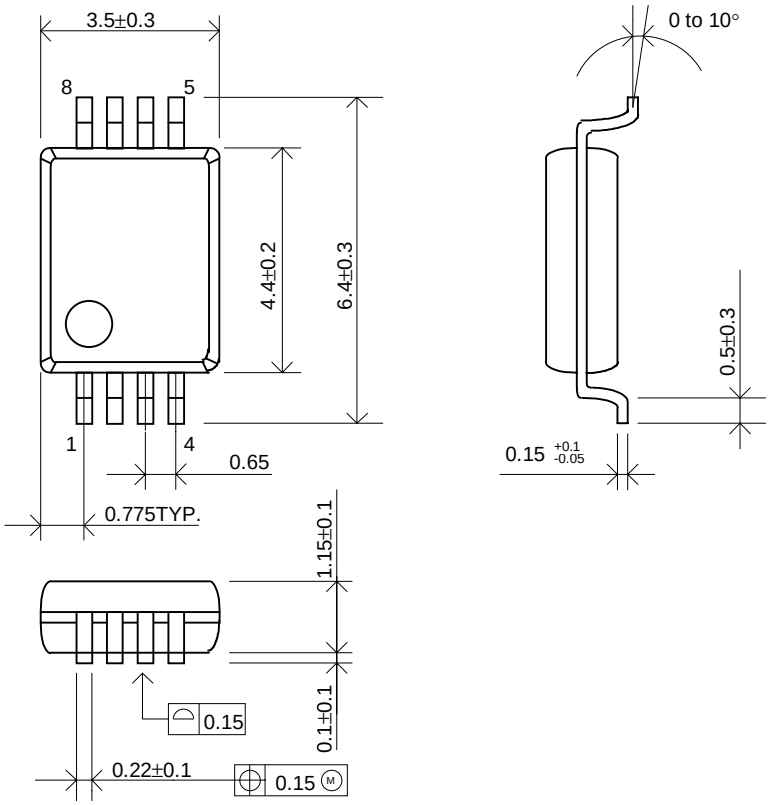
P Stop Condition

Sr Repeated Start condition

*For detailed information refer to "■Operation 1.2. I²C-BUS transmission system"

■ Package Dimensions (Unit : mm)

● RS5C372B (8pin SSOP)

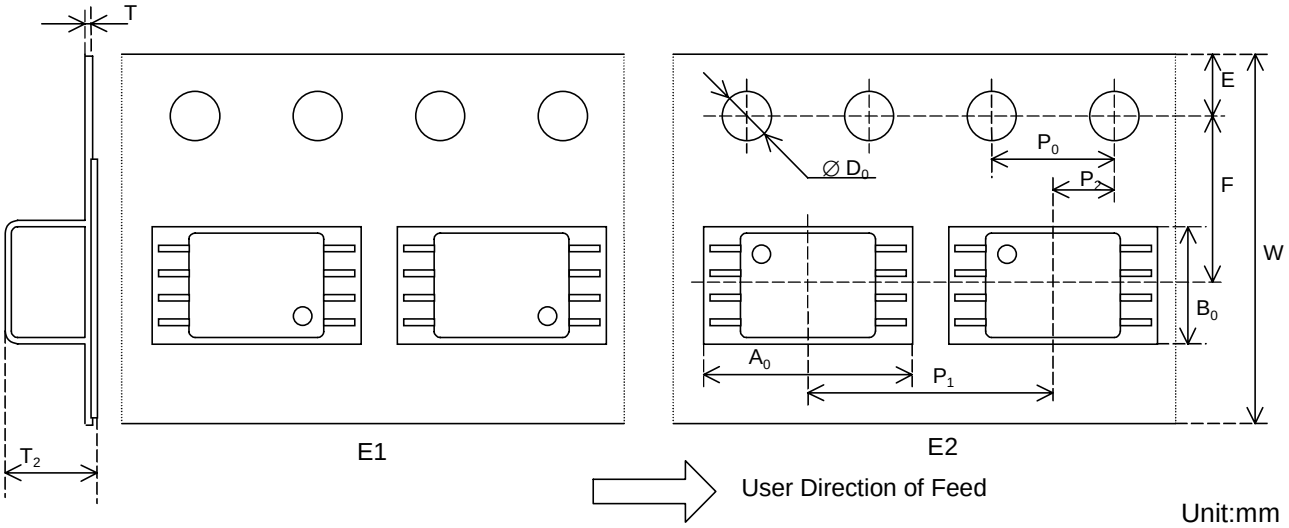


■ Selection Guide

Taping type can be designated as follows: (Standard type is E2)

RS5C372B-E1, RS5C372B-E2

■ Taping Specification



A_0	B_0	W	F	E	P_1	P_2	P_0	D_0	T	T_2
6.7	3.9	12.0 ±0.3	5.5 ±0.05	1.75 ±0.1	8.0 ±0.1	2.0 ±0.05	4.0 ±0.1	1.5 +0.1 0	0.3 ±0.1	2.7 Max

■ Outline Description

1. Interfacing with the CPU

The RS5C372B reads/writes data over I^2C-bus interface via two signal lines: SDA (data) and SCL (clock). Since the output of the I/O pin of SDA is open drain, data interfacing with a CPU with different supply voltage is possible by applying pull-up resistance on the circuit board. The maximum clock frequency of 400kHz of SCL enables data transfer in I^2C-bus high-speed mode.

2. Clock function

The clock function of the RS5C372B allows write/read data from lower two digits of the dominical year to seconds to and from the CPU. When lower two digits of the dominical year are multiples of 4, the year is recognized as a leap year automatically. Up to the year 2099 leap years will be automatically recognized.

*) The year 2000 is a leap year while the year 2100 is not.

3. Alarm function

The RS5C372B has an alarm function that outputs an interrupt signal from /INTR output pins to the CPU when the day of the week, hour or minute corresponds to the setting. These two systems of alarms (ALARM_A, ALARM_B), each may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week.

The ALARM_A and ALARM_B is output from the /INTR pins. Polling is possible separately for each alarm system.

4. High precision time trimming function

The RS5C372B has internal oscillation circuit capacitance CG and CD so that an oscillation circuit may be configured simply by externally connecting a crystal. Either 32.768kHz or 32.000kHz may be selected as a crystal oscillator by setting the internal register appropriately. The RS5C372B incorporates a time trimming circuit that adjusts gain or loss of the clock from the CPU up to approx. ±189ppm (±194ppm when 32.000kHz crystal is used) by approximately 3ppm steps to correct discrepancy in oscillation frequency. (Error after correction:±1.5ppm:25°C)

Thus by adjusting frequencies for each system,

- Clock display is possible at much higher precision than conventional real-time clock while using a crystal with broader fluctuation in precision.
- Even seasonal frequency fluctuation may be corrected by adjusting seasonal clock error.
- For those systems that have temperature detection precision of clock function may be increased by correcting clock error according to temperature fluctuations.

5. Oscillation halt sensing

The oscillation halt sensing function uses a register to store oscillation halt information. This function may be used to determine if the RS5C372B supply power has been booted from 0V and if it has been backed up. This function is useful for deter-mining if clock data is valid or invalid.

6. Periodic interrupt

The RS5C372B can output periodic interrupt pulses in addition to alarm function from the /INTR pin. This frequency may be selected from 2Hz (every 0.5 seconds), 1Hz (every second), 1/60Hz (every minute), 1/3600Hz (every hour) and monthly (1st of month).

Output wave form for periodic interrupt may be selected from regular pulse wave form (2Hz and 1Hz) and wave forms (every second, every minute, every hour and every month) that are appropriate for CPU level interrupt. The RS5C372B has polling function that monitors pin status in the register.

7. 32kHz clock output

The RS5C372B may output oscillation frequency from the 32KOUT pin. This clock output is set for output by default, which is set to on or off by setting the register. This pin functions as an CMOS push-pull output.

Notes:
The year-digit counter of RS5C372B counts only lower two digits of a year and no counter is supplied for upper two digits. When you are going to use this product in a system that must cope with “2000 year problem” which shall be corrected by software.

Notes:
Purchase of I^2C components of Ricoh Company, Ltd. conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system comforms to the I^2C Standard Specification as defined by Philips.

■ Functional Description

1. Allocation of Internal Addresses

	Internal Address	Contents	Data *1)							
	A3A2A1A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0 0 0 0	Second Counter	-*2)	S40	S20	S10	S8	S4	S2	S1
1	0 0 0 1	Minute Counter	-	M40	M20	M10	M8	M4	M2	M1
2	0 0 1 0	Hour Counter	-	-	H20 P·/A	H10	H8	H4	H2	H1
3	0 0 1 1	Day-of- the-Week Counter	-	-	-	-	-	W4	W2	W1
4	0 1 0 0	Day Counter	-	-	D20	D10	D8	D4	D2	D1
5	0 1 0 1	Month Counter	-	-	-	MO10	MO8	MO4	MO2	MO1
6	0 1 1 0	Year Counter	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
7	0 1 1 1	Time Trimming Register	/XSL	F6	F5	F4	F3	F2	F1	F0
8	1 0 0 0	Alarm_A (Minute Register)	-	AM40	AM20	AM10	AM8	AM4	AM2	AM1
9	1 0 0 1	Alarm_A (Hour Register)	-	-	AH20 AP·/A	AH10	AH8	AH4	AH2	AH1
A	1 0 1 0	Alarm_A (Day-of-the-week Register)	-	AW6	AW5	AW4	AW3	AW2	AW1	AW0
B	1 0 1 1	Alarm_B (Minute Register)	-	BM40	BM20	BM10	BM8	BM4	BM2	BM1
C	1 1 0 0	Alarm_B (Hour Register)	-	-	BH20 BP·/A	BH10	BH8	BH4	BH2	BH1
D	1 1 0 1	Alarm_B (Day-of-the-week Register)	-	BW6	BW5	BW4	BW3	BW2	BW1	BW0
E	1 1 1 0	Control Register 1	AALE	BALE	0 *5)	0 *5)	TEST	CT2	CT1	CT0
F	1 1 1 1	Control Register 2	-	-	/12·24	ADJ XSTP *3),*4)	/CLEN	CTFG	AAFG	BAFG

*1) All the listed data can be read and written except for ADJ/XSTP.
*2) The "–" mark indicates data which can be read only and set to "0" when read.
*3) The ADJ/XSTP bit of the control register2 is set to ADJ for write and XSTP for read operation.
The XSTP bit is set to "0" by writing data into the control register2 for normal oscillation.
*4) When XSTP is set to "1" the /XSL, F6 to F0, CT2 to CT0, AALE, BALE, /CLEN and TEST bits are reset to "0".
*5) These bits must be set to "0" in any case.

2. Functions of Registers

2.1. Control Register 1 (Internal address at Eh)

D7	D6	D5	D4	D3	D2	D1	D0	
AALE	BALE	0 *1)	0 *1)	TEST	CT2	CT1	CT0	(For write operation)
AALE	BALE	0	0	TEST	CT2	CT1	CT0	(For read operation)
0	0	0	0	0	0	0	0	Default *2)

*1) These bits must be set “0” in any case.

*2) The default means read values when XSTP=”1” by after initial power-on or supply voltage drop,etc.

2.1.1. AALE,BALE Alarm_A, Alarm_B enable bit

AALE,BALE	Description	
0	Alarm_A (Alarm_B) correspondence action invalid	(Default)
1	Alarm_A (Alarm_B) correspondence action valid	

2.1.2. TEST Test bit

TEST	Description	
0	Ordinary operation mode	(Default)
1	Test mode	

The test bit is used for IC test. Set the TEST bit to 0 in ordinary operation.

2.1.3. CT2,CT1,CT0 Periodic interrupt frequency select bit

CT2	CT1	CT0	Description		
			Wave form mode	Frequency and falling timing	
0	0	0	-	OFF(H)	(Default)
0	0	1	-	Fixed at “L”	
0	1	0	Pulse mode	2Hz(Duty50%)	
0	1	1	Pulse mode	1Hz(Duty50%)	
1	0	0	Level mode	Every second (synchronized with second count up)	
1	0	1	Level mode	Every minute (00 second of every minute)	
1	1	0	Level mode	Every hour (00 minute(s) 00 second(s) of every hour)	
1	1	1	Level mode	Every month (the 1st day 00 AM 00 minute(s) 00 second(s) of every month)	

1) Pulse mode: Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds, see the diagram on the next page.

*) When 32000Hz crystal is used

In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternately. Duty cycle for 1Hz clock pulses becomes 50.4% (“L” duration is 0.496s while “H” duration is 0.504s).

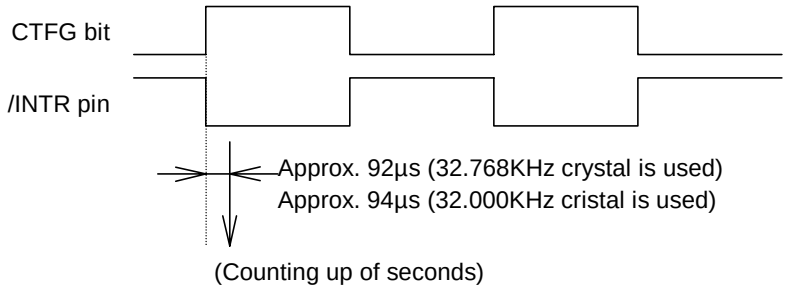
2) Level mode: One second, one minute or one month may be selected for an interrupt frequency. Counting up of seconds is matched with falling edge of interrupt output.

3) When the clock error correction circuit is used, periodic interrupt frequency changes every 20 seconds.

Pulse mode: “L” duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.) For example, Duty will be 50±0.3784% (or 50±0.3875% when 32.000kHz crystal is used) at 1Hz.

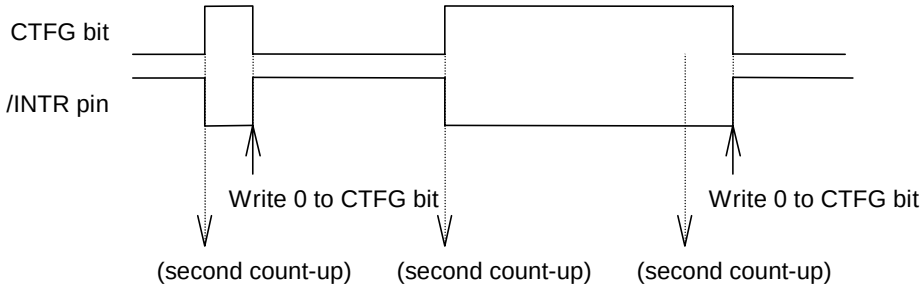
Level mode: Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)

Pulse mode



*) Since counting up of seconds and the falling edge has a time lag of approx. 92µs (at 32.768kHz) (approx. 94µs when 32.000kHz crystal is used), time with apparently approx. one second of delay from time of the real-time clock may be read when time is read in synchronization with the falling edge of output.

Level mode



2.2. Control Register 2 (Internal address at Fh)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	/12·24	ADJ	/CLEN	CTFG	AAFG	BAFG	(For Write operation)
0	0	/12·24	XSTP	/CLEN	CTFG	AAFG	BAFG	(For Read operation)
0	0	unde-fined	1	0	0	0	0	Default (*)

*)The default means read values when XSTP=”1” by after initial power-on or supply voltage drop,etc.

2.2.1. /12·24 /12·24-hour Time Display Selection bit

/12·24	Description
0	12-hour time display system
1	24-hour time display system

Being set this bit at “0” indicates 12-hour display system while “1” indicates 24-hour system.

Time Display Digit Table

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

*) Either the 12-hour or 24-hour time display system should be selected before writing time data.

2.2.2. ADJ ±30 Second Adjust Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

• The following operations are performed by setting the second ADJ bit to 1.

1) For second digits ranging from “00” to “29” seconds:
Time counters smaller than seconds are reset and second digits are set to “00”.

2) For second digits ranging from “30” to “59” seconds:
Time counters smaller than seconds are reset and second digits are set to “00”. Minute digits are incremented by 1.

• Second digits are adjusted within 122µs (within 125µs:when 32.000kHz crystal is used) from writing operation to ADJ.

• The ADJ bit is for write only and allows no read operation.

2.2.3. XSTP Oscillator Halt Sensing Bit

XSTP	Description	
0	Ordinary oscillation	
1	Oscillator halt sensing	(Default)

The XSTP bit senses the oscillator halt.

• When oscillation is halted after initial power on from 0V or drop in supply voltage the bit is set to “1” and which remains to be “1” after it is restarted. This bit may be used to judge validity of clock and calendar count data after power on or supply voltage drop.

• When this bit is set to “1”, /XSL, F6-F0, CT2, CT1, CT0, AALE, BALE, /CLEN and TEST bits are reset to “0”. /INTR will stop output and the 32KOUT outputs 32kHz clock pulses.

• The XSTP bit is set to "0" by setting some data to the control register 2 (address Fh) during ordinary oscillation.

2.2.4. /CLEN 32kHz Clock Output Bit

/CLEN	Description	
0	32kHz clock output enabled	(Default)
1	32kHz clock output disabled	

By setting this bit to “0”, output of clock pulses of the same frequency as the crystal oscillator from 32KOUT pin, is enabled.

2.2.5. CTFG Periodic Interrupt Flag Bit

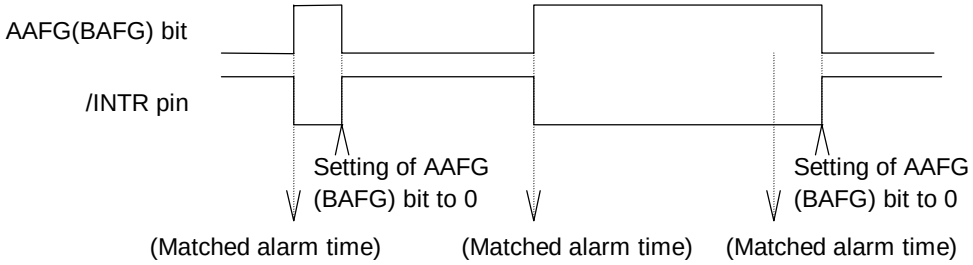
CTFG	Description	
0	Periodic interrupt output = OFF (H)	(Default)
1	Periodic interrupt output = ON (L)	

This bit is set to “1” when periodic interrupt pulses are output (/INTR=L).
The CTFG bit may be set only to “0” in the interrupt level mode. Setting this bit to “0” sets the /INTR pin to OFF (H). When this bit is set to “1”, nothing happens.

2.2.6. AAFG,BAFG Alarm_A (Alarm_B) Flag bit

AAFG,BAFG	Description	
0	Unmatched alarm register with clock counter	(Default)
1	Matched alarm register with clock counter	

• The alarm interruption is enabled only when the AALE, BALE bits are set to “1”. This bit turns to “1” when matched time is sensed for each alarm.
• The AAFG, BAFG bit may be set only to “0”. Setting this bit to “0” sets the /INTR to the OFF(H). When this bit is set to “1” nothing happens.
• When the AALE, BALE bit is set to “0”, alarm operation is disabled and “0” is read from the AAFG, BAFG bit.



2.3. Clock Counter (Internal address at 0-2h)

2.3.1. Second Digit Register (Internal address at 0h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	S40	S20	S10	S8	S4	S2	S1	(for write operation)
0	S40	S20	S10	S8	S4	S2	S1	(for read operation)
0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

2.3.2. Minute Digit Register (Internal address at 1h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	M40	M20	M10	M8	M4	M2	M1	(for write operation)
0	M40	M20	M10	M8	M4	M2	M1	(for read operation)
0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

2.3.3. Hour Digit Register (Internal address at 2h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	P·/AorH20	H10	H8	H4	H2	H1	(for write operation)
0	0	P·/AorH20	H10	H8	H4	H2	H1	(for read operation)
0	0	unde -fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

*)The default means read values when XSTP=”1” by after initial power-on or supply voltage drop,etc.
• Time digit display (in BCD code)
Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.

Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
Hour digits: See descriptions on the 12/24 bit (Section 2.2.1).
Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

- Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

2.4. Day of the Week Counter (Internal address at 3h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	W4	W2	W1	(for write operation)
0	0	0	0	0	W4	W2	W1	(for read operation)
0	0	0	0	0	unde-fined	unde-fined	unde-fined	Default(*)

*)The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

- Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
- Day-of-the-week digits display (incremented in septimal notation):
  (W4W2W1)=(000)→(001) →·····→ (110) → (000)
- The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=0,0,0).
- The (W4, W2, W1) should not be set to (1, 1, 1).

2.5. Calendar Counter (Internal address at 4-6h)

2.5.1. Day Digit Register (Internal address at 4h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	D20	D10	D8	D4	D2	D1	(for write operation)
0	0	D20	D10	D8	D4	D2	D1	(for read operation)
0	0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

2.5.2. Month Digit Register (Internal address at 5h)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	MO10	MO8	MO4	MO2	MO1	(for write operation)
0	0	0	MO10	MO8	MO4	MO2	MO1	(for read operation)
0	0	0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

2.5.3. Year Digit Register (Internal address at 6h)

D7	D6	D5	D4	D3	D2	D1	D0	
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	(for write operation)
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	(for read operation)
unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*)

*)The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

- The automatic calendar function provides the following calendar digit displays in BCD code.

Day digits: Range from 1 to 31 (for January, March, May, July, August, October, and December).
Range from 1 to 30 (for April, June, September, and November).
Range from 1 to 29 (for February in leap years).
Range from 1 to 28 (for February in ordinary years).
Carried to month digits when cycled to 1.

Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
Year digits: Range from 00 to 99 and 00, 04, 08,..., 92, and 96 are counted as leap years.

• Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

2.6. Time Trimming Register (Internal address at 7h)

D7	D6	D5	D4	D3	D2	D1	D0	
/XSL	F6	F5	F4	F3	F2	F1	F0	(for write operation)
/XSL	F6	F5	F4	F3	F2	F1	F0	(for read operation)
0	0	0	0	0	0	0	0	Default(*)

*)The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

2.6.1. /XSL bit

The /XSL bit is used to select a crystal oscillator.

Set the /XSL to "0" (default) to use 32.768kHz.

Set the /XSL to "1" to use 32.000kHz.

2.6.2 F6 to F0

The Time Trimming Circuit adjust one second count based on this register readings when second digit is 00, 20, or 40 seconds. Normally, counting up to seconds is made once per 32768 of clock pulse (or 32000 when 32.000kHz crystal is used) generated by the oscillator. Setting data to this register activates the time trimming circuit.

Register counts will be incremented as ((F5, F4, F3, F2, F1, F0)-1) x 2 when F6 is set to "0".
Register counts will be decremented as ((/F5, /F4, /F3, /F2, /F1, /F0)+1) when F6 is set to "1".
Counts will not change when (F6, F5, F4, F3, F2, F1, F0) are set to (*, 0, 0, 0, 0, 0, *).

For example, when 32.768kHz crystal is used.
When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 1, 1, 1), counts will change as:32768+(7-1) x 2=32780 (clock will be delayed) when second digit is 00, 20, or 40.
When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32768 without changing when second digit is 00, 20, or 40.
When (F6, F5, F4, F3, F2, F1, F0) are set to (1, 1, 1, 1, 1, 1, 0), counts will change as:32768+(-2) x 2=32.764 (clock will be advanced) when second digit is 00, 20, or 40.

Adding 2 clock pulses every 20 seconds:2/(32.768 x 20)=3.051ppm (or 3.125ppm when 32.000kHz crystal is used), delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of ±1.5ppm.

Note : The clock adjust function only adjust clock timing.
Oscillation frequency and 32kHz clock output is not adjusted.

2.7. Alarm_A, Alarm_B Register (Alarm_A: Internal address at 8-Ah,Alarm_B: Internal address at B-Dh)

2.7.1. Alarm_A, Alarm_B Minute Register (Alarm_A: Internal address at 8h, Alarm_B: Internal address at Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
-	AM40(*1)	AM20	AM10	AM8	AM4	AM2	AM1	(for write operation)
0	AM40	AM20	AM10	AM8	AM4	AM2	AM1	(for read operation)
0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*2)

*1) AXXX in this table is the name for Alarm_A function, for Alarm_B function it is BXXX.
*2) The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

2.7.2. Alarm_A,Alarm_B hour register (Alarm_A:Internal address at 9h, Alarm_B: Internal address at Ch)

D7	D6	D5	D4	D3	D2	D1	D0	
-	-	AH20(*1) AP/A	AH10	AH8	AH4	AH2	AH1	(for write operation)
0	0	AH20 AP/A	AH10	AH8	AH4	AH2	AH1	(for read operation)
0	0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default (*2)

*1) AXXX in this table is the name for Alarm_A function, for Alarm_B function it is BXXX.
*2) The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

2.7.3. Alarm_A, Alarm_B day of the week register
(Alarm_A: internal address at Ah, Alarm_B: internal address at Dh)

D7	D6	D5	D4	D3	D2	D1	D0	
-	AW6(*1)	AW5	AW4	AW3	AW2	AW1	AW0	(for write operation)
0	AW6	AW5	AW4	AW3	AW2	AW1	AW0	(for read operation)
0	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	unde-fined	Default(*2)

*1) AXXX in this table is the name for Alarm_A function, for Alarm_B function it is BXXX.
*2) The default means read values when XSTP="1" by after initial power-on or supply voltage drop,etc.

- Alarm_A, Alarm_B hour register D5 is set to 0 for AM and 1 for PM in the 12-hour display system at AP/A. The register D5 indicates 10 digit of hour digit in 24-hour display system at AH20.
- To activate alarm operation, any imaginary alarm time setting should not be left to avoid unmatching.
- In hour digit display midnight is set to 12, noon is set to 32 in 12-hour display system. (See section 2.2.1.)
- AW0 to AW6 correspond to the day-of-the-week counter (W4, W2, W1) being set at (0, 0, 0) to (1, 1, 0).
- No alarm pulses are output when all of AW0 to AW6 are set to "0".

Example of Alarm Time settings

Alarm Time Settings	Day-of-the-week							12-hour system				24-hour system			
	Sun AW0	Mon. AW1	Tues. AW2	Wed. AW3	Th. AW4	Fri. AW5	Sat. AW6	10-hour	1-hour	10-min.	1-min.	10-hour	1-hour	10-min.	1-min.
00:00 AM every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 AM every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 AM every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 PM on Monday through Friday	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 PM on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 PM on Mon., Wed., and Fri.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Designation of days of the week and AW0 through AW6 in the above table is an example.

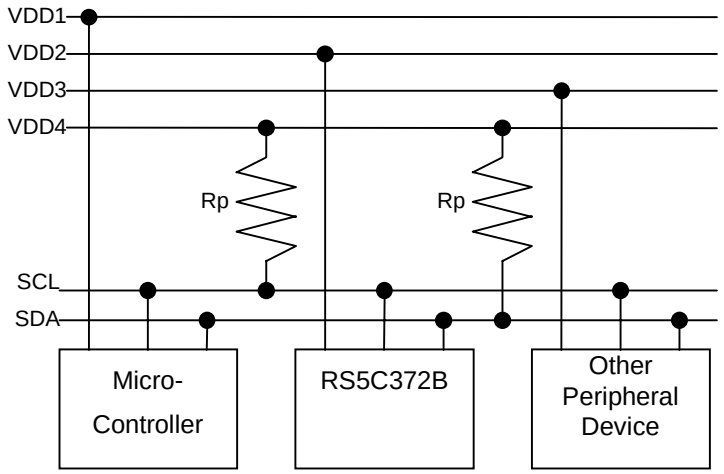
■ Functional Description

1. Interfacing with the CPU

The RS5C372B employs the I^2C-bus system to be connected to the CPU via two signal lines. Connection and transfer system of I^2C-bus are described in the following section

1.1. Connection of I^2C-bus

Two signal lines, SCL and SDA which are connected to I^2C-bus are used for transmit clock pulses and data respectively. All ICs that are connected to these lines are designed that will be not be clamped when a voltage beyond supply voltage is applied to input or output pins. Open drain pins are used for output. This construction allows communication of signals between ICs with different supply voltages by adding a pull-up resistance to each signal line as shown in the figure below. Each IC is de-signed not to affect SCL and SDA signal lines when power to each of these is turned off separately.



*) For data interface, the following conditions must be met:
VDD4≥VDD1
VDD4≥VDD2
VDD4≥VDD3

*) When the master is one, the micro controller is ready for driving SCL to "H" and Rp of SCL may not be required.

Cautions on determining RP resistance

(1) Voltage drop at RP due to sum of input current or output current at off conditions on each IC pin connected to the I^2C-bus shall be adequately small.
(2) Rising time shall be kept short even when all capacity of the bus is driven.
(3) Current consumed in I^2C-bus is small compared to the consumption current permitted for the entire system.

When all ICs connected to I^2C-bus are CMOS type, condition (1) may usually be ignored since input current and off state output current is extremely small for the many CMOS type ICs. Thus the maximum resistance of RP may be determined based on (2) while the minimum on (3) in most cases.

In actual cases a resistor may be place between the bus and input/output pins of each IC to improve noise margins in which case the RP minimum value may be determined by the resistance.

Consumption current in the bus to review (3) above may be expressed by the formula below:

Bus consumption current

$$\approx \frac{\text{(Sum of input current and off state output current of all devices in stand-by mode)} \times \text{Bus stand-by duration}}{\text{Bus stand-by duration + bus operation duration}}$$

$$+ \frac{\text{Supply voltage} \times \text{bus operation duration} \times 2}{\text{Rp resistance} \times 2 \times \text{(bus stand-by duration + bus operation duration)}}$$

+ supply voltage×bus capacity×charging/discharging times per unit time

Operation of "x 2" in the second member denominator in the above formula is derived from assumption that "L" duration of SDA and SCL pins are the half of bus operation duration. "x 2" in the numerator of the same member is because there are two pins of SDA and SCL. The third member, (charging/discharging

times per unit time) means number of transition from “H” to “L” of the signal line.

Calculation example is shown below:
Pull-up resistance (RP)=10kΩ, Bus capacity=50pF (both for SCL and SDA), VDD=3V
In as system with sum of input current and off state output current of each pin=0.1μA, I^2C-bus is used for 10ms every second while the rest of 990ms is in the stand-by mode. In this mode number of transitions of the SCL pin from “H” to “L” state is 100 while SDA 50.

$$\text{Bus consumption current} \approx \frac{0.1\mu A \times 990msec}{990msec+10msec}$$

$$+ \frac{3V \times 10msec \times 2}{10K\Omega \times 2 \times (990msec + 10msec)}$$

$$+ 3V \times 50pF \times (100 + 50)$$

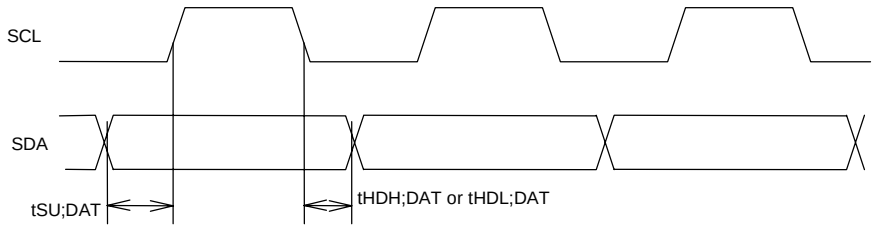
$$\approx 0.099\mu A+3.0\mu A+0.0225\mu A \approx 3.12\mu A$$

Generally, the second member of the above formula is larger enough than the first and the third members, bus consumption current may be determined by the second member.

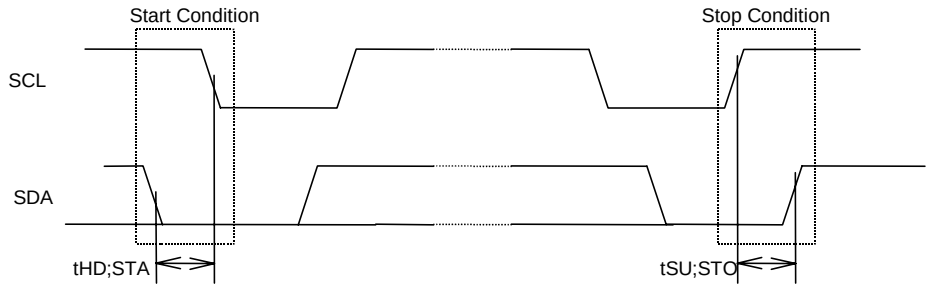
1.2. I^2C-bus transmission system

1.2.1. Start Condition and Stop Condition

In I^2C-bus, SDA must be kept at a certain state while SCL is at the “H” state as shown below during data transmission.



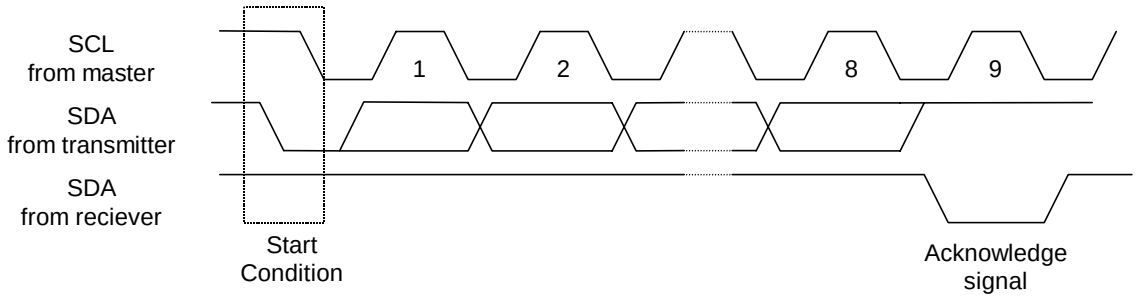
The SCL and SDA pins are at the “H” level when no data transmission is made. Changing the SDA from “H” to “L” when the SCL and the SDA are “H” activates the Start Condition and access is started. Changing the SDA from “L” to “H” when the SCL is “H” activates Stop Condition and accessing stopped. Generation of Start and Stop Conditions are always made by the master (see the figure below).



1.2.2. Data transmission and its acknowledge

After start condition is entered, data is transmitted by 1 byte (8 bits). Any bytes of data may be serially transmitted. The receiver will send an acknowledge signal to the transmission side each time 8bit data is transmitted. The acknowledge signal is sent immediately after falling to “L” of SCL8bit clock pulses of data transmission, by releasing the SDA by the transmitter that has asserted the bus at that time and by turning the SDA to “L” by the receiver. When transmission of 1 byte data next to preceding 1 byte of data is received the receiver releases the SDA pin at falling edge of the SCL 9 bit of clock pulses or when the receiver switches to the transmitter it starts data

transmission. When the master is the receiver, it generates no acknowledge signal after the last 1 byte of data from the slave to tell the transmitter that data transmission has completed when the slave side (transmitter) continues to release the SDA pin so that the master will be able to generate Stop Condition.

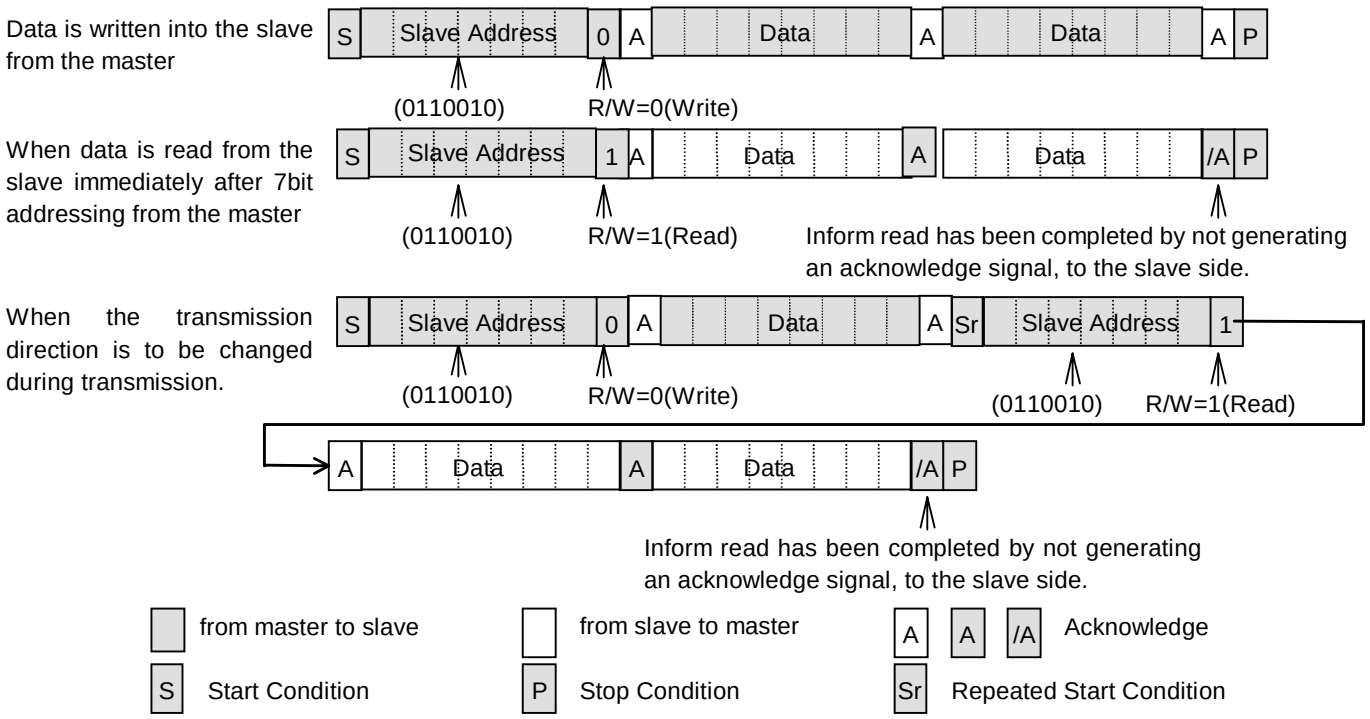


1.2.3. Data transmission format in I^2C-bus

I^2C-bus generates no CE signals. In place of it each device has a 7bit slave address allocated. The first 1byte is allocated to this 7bit of slave address and to the command (R/W) for which data transmission direction is designated by the data transmission thereafter. 7bit address is sequentially transmitted from the MSB and 2 and after bytes are read, when 8bit is “H” and write when “L”.

The slave address of the RS5C372B is specified at (0110010).

At the end of data transmission/receiving stop condition is generated to complete transmission. However, if start condition is generated without generating Stop Condition, Repeated Start Condition is met and transmission/receiving data may be continued by setting the slave address again. Use this procedures when the transmission direction needs to be changed during one transmission.

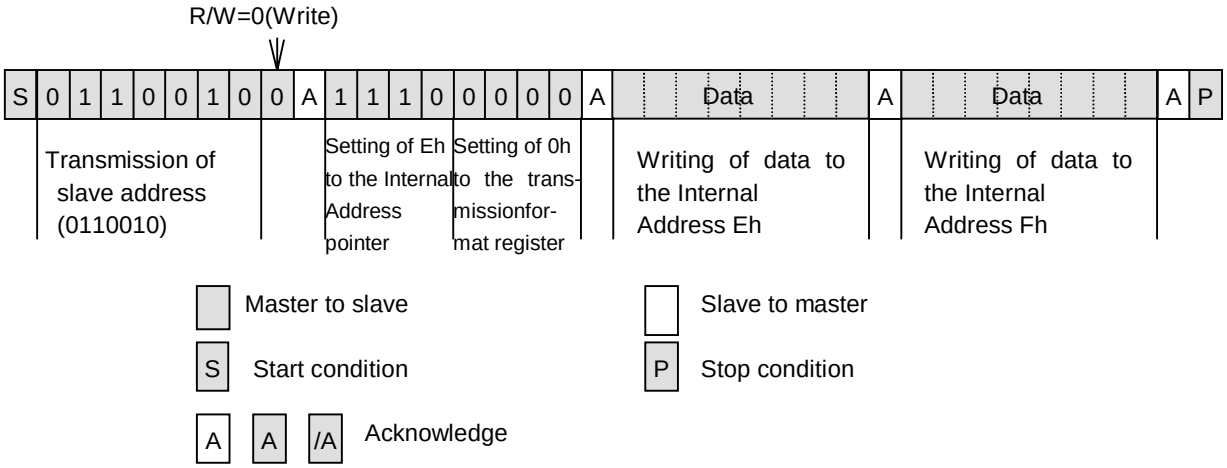


1.2.4. Data transmission write format in the RS5C372B

Although the I^2C-bus standard defines a transmission format for the slave address allocated for each IC, transmission method of address information in IC is not defined. The RS5C372B transmits data the internal address pointer (4bit) and the transmission format register (4bit) at the 1byte next to one which transmitted a slave address and a write command. For write operation only one transmission format is available and (0000) is set to the transmission format register. The 3byte transmits data to the address

specified by the internal address pointer written to the 2 byte. Internal address pointer settings are automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h on transmitting the next byte.

Example of data writing (When writing to internal address Eh-Fh)

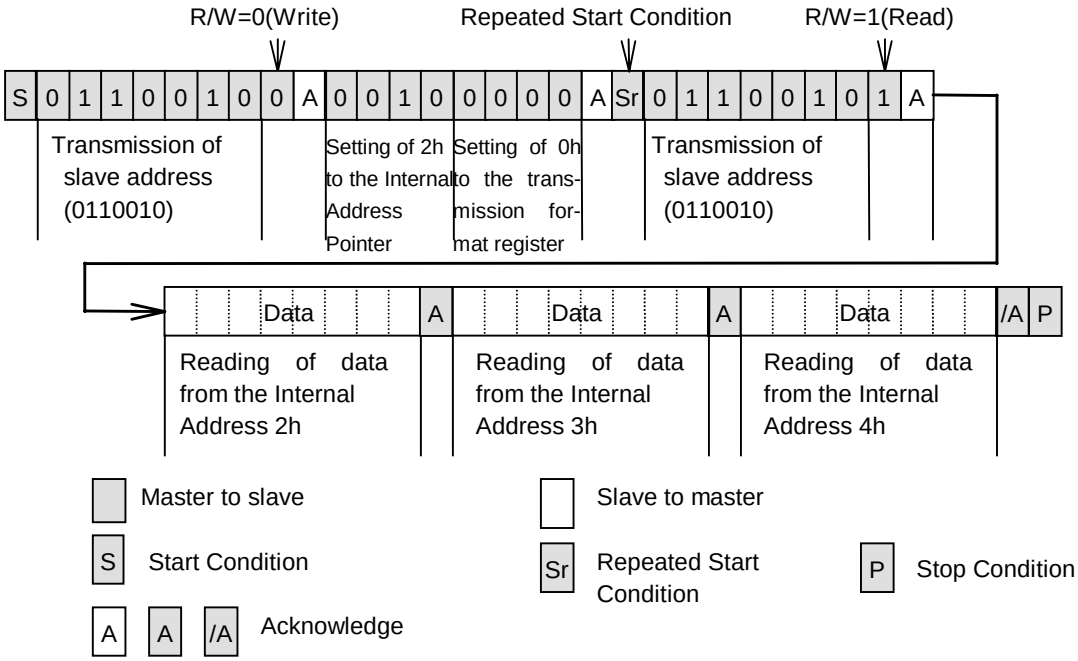


1.2.5. Data transmission read format of the RS5C372B

The RS5C372B allows the following three readout methods of data from internal registers.

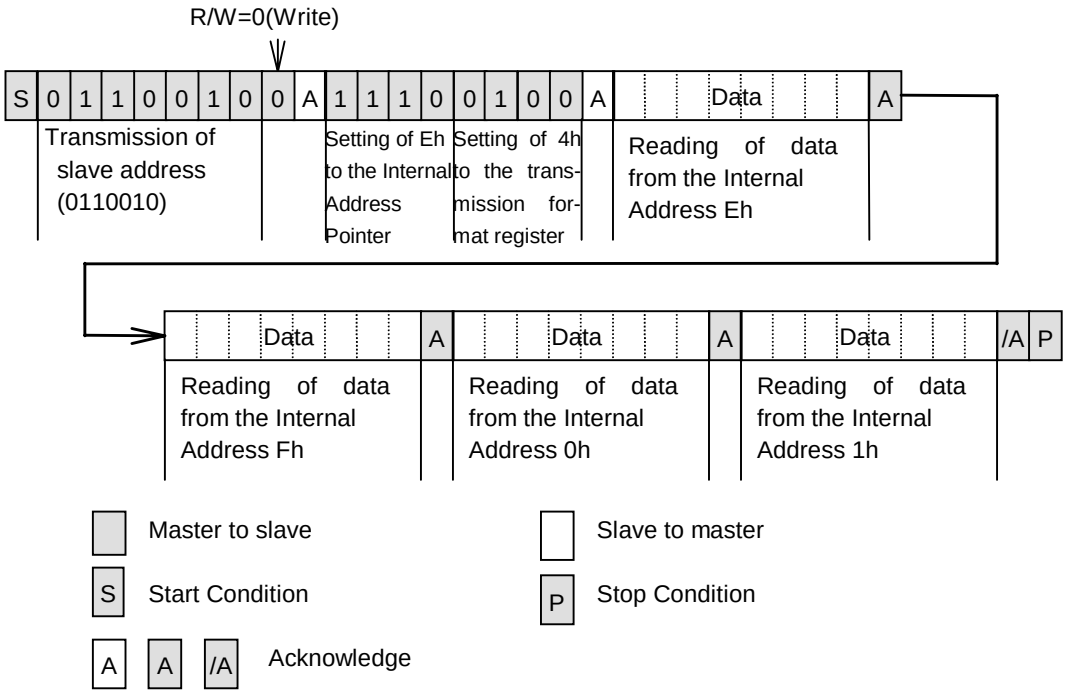
1) The first method to reading data from the internal register is to specify an internal address by setting the internal address pointer and the transmission format register described 1.2.4., generate the repeated start condition (see section 1.2.3.) to change the data transmission direction to perform reading.
The internal address pointer is set to Fh when the stop condition is met. Therefore, this method of reading allows no insertion of the stop condition before the resend start condition. Set 0h to the transmission format register when this method is used.

Example1 of data read (when data is read from 2h-4h)



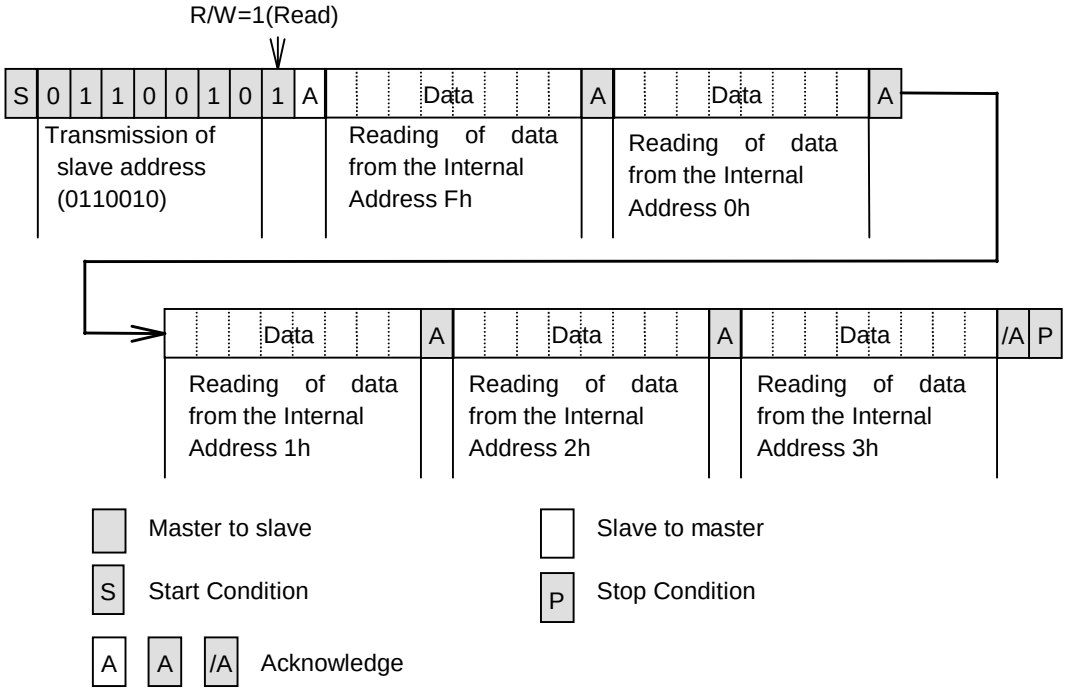
2) The second method to reading data from the internal register is to start reading immediately after writing to the Internal Address pointer and the transmission format register. Although this method is not based on the I^2C-bus standard in a strict sense it still effective to shorten read time to ease load to the master. Set 4h to the transmission format register when this method is used.

Example2 of data read (when data is read from Eh-1h)



3) The third method to reading data from the internal register is to start reading immediately after writing to the slave address and the R/W bit. Since the internal address pointer is set to Fh by default as described in 1), This method is only effective when reading is started from the internal address Fh.

Example3 of data read (when data is read from Fh-3h)



1.2.8. Data transmission under special condition

The RS5C372B holds the clock tentatively for duration from Start Condition to Stop Condition to avoid invalid read or write clock on carrying clock. When clock is carried during this period, which will be adjusted within approx. 61µs from Stop Condition. To prevent invalid read or write clock shall be made during one transmission operation (from Start Condition to Stop Condition). When 0.5 to 1.0 second elapses after start condition any access to the RS5C372B is automatically released to release tentative hold of the clock, set Fh to the address pointer, and access from the CPU is forced to be terminated (the same action as made stop condition is received: Automatic Resume Function from the I^2C-Bus interface). Therefore, one access must be completed within 0.5 seconds. The Automatic Resume Function prevents delay in clock even if the SCL is stopped from sudden failure of the system during clock read operation.
Also a second Start Condition after the first Start Condition and before the Stop Condition is regarded as the "Repeated Start Condition." Therefore, when 0.5 to 1.0 seconds passed after the first Start Condition, access to the RS5C372B is automatically released.
If access is tried after Automatic Resume Function is activated, no Acknowledge signal will be output for writing while FFh will be output for reading.

Access to the real-time clock

1) No stop condition shall be generated until clock read/write is started and completed.
2) One clock read/write operation shall be completed within 0.5 seconds.

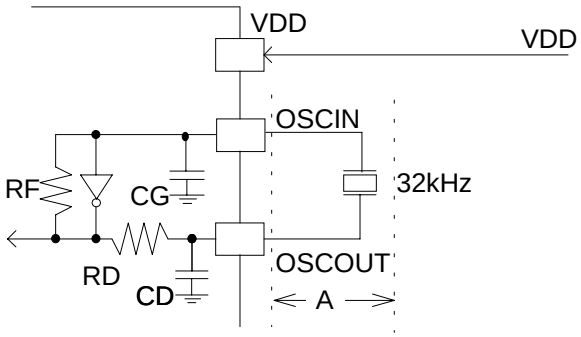
The user shall always be able to access the real-time clock as long as these two conditions are met.

Bad example of reading from seconds to hours (invalid read)
(Start condition) → (Read of seconds) → (Read of minutes) → (Stop condition) → (Start condition) → (Read of hour) → (Stop condition)

Assuming read was started at 05:59:59 P.M. and while reading seconds and minutes the time advanced to 06:00:00 P.M. At this time second digit is hold so the read as 05:59:59. Then the RS5C372B confirms (Stop condition) and carries second digit being hold and the time changes to 06:00:00 P.M. Then, when the hour digit is read, it changes to 6. The wrong results of 06:59:59 will be read.

2. Configuration of Oscillating Circuit and Time Trimming

2.1. Configuration of Oscillating Circuit



Typical external devices

X'tal : 32.768kHz or 32.000KHz

(R1=30kΩ typ)

(CL=6pF to 8pF)

Typical value of internal devices

RF 15MΩ typ

RD 60kΩ typ

CG,CD 10pF typ

The oscillation circuit is driven at a constant voltage of about 1.2V relative to the Vss level. Consequently, it generates a wave form having a peak-to-peak amplitude of about 1.2V on the positive side of the Vss level.

Considerations on crystal oscillator

Basic characteristics of a crystal oscillator includes R1 (equivalent series resistance: ease of oscillation) and CL (load capacitance: rank of center frequency). R1=typ. of 30kΩ, CL=6 to 8pF is recommended for the RS5C372B. Confirm recommended values to the manufacturer of the crystal oscillator used.

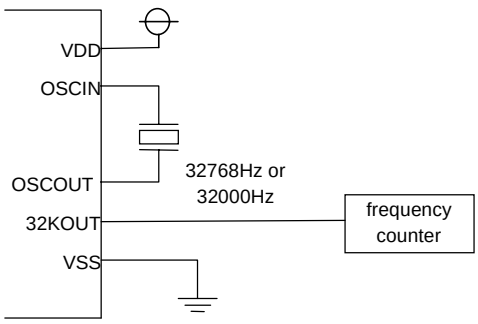
Considerations in Mounting Components Surrounding Oscillating Circuit

1) Mount the crystal oscillators in the closest possible position to the IC.
2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with ←A→ in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB.
4) Avoid using any long parallel line to wire the OSCIN or OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) When applying an external input of clock pulses (32.768kHz or 32.000kHz) to the OSCIN pin:
   DC coupling: Prohibited due to mismatching of input levels.
   AC coupling: Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc.
2) Avoid using the oscillator output of the RS5C372B (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation.

2.2. Measurement of oscillation frequency

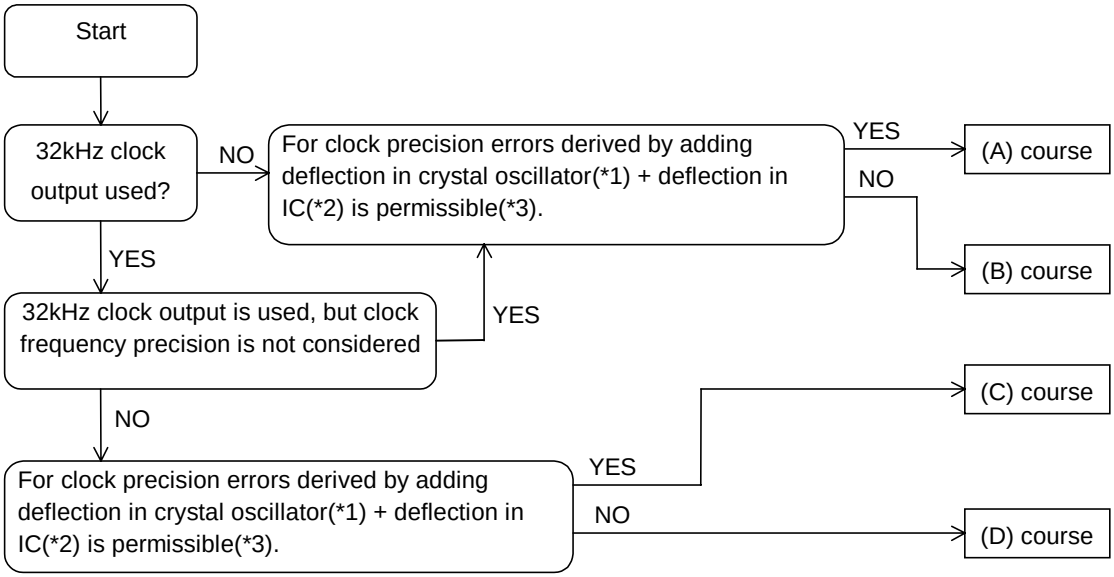


*1) Clock pulse of 32.768kHz or 32.000kHz is output from the 32KOUT output pin on powering on (XSTP is set to 1).

*2) Use a frequency counter having at least 6 digits (7 digits or more recommended).

2.3. Oscillation Frequency Adjustment

Adjustment method of oscillation frequency may differ dependent on how the RS5C372B is used or how much clock error is permissible in the system it is installed. Use the flow chart shown below find an optimal oscillation frequency adjustment method.



*1) In general crystal oscillators are classified by their central frequency of CL (load capacitance) and available further grouped in several ranks as ±10, ±20 and ±50ppm of fluctuations in precision.
*2) Fluctuations in frequency due to the IC used is generally from ±5 to 10ppm at a room temperature.
*3) Clock precision here is at a room temperature and is subjected to change due to temperature characteristics of the crystal itself.

(A) course

Adjustment of clock is not made for IC (no adjustment) and any CL value may be used for the crystal oscillator. Precision fluctuations of a crystal oscillator may be selected as long as clock precision allows. Obtain the central frequency as described in section 2.2 using several crystal oscillator and ICs, determine an adjustment value as described in “2.4. Time Trimming Circuit” which shall be set to the RS5C372B.

(B) course

To keep clock precision within the range of (fluctuation in crystal oscillator + fluctuation in IC), clock shall be adjustment is required for each IC. On adjusting procedures see “2.4 Time Trimming Circuit.” Available selection range for the frequency precision fluctuations and CL (load capacitance) for a crystal oscillator may be widened by adjusting clock frequency. Obtain the central frequency as described in section 2.2. using the crystal oscillator and IC to be used, determine if an adjustment is possible or not using the clock adjustment circuit, perform adjustment for each IC using the clock adjustment circuit. Up to ±1.5ppm may be adjusted at a room temperature.

(C) course

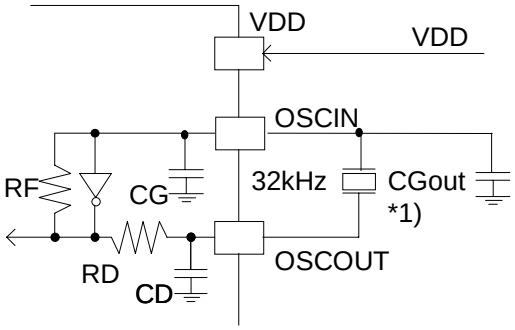
In (C) and (D) courses, adjustment of 32kHz clock output frequency as well as clock is necessary. Frequency adjustment for the crystal oscillator is made by adjusting both of CG and OD connected to the both ends of the oscillator. Since the RS5C372B incorporates the CG and CD, oscillating frequency is required using CL of the crystal oscillator as the reference.

Generally, relation between CL and CG or CD is as follows:

$$CL = \frac{CG \times CD}{CG + CD} + CS \qquad \text{CS: Board floating capacitance}$$

Although a crystal oscillator having CL value of around 6 to 8pF is recommended for the RS5C372B, measure oscillation frequency as described in section 2.2 and if frequency is high (clock gains) switch to a crystal oscillator with smaller CL while if frequency is small (clock loses) switch to an oscillator with larger CL. Using

these procedures select a crystal oscillator with optimal CL and set unadjusted value to the time trimming register. (See section 2.4, "Time Trimming Circuit".) We recommend to consult the crystal manufacturer on compatibility of CL values.
High oscillation frequency (clock gains) may be adjusted by externally adding CGout as shown below.



*1) CGout = 0 to 15pF

(D) course
Select a crystal oscillator as in the (C) course, then adjust clock error for each IC as in (B) course. For clock adjusting procedures, see "2.4. Time Trimming Circuit."

2.4. Time Trimming Circuit
Using the Time Trimming Circuit gain or lose of clock may be adjusted with high precision by changing clock pulses for one second every 20 seconds. When adjustment with this circuit is not necessary, set (F6, F5, F4, F3, F2, F1, F0) to (*, 0, 0, 0, 0, 0, *) to disable adjustment. (* mark indicates 0 or 1.)
Adjustment amount may be calculated using the following formula.

2.4.1. When oscillation frequency (*1)>target frequency(*2) (clock gains)

$$\text{Adjustment amount(*3)} = \frac{\text{(Oscillation frequency-Target frequency(*2) + 0.1)}}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\approx \text{(Oscillation frequency-Target frequency)} \times 10 + 1$$

When 32.000kHz crystal oscillator is used, the same formula is used.

$$\text{Adjustment amount} = \frac{\text{(Oscillation frequency-Target frequency + 0.1)}}{\text{Oscillation frequency} \times 3.125 \times 10^{-6}}$$

$$\approx \text{(Oscillation frequency-Target frequency)} \times 10 + 1$$

*1) Oscillation frequency: Clock frequency output from the 32KOUT as in "2.2 Oscillation Frequency Measurement" at a room temperature.
*2) Target frequency: A frequency to be adjusted to. Since temperature characteristics of a 32.768kHz crystal oscillator are such that it will generally generates the highest frequency at a room temperature, we recommend to set the target frequency to approx. 32768.00Hz to 32768.10Hz (+3.05ppm to 32768Hz).
We also recommend setting of approx. 32000.00Hz to 32000.10Hz (3.125ppm to 32000Hz) also for the 32000kHz crystal. Note that this value may differ based on the environment or place where the device will be used.
*3) Adjustment amount: A value to be set finally to F6 to F0 bits. This value is expressed in 7bit binary digits with sign bit (two's compliment).

2.4.2. When oscillation frequency = target frequency (no clock gain or loss)

Set the adjustment value to 0 or +1, or –64 or –63 to disable adjustment.

2.4.3. When oscillation frequency<target frequency (clock loses)

$$\text{Adjustment amount} = \frac{\text{(Oscillation frequency-Target frequency)}}{\text{Oscillation frequency}\times 3.051\times 10^{-6}}$$

$$\approx \text{(Oscillation frequency-Target frequency)} \times 10$$

Also a 32.000kHz crystal is used, the same formula is used.

$$\text{Adjustment amount} = \frac{\text{(Oscillation frequency-Target frequency)}}{\text{Oscillation frequency}\times 3.125\times 10^{-6}}$$

$$\approx \text{(Oscillation frequency-Target frequency)} \times 10$$

Example of calculations

(1) When Oscillation frequency = 32768.85Hz; Target frequency = 32768.05Hz

Adjustment amount = $(32768.85-32768.05 + 0.1)/(32768.85\times 3.051\times 10^{-6})$

$\approx (32768.85 + 32768.05) \times 10 + 1 = 9.001 \approx 9$

Set (F6,F5,F4,F3,F2,F1,F0) to (0,0,0,1,0,0,1)

As this example shows, adjustments to be used when the clock gains shall be distance from 01h.

(2) When Oscillation frequency = 32763.95Hz; Target frequency = 32768.05Hz

Adjustment amount = $(32763.95-32768.05)/(32763.95\times 3.051\times 10^{-6})$

$\approx (32763.95-32768.05) \times 10 = -41.015 \approx -41$

To express –41 in 7bit binary digits with sign bit (two's compliment),

Subtract 41(29h) from 128(80h) in the above case, 80h–29h=57h.

Thus, set (F6, F5, F4, F3, F2, F1, F0) to (1, 0, 1, 0, 1, 1, 1).

As this example shows, Adjustment amount to be used when the clock loses shall be distance from 80h.

After adjustment, adjustment error against the target frequency will be approx. ±1.5ppm at a room temperature.

Notes

1) Clock frequency output from the 32KOUT pin will not change after adjustment by the time trimming circuit.
2) Adjustable range: The range of adjustment values for a case oscillation frequency is higher than target frequency (clock gains) is (F6, F5, F4, F3, F2, F1, F0)=(0, 0, 0, 0, 0, 1, 0) to (0, 1, 1, 1, 1, 1, 1) and the amount actually adjustable shall be -3.05ppm to -189.2ppm (-3.125ppm to -193.8ppm for 32.000kHz crystal), thus adjustment is possible until –189.2ppm of delay is generated (+193.8ppm for 32.000kHz crystal). While, the range of adjustment values for a lower case is (F6, F5, F4, F3, F2, F1, F0)=(1, 1, 1, 1, 1, 1, 1) to (1, 0, 0, 0, 0, 1, 0) and the amount actually adjustable shall be +3.05ppm to +189.2ppm (+3.125ppm to +193.8ppm for 32.000kHz crystal), thus adjustment is possible until +189.2ppm of delay is generated (-193.8ppm for 32.000kHz crystal).

3. Oscillation Halt Sensing

Oscillation halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to 0 by writing data to the control register 2. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity. When the XSTP bit is 1, /XSL, F6 to F0, CT2, CT1, CT0, AALE, BALE, /CLEN and TEST bit are reset to 0.

1) The XSTP bit is set to 1 upon power-on from 0V.Note that any instantaneous power disconnection may cause operation failure.
2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

Considerations in Use of XSTP Bit

Ensure error-free oscillation halt sensing by preventing the following events:

1) Instantaneous disconnection of VDD
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC.

4. /INTR output pins

The following two output wave forms can be output from the /INTR pin.

1) Alarm Interrupt

When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with the output pin being on (“L”). Alarm interrupt consists of Alarm_A and Alarm_B, both have equivalent functions.

2) Periodic Interrupt

Outputs an output wave form selected by setting the periodic interrupt frequency select bit. Wave forms include pulse mode and level mode.

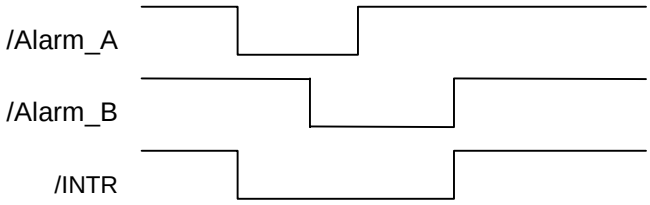
4.1. Control of the /INTR output (flag bit, enable bit)

Of the two output wave forms listed above, interrupt output conditions may be set by setting the flag bit that monitors output state on the register, the enable bit that enables an output wave form.

	Flag bit	Enable bit
Alarm_A	AAFG (D1 at internal address Fh)	AALE (D7 at internal address Eh)
Alarm_B	BAFG (D0 at internal address Fh)	BALE (D6 at internal address Eh)
Periodic Interrupt	CTFG (D2 at internal address Fh)	Disabled at CT2=CT1=CT0=0 (D2-0 at internal address Eh)

- When power ON (XSTP=1) since AALE=BALE=CT2=CT1=CT0=0, /INTR=OFF (H).
- When more than one output wave forms are output from a single output pin, the output will have or wave form of negative logic of both.

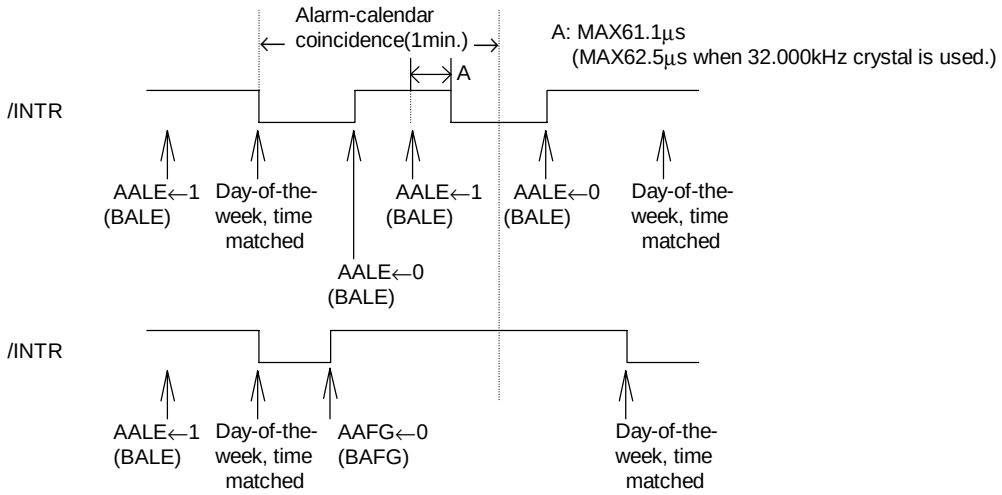
Example:When Alarm_A and Alarm_B are output from the /INTR pin.



In such a case which output wave form is output from the pin may be confirmed by reading the flag bits.

4.2. Alarm Interrupt

For setting an alarm time, designated time such as day-of-the-week, hour or minute should be set to the alarm registers being AALE (BALE) bit to 0. After that set the AALE (BALE) bit to 1, from this moment onward when such registered alarm time coincide the value of calendar counter the /INTR comes down to “L” (ON). The /INTR output can be controlled by operating to the AALE (BALE) and AAFG (BAFG) bits.



*) Note that AAFG (BAFG) has an output wave form of reversed logic.

4.3. Periodic Interrupt

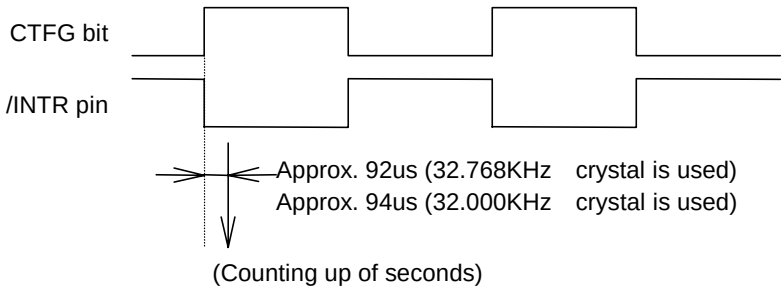
The /INTR pin outputs, the Periodic interrupt frequency select register, and the Interrupt output select bit can be used to interrupt the CPU in a certain cycle. The Periodic interrupt frequency select register can be used to select either one of two interrupt output modes: the pulse mode and the level mode.

Periodic interrupt frequency select register (D2-0 at internal address Eh)

CT2	CT1	CT0	Description		
			Wave form mode	Frequency and falling timing	
0	0	0	-	OFF(H)	(Default)
0	0	1	-	Fixed at “L”	
0	1	0	Pulse mode	2Hz(Duty50%)	
0	1	1	Pulse mode	1Hz(Duty50%)	
1	0	0	Level mode	Every second (synchronized with second count up)	
1	0	1	Level mode	Every minute (00 second of every minute)	
1	1	0	Level mode	Every hour (00 minute(s) 00 second(s) of every hour)	
1	1	1	Level mode	Every month (the 1st day 00 AM 00 minute(s) 00 second(s) of every month)	

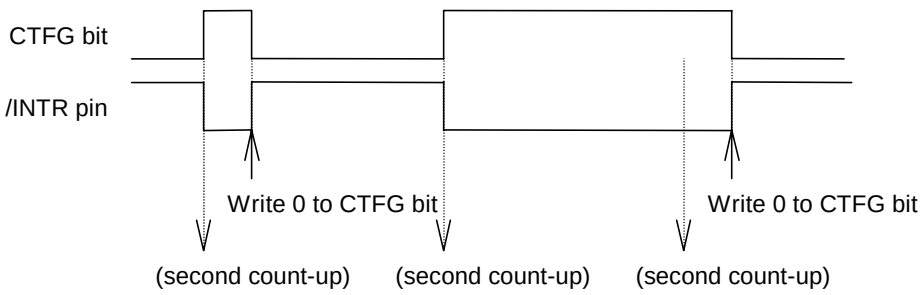
1) Pulse mode: Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds, see the diagram on the next page.
   *) When 32000Hz crystal is used
   In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternately.
   Duty cycle for 1Hz clock pulses becomes 50.4%
   (“L” duration is 0.496s while “H” duration is 0.504s)
1) Level mode: One second, one minute or one month may be selected for an interrupt frequency. Counting up of seconds is matched with falling edge of interrupt output.
2) When the clock error correction circuit is used, periodic interrupt frequency changes every 20 seconds.
   Pulse mode: “L” duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.) For example, Duty will be 50±0.3784% (or 50±0.3875% when 32.000kHz crystal is used) at 1Hz.
   Level mode: Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)

Pulse mode



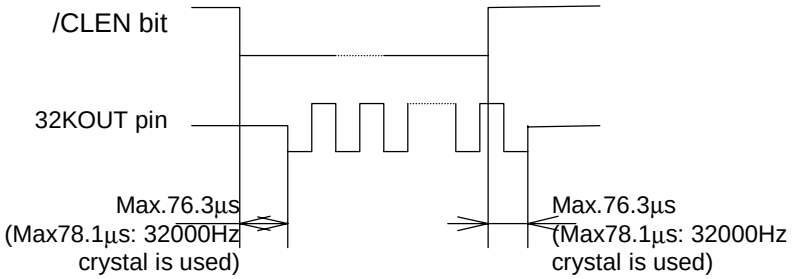
*) Since counting up of seconds and the falling edge has a time lag of approx. 92µs (at 32.768kHz) (approx. 94µs when 32.000kHz crystal is used), time with apparently approx. one second of delay from time of the real-time clock may be read when time is read in synchronization with the falling edge of output.

Level mode



5. 32kHz Clock Output
   The crystal oscillator can generate clock pulses of 32kHz from the 32KOUT pin. The pin is changed to High impedance by setting the /CLEN bit to 1.

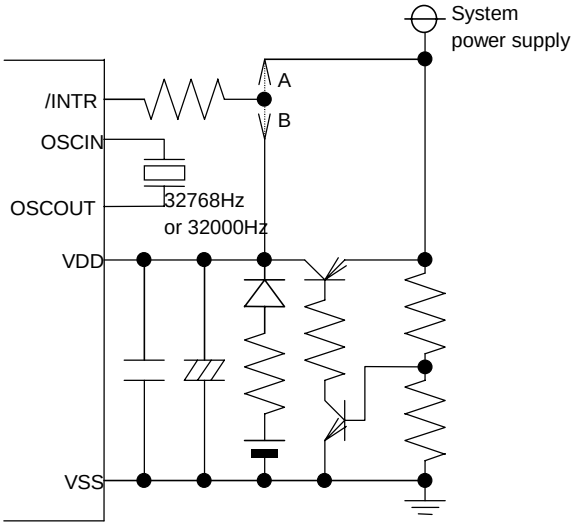
*) 32kHz clock output will not be affected from settings in the clock adjustment register.
*) When power ON (XSTP=1) 32kHz clock pulses are output from the 32KOUT pin.



6. Typical Applications

6.1. Examples of power supply circuits

Example 1

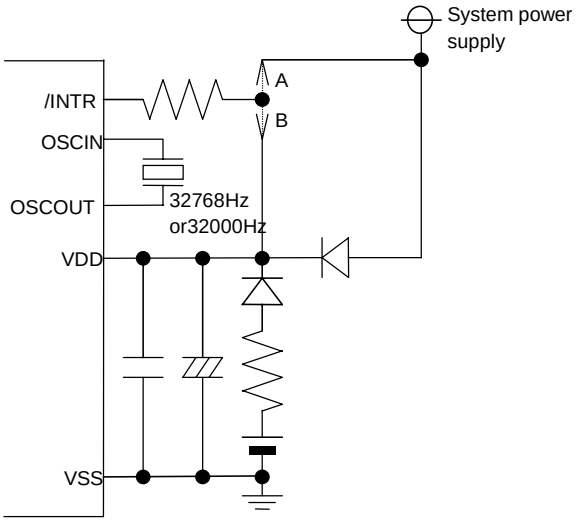


1) Install the bypass capacitors closest to the IC , and capacitors for high frequency and low frequency will be parallel.

2) Carefully select a position to connect /INTR pin pull-up resistor, that is appropriate for specific use for battery backup as follows.

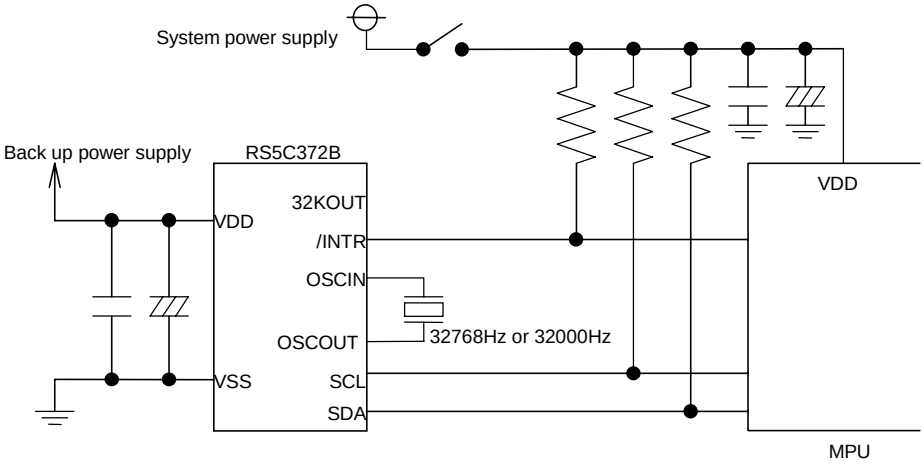
- Not used for battery backup: Connect as A in the left figure.
- Also used for battery backup: Connect as B in the left figure.

Example 2



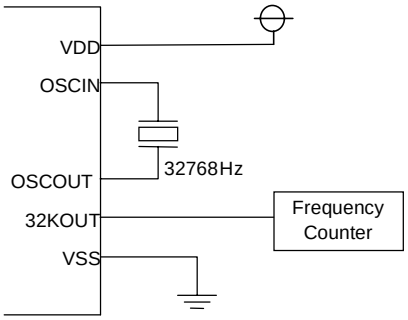
*) Connection in the example shown left may not affect the RS5C372B since it is designed to be operational even when the pin voltage exceeds VDD, except 32KOUT pin.

6.2. Example of interface circuit to the CPU



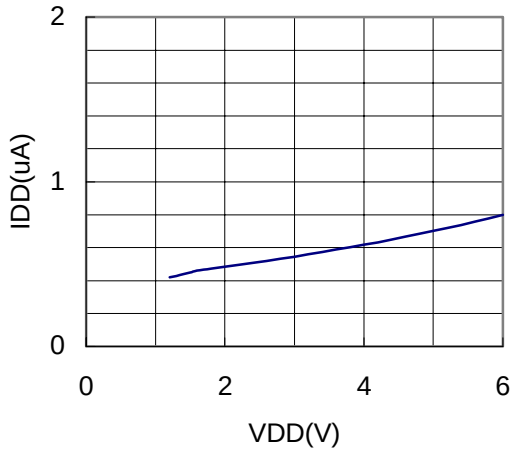
*) The SCL and SDA pins of the RS5C372B contains protective no diode on VDD side.
Therefore, back up power supply<system power supply causes no adverse effect.

3. Typical Characteristics Measurement

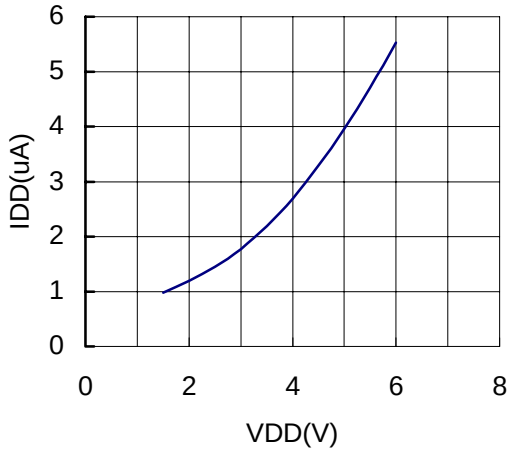


X'tal : 32.768kHz
(R1=30kΩ typ)
(CL=6pF to 8pF)
Topt : 25°C
Output pins : Open

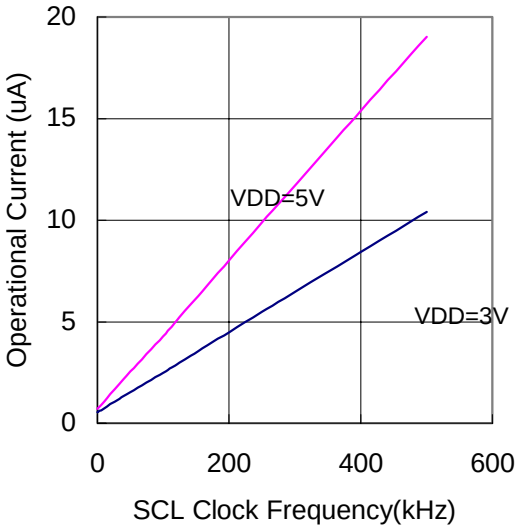
3.1. Standby Current vs. VDD
(Topt=25°C,32KOUT= OFF)



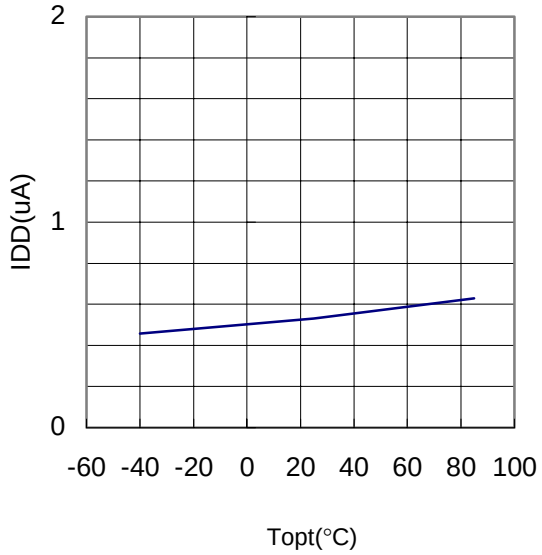
3.2. Standby Current (32KOUT= ON) vs. VDD
(Topt=25°C,32KOUT = OPEN)



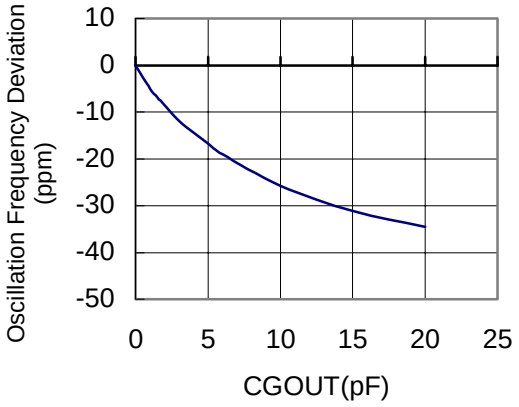
3.3. Operational Current vs. SCL Clock Frequency
(Topt=25°C,SDA = OPEN)



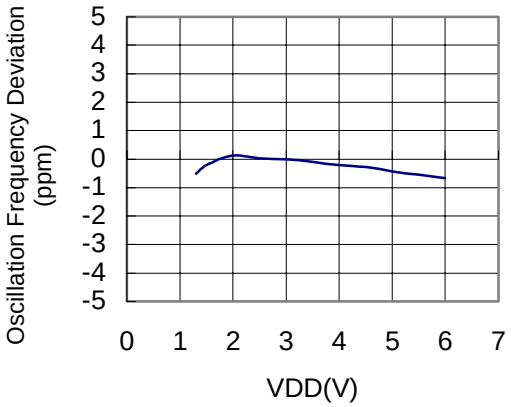
3.4. Stand-by Current vs. Temperature
(VDD=3.0V,SDA=OPEN)



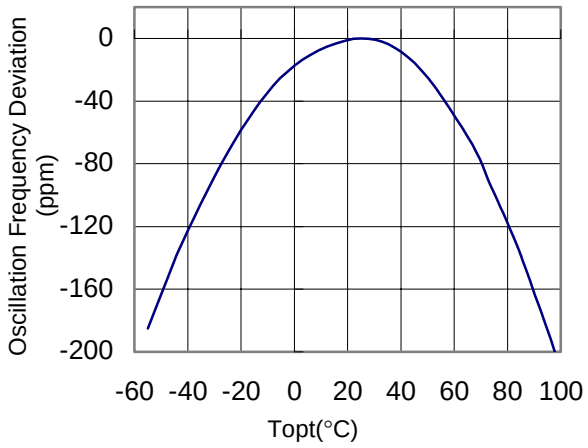
3.5. Oscillation Frequency Deviation vs. CGOUT
(Topt=25°C,VDD=3V,CGOUT=0pF reference)



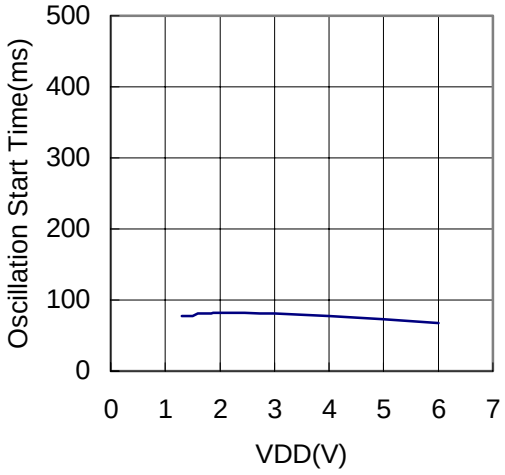
3.6. Oscillation Frequency Deviation vs. VDD
(Topt=25°C,VDD=3V reference)



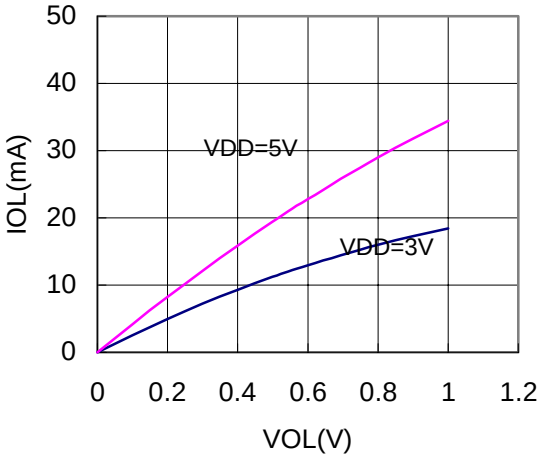
3.7. Oscillation Frequency Deviation vs. Temperature
(VDD=3V,Topt=25°C reference)



3.8. Oscillation Start Time vs. VDD
(Topt=25°C)

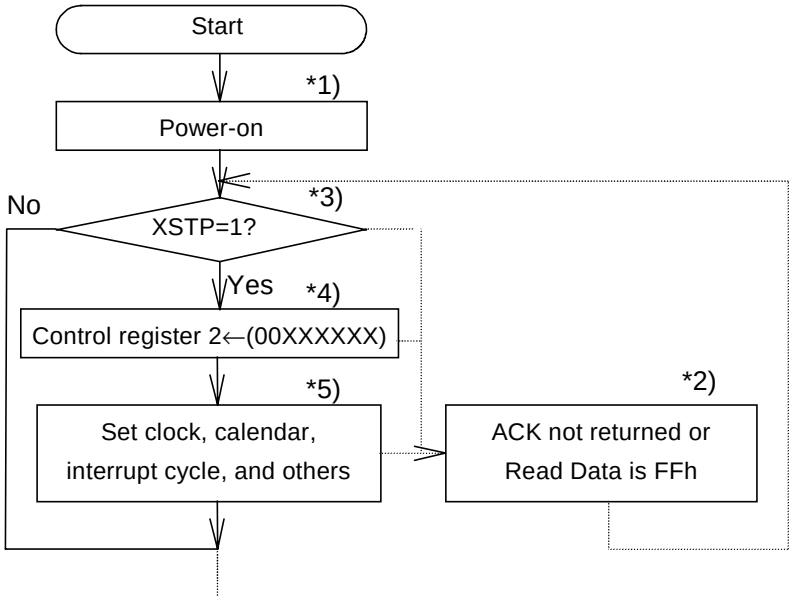


3.9. VOL vs. IOL (/INTR pin)
(Topt=25°C)



4. Typical Software-based Operation

4.1. Initialization upon Power-on



*1) Start access after waiting one to two seconds that are required for starting up of oscillation and internal initialization after power on from 0V.

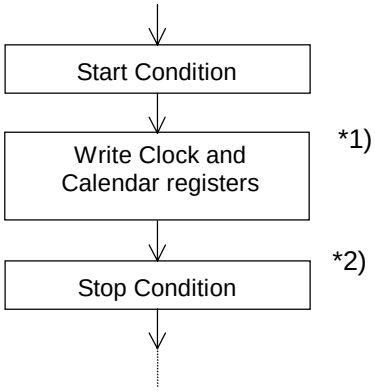
*2) If access is tried during IC internal initialization period described in *1), acknowledge signal may not be output, it is output only at first, or values read may FFh. If any of these occurs, repeat accessing. This will be required also for ordinary routines when accessing may require 0.5 seconds or more.

*3) When XSTP=0 in oscillation halt sensing, it indicates power has not been booted from 0V but from back up supply.

*4) The XSTP shall be set to 0 by setting any data to the control register 2.

*5) Perform ordinary initial setting including clock calendar or interrupt cycle.

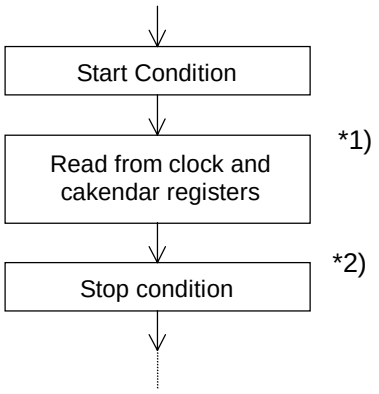
4.2. Write Operation to Clock and Calendar Counters



*1) When writing to clock and calendar registers, do not insert stop condition until all times from second to year have been written to prevent error in writing time.

*2) Take care so that process from start condition to stop condition will be completed within 0.5 seconds. (The RS5C372B forces access to the CPU to terminate within 0.5 to 1.0 seconds after start condition has occurred in case the CPU is failed during access.)

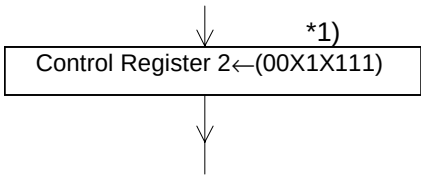
4.3. Read Operation to Clock and Calendar Registers



*1) When reading from clock and calendar registers, do not insert stop condition until all times from second to year have been read to prevent error in writing time.

*2) Take care so that process from start condition to stop condition will be completed within 0.5 seconds. (The RS5C372B forces access to the CPU to terminate within 0.5 to 1.0 seconds after start condition has occurred in case the CPU is failed during access.)

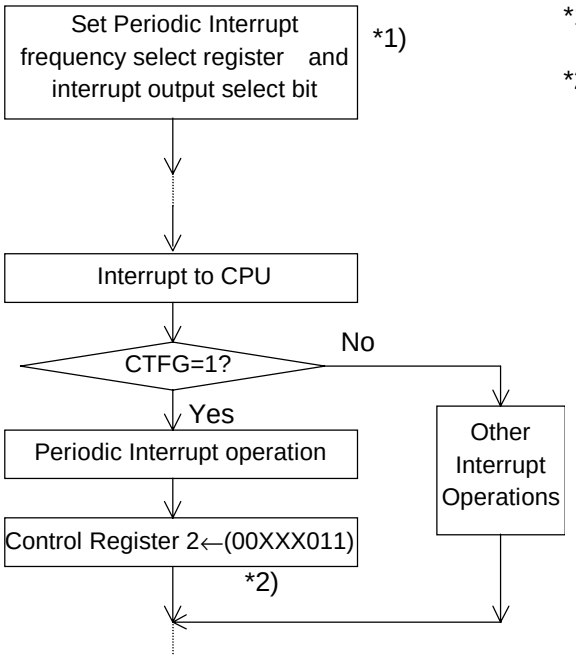
4.4. Second digit Adjustment by ±30 seconds



*1) Write 1 to the ADJ bit. (The ±30 seconds of adjustment is made within 122.1 µs (125 µs when 32.000kHz crystal is used) after the ADJ bit is set to 1.

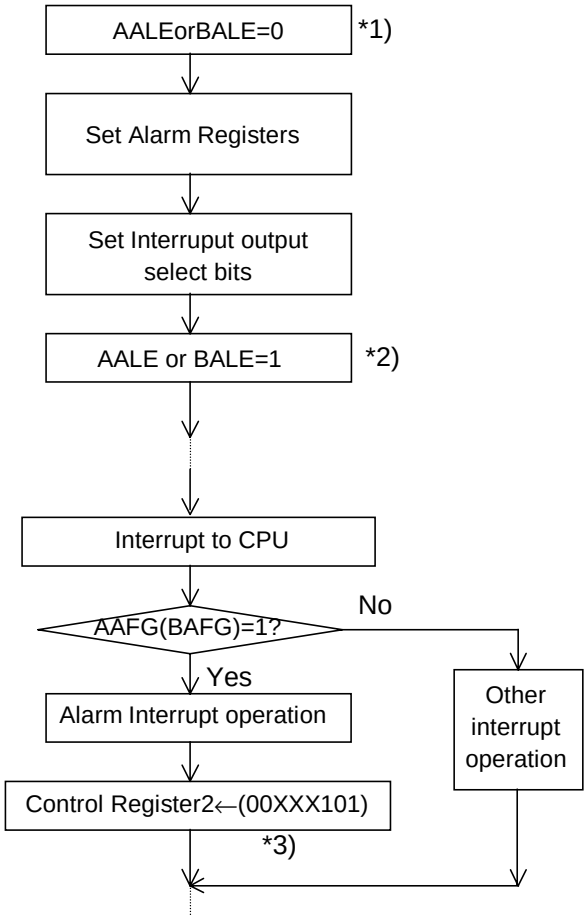
4.5. Interrupt Operation

4.5.1. Periodic Interrupt



*1) The level mode is used for the periodic interrupt frequency select bit.
*2) Interrupt to the CPU may be released by setting the CTFG bit to 0.

4.5.2. Alarm Interrupt Operation



*1) Before setting alarm time, disable alarm function tentatively by setting AALE or BALE to 0 in case the set time agrees with the current time.

*2) After all alarm settings have been completed, enable alarm function.

*3) Tentatively unlock alarm.
Write (00xxx101) when Alarm_A is used.
Write (00xxx110) when Alarm_B is used.

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