NOIP1SN5000A, NOIP1SN2000A

PYTHON 5.0/2.0 MegaPixels Global Shutter CMOS Image Sensors

ON Semiconductor®

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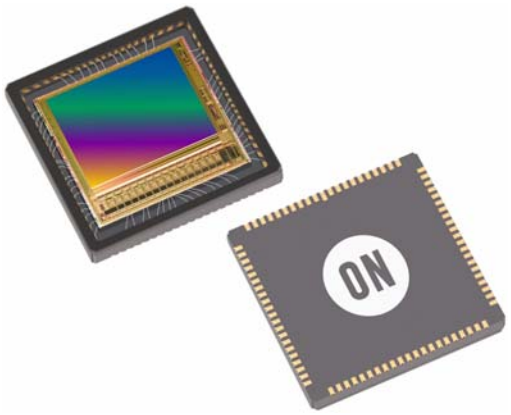


Figure 1. PYTHON 5000

Features

- 5 MegaPixels: 2592 x 2048 Active Pixels
  2 MegaPixels: 1920 x 1200 Active Pixels
- 4.8 μm x 4.8 μm Low Noise Global Shutter Pixels with In-pixel CDS
- Monochrome (SN), Color (SE) and NIR (FN)
- Zero ROT Mode Enabling Higher Frame Rate
- Frame Rate at Full Resolution/HD (LVDS)
  - 100/85 frames per second @ 5 MP (Zero ROT/Non−Zero ROT)
  - 230/180 frames per second @ 2 MP (Zero ROT/Non−Zero ROT)
  - 250/200 frames per second @ Full HD (Zero ROT/Non−Zero ROT)
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 8-bit or 10-bit Output Mode
- Eight Low Voltage Differential Signaling (LVDS) High Speed Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter
- LVDS Channel Multiplexing
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR)
- Dual Power Supply (3.3 V and 1.8 V)
- −40°C to +85°C Operational Temperature Range
- 84-pin LCC
- 1.5 W Power Dissipation
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Machine Vision
- Motion Monitoring
- Security
- Intelligent Traffic Systems (ITS)

Description

The PYTHON's high sensitivity 4.8 μm x 4.8 μm pixels support low noise "pipelined" and "triggered" global shutter readout modes. In global shutter mode, the sensor supports correlated double sampling (CDS) readout, reducing noise and increasing dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on-chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to sixteen regions can be programmed, achieving even higher frame rates.

The image data interface part consists of eight LVDS lanes, facilitating frame rates up to 100 frames per second in Zero ROT mode. Each channel runs at 720 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receiving end.

The PYTHON medium resolution family is packaged in a 84-pin LCC package and is available in a monochrome and color version. For more information, please contact your local distributor or email us at imagesensors@onsemi.com.

ORDERING INFORMATION

Part Number	Family	Description	Package	Product Status
NOIP1SN5000A−QDI	PYTHON 5000	5 MegaPixel, LVDS mono micro lens	84−pin LCC	Production: Q1, 2015
NOIP1SE5000A−QDI		5 MegaPixel, LVDS color micro lens		
NOIP1FN5000A−QDI		5 MegaPixel, LVDS mono micro lens, NIR Spectrum		
NOIP1SN2000A−QDI	PYTHON 2000	2 MegaPixel, LVDS mono micro lens		
NOIP1SE2000A−QDI		2 MegaPixel, LVDS color micro lens		
NOIP1FN2000A−QDI		2 MegaPixel, LVDS mono micro lens, NIR Spectrum		

The P1−SN/SE base part is used to reference the mono, color and NIR enhanced versions of the LVDS interface. More details on the part number coding can be found at http://www.onsemi.com/pub_link/Collateral/TND310−D.PDF

Package Mark

Line 1: **NOI P1xx RRRRA** where xx denotes mono micro lens (SN) or color micro lens (SE) option or NIR micro lens (FN), RRRR is the resolution (5000), (2000)

Line 2: **−QDI**

Line 3: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4−digit date code

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS (Note 1)

Parameter	Specification
Pixel Type	Global shutter pixel architecture
Shutter Type	Pipelined and triggered global shutter
Frame Rate at Full Resolution	100 frames per second @ 5 MegaPixels 230 frames per second @ 2 MegaPixels 250 frames per second @ Full HD
Master Clock	72 MHz when PLL is used, 360 MHz (10-bit) / 288 MHz (8-bit) when PLL is not used
Windowing	16 Randomly programmable windows. Normal, sub-sampled and binned readout modes
ADC Resolution (Note 1)	10-bit, 8-bit
LVDS Outputs	8 data + sync + clock
Data Rate	8 x 720 Mbps (10-bit) / 8 x 576 Mbps (8-bit)
Power Dissipation	1.5 W in 10-bit mode
Package Type	84-pin LCC

Table 2. NOMINAL ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Active Pixels	5 MegaPixels: 2592 (H) x 2048 (V) 2 MegaPixels: 1984 (H) x 1264 (V)
Pixel Size	4.8 μm x 4.8 μm
Conversion Gain	0.107 LSB10/e^-, 143 μV/e^-
Temporal Noise	< 10.7 e^- (Non−Zero ROT, 1x gain) < 9.4 e^- (Non−Zero ROT, 2x gain)
Responsivity at 550 nm	7.5 V/lux.s
Parasitic Light Sensitivity (PLS)	<1/5000
Full Well Charge	10000 e^-
Quantum Efficiency (QE x FF)	57%
Pixel FPN	< 1.25 (Non−Zero ROT) < 1.35 (Zero−ROT)
PRNU	< 10 LSB10
MTF	63% @ 535 nm − X-dir & Y-dir 63% @ 535 nm − X-dir & Y-dir (NIR)
PSNL @ 20°C (t_int = 30 ms)	300 LSB10/s, 2800 e^-/s
Dark Signal @ 20°C	9.3 e^-/s, 1.0 LSB10/s
Dynamic Range	60 dB
Signal to Noise Ratio (SNR max)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
T_J	Operating temperature range	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 3 and 4)

Symbol	Parameter	Min	Max	Unit
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.2	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
T_S	ABS storage temperature range	−40	+150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2012	2000		V
	Charged Device Model (CDM): EIA/JESD22−C101, Class C1	500		
LU	Latch−up: JESD−78	100		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The ADC is 11−bit, down−scaled to 10−bit. The PYTHON uses a larger word−length internally to provide 10−bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 5, 6, 7, 8 and 9)

Parameter	Description	Min	Typ	Max	Unit
Power Supply Parameters – P1−SN/SE LVDS (Note: All ground pins (gnd_18, gnd_33 and gnd_colpc) should be connected to an external 0 V ground reference.)					
vdd_33	Supply voltage, 3.3 V	**3.0**	3.3	**3.6**	V
Idd_33	Current consumption 3.3 V supply		345		mA
vdd_18	Supply voltage, 1.8 V	**1.6**	1.8	**2.0**	V
Idd_18	Current consumption 1.8 V supply		140		mA
vdd_pix	Supply voltage, pixel	**3.25**	3.3	**3.35**	V
Idd_pix	Current consumption pixel supply		35		mA
Ptot	Total power consumption at vdd_33 = 3.3 V, vdd_18 = 1.8 V		1.5		W
Pstby_lp	Power consumption in low power standby mode			50	mW
Popt	Power consumption at lower pixel rates	Configurable			
I/O – P1−SN/SE LVDS (EIA/TIA−644): Conforming to standard/additional specifications and deviations listed					
fserdata	Data rate on data channels DDR signaling – 4 data channels, 1 synchronization channel			720	Mbps
fserclock	Clock rate of output clock Clock output for mesochronous signaling			360	MHz
Vicm	LVDS input common mode level	0.3	1.25	1.8	V
Tccsk	Channel to channel skew (Training pattern should be used to correct per channel skew)			50	ps
Electrical Interface – P1−SN/SE LVDS					
fin	Input clock rate when PLL used			72	MHz
fin	Input clock when LVDS input used			360	MHz
tidc	Input clock duty cycle when PLL used	45	50	55	%
tj	Input clock jitter			20	ps
fspi	SPI clock rate when PLL used at fin = 72 MHz			10	MHz

Frame Specifications – P1−SN/SE−LVDS

		Typical		Max	Units
		Non−Zero ROT	Zero ROT		
fps_roi1	Xres x Yres = 2592 x 2048	85	100		fps
fps_roi2	Xres x Yres = 2048 x 2048	100	130		fps
fps_roi3	Xres x Yres = 1920 x 1200	180	230		fps
fps_roi4	Xres x Yres = 1920 x 1080	200	250		fps
fps_roi5	Xres x Yres = 1600 x 1200	205	275		fps
fps_roi6	Xres x Yres = 1024 x 1024	320	480		fps
fps_roi7	Xres x Yres = 1280 x 720	390	550		fps
fps_roi8	Xres x Yres = 800 x 600	615	985		fps
fps_roi9	Xres x Yres = 640 x 480	845	1450		fps
fps_roi10	Xres x Yres = 512 x 512	880	1555		fps
fps_roi11	Xres x Yres = 256 x 256	2035	2790		fps
fps_roi12	Xres x Yres = 544 x 20	7925	10400		fps
fpix	Pixel rate (8 channels at 72 Mpix/s)			576	Mpix/s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. Refer to ACSPYTHON5000 available at CISP extranet for detailed acceptance criteria specifications.
9. For power supply management recommendations, please refer to Application Note AND9158.

Color Filter Array

The PYTHON color sensors are processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left.

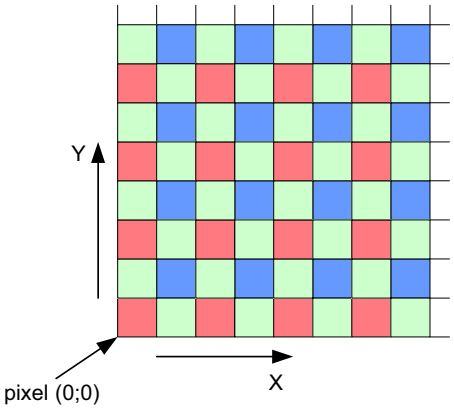


Figure 2. Color Filter Array for the Pixel Array

Spectral Response Curve

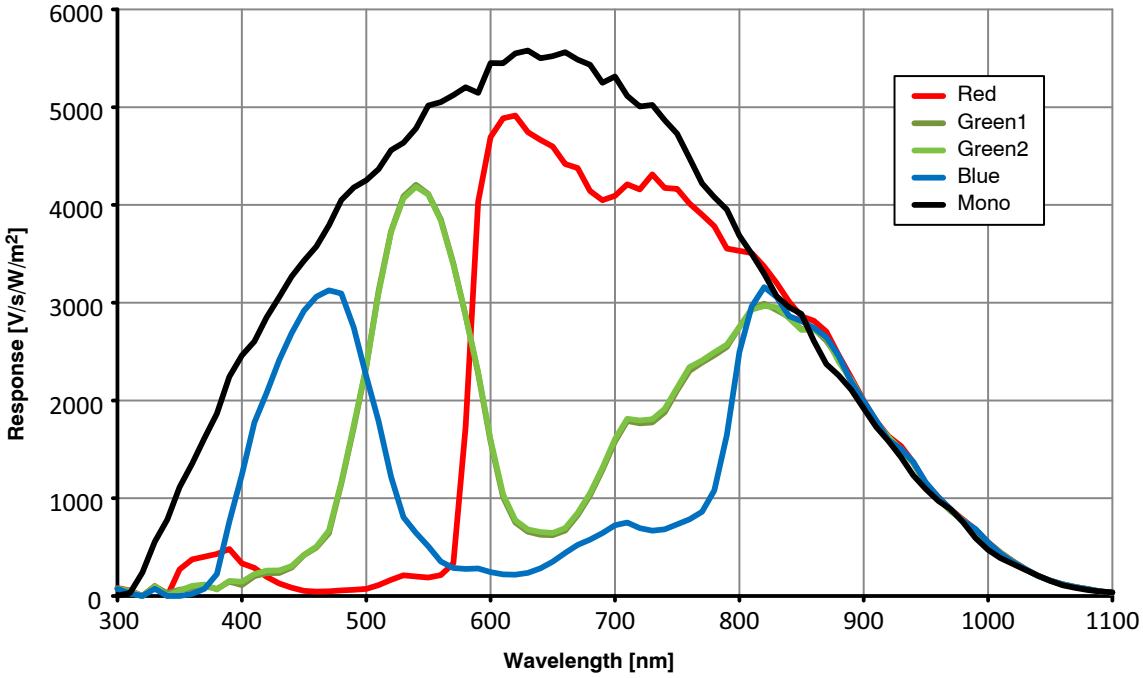


Figure 3. Spectral Response Curve for Mono and Color

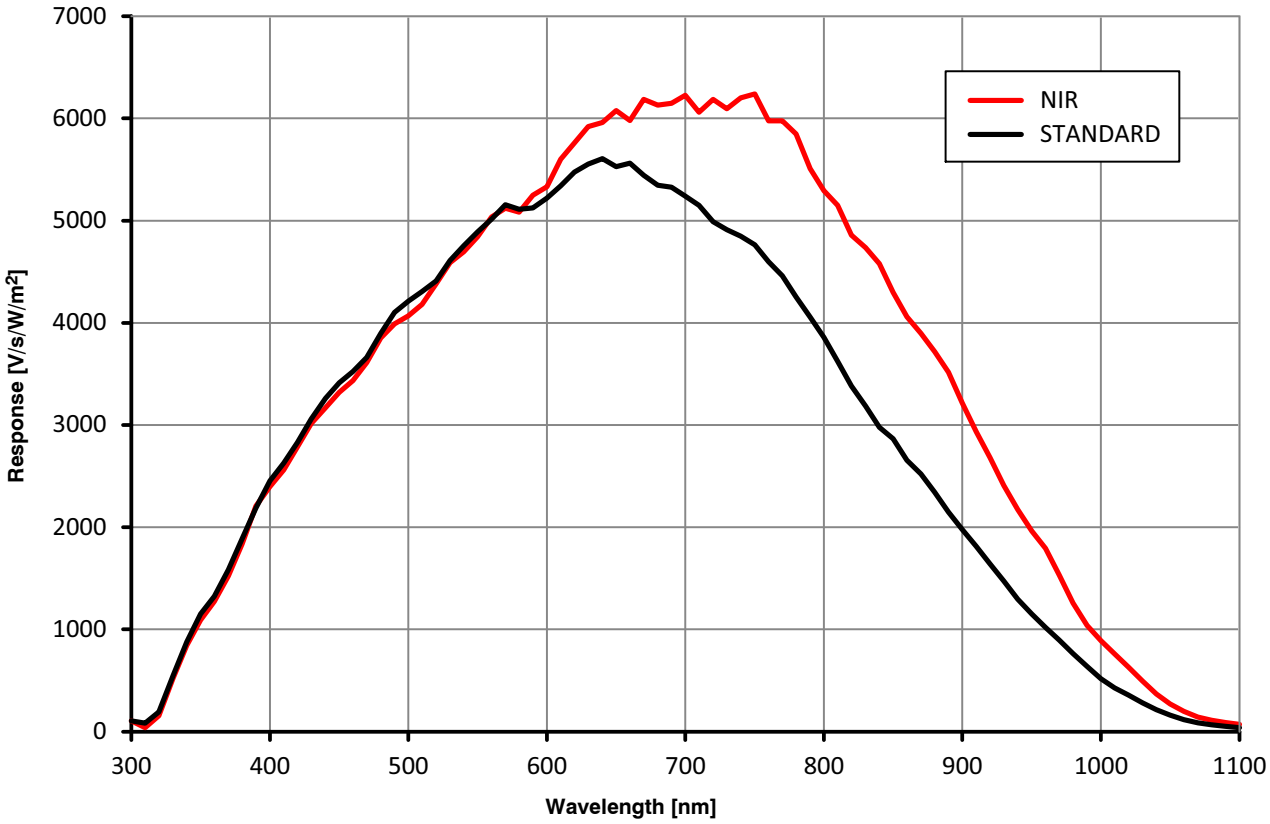


Figure 4. Spectral Response Curve for Standard and NIR Mono

Ray Angle and Microlens Array Information

An array of microlenses is placed over the CMOS pixel array in order to improve the absolute responsivity of the photodiodes. The combined microlens array and pixel array has two important properties:

Angular Dependency of Photoresponse of a Pixel

The photoresponse of a pixel with microlens in the center of the array to a fixed optical power with varied incidence angle is as plotted in Figure 5, where definitions of angles ϕx and ϕy are as described by Figure 6.

Microlens Shift across Array and CRA

The microlens array is fabricated with a slightly smaller pitch than the array of photodiodes. This difference in pitch creates a varying degree of shift of a pixel's microlens with regards to its photodiode. A shift in microlens position versus photodiode position will cause a tilted angle of peak photoresponse, here denoted Chief Ray Angle (CRA). Microlenses and photodiodes are aligned with 0 shift and CRA in the center of the array, while the shift and CRA increases radially towards its edges, as illustrated by Figure 7.

The purpose of the shifted microlenses is to improve the uniformity of photoresponse when camera lenses with a finite exit pupil distance are used. In the standard version of Python 5000, the CRA varies nearly linearly with distance from the center as illustrated in Figure 8, with a corner CRA of approximately 5.4 degrees. This edge CRA is matching a lens with exit pupil distance of ~80 mm.

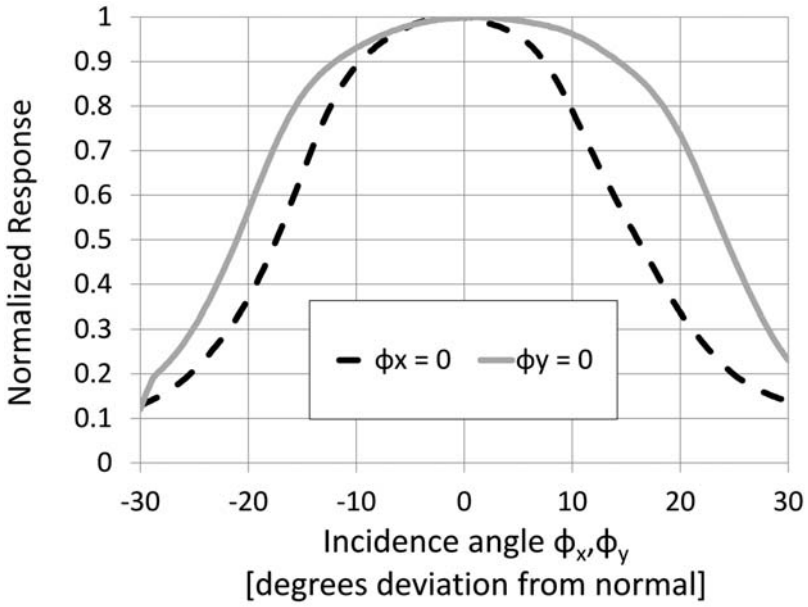


Figure 5. Center Pixel Photoresponse to a Fixed Optical Power with Incidence Angle Varied along ϕx and ϕy. Note that the Photoresponse Peaks near Normal Incidence for Center Pixels

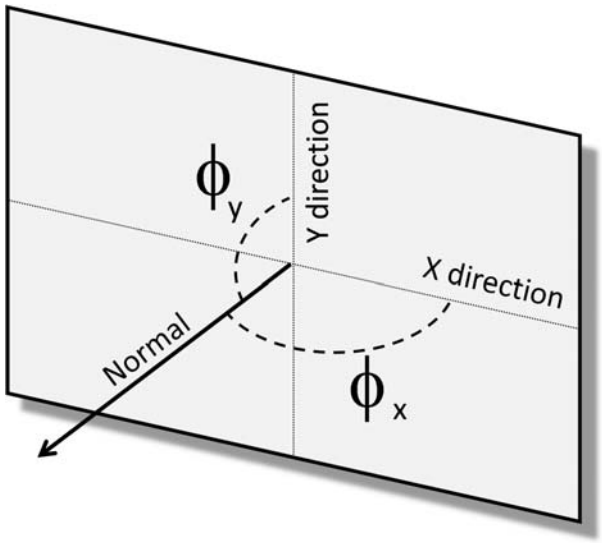


Figure 6. Definition of Angles Used in Figure 5

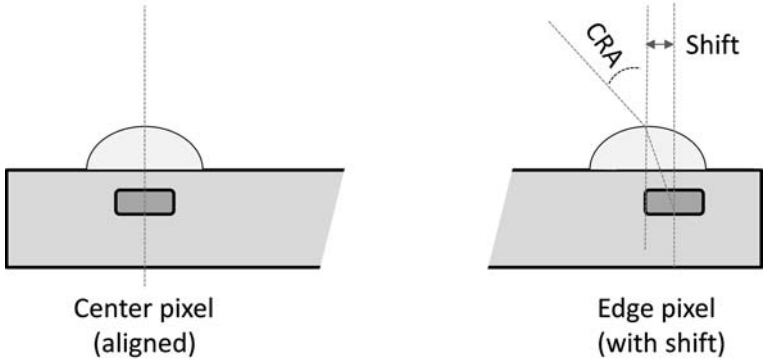


Figure 7. Principle of Microlens Shift. The Center Axes of the Microlens and the Photodiode Coincide for the Center Pixels. For the Edge Pixels, there is a Shift between the Axes of the Microlens and the Photodiode Causing a Peak Response Incidence Angle (CRA) that Deviates from the Normal of the Pixel Array

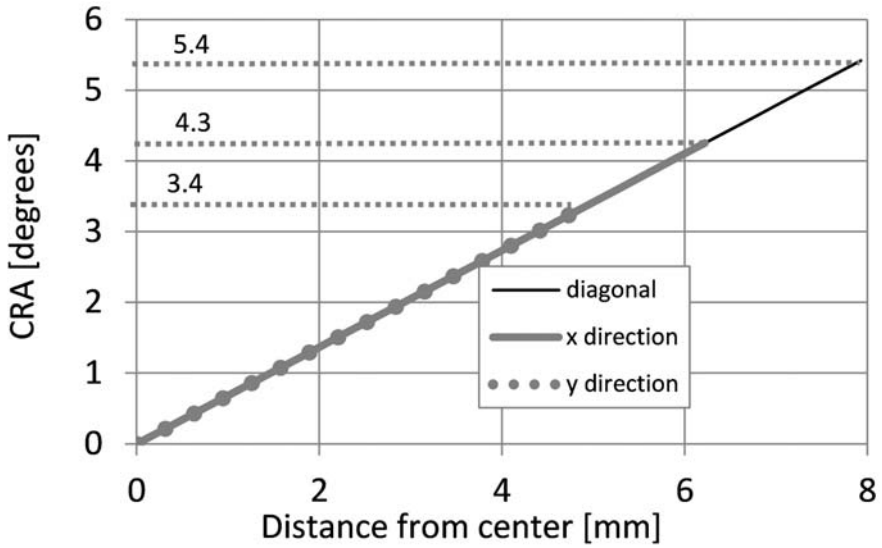


Figure 8. Variation of Peak Responsivity Angle (CRA) as a Function of Distance from the Center of the Array

OVERVIEW

Figures 9 gives an overview of the major functional blocks of the PYTHON sensor.

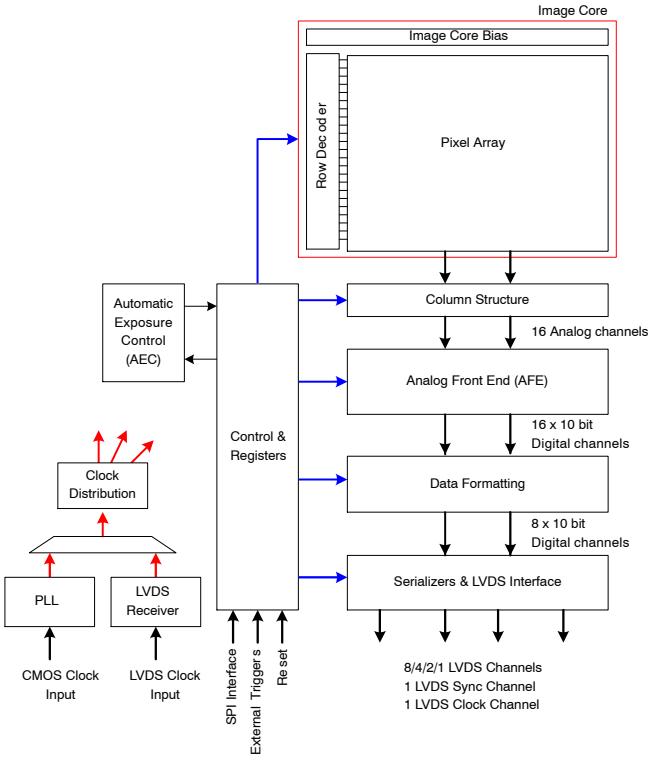


Figure 9. Block Diagram

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The PYTHON 5000 pixel array contains 2592 (H) x 2048 (V) readable pixels with a pixel pitch of 4.8 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses in−pixel CDS architecture, which makes it possible to achieve a low noise read out of the pixel array in global shutter mode with CDS.

The PYTHON 2000 image array contains 1984 (H) x 1264 (V) readable pixels, inclusive of 32 pixels on each side to allow for reprocessing or color reconstruction.

The function of the row drivers is to access the image array to reset or read the pixel data. The row drivers are controlled by the on−chip sequencer and can access the pixel array.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 72 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 360 MHz in 10−bit mode and 288 MHz in 8−bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample−and−hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 16 parallel differential outputs operating at a frequency of 36 MHz. At this stage, the reset signal and integrated signal values are transferred into an FPN−corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal. The column multiplexer also supports read−1−skip−1 and read−2−skip−2 mode. Enabling this mode increases the frame rate, with a decrease in resolution.

Bias Generator

The bias generator generates all required reference voltages and bias currents used on chip. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

Analog Front End

The AFE contains 16 channels, each containing a PGA and a 10−bit ADC.

For each of the 16 channels, a pipelined 10−bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block transmits synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface

The serializer and LVDS interface block receives the formatted (10−bit or 8−bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10−bit mode, the maximum output data rate is 720 Mbps per channel. In 8−bit mode, the maximum output data rate is 576 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system−level image reconstruction.

Channel Multiplexer

The LVDS channel multiplexer provides a 8:4, 8:2 and 8:1 feature, in addition to utilizing all 8 output channels.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

OPERATING MODES

Global Shutter Mode

The PYTHON operates in pipelined or triggered global shutter modes. In this mode, light integration takes place on all pixels in parallel, although subsequent readout is sequential. Figure 10 shows the integration and readout sequence for the global shutter mode. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

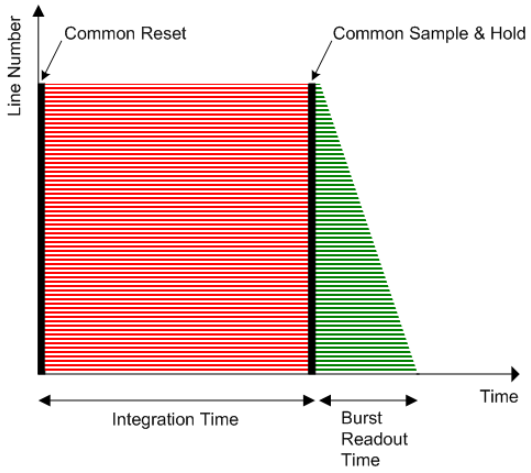


Figure 10. Global Shutter Operation

Pipelined Global Shutter Mode

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line per line and the readout of each line is preceded by the Row Overhead Time (ROT). Figure 11 shows the exposure and readout time line in pipelined global shutter mode.

Master Mode

In this mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

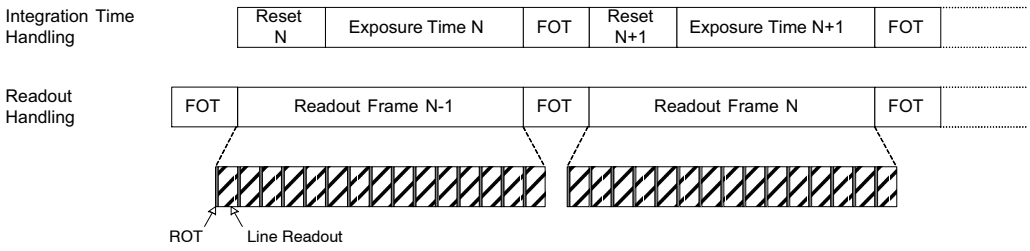


Figure 11. Pipelined Shutter Operation in Master Mode

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins. Figure 12 shows the relation between the external trigger signal and the exposure/readout timing.

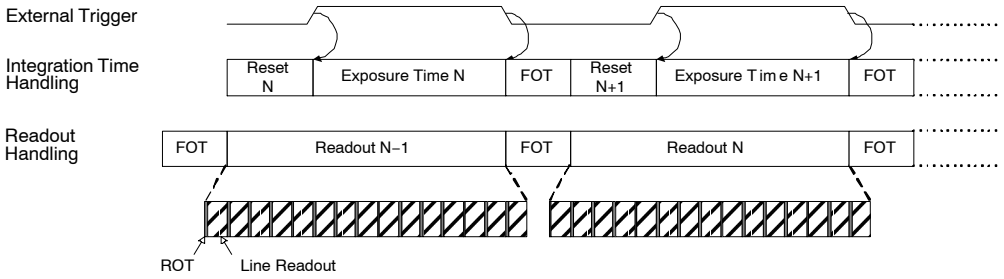


Figure 12. Pipelined Shutter Operation in Slave Mode

Triggered Global Shutter Mode

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences with the pipelined global shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is under user control through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global shutter mode can also be controlled in a master or in a slave mode.

Master Mode

In this mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is readout sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge. Figure 13 shows the relation between the external trigger signal and the exposure/readout timing.

If a rising edge is applied on the external trigger before the exposure time and FOT of the previous frame is complete, it is ignored by the sensor.

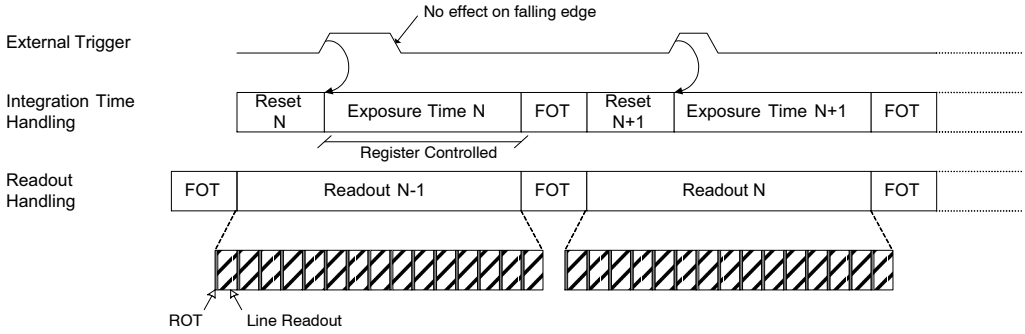


Figure 13. Triggered Shutter Operation in Master Mode

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. An external synchronization pin controls the start of integration. When it is de−asserted, the FOT starts. The analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

Non−Zero and Zero Row Overhead Time (ROT) Modes

In pipelined global shutter mode, the integration and readout are done in parallel. Images are continuously read out and integration of frame N is ongoing during readout of the previous frame N−1. The readout of every frame starts with a Frame Overhead Time (FOT), during which the analog value of the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by a Row Overhead Time (ROT) as shown in Figure 14.

In Reduced/Zero ROT operation mode (refer to Figure 15), the row blanking and kernel readout occur in parallel. This mode is called reduced ROT as a part of the ROT is done while the image row is readout. The actual ROT can thus be longer, however the perceived ROT will be shorter (‘overhead’ spent per line is reduced).

This operation mode can be used for two reasons:

- Reduced total line time.
- Lower power due to reduced clock−rate.

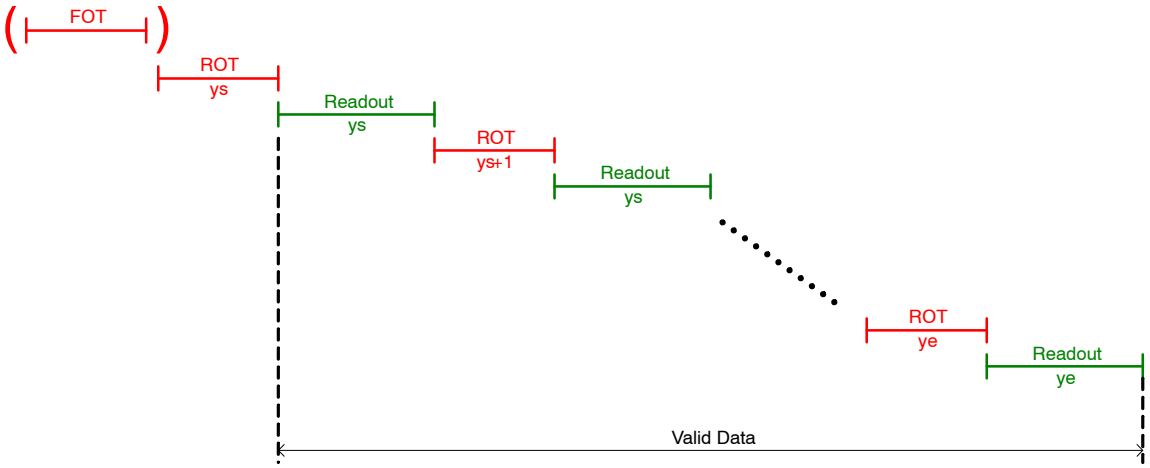


Figure 14. Integration and Readout Sequence of the Sensor Operating in Pipelined Global Shutter Mode with Non−Zero ROT Readout.

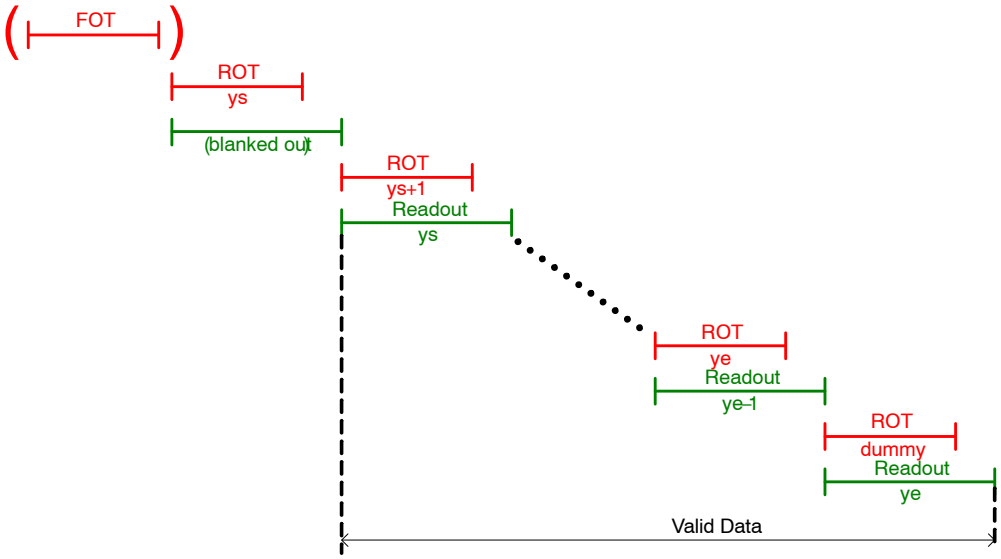


Figure 15. Integration and Readout Sequence of the Sensor operating in Pipelined Global Shutter Mode with Zero ROT Readout.

SENSOR OPERATION

Flowchart

Figure 16 shows the sensor operation flowchart. The sensor has six different ‘states’. Every state is indicated with the oval circle. These states are Power off, Low power standby, Standby (1), Standby (2), Idle, Running.

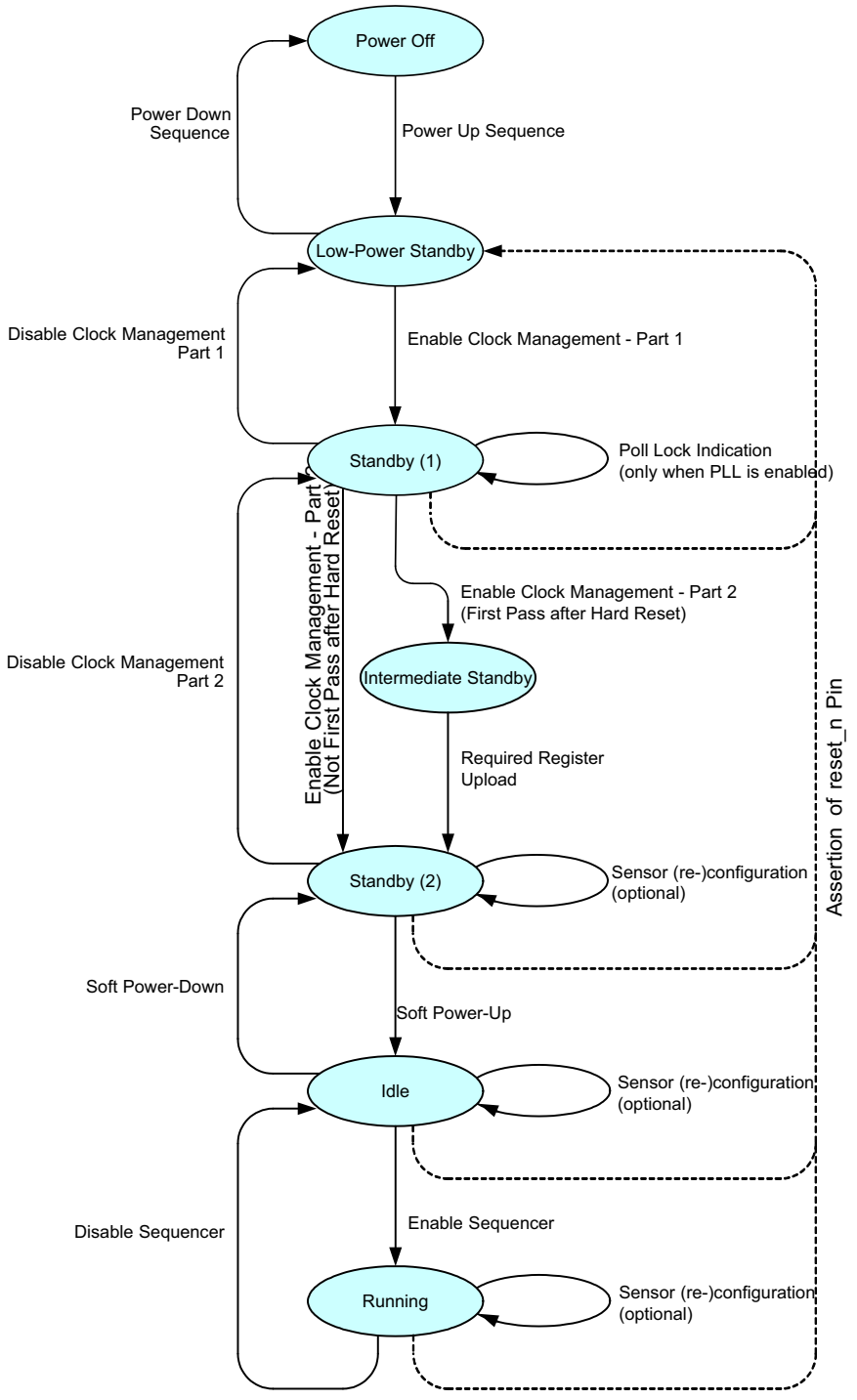


Figure 16. Sensor Operation Flowchart

Sensor States

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled).

All register settings are set to their default values (see Table 35).

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the ‘Enable Clock Management’ action described in Enable Clock Management − Part 1 on page 16

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images. The sensor can be operated in global master/slave modes.

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 17 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp−up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de−asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

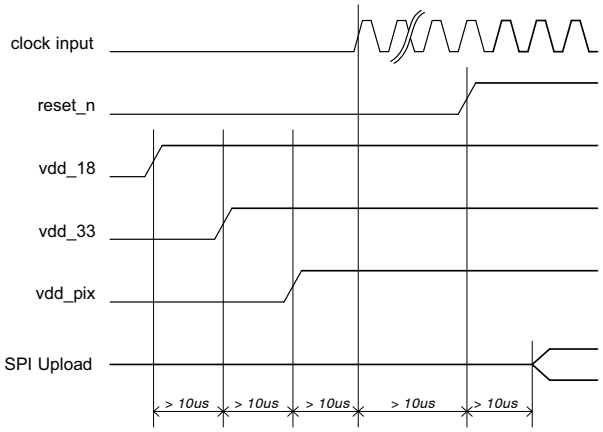


Figure 17. Power Up Sequence

Enable Clock Management − Part 1

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre−defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for P1−SN/SE 8−bit and 10−bit serial, with and without the PLL.

If the PLL is not used, the LVDS clock input must be running.

It is important to follow the upload sequence listed in Table 6.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

Check the PLL_lock flag 24[0] by reading the SPI register. When the flag is set, the ‘Enable Clock Management− Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 16 on page 14.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 1

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	2	0x000C	Monochrome sensor
		0x000D	Color sensor
2	32	0x000C	Configure clock management
3	20	0x0000	Configure clock management
4	17	0x210F	Configure PLL
5	26	0x1180	Configure PLL lock detector
6	27	0xCCBC	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
P1−SN/SE 8−bit mode without PLL			
1	2	0x000C	Monochrome sensor
		0x000D	Color sensor
2	32	0x0008	Configure clock management
3	20	0x0001	Enable LVDS clock input
P1−SN/SE 10−bit mode with PLL			
1	2	0x000C	Monochrome sensor
		0x000D	Color sensor
2	32	0x0004	Configure clock management
3	20	0x0000	Configure clock management
4	17	0x2113	Configure PLL
5	26	0x2280	Configure PLL lock detector
6	27	0x3D2D	Configure PLL lock detector
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
P1−SN/SE 10−bit mode without PLL			
1	2	0x000C	Monochrome sensor
		0x000D	Color sensor
2	32	0x0000	Configure clock management
3	20	0x0001	Enable LVDS clock input

Enable Clock Management – Part 2

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 7. Note that it is important to follow the upload sequence listed in Table 7.

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x000E	Enable logic clock
3	34	0x0001	Enable logic blocks
P1−SN/SE 8−bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x000A	Enable logic clock
3	34	0x0001	Enable logic blocks
P1−SN/SE 10−bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x0006	Enable logic clock
3	34	0x0001	Enable logic block
P1−SN/SE 10−bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x0002	Enable logic clock
3	34	0x0001	Enable logic blocks

Required Register Upload

In this phase, the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction.

Table 8. REQUIRED REGISTER UPLOADS FOR 10−BIT, ZERO−ROT, PIPELINED GLOBAL SHUTTER MASTER MODE

Upload #	Address	Data (Zero ROT)
1	41	0x0855
2	42	0x0003
3	43	0x0008
4	65	0xF8CB
5	66	0x53C8
6	67	0x8788
7	69	0x0888
8	70	0x4111
9	71	0x9788
10	72	0x3337
11	81	0x86A5
12	128	0x4714
13	129**	0x0001
14	171	0x1001
15	176	0x00F1
16	192	0x000C
17	193*	0x0800
18	194	0x0224
19	197	0x0104
20	204	0x01E1
21	211	0x0E49
22	215	0x111F
23	216	0x7F00
24	219	0x0020
25	220	0x2434
26	224	0x3E07
27	227	0x0000
28	250	0x1081
29	384	0xC800
30	385	0xFB1F
31	386	0xFB1F
32	387	0xFB12
33	388	0xF912
34	389	0xF902
35	390	0xF804
36	391	0xF008

Upload #	Address	Data (Zero ROT)
37	392	0xF102
38	393	0xF30F
39	394	0xF30F
40	395	0xF30F
41	396	0xF30F
42	397	0xF30F
43	398	0xF30F
44	399	0xF102
45	400	0xF008
46	401	0xF24A
47	402	0xF264
48	403	0xF226
49	404	0xF021
50	405	0xF002
51	406	0xF40A
52	407	0xF005
53	408	0xF20F
54	409	0xF20F
55	410	0xF20F
56	411	0xF20F
57	412	0xF005
58	413	0xEC05
59	414	0xC801
60	415	0xC800
61	416	0xC800
62	417	0xCC0A
63	418	0xC806
64	419	0xC800
65	420	0x0030
66	421	0x2179
67	422	0x2071
68	423	0x0071

Upload #	Address	Data (Zero ROT)
69	424	0x107F
70	425	0x1079
71	426	0x0071
72	427	0x0031
73	428	0x01B4
74	429	0x21B9
75	430	0x20B1
76	431	0x00B1
77	432	0x10BF
78	433	0x10B9
79	434	0x00B1
80	435	0x0030
81	436	0x0030
82	437	0x2079
83	438	0x2071
84	439	0x0071
85	440	0x107F
86	441	0x1079
87	442	0x0071
88	443	0x0031
89	444	0x01B4
90	445	0x21B9
91	446	0x20B1
92	447	0x00B1
93	448	0x10BF
94	449	0x10B9
95	450	0x00B1
96	451	0x0030
Upload #	**Address**	**Data (Non−Zero ROT)**
15	193*	0x5000
Upload #	**Address**	**Data (8−bit mode)**
13	129**	0x2001

*Required Uploads for Non−Zero ROT / 8−bit mode are the same as for Zero ROT 10−bit mode with the exceptions noted.

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

Table 9. SOFT POWER UP REGISTER UPLOADS

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	10	0x0000	Release soft reset state
2	32	0x000F	Enable analogue clock
3	64	0x0001	Enable biasing clock
4	40	0x0003	Enable column multiplexer
5	48	0x0001	Enable AFE
6	68	0x0085	Enable LVDS bias
7	72	0x3337	Enable charge pump
8	112	0x0007	Enable LVDS transmitters
P1−SN/SE 8−bit mode without PLL			
1	10	0x0000	Release soft reset state
2	32	0x000B	Enable analogue clock
3	64	0x0001	Enable biasing clock
4	40	0x0003	Enable column multiplexer
5	48	0x0001	Enable AFE
6	68	0x0085	Enable LVDS bias
7	72	0x3337	Enable charge pump
8	112	0x0007	Enable LVDS transmitters
P1−SN/SE 10−bit mode with PLL			
1	10	0x0000	Release soft reset state
2	32	0x0007	Enable analogue clock
3	64	0x0001	Enable biasing clock
4	40	0x0003	Enable column multiplexer
5	48	0x0001	Enable AFE
6	68	0x0085	Enable LVDS bias
7	72	0x3337	Enable charge pump
8	112	0x0007	Enable LVDS transmitters
P1−SN/SE 10−bit mode without PLL			
1	10	0x0000	Release soft reset state
2	32	0x0003	Enable analogue clock
3	64	0x0001	Enable biasing clock
4	40	0x0003	Enable column multiplexer
5	48	0x0001	Enable AFE
6	68	0x0085	Enable LVDS bias
7	72	0x3337	Enable charge pump
8	112	0x0007	Enable LVDS transmitters

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 15.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 10.

Table 10. ENABLE SEQUENCER REGISTER UPLOADS

Upload #	Address	Data
1	192	0x000D

User Actions: Functional Modes to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of a set of register uploads. as listed in Table 11.

Table 11. DISABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data
1	192	0x000C

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 12.

Table 12. SOFT POWER DOWN REGISTER UPLOADS

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	112	0x0000	Disable LVDS transmitters
2	72	0x3330	Disable charge pump
3	48	0x0000	Disable AFE
4	40	0x0000	Disable column multiplexer
5	64	0x0000	Disable biasing clock
6	32	0x000E	Disable analogue clock
7	10	0x0999	Soft reset
P1−SN/SE 8−bit mode without PLL			
1	112	0x0000	Disable LVDS transmitters
2	72	0x3330	Disable charge pump
3	48	0x0000	Disable AFE
4	40	0x0000	Disable column multiplexer
5	64	0x0000	Disable biasing clock
6	32	0x000A	Disable analogue clock
7	10	0x0999	Soft reset
P1−SN/SE 10−bit mode with PLL			
1	112	0x0000	Disable LVDS transmitters
2	72	0x3330	Disable charge pump
3	48	0x0000	Disable AFE
4	40	0x0000	Disable column multiplexer
5	64	0x0000	Disable biasing clock
6	32	0x0006	Disable analogue clock
7	10	0x0999	Soft reset
P1−SN/SE 10−bit mode without PLL			
1	112	0x0000	Disable LVDS transmitters
2	72	0x3330	Disable charge pump

Table 12. SOFT POWER DOWN REGISTER UPLOADS

Upload #	Address	Data	Description
3	48	0x0000	Disable AFE
4	40	0x0000	Disable column multiplexer
5	64	0x0000	Disable biasing clock
6	32	0x0002	Disable analogue clock
7	10	0x0999	Soft reset

Disable Clock Management – Part 2

The 'Disable Clock Management' action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 13.

Table 13. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	32	0x000C	Disable logic clock
2	34	0x0000	Disable logic blocks
3	9	0x0009	Soft reset clock generator
P1−SN/SE 8−bit mode without PLL			
1	32	0x0008	Disable logic clock
2	34	0x0000	Disable logic blocks
3	9	0x0009	Soft reset clock generator
P1−SN/SE 10−bit mode with PLL			
1	32	0x0004	Disable logic clock
2	34	0x0000	Disable logic blocks
3	9	0x0009	Soft reset clock generator
P1−SN/SE 10−bit mode without PLL			
1	32	0x0000	Disable logic clock
2	34	0x0000	Disable logic blocks
3	9	0x0009	Soft reset clock generator

Disable Clock Management – Part 1

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
P1−SN/SE 8−bit mode with PLL			
1	8	0x0099	Soft reset PLL
2	16	0x0000	Disable PLL
P1−SN/SE 8−bit mode without PLL			
1	20	0x0000	Configure clock management
P1−SN/SE 10−bit mode with PLL			
1	8	0x0099	Soft reset PLL
2	16	0x0000	Disable PLL
P1−SN/SE 10−bit mode without PLL			
1	20	0x0000	Configure clock management

Power Down Sequence

Figure 18 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

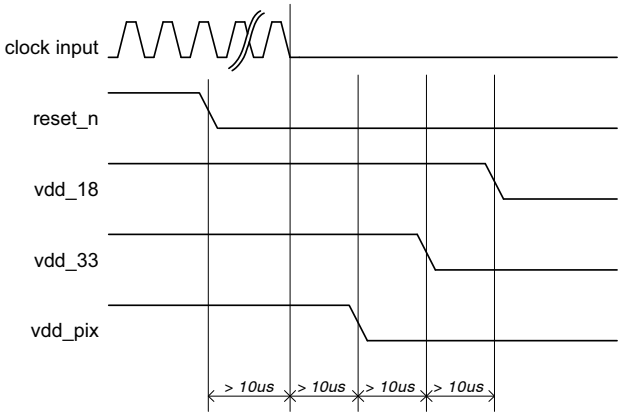


Figure 18. Power Down Sequence

Sensor reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states by modifying registers 199 to 203. Refer to page 30−32 for more information.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states by modifying registers 204/205. Refer to page 37 for more information.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Multiple Window Readout on page 31 for more information.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states by modifying register 192. Refer to Subsampling on page 32 for more information.
- Shutter Mode: The shutter mode can only be changed during standby or idle mode by modifying register 192. Reconfiguring the shutter mode during running state is not supported.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 15 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 15. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
Charge Pump	72	Configure according to recommendation
LVDS	112	Configure according to recommendation
Sequencer mode selection	192 [6:1]	Operation modes are: • triggered_mode • slave_mode
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 16. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[12:8]	Reconfiguration of these registers may have an impact on the black−level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 116–126	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144, 146–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 17. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 17. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	192[7] 192[8]	Subsampling or binning is synchronized to a new frame start.
ROI configuration	195 256–303	A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	199–203	Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to '1' in triggered global mode (master).
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] – gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re−enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 19 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

Figure 20 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de−asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

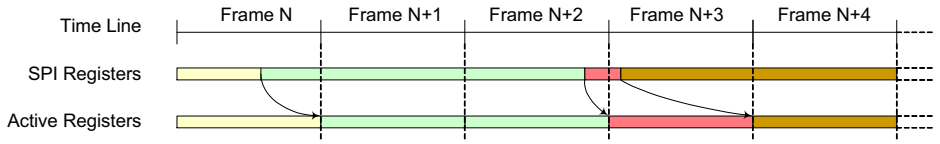


Figure 19. Frame Synchronization of Configurations (no freezing)

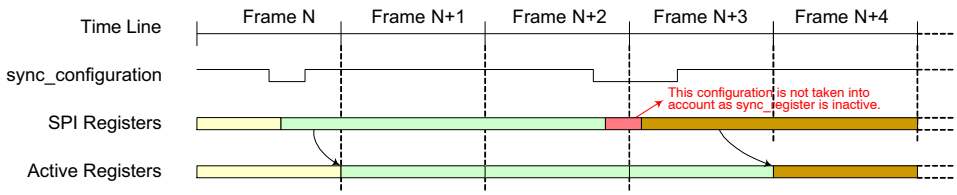


Figure 20. reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 18 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 18. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[15:0] subsampling binning	Update of active ROI configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. reconfiguration of active windows is not gated by this setting.

Window Configuration

Global Shutter Mode

Up to 16 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 303. Each window can be activated or deactivated separately using register 195. It is possible to reconfigure the inactive windows while the sensor is acquiring images.

Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one register.

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 16 columns contained in one kernel. This implies 16 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black−level algorithm are listed in Table 19.

Table 19. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Address	Register Name	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255. **Note:** When the automatic black−level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black−level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: Each black line contains 162 kernels.
197[12:8]	gate_first_line	A number of black lines are blanked out when a value different from 0 is configured. These blanked out lines are not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black−level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black−level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.

Table 19. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Address	Register Name	Description
Black Line Generation		
128[10:8]	black_samples	The black samples are low−pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is 2^ black_samples. **Note:** An error is reported by the device if more samples than available are requested (refer to register 136).
Black Level Filtering Monitoring		
136	blackcal_error0	An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation: • Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197). • Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128). • Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.

NOTE: The maximum number of samples taken into account for black level statistics is half the number of kernels.

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 21 shows the communication protocol for read and write accesses of the SPI registers. The PYTHON sensor uses 9−bit addresses and 16−bit data words.

Data driven by the system is colored blue in Figure 16, while data driven by the sensor is colored yellow. The data in grey indicates high−Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle after selecting the sensor, the 9−bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 21. The sensor samples this address data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16−bit data, most significant bit first.
   - For read commands, the sensor returns the data on the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI depends on the input clock and type of sensor. The frequency is $1/6^{th}$ of the PLL input clock or $1/30^{th}$ (in 10−bit mode) and $1/24^{th}$ (in 8−bit mode) of the LVDS input clock frequency.

At nominal input frequency, the maximum frequency for the SPI is 10 MHz. Consecutive SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

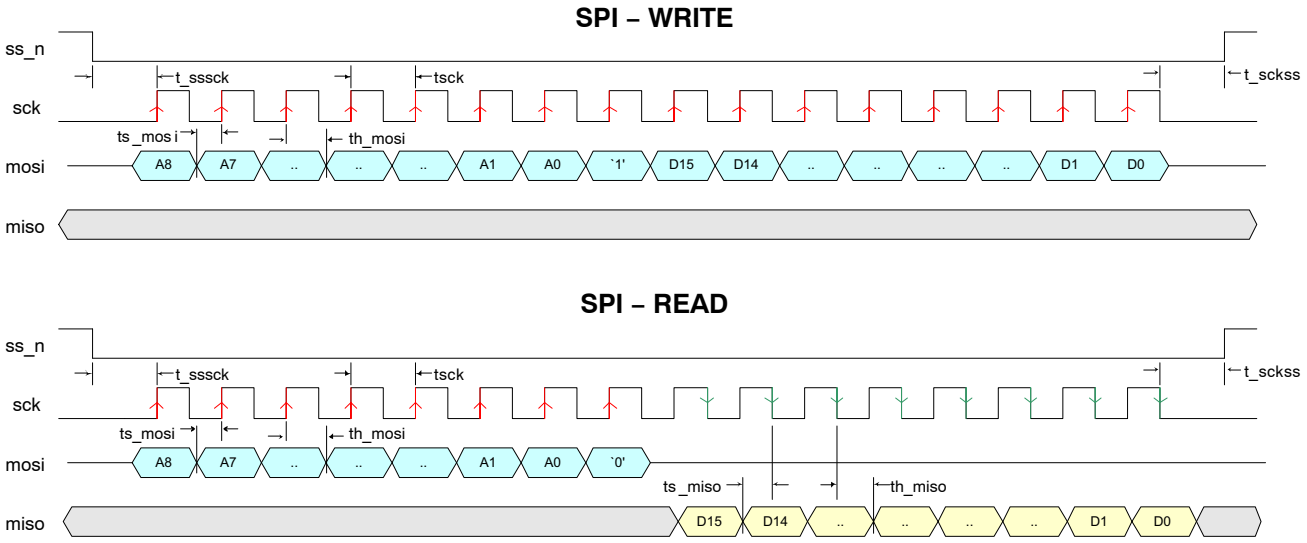


Figure 21. SPI Read and Write Timing Diagram

Table 20. SPI TIMING REQUIREMENTS

Group	Addresses	Description	Units
tsck	sck clock period	100 (*)	ns
tsssck	ss_n low to sck rising edge	tsck	ns
tsckss	sck falling edge to ss_n high	tsck	ns
ts_mosi	Required setup time for mosi	20	ns
th_mosi	Required hold time for mosi	20	ns
ts_miso	Setup time for miso	tsck/2−10	ns
th_miso	Hold time for miso	tsck/2−20	ns
tspi	Minimal time between two consecutive SPI accesses (not shown in figure)	2 x tsck	ns

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as $1/f_{SPI}$. See text for more information on SPI clock frequency restrictions.

IMAGE SENSOR TIMING AND READOUT

The following sections describe the configurations for single slope reset mechanism. Dual and triple slope handling during global shutter operation is similar to the single slope operation. Extra integration time registers are available.

Global Shutter Mode

Pipelined Global Shutter (Master)

The integration time is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers reset_length and exposure and is read as number of system clock cycles.

The exposure control for (Pipelined) Global Master mode is depicted in Figure 22.

The pixel values are transferred to the storage node during FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the reset_length and mult_timer registers, as shown in the figure. Note that meanwhile the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTE: The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.

- Make sure that the sum of the reset time and exposure time exceeds the time required to readout all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.
- Alternatively, it is possible to specify the frame time and exposure time. The sensor automatically calculates the required reset time. This mode is enabled by the fr_mode register. The frame time is specified in the register fr_length.

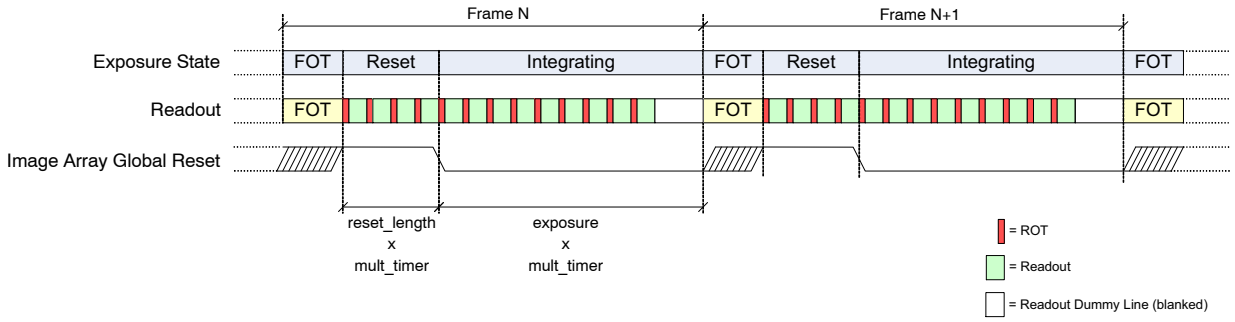


Figure 22. Integration Control for (Pipelined) Global Shutter Mode (Master)

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger0 pin. The exposure or integration time is defined by the registers exposure and mult_timer, as in the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 23.

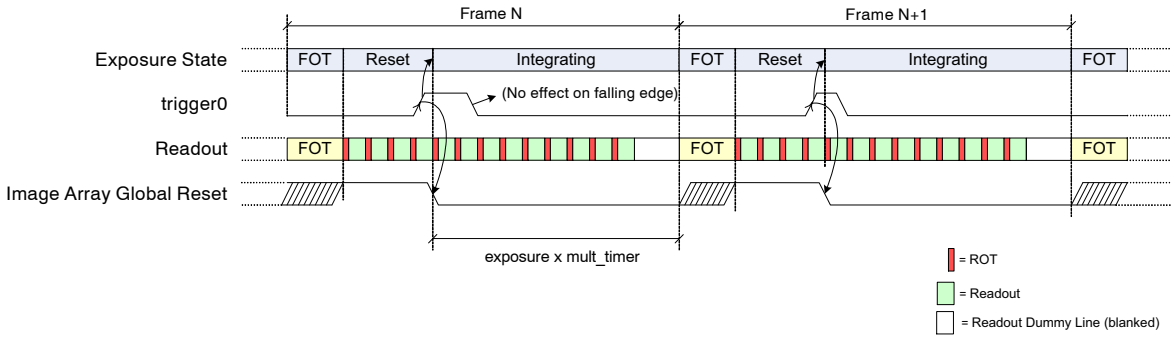


Figure 23. Exposure Time Control in Triggered Shutter Mode (Master)

Notes:

- The falling edge on the trigger pin does not have any impact. Note however the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

Triggered Global Shutter (Slave)

Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The registers fr_length, exposure and mult_timer are ignored by the sensor.

A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer to the pixel storage node and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.

The use of the trigger during slave mode is shown in Figure 24.

Notes:

- The registers exposure, fr_length, and mult_timer are not used in this mode.
- The start of exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. As a consequence, the effective time during which the image core is in a reset state is extended to the start of a new line.
- If the trigger is de−asserted before the end of readout, the exposure time is extended until the end of the last active line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (eg. use monitor0, indicating the very first line when monitor_select = 0x5 − a new trigger can be initiated after a rising edge on monitor0).

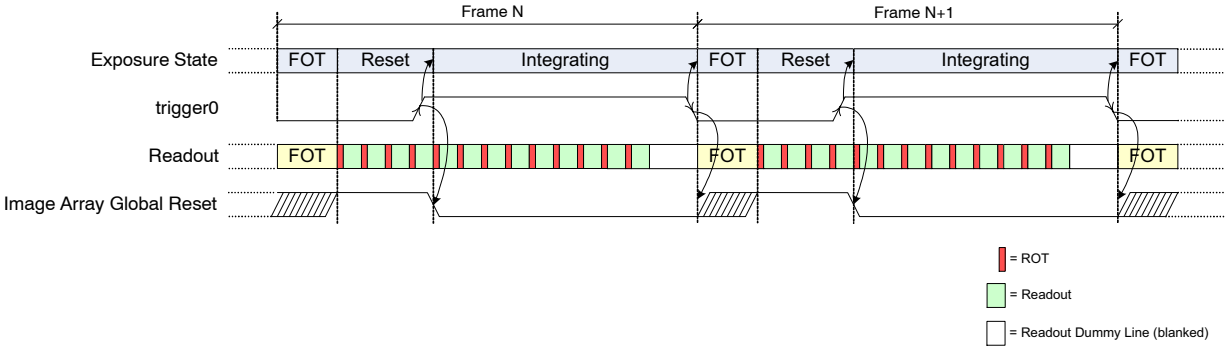


Figure 24. Exposure Time Control in Global−Slave Mode

ADDITIONAL FEATURES

Multiple Window Readout

The PYTHON sensor supports multiple window readout, which means that only the user−selected Regions Of Interest (ROI) are read out. This allows limiting data output for every frame, which in turn allows increasing the frame rate. In global shutter mode, up to eight ROIs can be configured.

Window Configuration

Figure 25 shows the four parameters defining a region of interest (ROI).

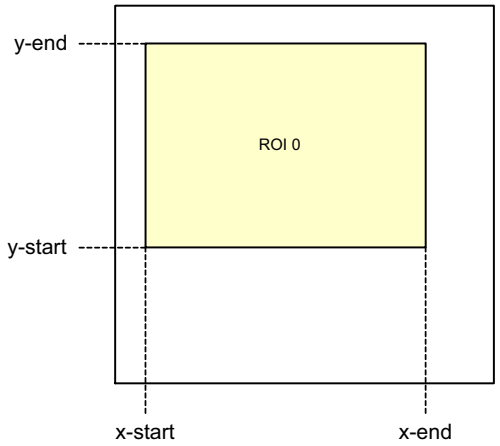


Figure 25. Region of Interest Configuration

- x−start[7:0]

x−start defines the x−starting point of the desired window. The sensor reads out 16 pixels in one single clock cycle. As a consequence, the granularity for configuring the x−start position is also 16 pixels for no sub sampling. The value configured in the x−start register is multiplied by 16 to find the corresponding column in the pixel array.

- x−end[7:0]

This register defines the window end point on the x−axis. Similar to x−start, the granularity for this configuration is one kernel. x−end needs to be larger than x−start.

- y−start[9:0]

The starting line of the readout window. The granularity of this setting is one line, except with color sensors where it needs to be an even number.

- y−end[9:0]

The end line of the readout window. y−end must be configured larger than y−start. This setting has the same granularity as the y−start configuration.

Up to eight windows can be defined, possibly (partially) overlapping, as illustrated in Figure 26.

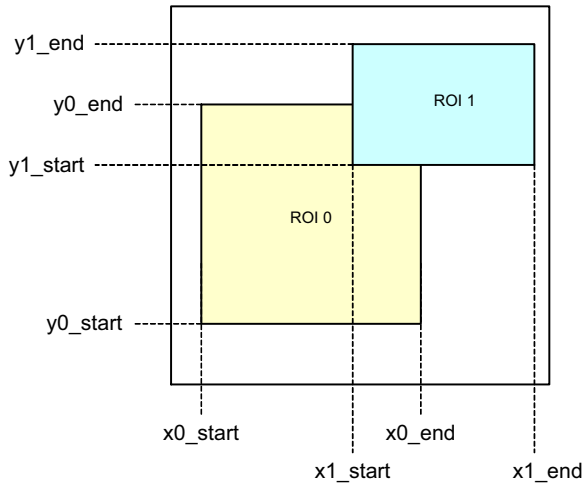


Figure 26. Overlapping Multiple Window Configuration

The sequencer analyses each line that needs to be read out for multiple windows.

Restrictions

The following restrictions for each line are assumed for the user configuration:

- Windows are ordered from left to right, based on their x−start address:

$$x\_start\_roi(i) \leq x\_start\_roi(j) \; AND$$

$$x\_end\_roi(i) \leq x\_end\_roi(j)$$

$$\text{Where } j > i$$

Processing Multiple Windows

The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y−counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, it is initialized to the y−start address of the first window and it runs until the y−end address of the last window to be read out. The last window is configured by the configuration registers and it is not necessarily window #15.

The x−counter starts counting from the x−start address of the window with the lowest ID which is active on the addressed line. Only windows for which the current y−address is enclosed are taken into account for scanning. Other windows are skipped.

Figure 27 illustrates a practical example of a configuration with five windows. The current position of the

read pointer (ys) is indicated by a red line crossing the image array. For this position of the read pointer, three windows need to be read out. The initial start position for the x−kernel pointer is the x−start configuration of ROI1. Kernels are scanned up to the ROI3 x−end position. From there, the x−pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4's x−end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI1.

Notes:

- The starting point for the readout pointer at the start of a frame is the y−start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in y−direction. In Figure 27, this is the case when reaching the end of ROI0 where the read pointer jumps to the y−start position of ROI1
- The x−pointer starting position is equal to the x−start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x−pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.
- Each window can be activated separately. There is no restriction on which window and how many of the 16 windows are active.

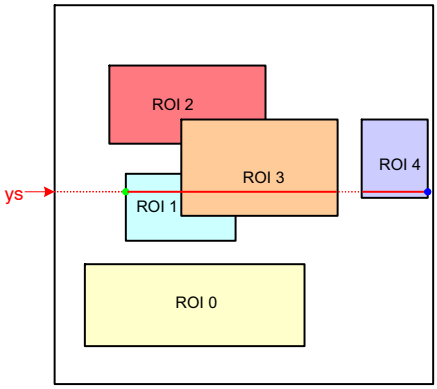


Figure 27. Scanning the Image Array with Five Windows

Subsampling

Subsampling is used to reduce the image resolution. This allows increasing the frame rate. Two subsampling modes are supported:

Monochrome Sensors

For monochrome sensors, the read−1−skip−1 subsampling scheme is used. Subsampling occurs both in x− and y− direction.

Color Sensors

For color sensors, the read−2−skip−2 subsampling scheme is used. Subsampling occurs both in x− and y− direction. Figure 28 shows which pixels are read and which ones are skipped.

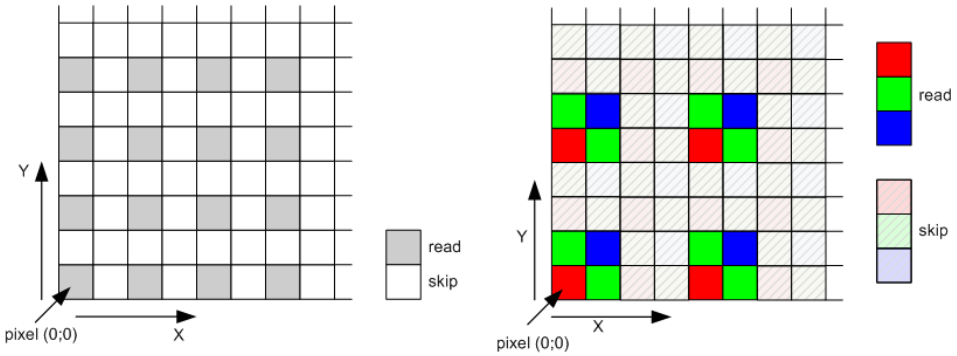


Figure 28. Subsampling Scheme for Monochrome and Color Sensors

Binning

Pixel binning is a technique in which different pixels belonging to a rectangular bin are averaged in the analog domain. Two−by−two pixel binning is available with the PYTHON monochrome sensor. This implies that two adjacent pixels are averaged both in column and row. Binning is configurable using a register setting. Pixel binning is not supported on PYTHON color option and in Zero ROT mode.

NOTES:

1. Pixel binning can be configured independently in x and y. Configure binning_mode to 0x0 for 2x2 binning and to 0x1 for 2x1 binning (binning in x direction only).
2. Binning in y-direction cannot be used in combination with pipelined integration and readout. The integration time and readout time should be separated in time (do not coincide).

Reverse Readout in Y−direction

Reverse readout in y−direction can be done by asserting reverse_y (reg 194[8]). The reference for y_start and y_stop pointers is reversed.

Down−Multiplexing

The PYTHON sensor contains a function for down−multiplexing the output channels. Using this function, one may for instance use the PYTHON 5000 with sync+clock+4 data channels instead of sync+clock+8 data channels.

Enabling the down−multiplexing is done through register 32[5:4]. The default value of 0 disables all down−multiplexing. Higher values sets higher degree of down−multiplexing, The channels that are used per degree of multiplexing are shown in Table 21. The unused data channels are powered down and will not send any data.

Table 21. ILLUSTRATION OF WHICH CHANNELS THAT ARE USED DEPENDING ON DEGREE OF DOWN MULTIPLEXING

Multiplex Mode	PYTHON 5000/2000 − 8 LVDS Channels							
8 channels	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7
4 channels	Ch 0		Ch 2		Ch 4		Ch 6	
2 channels	Ch 0				Ch 4			
1 channel	Ch 0							

Multiple Slope Integration

'Multiple Slope Integration' is a method to increase the dynamic range of the sensor. The PYTHON supports up to three slopes.

Figure 29 shows the sensor response to light when the sensor is used with one slope, two slopes, and three slopes. The X−axis represents the light power; the Y−axis shows the sensor output signal. The kneepoint of the multiple slope curves are adjustable in both position and voltage level.

It is clear that when using only one slope (red curve), the sensor has the same responsivity over the entire range, until the output saturates at the point indicated with 'single slope saturation point'.

To increase the dynamic range of the sensor, a second slope is applied in the dual slope mode (green curve). The sensor has the same responsivity in the black as for a single slope, but from 'knee point 1' on, the sensor is less responsive to incoming light. The result is that the saturation point is at a higher light power level.

To further increase the dynamic range, a third slope can be applied, resulting in a second knee point.

Refer to section Global Shutter Mode on page 29 for general notes applicable to the global shutter operation and more particular to the use of the trigger0 pin.

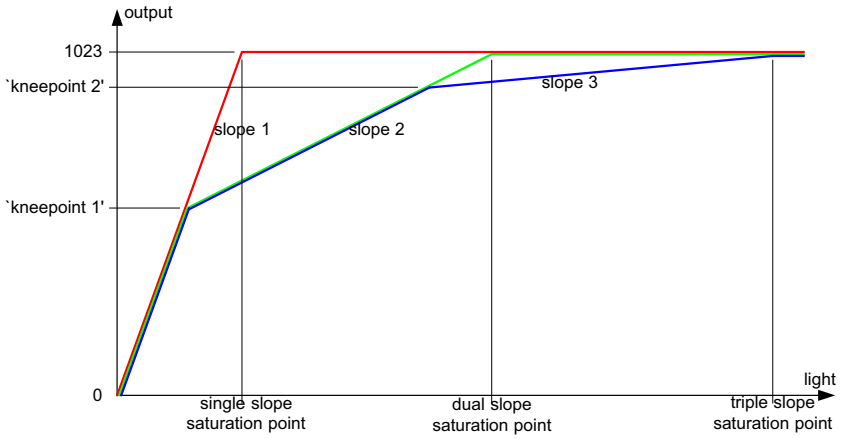


Figure 29. Multiple Slope Operation

Kneepoint Configuration (Multiple Slope Reset Levels)

The kneepoint reset levels are configured by means of DAC configurations in the image core. The dual slope kneepoint is configured with the *dac_ds* configuration, while the triple slope kneepoint is configured with the *dac_ts* register setting. Both are located on address 41.

Multiple Slope Integration in "Master Mode" (Pipelined or Triggered)

In master mode, the time stamps for the double and triple slope resets are configured in a similar way as the exposure time. They are enabled through the registers *dual_slope_enable* and *triple_slope_enable* and their values are defined by the registers *exposure_ds* and *exposure_ts*.

NOTE: Dual and triple slope sequences must start after readout of the previous frame is fully completed.

Figure 30 shows the frame timing for pipelined master mode with dual and triple slope integration and fr_mode = '0' (fr_length representing the reset length).

In triggered master mode, the start of integration is initiated by a rising edge on *trigger0*, while the falling edge does not have any relevance. Exposure duration and dual/triple slope points are defined by the registers.

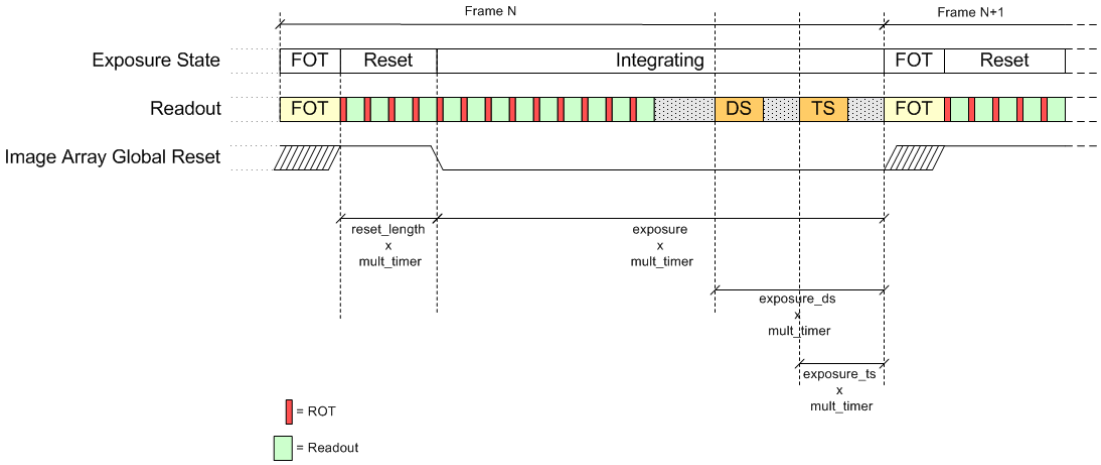


Figure 30. Multiple Slope Operation in Master Mode for fr_mode = '0' (Pipelined)

Slave Mode

In slave mode, the register settings for integration control are ignored. The user has full control through the *trigger0, trigger1* and *trigger2* pins. A falling edge on *trigger1* initiates the dual slope reset while a falling edge on *trigger2* initiates the triple slope reset sequence. Rising edges on *trigger1* and *trigger2* do not have any impact.

NOTE: Dual and triple slope sequences must start after readout of the previous frame is fully completed.

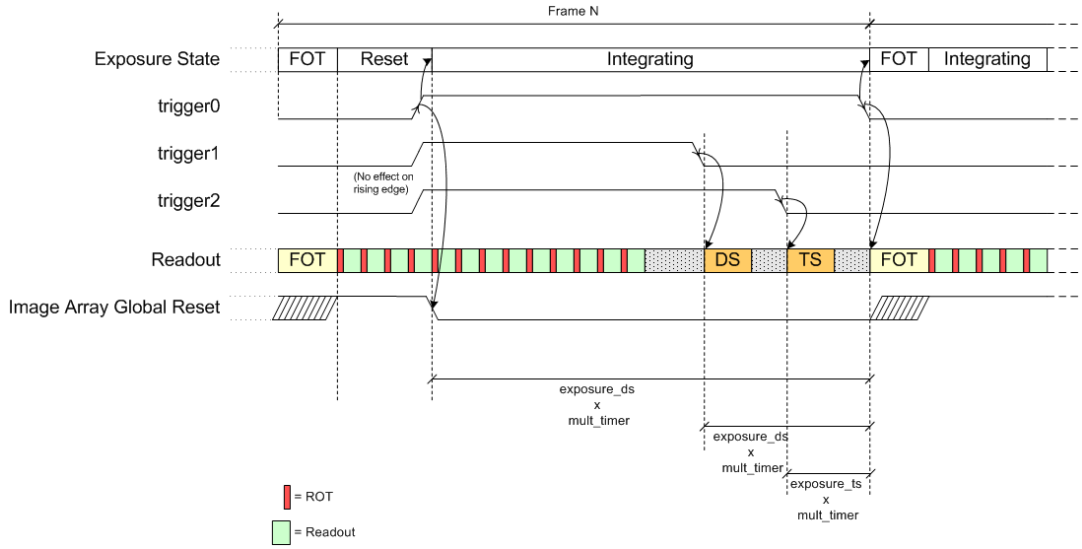


Figure 31. Multiple Slope Operation in Slave Mode

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is minimal equal to 1. The length of the black lines depends on the operation mode. The sensor always reads out the entire line (162 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual output interface, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, however without Frame Start and Ends (only Line Start/End). The Sync code following the Line Start and Line End indications (“window ID”) contains the active window number, which is 0. Black reference data is classified by a BL code.

Signal Path Gain

Analog Gain Stages

Referring to Table 22, two gain settings are available in the analog data path to apply gain to the analog signal before it is digitized.

The moment a gain reconfiguration is applied and becomes valid can be controlled by the gain_lat_comp configuration.

With ‘gain_lat_comp’ set to ‘0’, the new gain configurations are applied from the very next frame.

With ‘gain_lat_comp’ set to ‘1’, the new gain settings are postponed by one extra frame. This feature is useful when exposure time and gain are reconfigured together, as an exposure time update always has one frame latency.

Table 22. SIGNAL PATH GAIN STAGES

(Analog Gain Stages – register 204)

gain_stage1 (mux_gainsw0)	Gain Stage 1	gain_stage2 (afe_gain0)	Gain Stage 2	GAIN Total
0x1	1.00	0xF	1.00	1.00
0x4	1.88	0xF	1.00	1.88

Digital Gain Stage

The digital gain stage allows fine gain adjustments on the digitized samples. The gain configuration is an absolute 5.7 unsigned number (5 digits before and 7 digits after the decimal point).

Automatic Exposure Control

The exposure control mechanism has the shape of a general feedback control system. Figure 32 shows the high level block diagram of the exposure control loop.

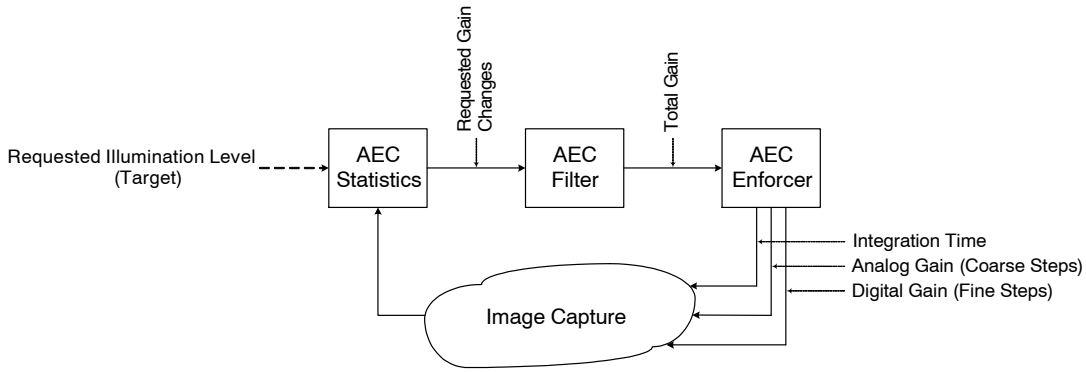


Figure 32. Automatic Exposure Control Loop

Three main blocks can be distinguished:

- The **statistics block** compares the average of the current image's samples to the configured target value for the average illumination of all pixels
- The relative gain change request from the statistics block is filtered through the **AEC Filter block** in the time domain (low pass filter) before being integrated. The output of the filter is the total requested gain in the complete signal path.
- The **enforcer block** accepts the total requested gain and distributes this gain over the integration time and gain stages (both analog and digital)

The automatic exposure control loop is enabled by asserting the aec_enable configuration in register 160.

NOTE: Dual and Triple slope integration is not supported in conjunction with the AEC.

AEC Statistics Block

The statistics block calculates the average illumination of the current image. Based on the difference between the calculated illumination and the target illumination the statistics block requests a relative gain change.

Statistics Subsampling and Windowing

For average calculation, the statistics block will sub−sample the current image or windows by taking every fourth sample into account. Note that only the pixels read out through the active windows are visible for the AEC. In the case where multiple windows are active, the samples will be selected from the total samples. Samples contained in a region covered by multiple (overlapping) window will be taking into account only once.

It is possible to define an AEC specific sub−window on which the AEC will calculate it's average. For instance, the sensor can be configured to read out a larger frame, while the illumination is measured on a smaller region of interest, e.g. center weighted as shown in Table 23.

Table 23. AEC SAMPLE SELECTION

Register	Name	Description
192[10]	roi_aec_enable	When 0x0, all active windows are selected for statistics calculation. When 0x1, the AEC samples are selected from the active pixels contained in the region of interest defined by roi_aec
253−255	roi_aec	These registers define a window from which the AEC samples will be selected when roi_aec_enable is asserted. Configuration is similar to the regular region of interests. The intersection of this window with the active windows define the selected pixels. It is important that this window at least overlaps with one or more active windows.

Target Illumination

The target illumination value is configured by means of register *desired_intensity* as shown in Table 24.

Table 24. AEC TARGET ILLUMINATION CONFIGURATION

Register	Name	Description
161[9:0]	desired_intensity	Target intensity value, on 10−bit scale. For 8−bit mode, target value is configured on desired_intensity[9:2]

Color Sensor

The weight of each color can be configured for color sensors by means of scale factors. Note these scale factor are only used to calculate the statistics in order to compensate for (off−chip) white balancing and/or color matrices. The pixel values itself are not modified.

The scale factors are configured as 3.7 unsigned numbers (0x80 = unity). Refer to Table 25 for color scale factors. For mono sensors, configure these factors to their default value.

Table 25. COLOR SCALE FACTORS

Register	Name	Description
162[9:0]	red_scale_factor	Red scale factor for AEC statistics
163[9:0]	green1_scale_factor	Green1 scale factor for AEC statistics
164[9:0]	green2_scale_factor	Green2 scale factor for AEC statistics
165[9:0]	blue_scale_factor	Blue scale factor for AEC statistics

AEC Filter Block

The filter block low−pass filters the gain change requests received from the statistics block.

The filter can be restarted by asserting the restart_filter configuration of register 160.

AEC Enforcer Block

The enforcer block calculates the four different gain parameters, based on the required total gain, thereby respecting a specific hierarchy in those configurations. Some (digital) hysteresis is added so that the (analog) sensor settings don't need to change too often.

Exposure Control Parameters

The several gain parameters are described below, in the order in which these are controlled by the AEC for large adjustments. Small adjustments are regulated by digital gain only.

- Exposure Time

The exposure is the time between the global image array reset de−assertion and the pixel charge transfer. The granularity of the integration time steps is configured by the *mult_timer* register.

NOTE: The *exposure_time* register is ignored when the AEC is enabled. The register *fr_length* defines the frame time and needs to be configured accordingly.

- Analog Gain

The sensor has two analog gain settings. Typically the AEC shall only regulate the first stage.

- Digital Gain

The last gain stage is a gain applied on the digitized samples. The digital gain is represented by a 5.7 unsigned number (i.e. 7 bits after the decimal point). While the analog gain steps are coarse, the digital gain stage makes it possible to achieve very fine adjustments.

AEC Control Range

The control range for each of the exposure parameters can be pre−programmed in the sensor. Table 26 lists the relevant registers.

Table 26. MINIMUM AND MAXIMUM EXPOSURE CONTROL PARAMETERS

Register	Name	Description
168[15:0]	min_exposure	Lower bound for the integration time applied by the AEC
169[1:0]	min_mux_gain	Lower bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
169[3:2]	min_afe_gain	Lower bound for the second stage analog amplifier. This stage has only one configuration with the following approximative gain: 0x0 = 1.00x
169[15:4]	min_digital_gain	Lower bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format
170[15:0]	max_exposure	Upper bound for the integration time applied by the AEC
171[1:0]	max_mux_gain	Upper bound for the first stage analog amplifier. This stage has two configurations with the following approximative gains: 0x0 = 1x 0x1 = 2x
171[3:2]	max_afe_gain	Upper bound for the second stage analog amplifier This stage has only one configuration with the following approximative gain: 0x0 = 1.00x
171[15:4]	max_digital_ gain	Upper bound for the digital gain stage. This configuration specifies the effective gain in 5.7 unsigned format

AEC Update Frequency

As an integration time update has a latency of one frame, the exposure control parameters are evaluated and updated every other frame.

Note: The gain update latency must be postpone to match the integration time latency. This is done by asserting the *gain_lat_comp* register on address 204[13].

Exposure Control Status Registers

Configured integration and gain parameters are reported to the user by means of status registers. The sensor provides two levels of reporting: the status registers reported in the AEC address space are updated once the parameters are recalculated and requested to the internal sequencer. The status registers residing in the sequencer's address space on the other hand are updated once these parameters are taking effect on the image readout. Refer to Table 27 reflecting the AEC and Sequencer Status registers.

Table 27. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
AEC Status Registers		
184[15:0]	total_pixels	Total number of pixels taken into account for the AEC statistics.
186[9:0]	average	Calculated average illumination level for the current frame.
187[15:0]	exposure	AEC calculated exposure. Note: this parameter is updated at the frame end.
188[1:0]	mux_gain	AEC calculated analog gain (1^{st} stage) Note: this parameter is updated at the frame end.
188[3:2]	afe_gain	AEC calculated analog gain (2^{st} stage) Note: this parameter is updated at the frame end.
188[15:4]	digital_gain	AEC calculated digital gain (5.7 unsigned format) Note: this parameter is updated at the frame end.

Table 27. EXPOSURE CONTROL STATUS REGISTERS

Register	Name	Description
Sequencer Status Registers		
242[15:0]	mult_timer	mult_timer for current frame Note: this parameter is updated once it takes effect on the image.
243[15:0]	reset_length	Image array reset length for the current frame. Note: this parameter is updated once it takes effect on the image.
244[15:0]	exposure	Exposure for the current frame. Note: this parameter is updated once it takes effect on the image.
245[15:0]	exposure_ds	Dual slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
246[15:0]	exposure_ts	Triple slope exposure for the current frame. Note this parameter is not controlled by the AEC. Note: this parameter is updated once it takes effect on the image.
247[4:0]	mux_gainsw	1st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
247[12:5]	afe_gain	2st stage analog gain for the current frame. Note: this parameter is updated once it takes effect on the image.
248[11:0]	db_gain	Digital gain configuration for the current frame (5.7 unsigned format). Note: this parameter is updated once it takes effect on the image.
248[12]	dual_slope	Dual slope configuration for the current frame **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.
248[13]	triple_slope	Triple slope configuration for the current frame. **Note 1**: this parameter is updated once it takes effect on the image. **Note 2**: This parameter is not controlled by the AEC.

Temperature Sensor

The PYTHON has an on−chip temperature sensor which returns a digital code (Tsensor) of the silicon junction temperature. The Tsensor output is a 8−bit digital count between 0 and 255, proportional to the temperature of the silicon substrate. This reading can be translated directly to a temperature reading in °C by calibrating the 8−bit readout at 0°C and 85°C to achieve an output accuracy of ±2°C. The Tsensor output can also be calibrated using a single temperature point (example: room temperature or the ambient temperature of the application), to achieve an output accuracy of ±5°C.

Note that any process variation will result in an offset in the bit count and that offset will remain within ±5°C over the temperature range of 0°C and 85°C. Tsensor output digital code can be read out through the SPI interface.

Output of the temperature sensor to the SPI:

tempd_reg_temp<7:0>: This is the 8−bit N count readout proportional to temperature.

Input from the SPI:

The *reg_tempd_enable* is a global enable and this enables or disables the temperature sensor when logic high or logic low respectively. The temperature sensor is reset or disabled when the input *reg_tempd_enable* is set to a digital low state.

Calibration using one temperature point

The temperature sensor resolution is fixed for a given type of package for the operating range of 0°C to +85°C and hence devices can be calibrated at any ambient temperature of the application, with the device configured in the mode of operation.

Interpreting the actual temperature for the digital code readout:

The formula used is

T_J = R (Nread − Ncalib) + Tcalib

T_J = junction die temperature

R = resolution in degrees/LSB (typical 0.75 deg/LSB)

Nread = Tsensor output (LSB count between 0 and 255)

Tcalib = Tsensor calibration temperature

Ncalib = Tsensor output reading at Tcalib

Monitor Pins

The internal sequencer has two monitor outputs (monitor0 and monitor1) that can be used to communicate the internal states from the sequencer. A three−bit register configures the assignment of the pins as shown in Table 28.

Table 28. REGISTER SETTING FOR THE MONITOR SELECT PIN

monitor_select [2:0] 192 [13:11]	monitor pin	Description
0x0	monitor0 monitor1	‘0’ ‘0’
0x1	monitor0 monitor1	Integration Time ROT Indication (‘1’ during ROT, ‘0’ outside)
0x2	monitor0 monitor1	Integration Time Dual/Triple Slope Integration (asserted during DS/TS FOT sequence)
0x3	monitor0 monitor1	Start of x−Readout Indication Black Line Indication (‘1’ during black lines, ‘0’ outside)
0x4	monitor0 monitor1	Frame Start Indication Start of ROT Indication
0x5	monitor0 monitor1	First Line Indication (‘1’ during first line, ‘0’ for all others) Start of ROT Indication
0x6	monitor0 monitor1	ROT Indication (‘1’ during ROT, ‘0’ outside) Start of X−Readout Indication
0x7	monitor0 monitor1	Start of X−readout Indication for Black Lines Start of X−readout Indication for Image Lines

DATA OUTPUT FORMAT

P1−SN/SE: LVDS Interface Version

The P1−SN/SE has eight LVDS output channels, together with an LVDS clock and an LVDS synchronization output channel.

LVDS Output Channels

The image data output occurs through eight LVDS data channels where a synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The eight data channels are used to output the image data only. The sync channel transmits information about the data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC codes).

8−bit / 10−bit Mode

The sensor can be used in 8−bit or 10−bit mode.

In 10−bit mode, the words on data and sync channel have a 10−bit length. The output data rate is 720 Mbps.

In 8−bit mode, the words on data and sync channel have an 8−bit length, the output data rate is 576 Mbps.

Note that the 8−bit mode can only be used to limit the data rate at the consequence of image data word depth. It is not supported to operate the sensor in 8−bit mode at a higher clock frequency to achieve higher frame rates.

Frame Format

The frame format in 8−bit mode is identical to the 10−bit mode with the exception that the Sync and data word depth is reduced to eight bits.

The frame format in 10−bit mode is explained by example of the readout of two (overlapping) windows as shown in Figure 33(a).

The readout of a frame occurs on a line−by−line basis. The read pointer goes from left to right, bottom to top.

Figure 33 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes information of ‘ROI 0’ are sent out, starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of ‘ROI 0’ and ‘ROI 1’ are sent out, until the line position of y0_end is reached. From there on, only data of ‘ROI 1’ appears on the data output channels until line position y1_end is reached

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the four data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS); the line end of the last line is replaced with a Frame End indication (FE). Each such frame synchronization code is followed by a window ID (range 0 to 7). For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out (as shown in the illustration: no LE/FE is transmitted for the overlapping part of window 0).

NOTES: In Figure 33, only Frame Start and Frame End Sync words are indicated in (b). CRC codes are also omitted from the figure.

For additional information on the synchronization codes, please refer to Application Note AND5001.

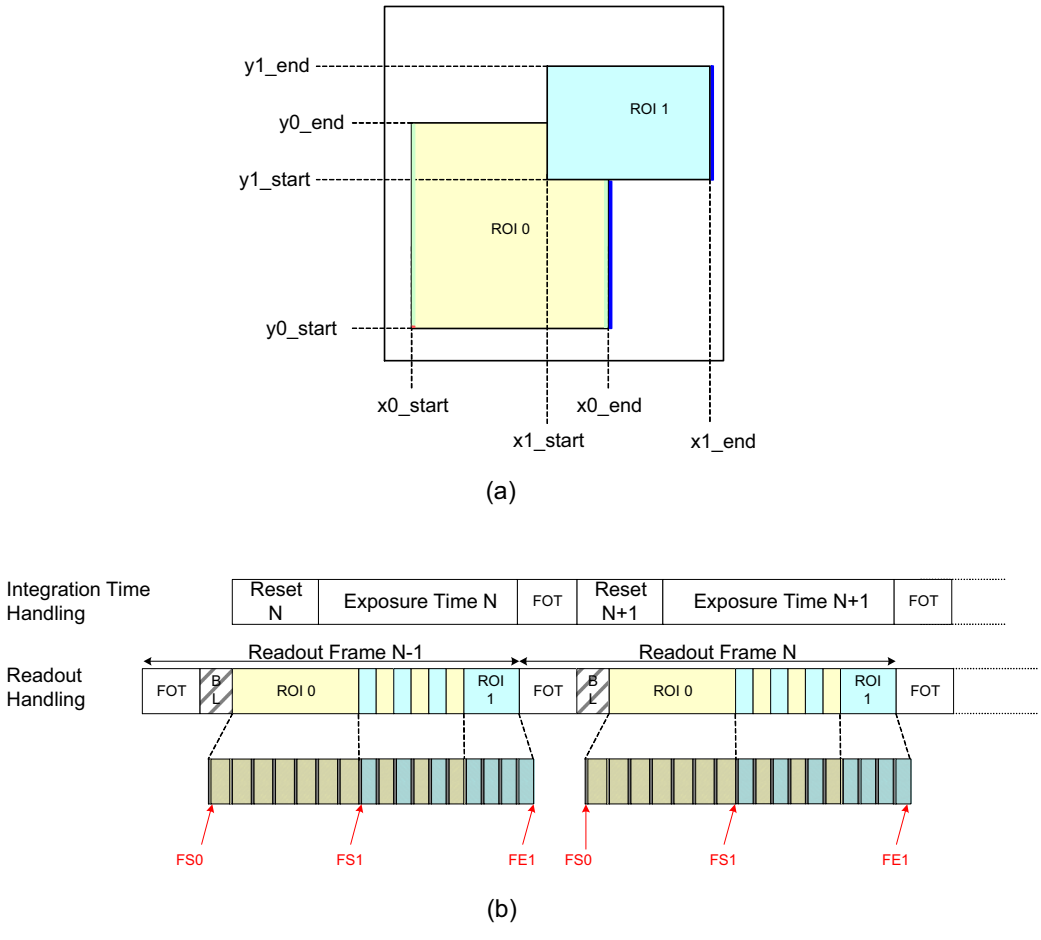


Figure 33. Frame Sync Codes

Figure 34 shows the detail of a black line readout during global or full−frame readout.

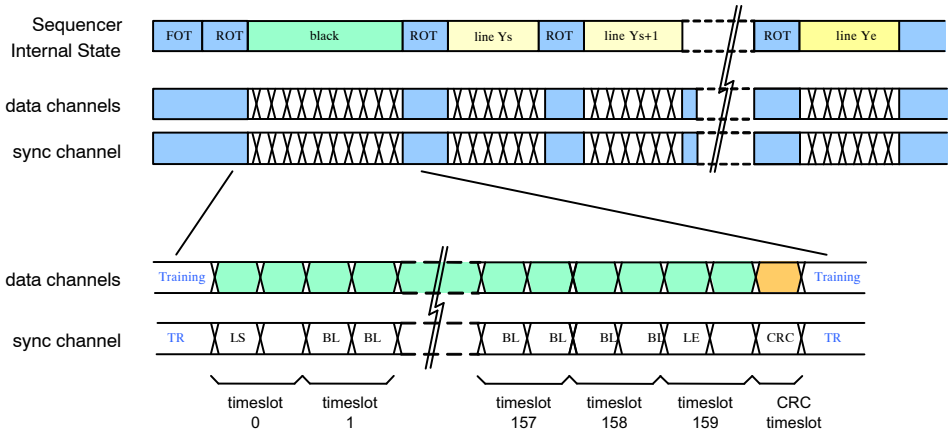


Figure 34. Time Line for Black Line Readout

Figure 35 shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.

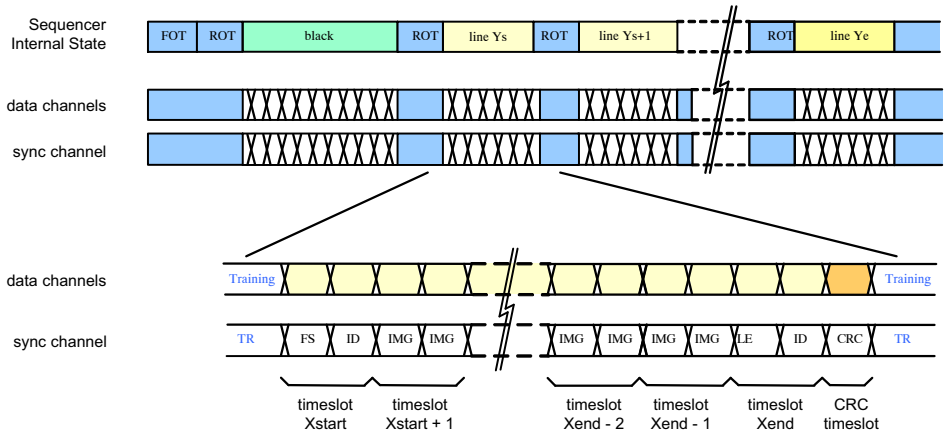


Figure 35. Time Line for Single Window Readout (at the start of a frame)

Figure 36 shows the detail of the readout of a number of lines for readout of two overlapping windows.

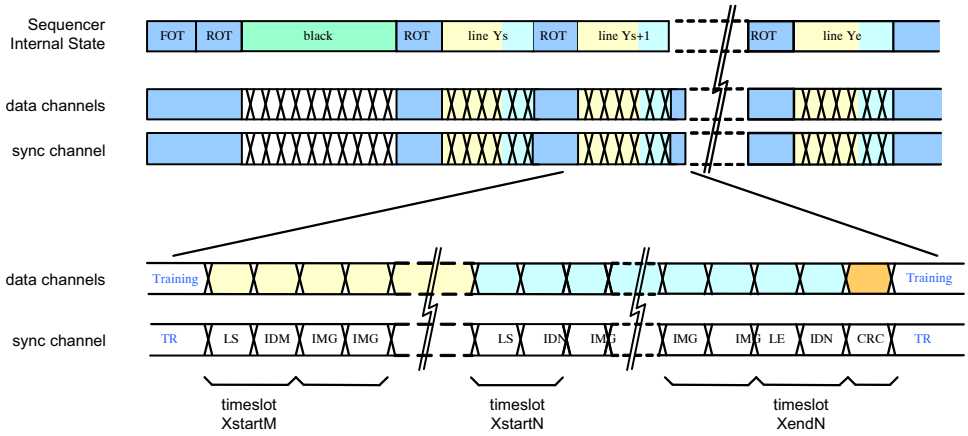


Figure 36. Time Line Showing the Readout of Two Overlapping Windows

Frame Synchronization for 10−bit Mode

Table 29 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable) for 10−bit mode. If more than one window is active at the same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 29. FRAME SYNCHRONIZATION CODE DETAILS FOR 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:7	N/A	0x5	Frame start (FS) indication
9:7	N/A	0x6	Frame end (FE) indication
9:7	N/A	0x1	Line start (LS) indication
9:7	N/A	0x2	Line end (LE) indication
6:0	117[6:0]	0x2A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting

Window Identification

Frame synchronization codes are always followed by a 4−bit window identification (bits 3:0). This is an integer number, ranging from 0 to 15, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 30.

Table 30. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:0	118 [9:0]	0x015	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
9:0	119 [9:0]	0x035	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
9:0	125 [9:0]	0x059	CRC value. The data on the data output channels is the CRC code of the finished image data line.
9:0	126 [9:0]	0x3A6	Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Frame Synchronization in 8−bit Mode

The frame synchronization words are configured using the same registers as in 10−bit mode. The two least significant bits of these configuration registers are ignored and not sent out. Table 32 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8−bit mode.

Table 31. FRAME SYNCHRONIZATION CODE DETAILS FOR 8−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:5	N/A	0x5	Frame start (FS) indication
7:5	N/A	0x6	Frame end (FE) indication
7:5	N/A	0x1	Line start (LS) indication
7:5	N/A	0x2	Line end (LE) indication
4:0	117 [6:2]	0x0A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting.

Window Identification

Similar to 10−bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 5:2 (all other bit positions are ‘0’). The same restriction for overlapping windows applies in 8−bit mode.

Data Classification Codes

BL, IMG, CRC, and TR codes are defined by the same registers as in 10−bit mode. Bits 9:2 of the respective configuration registers are used as classification code with default values shown in Table 32.

Table 32. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 8−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:0	118 [9:2]	0x05	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
7:0	119 [9:2]	0x0D	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
7:0	125 [9:2]	0x16	CRC value. The data on the data output channels is the CRC code of the finished image data line.
7:0	126 [9:2]	0xE9	Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Training Patterns on Data Channels

In 10−bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable independent of the training code on the sync channel as shown in Table 33.

Table 33. TRAINING CODE ON SYNC CHANNEL IN 10−BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
[9:0]	116 [9:0]	0x3A6	Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel.

In 8−bit mode, the training pattern for the data channels is defined by the same register as in 10−bit mode, where the lower two bits are omitted; see Table 34.

Table 34. TRAINING PATTERN ON DATA CHANNEL IN 8−BIT MODE

Data Word Bit Position	Register Address	Default Value	Description
[7:0]	116 [9:2]	0xE9	Data Channel Training Pattern (Training pattern).

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10−bit operation mode is $x^{10} + x^9 + x^6 + x^3 + x^2 + x + 1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the crc_seed register. When ‘0’, the CRC is seeded by all−‘0’; when ‘1’ it is seeded with all−‘1’.

In 8−bit mode, the polynomial is $x^8 + x^6 + x^3 + x^2 + 1$. The CRC seed is configured by means of the crc_seed register.

NOTE: The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

Data Order for P1−SN/SE Version

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is sixteen pixels in x−direction by one pixel in y−direction. The data order in 8−bit mode is identical to the 10−bit mode. Figure 37 indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner. The data order of this image data on the data output channels depends on the subsampling mode.

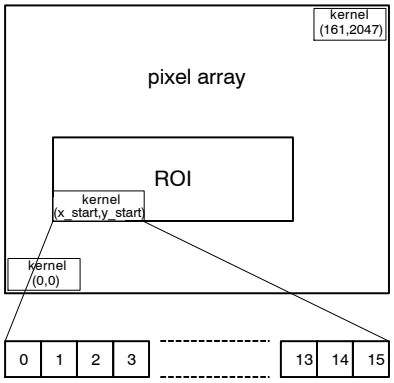


Figure 37. Kernel Organization in Pixel Array

- P1−SN/SE: Subsampling Disabled
  - 8 LVDS Output Channels

The image data is read out in kernels of 16 pixels in x−direction by one pixel in y−direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 38 shows how a kernel is read out over the eight output channels. For even positioned kernels, the kernels are read out ascending, while for odd positioned kernels the data order is reversed (descending).

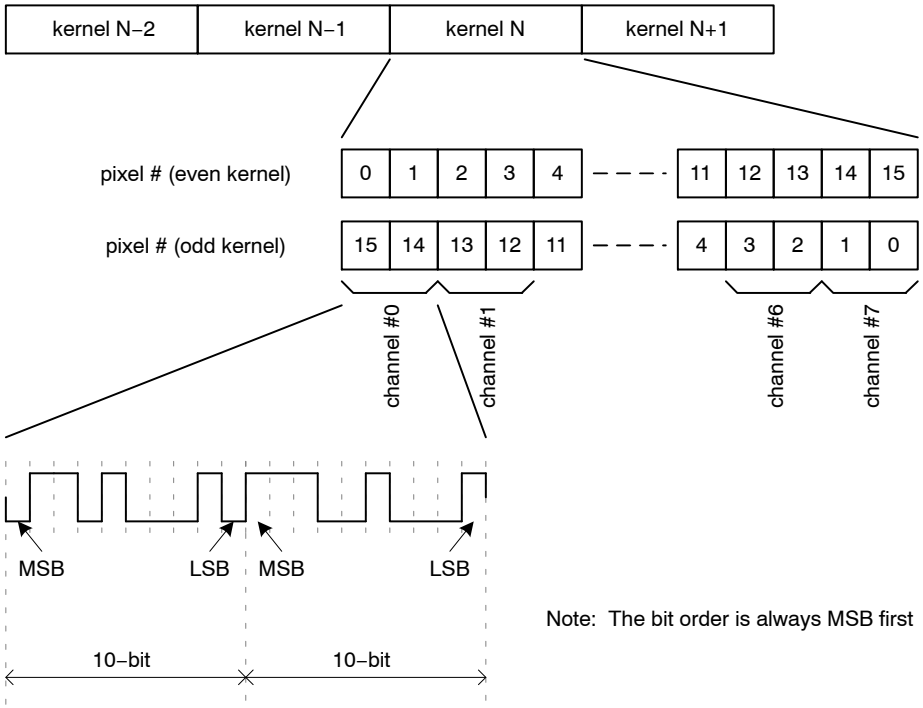


Figure 38. 8 LVDS Data Output Order when Subsampling is Disabled

♦ 4 LVDS Output Channels

Figure 39 shows how a kernel is read out over the four output channels. For even positioned kernels, the kernels are read out ascending but in pair of even and odd pixels, while for odd positioned kernels, the data order is reversed (descending – in pair of even and odd pixels).

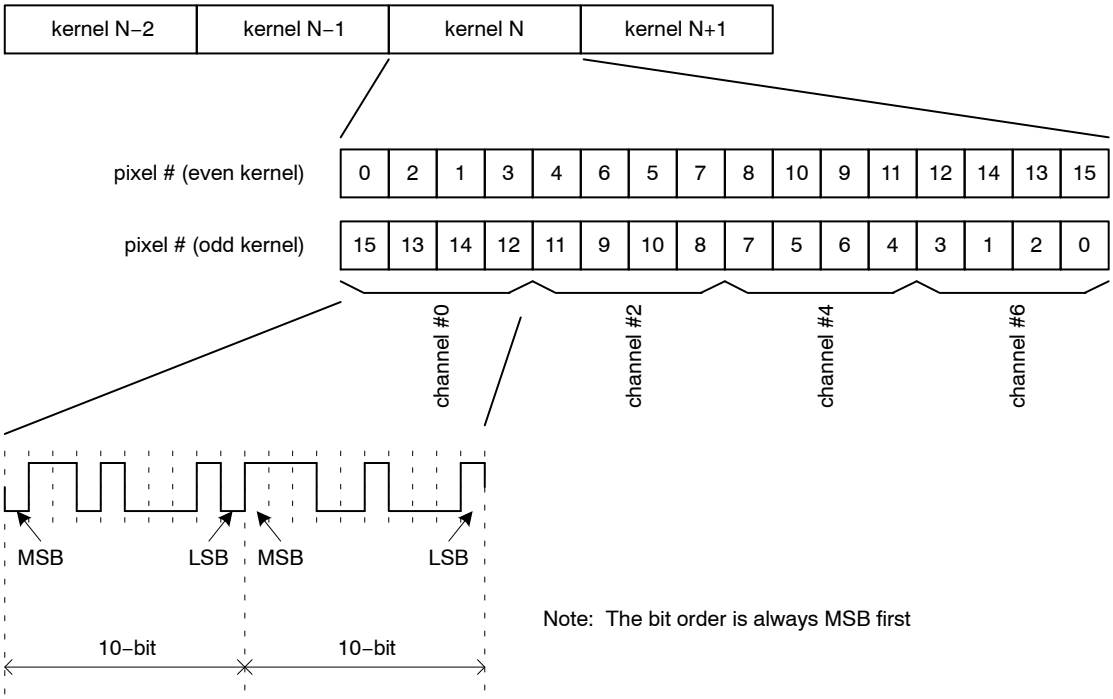


Figure 39. 4 LVDS Data Output Order when Subsampling is Disabled

♦ 2 LVDS Output Channels

Figure 40 shows how a kernel is read out over 2 output channels. Each group of four adjacent channels is multiplexed on to one channel. For even positioned kernels, the kernels are read out in an ascending order but in sets of four even and four odd pixels, while for odd positioned kernels the data order is reversed (descending and in sets of four odd and four even pixels).

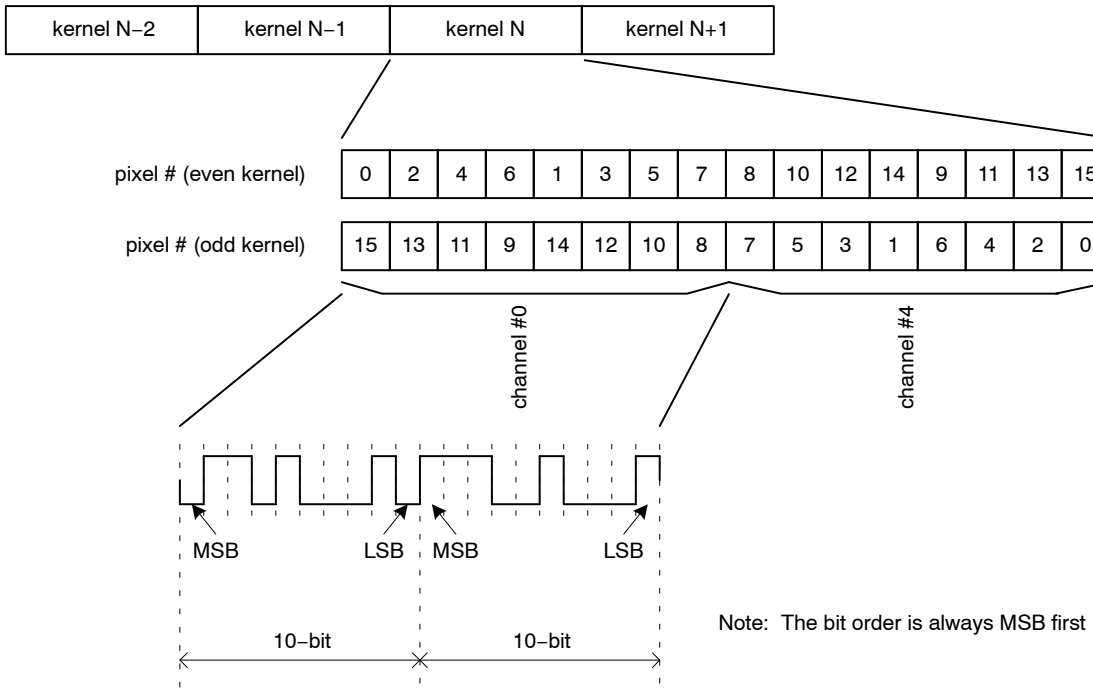


Figure 40. 2 LVDS Data Output Order when Subsampling is Disabled

♦ 1 LVDS Output Channel

Figure 41 shows how a kernel is read out over 1 output channel. Eight adjacent channels are multiplexed into one channel. For even positioned kernels, the kernels are read out ascending but in sets of 8 even and 8 odd pixels, while for odd positioned kernels the data order is reversed (descending – in sets of 8 odd and 8 even pixels).

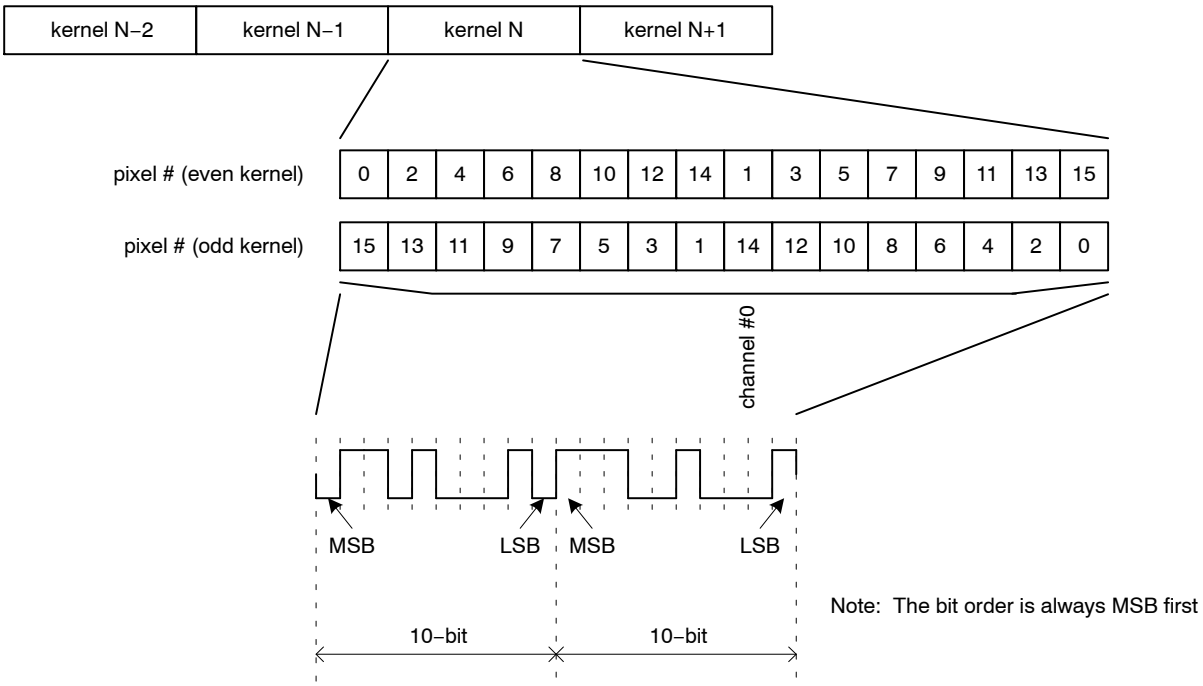


Figure 41. 1 LVDS Data Output Order when Subsampling is Disabled

• Subsampling on Monochrome Sensor

During subsampling on a monochrome sensor, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 32 pixels in the x−direction and one pixel in the y−direction. Only the pixels at the even pixel positions inside that kernel are read out.

♦ 8 LVDS Output Channels

Figure 42 shows the data order for 8 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

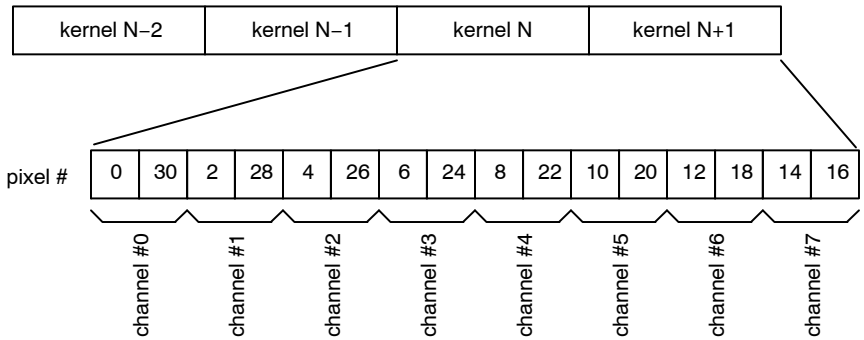


Figure 42. Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

♦ 4 LVDS Output Channels

Figure 43 shows the data order for 4 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

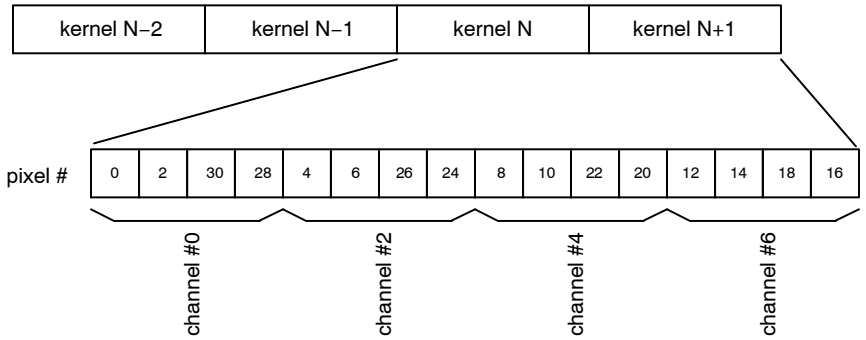


Figure 43. Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

♦ 2 LVDS Output Channels

Figure 44 shows the data order for 2 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

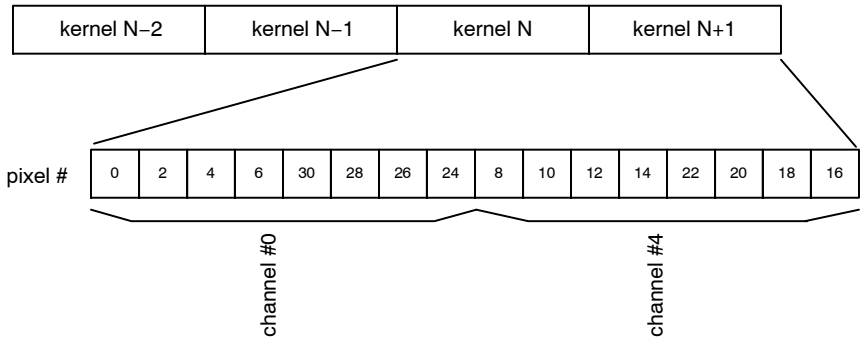


Figure 44. Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

♦ 1 LVDS Output Channel

Figure 45 shows the data order for 1 LVDS output channel. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

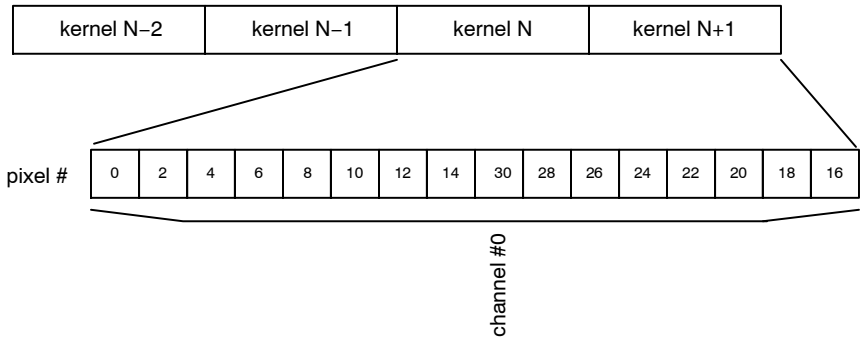


Figure 45. Data Output Order for 1 LVDS Output Channels in Subsampling Mode on a Monochrome Sensor

- Binning on Monochrome Sensor

The output order in binning mode is identical to the subsampled mode.

- Subsampling on Color Sensor

During subsampling on a color sensor, lines are read in a read-2-skip−2 manner. To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x−direction and one pixel in the y−direction. Only the pixels 0, 1, 4, 5, 8, 9, … 28, 29 are read out.

♦ 8 LVDS Output Channels

Figure 46 shows the data order for 8 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

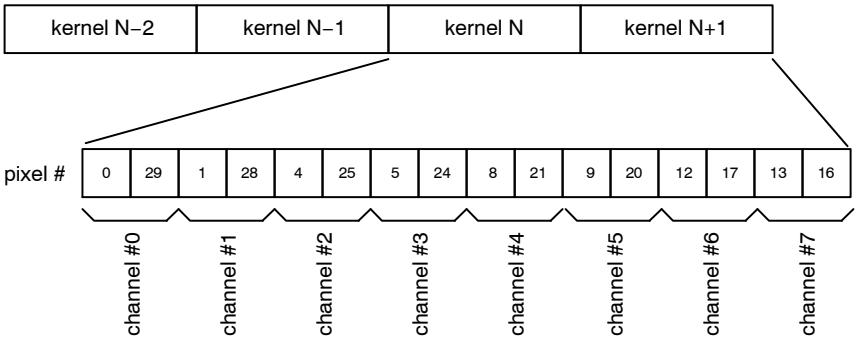


Figure 46. Data Output Order for 8 LVDS Output Channels in Subsampling Mode on a Color Sensor

♦ 4 LVDS Output Channels

Figure 47 shows the data order for 4 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

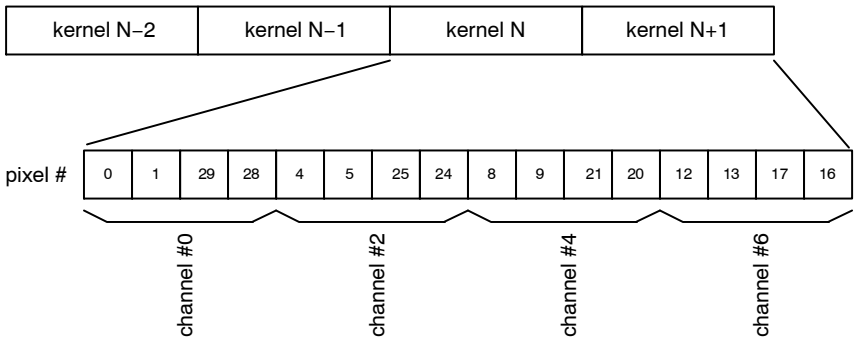


Figure 47. Data Output Order for 4 LVDS Output Channels in Subsampling Mode on a Color Sensor

♦ 2 LVDS Output Channels

Figure 48 shows the data order for 2 LVDS output channels. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

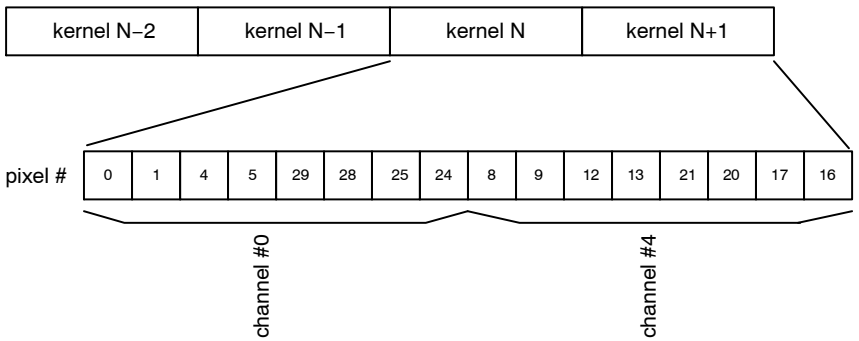


Figure 48. Data Output Order for 2 LVDS Output Channels in Subsampling Mode on a Color Sensor

♦ 1 LVDS Output Channel

Figure 49 shows the data order for 1 LVDS output channel. Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout described in previous section.

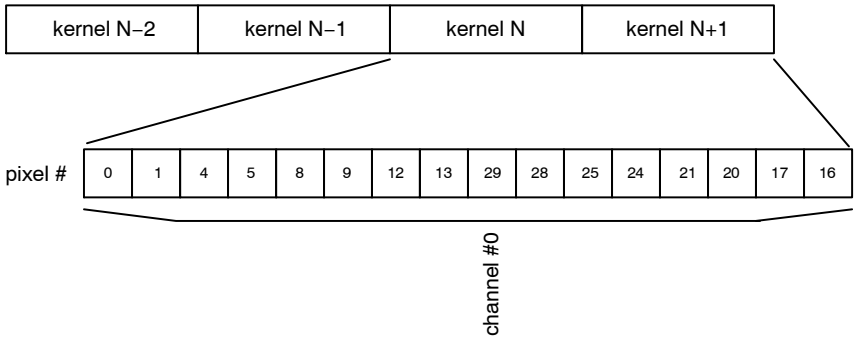


Figure 49. Data Output Order for 1 LVDS Output Channel in Subsampling Mode on a Color Sensor

REGISTER MAP

The table below represents the register map for the NOIP1xx5000A part. Deviating default values for the NOIP1xx2000A sensor are mentioned between brackets (“[ ]”).

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
Chip ID [Block Offset: 0]							
0	0		chip_id	0x5032	20530	Chip ID	Status
		[15:0]	id	0x5032	20530	Chip ID	
1	1		reserved	0x0001 [0x0101]	1 [257]	Reserved	Status
		[3:0]	reserved	0x1	1	Reserved	
		[9:8]	resolution	0x0 [0x1]	0 [1]	Sensor Resolution ‘0’: NOIP1xx5000A ‘1’: NOIP1xx2000A	
		[11:10]	reserved	0x0	0	Reserved	
2	2		chip_configuration	0x0000	0	Chip General Configuration	RW
		[0]	color	0x0	0	Colour/Monochrome Configuration ‘0’: Monochrome ‘1’: Color	
		[3:2]	glob_config	0x0	0	Sensor pinout configuration	
		[15:4]	reserved	0x000	0	Reserved	
Reset Generator [Block Offset: 8]							
0	8		soft_reset_pll	0x0099	153	PLL Soft Reset Configuration	RW
		[3:0]	pll_soft_reset	0x9	9	PLL Reset 0x9: Soft Reset State others: Operational	
		[7:4]	pll_lock_soft_reset	0x9	9	PLL Lock Detect Reset 0x9: Soft Reset State others: Operational	
1	9		soft_reset_cgen	0x0009	9	Clock Generator Soft Reset	RW
		[3:0]	cgen_soft_reset	0x9	9	Clock Generator Reset 0x9: Soft Reset State others: Operational	
2	10		soft_reset_analog	0x0999	2457	Analog Block Soft Reset	RW
		[3:0]	mux_soft_reset	0x9	9	Column MUX Reset 0x9: Soft Reset State others: Operational	
		[7:4]	afe_soft_reset	0x9	9	AFE Reset 0x9: Soft Reset State others: Operational	
		[11:8]	ser_soft_reset	0x9	9	Serializer Reset 0x9: Soft Reset State others: Operational	
PLL [Block Offset: 16]							
0	16		power_down	0x0004	4	PLL Configuration	RW
		[0]	pwd_n	0x0	0	PLL Power Down ‘0’: Power Down, ‘1’: Operational	
		[1]	enable	0x0	0	PLL Enable ‘0’: disabled, ‘1’: enabled	
		[2]	bypass	0x1	1	PLL Bypass ‘0’: PLL Active, ‘1’: PLL Bypassed	
1	17		reserved	0x2113	8467	Reserved	RW
		[7:0]	reserved	0x13	19	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[12:8]	reserved	0x1	1	Reserved	
		[14:13]	reserved	0x1	1	Reserved	
I/O [Block Offset: 20]							
0	20		config1	0x0000	0	IO Configuration	RW
		[0]	clock_in_pwd_n	0x0	0	Power down Clock Input	
		[9:8]	reserved	0x0	0	Reserved	
		[10]	reserved	0x0	0	Reserved	
PLL Lock Detector [Block Offset: 24]							
0	24		pll_lock	0x0000	0	PLL Lock Indication	Status
		[0]	lock	0x0	0	PLL Lock Indication	
2	26		reserved	0x2280	8832	Reserved	RW
		[7:0]	reserved	0x80	128	Reserved	
		[10:8]	reserved	0x2	2	Reserved	
		[14:12]	reserved	0x2	2	Reserved	
3	27		reserved	0x3D2D	15661	Reserved	RW
		[7:0]	reserved	0x2D	45	Reserved	
		[15:8]	reserved	0x3D	61	Reserved	
Clock Generator [Block Offset: 32]							
0	32		config0	0x0004	4	Clock Generator Configuration	RW
		[0]	enable_analog	0x0	0	Enable analogue clocks ‘0’: disabled, ‘1’: enabled	
		[1]	enable_log	0x0	0	Enable logic clock ‘0’: disabled, ‘1’: enabled	
		[2]	select_pll	0x1	1	Input Clock Selection ‘0’: Select LVDS clock input, ‘1’: Select PLL clock input	
		[3]	adc_mode	0x0	0	Set operation mode of CGEN block ‘0’: divide by 5 mode (10−bit mode), ‘1’: divide by 4 mode (8−bit mode)	
		[5:4]	mux	0x0	0	Multiplex Mode	
		[11:8]	reserved	0x0	0	Reserved	
		[14:12]	reserved	0x0	0	Reserved	
General Logic [Block Offset: 34]							
0	34		config0	0x0000	0	Clock Generator Configuration	RW
		[0]	enable	0x0	0	Logic General Enable Configuration ‘0’: Disable ‘1’: Enable	
0	38		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
1	39		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
Image Core [Block Offset: 40]							
0	40		image_core_config0	0x0000	0	Image Core Configuration	RW
		[0]	imc_pwd_n	0x0	0	Image Core Power Down ‘0’: powered down, ‘1’: powered up	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[1]	mux_pwd_n	0x0	0	Column Multiplexer Power Down ‘0’: powered down, ‘1’: powered up	
		[2]	colbias_enable	0x0	0	Bias Enable ‘0’: disabled ‘1’: enabled	
1	41		image_core_config1	0x0B5A	2906	Image Core Configuration	RW
		[3:0]	dac_ds	0xA	10	Double Slope Reset Level	
		[7:4]	dac_ts	0x5	5	Triple Slope Reset Level	
		[10:8]	reserved	0x3	3	Reserved	
		[12:11]	reserved	0x1	1	Reserved	
		[13]	reserved	0x0	0	Reserved	
		[14]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	
2	42		reserved	0x0001	1	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x0	0	Reserved	
		[6:4]	reserved	0x0	0	Reserved	
		[10:8]	reserved	0x0	0	Reserved	
		[15:12]	reserved	0x0	0	Reserved	
3	43		reserved	0x0000	0	Reserved	RW
		[0]	reserved	0x0	0	Reserved	
		[1]	reserved	0x0	0	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[6:4]	reserved	0x0	0	Reserved	
		[7]	reserved	0x0	0	Reserved	
		[15:8]	reserved	0x0	0	Reserved	
AFE [Block Offset: 48]							
0	48		power_down	0x0000	0	AFE Configuration	RW
		[0]	pwd_n	0x0	0	Power down for AFE’s ‘0’: powered down, ‘1’: powered up	
Bias [Block Offset: 64]							
0	64		power_down	0x0000	0	Bias Power Down Configuration	RW
		[0]	pwd_n	0x0	0	Power down bandgap ‘0’: powered down, ‘1’: powered up	
1	65		configuration	0x888B	34955	Bias Configuration	RW
		[0]	extres	0x1	1	External Resistor Selection ‘0’: internal resistor, ‘1’: external resistor	
		[3:1]	reserved	0x5	5	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
2	66		reserved	0x53C8	21448	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0xC	12	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[14:8]	reserved	0x53	83	Reserved	
3	67		reserved	0x8888	34952	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
4	68		lvds_bias	0x0088	136	LVDS Bias Configuration	RW
		[3:0]	lvds_ibias	0x8	8	LVDS Ibias	
		[7:4]	lvds_iref	0x8	8	LVDS Iref	
5	69		reserved	0x0888	2184	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
6	70		reserved	0x8888	34952	Reserved	RW
		[3:0]	reserved	0x8	8	Reserved	
		[7:4]	reserved	0x8	8	Reserved	
		[11:8]	reserved	0x8	8	Reserved	
		[15:12]	reserved	0x8	8	Reserved	
7	71		reserved	0x8888	34952	Reserved	RW
		[15:0]	reserved	0x8888	34952	Reserved	
Charge Pump [Block Offset: 72]							
0	72		configuration	0x2220	8736	Charge Pump Configuration	RW
		[0]	trans_pwd_n	0x0	0	PD Trans Charge Pump Enable ‘0’: disabled, ‘1’: enabled	
		[1]	resfd_calib_pwd_n	0x0	0	FD Charge Pump Enable ‘0’: disabled, ‘1’: enabled	
		[2]	sel_sample_pwd_n	0x0	0	Select/Sample Charge Pump Enable ‘0’: disabled ‘1’: enabled	
		[6:4]	reserved	0x2	2	Reserved	
		[10:8]	reserved	0x2	2	Reserved	
		[14:12]	reserved	0x2	2	Reserved	
Charge Pump [Block Offset: 80]							
0	80		reserved	0x0000	0	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[3:2]	reserved	0x0	0	Reserved	
		[5:4]	reserved	0x0	0	Reserved	
		[7:6]	reserved	0x0	0	Reserved	
		[9:8]	reserved	0x0	0	Reserved	
1	81		reserved	0x8881	34945	Reserved	RW
		[15:0]	reserved	0x8881	34945	Reserved	
Temperature Sensor [Block Offset: 96]							
0	96		enable	0x0000	0	Temperature Sensor Configuration	RW
		[0]	enable	0x0	0	Temperature Diode Enable ‘0’: disabled, ‘1’: enabled	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[1]	reserved	0x0	0	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[4]	reserved	0x0	0	Reserved	
		[5]	reserved	0x0	0	Reserved	
		[13:8]	offset	0x0	0	Temperature Offset (signed)	
1	97		temp	0x0000	0	Temperature Sensor Status	Status
		[7:0]	temp	0x00	0	Temperature Readout	
Temperature Sensor [Block Offset: 104]							
0	104		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0	0	Reserved	
1	105		reserved	0x0000	0	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[6:2]	reserved	0x0	0	Reserved	
		[7]	reserved	0x0	0	Reserved	
		[9:8]	reserved	0x0	0	Reserved	
		[14:10]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	
2	106		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
3	107		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
4	108		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
5	109		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
6	110		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
7	111		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
Serializers / LVDS / IO [Block Offset: 112]							
0	112		power_down	0x0000	0	LVDS Power Down Configuration	RW
		[0]	clock_out_pwd_n	0x0	0	Power down for Clock Output. ‘0’: powered down, ‘1’: powered up	
		[1]	sync_pwd_n	0x0	0	Power down for Sync channel ‘0’: powered down, ‘1’: powered up	
		[2]	data_pwd_n	0x0	0	Power down for data channels (4 channels) ‘0’: powered down, ‘1’: powered up	
Sync Words [Block Offset: 116]							
4	116		trainingpattern	0x03A6	934	Data Formating – Training Pattern	RW
		[9:0]	trainingpattern	0x3A6	934	Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels.	
5	117		sync_code0	0x002A	42	LVDS Power Down Configuration	RW
		[6:0]	frame_sync_0	0x02A	42	Frame Sync Code LSBs – Even kernels	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
6	118		sync_code1	0x0015	21	Data Formating – BL Indication	RW
		[9:0]	bl_0	0x015	21	Black Pixel Identification Sync Code – Even kernels	
7	119		sync_code2	0x0035	53	Data Formating – IMG Indication	RW
		[9:0]	img_0	0x035	53	Valid Pixel Identification Sync Code – Even kernels	
8	120		sync_code3	0x0025	37	Data Formating – IMG Indication	RW
		[9:0]	ref_0	0x025	37	Reference Pixel Identification Sync Code – Even kernels	
9	121		sync_code4	0x002A	42	LVDS Power Down Configuration	RW
		[6:0]	frame_sync_1	0x02A	42	Frame Sync Code LSBs – Odd kernels	
10	122		sync_code5	0x0015	21	Data Formating – BL Indication	RW
		[9:0]	bl_1	0x015	21	Black Pixel Identification Sync Code – Odd kernels	
11	123		sync_code6	0x0035	53	Data Formating – IMG Indication	RW
		[9:0]	img_1	0x035	53	Valid Pixel Identification Sync Code – Odd kernels	
12	124		sync_code7	0x0025	37	Data Formating – IMG Indication	RW
		[9:0]	ref_1	0x025	37	Reference Pixel Identification Sync Code – Odd kernels	
13	125		sync_code8	0x0059	89	Data Formating – CRC Indication	RW
		[9:0]	crc	0x059	89	CRC Value Identification Sync Code	
14	126		sync_code9	0x03A6	934	Data Formating – TR Indication	RW
		[9:0]	tr	0x3A6	934	Training Value Identification Sync Code	
15	127		reserved	0x02AA	682	Reserved	RW
		[9:0]	reserved	0x2AA	682	Reserved	
Data Block [Block Offset: 128]							
0	128		blackcal	0x4008	16392	Black Calibration Configuration	RW
		[7:0]	black_offset	0x08	8	Desired black level at output	
		[10:8]	black_samples	0x0	0	Black pixels taken into account for black calibration. Total samples = 2**black_samples	
		[14:11]	reserved	0x8	8	Reserved	
		[15]	crc_seed	0x0	0	CRC Seed ‘0’: All−0 ‘1’: All−1	
1	129		general_configuration	0x0001	1	Black Calibration and Data Formating Configuration	RW
		[0]	auto_blackcal_enable	0x1	1	Automatic blackcalibration is enabled when 1, bypassed when 0	
		[9:1]	blackcal_offset	0x00	0	Black Calibration offset used when auto_black_cal_en = ‘0’.	
		[10]	blackcal_offset_dec	0x0	0	blackcal_offset is added when 0, subtracted when 1	
		[11]	reserved	0x0	0	Reserved	
		[12]	reserved	0x0	0	Reserved	
		[13]	8bit_mode	0x0	0	Shifts window ID indications by 4 cycles. ‘0’: 10 bit mode, ‘1’: 8 bit mode	
		[14]	ref_mode	0x0	0	Data contained on reference lines: ‘0’: reference pixels ‘1’: black average for the corresponding data channel	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15]	ref_bcal_enable	0x0	0	Enable black calibration on reference lines ‘0’: Disabled ‘1’: Enabled	
2	130		reserved	0x000F	15	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x1	1	Reserved	
		[2]	reserved	0x1	1	Reserved	
		[3]	reserved	0x1	1	Reserved	
		[4]	reserved	0x0	0	Reserved	
		[8]	reserved	0x0	0	Reserved	
8	136		blackcal_error0	0x0000	0	Black Calibration Status	Status
		[15:0]	blackcal_error[15:0]	0x0000	0	Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0−16	
9	137		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
10	138		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
11	139		reserved	0x0000	0	Reserved	Status
		[15:0]	reserved	0x0000	0	Reserved	
12	140		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
13	141		reserved	0xFFFF	65535	Reserved	RW
		[15:0]	reserved	0xFFFF	65535	Reserved	
16	144		test_configuration	0x0000	0	Data Formating Test Configuration	RW
		[0]	testpattern_en	0x0	0	Insert synthesized testpattern when ‘1’	
		[1]	inc_testpattern	0x0	0	Incrementing testpattern when ‘1’, constant testpattern when ‘0’	
		[2]	prbs_en	0x0	0	Insert PRBS when ‘1’	
		[3]	frame_testpattern	0x0	0	Frame test patterns when ‘1’, unframed test-patterns when ‘0’	
		[4]	reserved	0x0	0	Reserved	
17	145		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved		0	Reserved	
18	146		test_configuration0	0x0100	256	Data Formating Test Configuration	RW
		[7:0]	testpattern0_lsb	0x00	0	Testpattern used on datapath #0 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern1_lsb	0x01	1	Testpattern used on datapath #1 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
19	147		test_configuration1	0x0302	770	Data Formating Test Configuration	RW
		[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
20	148		test_configuration2	0x0504	1284	Data Formating Test Configuration	RW
		[7:0]	testpattern4_lsb	0x04	4	Testpattern used on datapath #4 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern5_lsb	0x05	5	Testpattern used on datapath #5 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
21	149		test_configuration3	0x0706	1798	Data Formating Test Configuration	RW
		[7:0]	testpattern6_lsb	0x06	6	Testpattern used on datapath #6 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern7_lsb	0x07	7	Testpattern used on datapath #7 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.	
22	150		test_configuration16	0x0000	0	Data Formating Test Configuration	RW
		[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[9:8]	testpattern4_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[11:10]	testpattern5_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[13:12]	testpattern6_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[15:14]	testpattern7_msb	0x0	0	Testpattern used when testpattern_en = '1'	
26	154		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
27	155		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
AEC [Block Offset: 160]							
0	160		configuration	0x0010	16	AEC Configuration	RW
		[0]	enable	0x0	0	AEC Enable	
		[1]	restart_filter	0x0	0	Restart AEC filter	
		[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains	
		[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1	
		[4]	amp_pri	0x1	1	Column amplifier gets higher priority than AFE PGA in gain distribution if 1. Vice versa if 0	
1	161		intensity	0x60B8	24760	AEC Configuration	RW
		[9:0]	desired_intensity	0xB8	184	Target average intensity	
		[15:10]	reserved	0x018	24	Reserved	
2	162		red_scale_factor	0x0080	128	Red Scale Factor	RW
		[9:0]	red_scale_factor	0x80	128	Red Scale Factor 3.7 unsigned	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
3	163		green1_scale_factor	0x0080	128	Green1 Scale Factor	RW
		[9:0]	green1_scale_factor	0x80	128	Green1 Scale Factor 3.7 unsigned	
4	164		green2_scale_factor	0x0080	128	Green2 Scale Factor	RW
		[9:0]	green2_scale_factor	0x80	128	Green2 Scale Factor 3.7 unsigned	
5	165		blue_scale_factor	0x0080	128	Blue Scale Factor	RW
		[9:0]	blue_scale_factor	0x80	128	Blue Scale Factor 3.7 unsigned	
6	166		reserved	0x03FF	1023	Reserved	RW
		[15:0]	reserved	0x03FF	1023	Reserved	
7	167		reserved	0x0800	2048	Reserved	RW
		[1:0]	reserved	0x0	0	Reserved	
		[3:2]	reserved	0x0	0	Reserved	
		[15:4]	reserved	0x080	128	Reserved	
8	168		min_exposure	0x0001	1	Minimum Exposure Time	RW
		[15:0]	min_exposure	0x0001	1	Minimum Exposure Time	
9	169		min_gain	0x0800	2048	Minimum Gain	RW
		[1:0]	min_mux_gain	0x0	0	Minimum Column Amplifier Gain	
		[3:2]	min_afe_gain	0x0	0	Minimum AFE PGA Gain	
		[15:4]	min_digital_gain	0x080	128	Minimum Digital Gain 5.7 unsigned	
10	170		max_exposure	0x03FF	1023	Maximum Exposure Time	RW
		[15:0]	max_exposure	0x03FF	1023	Maximum Exposure Time	
11	171		max_gain	0x100D	4109	Maximum Gain	RW
		[1:0]	max_mux_gain	0x1	1	Maximum Column Amplifier Gain	
		[3:2]	max_afe_gain	0x3	3	Maximum AFE PGA Gain	
		[15:4]	max_digital_gain	0x100	256	Maximum Digital Gain 5.7 unsigned	
12	172		reserved	0x0083	131	Reserved	RW
		[7:0]	reserved	0x083	131	Reserved	
		[13:8]	reserved	0x00	0	Reserved	
		[15:14]	reserved	0x0	0	Reserved	
13	173		reserved	0x2824	10276	Reserved	RW
		[7:0]	reserved	0x024	36	Reserved	
		[15:8]	reserved	0x028	40	Reserved	
14	174		reserved	0x2A96	10902	Reserved	RW
		[3:0]	reserved	0x6	6	Reserved	
		[7:4]	reserved	0x9	9	Reserved	
		[11:8]	reserved	0xA	10	Reserved	
		[15:12]	reserved	0x2	2	Reserved	
15	175		reserved	0x0080	128	Reserved	RW
		[9:0]	reserved	0x080	128	Reserved	
16	176		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
17	177		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	
18	178		reserved	0x0080	128	Reserved	RW
		[9:0]	reserved	0x080	128	Reserved	
19	179		reserved	0x00AA	170	Reserved	RW
		[9:0]	reserved	0x0AA	170	Reserved	
20	180		reserved	0x0100	256	Reserved	RW
		[9:0]	reserved	0x100	256	Reserved	
21	181		reserved	0x0155	341	Reserved	RW
		[9:0]	reserved	0x155	341	Reserved	
24	184		total_pixels0	0x0000	0	AEC Status	Status
		[15:0]	total_pixels[15:0]	0x0000	0	Total number of pixels sampled for Average, LSB	
25	185		total_pixels1	0x0000	0	AEC Status	Status
		[7:0]	total_pixels[23:16]	0x0	0	Total number of pixels sampled for Average, MSB	
26	186		average_status	0x0000	0	ASE Status	Status
		[9:0]	average	0x000	0	AEC Average Status	
		[12]	avg_locked	0x0	0	AEC Average Lock Status	
27	187		exposure_status	0x0000	0	ASE Status	Status
		[15:0]	exposure	0x0000	0	AEC Expsosure Status	
28	188		gain_status	0x0000	0	ASE Status	Status
		[1:0]	mux_gain	0x0	0	AEC MUX Gain Status	
		[3:2]	afe_gain	0x0	0	AEC AFE Gain Status	
		[15:4]	digital_gain	0x000	0	AEC Digital Gain Status 5.7 unsigned	
29	189		reserved	0x0000	0	Reserved	Status
		[12:0]	reserved	0x000	0	Reserved	
		[13]	reserved	0x0	0	Reserved	
Sequencer [Block Offset: 192]							
0	192		general_configuration	0x0000	0	Sequencer General Cofniguration	RW
		[0]	enable	0x0	0	Enable sequencer ‘0’: Idle, ‘1’: enabled	
		[1]	reserved	0x0	0	Reserved	
		[2]	zero_rot_enable	0x0	0	Zero ROT mode Selection. ‘0’: Non−Zero ROT, ‘1’: Zero ROT’	
		[3]	reserved	0x0	0	Reserved	
		[4]	triggered_mode	0x0	0	Triggered Mode Selection (Snapshot Shutter only) ‘0’: Normal Mode, ‘1’: Triggered Mode	
		[5]	slave_mode	0x0	0	Master/Slave Selection (Snapshot Shutter only) ‘0’: master, ‘1’: slave	
		[6]	nzrot_xsm_delay_ enable	0x0	0	Insert delay between end of ROT and start of readout in Non−Zero ROT readout mode if ‘1’. ROT delay is defined by register xsm_delay	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[7]	subsampling	0x0	0	Subsampling mode selection ‘0’: no subsampling, ‘1’: subsampling	
		[8]	binning	0x0	0	Binning mode selection ‘0’: no binning, ‘1’: binning	
		[10]	roi_aec_enable	0x0	0	Enable windowing for AEC Statistics. ‘0’: Subsample all windows ‘1’: Subsample configured window	
		[13:11]	monitor_select	0x0	0	Control of the monitor pins	
		[14]	reserved	0x0	0	Reserved	
		[15]	sequence	0x0	0	Enable a sequenced readout with different parameters for even and odd frames.	
1	193		reserved	0x0000	0	Reserved	RW
		[7:0]	reserved	0x00	0	Reserved	
		[15:8]	reserved	0x00	0	Reserved	
2	194		integration_control	0x00E4	228	Integration Control	RW
		[0]	dual_slope_enable	0x0	0	Enable Dual Slope	
		[1]	triple_slope_enable	0x0	0	Enable Triple Slope	
		[2]	fr_mode	0x1	1	Representation of fr_length. ‘0’: reset length ‘1’: frame length	
		[3]	reserved	0x0	0	Reserved	
		[4]	int_priority	0x0	0	Integration Priority ‘0’: Frame readout has priority over integration ‘1’: Integration End has priority over frame readout	
		[5]	halt_mode	0x1	1	The current frame will be completed when the sequencer is disabled and halt_mode = ‘1’. When ‘0’, the sensor stops immediately when disabled, without finishing the current frame.	
		[6]	fss_enable	0x1	1	Generation of Frame Sequence Start Sync code (FSS) ‘0’: No generation of FSS ‘1’: Generation of FSS	
		[7]	fse_enable	0x1	1	Generation of Frame Sequence End Sync code (FSE) ‘0’: No generation of FSE ‘1’: Generation of FSE	
		[8]	reverse_y	0x0	0	Reverse readout ‘0’: bottom to top readout ‘1’: top to bottom readout	
		[9]	reserved	0x0	0	Reserved	
		[11:10]	subsampling_mode	0x0	0	Subsampling mode 0x0: Subsampling in x and y (VITA compatible) 0x1: Subsampling in x, not y 0x2: Subsampling in y, not x 0x3: Subsampling in x an y	
		[13:12]	binning_mode	0x0	0	Binning mode 0x0: Binning in x and y (VITA compatible) 0x1: Binning in x, not y 0x2: Binning in y, not x 0x3: Binning in x an y	
		[14]	reserved	0x0	0	Reserved	
		[15]	reserved	0x0	0	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
3	195		roi_active0_0	0x0001	1	Active ROI Selection	RW
		[15:0]	roi_active0	0x01	1	Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active	
4	196		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
5	197		black_lines	0x0102	258	Black Line Configuration	RW
		[7:0]	black_lines	0x02	2	Number of black lines. Minimum is 1. Range 1−255	
		[12:8]	gate_first_line	0x1	1	Blank out first lines 0: no blank 1−31: blank 1−31 lines	
6	198		reserved	0x0000	0	Reserved	RW
		[11:0]	reserved	0x000	0	Reserved	
7	199		mult_timer0	0x0001	1	Exposure/Frame Rate Configuration	RW
		[15:0]	mult_timer0	0x0001	1	Mult Timer Defines granularity (unit = 1/PLL clock) of exposure and reset_length	
8	200		fr_length0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	fr_length0	0x0000	0	Frame/Reset length Reset length when fr_mode = ‘0’, Frame Length when fr_mode = ‘1’ Granularity defined by mult_timer	
9	201		exposure0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure0	0x0000	0	Exposure Time Granularity defined by mult_timer	
10	202		exposure_ds0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure_ds0	0x0000	0	Exposure Time (Dual Slope) Granularity defined by mult_timer	
11	203		exposure_ts0	0x0000	0	Exposure/Frame Rate Configuration	RW
		[15:0]	exposure_ts0	0x0000	0	Exposure Time (Triple Slope) Granularity defined by mult_timer	
12	204		gain_configuration0	0x01E3	483	Gain Configuration	RW
		[4:0]	mux_gainsw0	0x03	3	Column Gain Setting	
		[12:5]	afe_gain0	0xF	15	AFE Programmable Gain Setting	
		[13]	gain_lat_comp	0x0	0	Postpone gain update by 1 frame when ‘1’ to compensate for exposure time updates latency. Gain is applied at start of next frame if ‘0’	
13	205		digital_gain_ configuration0	0x0080	128	Gain Configuration	RW
		[11:0]	db_gain0	0x080	128	Digital Gain	
14	206		sync_configuration	0x037F	895	Synchronization Configuration	RW
		[0]	sync_rs_x_length	0x1	1	Update of rs_x_length will not be sync’ed at start of frame when ‘0’	
		[1]	sync_black_lines	0x1	1	Update of black_lines will not be sync’ed at start of frame when ‘0’	
		[2]	sync_dummy_lines	0x1	1	Update of dummy_lines will not be sync’ed at start of frame when ‘0’	
		[3]	sync_exposure	0x1	1	Update of exposure will not be sync’ed at start of frame when ‘0’	
		[4]	sync_gain	0x1	1	Update of gain settings (gain_sw, afe_gain) will not be sync’ed at start of frame when ‘0’	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[5]	sync_roi	0x1	1	Update of roi updates (active_roi) will not be sync'ed at start of frame when '0'	
		[6]	sync_ref_lines	0x1	1	Update of ref_lines will not be sync'ed at start of frame when '0'	
		[8]	blank_roi_switch	0x1	1	Blank first frame after ROI switching	
		[9]	blank_ subsampling_ss	0x1	1	Blank first frame after subsampling/binning mode switching '0': No blanking '1': Blanking	
		[10]	exposure_sync_ mode	0x0	0	When '0', exposure configurations are sync'ed at the start of FOT. When '1', exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered snapshot – master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'.	
15	207		ref_lines	0x0000	0	Reference Line Configuration	RW
		[7:0]	ref_lines	0x00	0	Number of Reference Lines 0−255	
16	208		reserved	0xA100	41216	Reserved	RW
		[7:0]	reserved	0x00	0	Reserved	
		[15:8]	reserved	0xA1	161	Reserved	
19	211		reserved	0x0E5B	3675	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x1	1	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x1	1	Reserved	
		[6:4]	reserved	0x5	5	Reserved	
		[15:8]	reserved	0xE	14	Reserved	
20	212		reserved	0x0000	0	Reserved	RW
		[12:0]	reserved	0x0000	0	Reserved	
		[15]	reserved	0x0	0	Reserved	
21	213		reserved	0x07FF	2047	Reserved	RW
		[12:0]	reserved	0x07FF	2047	Reserved	
22	214		reserved	0x0000	0	Reserved	RW
		[7:0]	reserved	0x00	0	Reserved	
		[15:8]	reserved	0x0	0	Reserved	
23	215		reserved	0x0103	259	Reserved	RW
		[0]	reserved	0x1	1	Reserved	
		[1]	reserved	0x1	1	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[4]	reserved	0x0	0	Reserved	
		[5]	reserved	0x0	0	Reserved	
		[6]	reserved	0x0	0	Reserved	
		[7]	reserved	0x0	0	Reserved	
		[8]	reserved	0x1	1	Reserved	
		[9]	reserved	0x0	0	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[10]	reserved	0x0	0	Reserved	
		[11]	reserved	0x0	0	Reserved	
		[12]	reserved	0x0	0	Reserved	
		[13]	reserved	0x0	0	Reserved	
		[14]	reserved	0x0	0	Reserved	
24	216		reserved	0x7F08	32520	Reserved	RW
		[6:0]	reserved	0x08	8	Reserved	
		[14:8]	reserved	0x7F	127	Reserved	
25	217		reserved	0x4444	17476	Reserved	RW
		[6:0]	reserved	0x44	68	Reserved	
		[14:8]	reserved	0x44	68	Reserved	
26	218		reserved	0x4444	17476	Reserved	RW
		[6:0]	reserved	0x44	68	Reserved	
		[14:8]	reserved	0x44	68	Reserved	
27	219		reserved	0x0016	22	Reserved	RW
		[6:0]	reserved	0x016	22	Reserved	
		[14:8]	reserved	0x00	0	Reserved	
28	220		reserved	0x301F	12319	Reserved	RW
		[6:0]	reserved	0x1F	31	Reserved	
		[14:8]	reserved	0x30	48	Reserved	
29	221		reserved	0x6245	25157	Reserved	RW
		[6:0]	reserved	0x45	69	Reserved	
		[14:8]	reserved	0x62	98	Reserved	
30	222		reserved	0x6230	25136	Reserved	RW
		[6:0]	reserved	0x30	48	Reserved	
		[14:8]	reserved	0x62	98	Reserved	
31	223		reserved	0x001A	26	Reserved	RW
		[6:0]	reserved	0x1A	26	Reserved	
32	224		reserved	0x3E01	15873	Reserved	RW
		[3:0]	reserved	0x1	1	Reserved	
		[7:4]	reserved	0x00	0	Reserved	
		[8]	reserved	0x0	0	Reserved	
		[9]	reserved	0x1	1	Reserved	
		[10]	reserved	0x1	1	Reserved	
		[11]	reserved	0x1	1	Reserved	
		[12]	reserved	0x1	1	Reserved	
		[13]	reserved	0x1	1	Reserved	
33	225		reserved	0x5EF1	24305	Reserved	RW
		[4:0]	reserved	0x11	17	Reserved	
		[9:5]	reserved	0x17	23	Reserved	
		[14:10]	reserved	0x17	23	Reserved	
		[15]	reserved	0x0	0	Reserved	
34	226		reserved	0x6000	24576	Reserved	RW
		[4:0]	reserved	0x00	0	Reserved	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[9:5]	reserved	0x00	0	Reserved	
		[14:10]	reserved	0x18	24	Reserved	
		[15]	reserved	0x0	0	Reserved	
35	227		reserved	0x0000	0	Reserved	RW
		[0]	reserved	0x0	0	Reserved	
		[1]	reserved	0x0	0	Reserved	
		[2]	reserved	0x0	0	Reserved	
		[3]	reserved	0x0	0	Reserved	
		[4]	reserved	0x0	0	Reserved	
36	228		roi_active0_1	0x0001	1	Active ROI Selection	RW
		[7:0]	roi_active1	0x01	1	Active ROI Selection [0] Roi0 Active [1] Roi1 Active ... [15] Roi15 Active	
37	229		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
38	230		reserved	0x0001	1	Reserved	RW
		[15:0]	reserved	0x0001	1	Reserved	
39	231		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
40	232		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
41	233		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
42	234		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
43	235		reserved	0x01E3	483	Reserved	RW
		[4:0]	reserved	0x03	3	Reserved	
		[12:5]	reserved	0xF	15	Reserved	
44	236		reserved	0x0080	128	Reserved	RW
		[11:0]	reserved	0x080	128	Reserved	
45	237		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0000	0	Reserved	
46	238		reserved	0xFFFF	65535	Reserved	RW
		[15:0]	reserved	0xFFFF	65535	Reserved	
47	239		reserved	0x0000	0	Reserved	RW
		[15:0]	reserved	0x0	0	Reserved	
48	240		x_resolution	0x00A2 [0x007C]	162 [124]	Sequencer Status	Status
		[7:0]	x_resolution	0x000A2 [0x007C]	162 [124]	Sensor x resolution	
49	241		y_resolution	0x0800 [0x04F0]	2048 [1264]	Sequencer Status	Status
		[12:0]	y_resolution	0x0800 [0x04F0]	2048 [1264]	Sensor y resolution	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
50	242		mult_timer_status	0x0000	0	Sequencer Status	Status
		[15:0]	mult_timer	0x0000	0	Mult Timer Status (Master Snapshot Shutter only)	
51	243		reset_length_status	0x0000	0	Sequencer Status	Status
		[15:0]	reset_length	0x0000	0	Current Reset Length (not in Slave mode)	
52	244		exposure_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure	0x0000	0	Current Exposure Time (not in Slave mode)	
53	245		exposure_ds_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure_ds	0x0000	0	Current Exposure Time (not in Slave mode)	
54	246		exposure_ts_status	0x0000	0	Sequencer Status	Status
		[15:0]	exposure_ts	0x0000	0	Current Exposure Time (not in Slave mode)	
55	247		gain_status	0x0000	0	Sequencer Status	Status
		[4:0]	mux_gainsw	0x00	0	Current Column Gain Setting	
		[12:5]	afe_gain	0x00	0	Current AFE Programmable Gain	
56	248		digital_gain_status	0x0000	0	Sequencer Status	Status
		[11:0]	db_gain	0x000	0	Digital Gain	
		[12]	dual_slope	0x0	0	Dual Slope Enabled	
		[13]	triple_slope	0x0	0	Triple Slope Enabled	
58	250		reserved	0x0423	1059	Reserved	RW
		[4:0]	reserved	0x03	3	Reserved	
		[9:5]	reserved	0x01	1	Reserved	
		[14:10]	reserved	0x01	1	Reserved	
59	251		reserved	0x030F	783	Reserved	RW
		[7:0]	reserved	0xF	15	Reserved	
		[15:8]	reserved	0x3	3	Reserved	
60	252		reserved	0x0601	1537	Reserved	RW
		[7:0]	reserved	0x1	1	Reserved	
		[15:8]	reserved	0x6	6	Reserved	
61	253		roi_aec_ configuration0	0x0000	0	AEC ROI Configuration	RW
		[7:0]	x_start	0x00	0	AEC ROI X Start Configuration (used for AEC statistics when roi_aec_enable='1')	
		[15:8]	x_end	0x00	0	AEC ROI X End Configuration (used for AEC statistics when roi_aec_enable='1')	
62	254		roi_aec_ configuration1	0x0000	0	AEC ROI Configuration	RW
		[12:0]	y_start	0x0000	0	AEC ROI Y Start Configuration (used for AEC statistics when roi_aec_enable='1')	
63	255		roi_aec_ configuration2	0x0000	0	AEC ROI Configuration	RW
		[12:0]	y_end	0x0000	0	AEC ROI Y End Configuration (used for AEC statistics when roi_aec_enable='1')	
Sequencer ROI [Block Offset: 256]							
0	256		roi0_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
1	257		roi0_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
2	258		roi0_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
3	259		roi1_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
4	260		roi1_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
5	261		roi1_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
6	262		roi2_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
7	263		roi2_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
8	264		roi2_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
9	265		roi3_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
10	266		roi3_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
11	267		roi3_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
12	268		roi4_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
13	269		roi4_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
14	270		roi4_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
15	271		roi5_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
16	272		roi5_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
17	273		roi5_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
18	274		roi6_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
19	275		roi6_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
20	276		roi6_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
21	277		roi7_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
22	278		roi7_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
23	279		roi7_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
24	280		roi8_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
25	281		roi8_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
26	282		roi8_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
27	283		roi9_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
28	284		roi9_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
29	285		roi9_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
30	286		roi10_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
31	287		roi10_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
32	288		roi10_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
33	289		roi11_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
34	290		roi11_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
35	291		roi11_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
36	292		roi12_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
37	293		roi12_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
38	294		roi12_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
39	295		roi13_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	

Table 35. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default	Description	Type
		[15:8]	x_end	0xA1	161	X End Configuration	
40	296		roi13_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
41	297		roi13_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
42	298		roi14_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
43	299		roi14_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
44	300		roi14_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
45	301		roi15_configuration0	0xA100	41216	ROI Configuration	RW
		[7:0]	x_start	0x00	0	X Start Configuration	
		[15:8]	x_end	0xA1	161	X End Configuration	
46	302		roi15_configuration1	0x0000	0	ROI Configuration	RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
47	303		roi15_configuration2	0x07FF	2047	ROI Configuration	RW
		[12:0]	y_end	0x7FF	2047	Y End Configuration	
Sequencer ROI [Block Offset: 384]							
0	384		reserved			Reserved	RW
		[15:0]	reserved			Reserved	
	…	…	…			…	
			…			…	
127	511		reserved			Reserved	RW
		[15:0]	reserved			Reserved	

PACKAGE INFORMATION

Table 36. PIN LIST

The LVDS I/Os comply to the TIA/EIA−644−A Standard and the CMOS I/Os have a 3.3 V signal level.
This table reflects pin out for ISP8 compatibility.

Pkg Pin #	Signal	Description
1	vdd_33	Supply 3.3 V supply
2	nc	No connect
3	mosi	CMOS Input SPI Master Out Slave In
4	miso	CMOS Output SPI Master In Slave Out
5	sck	CMOS Input SPI Input Clock
6	gnd_18	Supply 1.8 V Ground
7	vdd_18	Supply 1.8 V Supply
8	doutn1	LVDS Output LVDS Data Output Channel #1 (Negative)
9	doutp1	LVDS Output LVDS Data Output Channel #1 (Positive)
10	doutn0	LVDS Output LVDS Data Output Channel #0 (Negative)
11	doutp0	LVDS Output LVDS Data Output Channel #1 (Positive)
12	nc	No connect
13	nc	No connect
14	clock_outn	LVDS Output LVDS Clock Output (Negative)
15	clock_outp	LVDS Output LVDS Clock Output (Positive)
16	doutn2	LVDS Output LVDS Data Output Channel #2 (Negative)
17	doutp2	LVDS Output LVDS Data Output Channel #2 (Positive)
18	doutn3	LVDS Output LVDS Data Output Channel #3 (Negative)
19	doutp3	LVDS Output LVDS Data Output Channel #3 (Positive)
20	gnd_18	Supply 1.8 V Ground
21	vdd_18	Supply 1.8 V Supply
22	nc	No connect
23	vdd_33	Supply 3.3 V Supply
24	gnd_33	Supply 3.3 V Ground
25	doutn4	LVDS Output LVDS Data Output Channel #4 (Negative)
26	doutp4	LVDS Output LVDS Data Output Channel #4 (Positive)
27	doutn5	LVDS Output LVDS Data Output Channel #5 (Negative)
28	doutp5	LVDS Output LVDS Data Output Channel #5 (Positive)
29	syncn	LVDS Output LVDS Sync Channel Output (Negative)
30	syncp	LVDS Output LVDS Sync Channel Output (Positive)
31	nc	No connect
32	nc	No connect
33	doutn7	LVDS Output LVDS Data Output Channel #7 (Negative)
34	doutp7	LVDS Output LVDS Data Output Channel #7 (Positive)
35	doutn6	LVDS Output LVDS Data Output Channel #6 (Negative)
36	doutp6	LVDS Output LVDS Data Output Channel #6 (Positive)
37	vdd_33	Supply 3.3 V Supply
38	gnd_33	Supply 3.3 V Ground
39	gnd_18	Supply 1.8 V Ground
40	vdd_18	Supply 1.8 V Supply
41	lvds_clock_inn	LVDS Input LVDS Clock Input (Positive)
42	lvds_clock_inp	LVDS Input LVDS Clock Input (Positive)
43	nc	No connect
44	clk_pll	CMOS Input Reference Clock Input for PLL

Table 36. PIN LIST

The LVDS I/Os comply to the TIA/EIA−644−A Standard and the CMOS I/Os have a 3.3 V signal level.
This table reflects pin out for ISP8 compatibility.

Pkg Pin #	Signal	Description
45	vdd_18	1.8 V Supply
46	gnd_18	Supply 1.8 V Ground
47	ibias_master	Analog I/O Master Bias Reference
48	nc	No connect
49	vdd_33	Supply 3.3 V Supply
50	gnd_33	Supply 3.3 V Ground
51	nc	No connect
52	nc	No connect
53	nc	No connect
54	nc	No connect
55	nc	No connect
56	nc	No connect
57	vdd_pix	Supply Pixel Array Supply
58	gnd_colpc	Supply Pixel Array Ground
59	nc	No connect
60	vdd_pix	Supply Pixel Array Supply
61	gnd_colpc	Supply Pixel Array Ground
62	gnd_33	Supply 3.3 V Ground
63	vdd_33	Supply 3.3 V Supply
64	nc	No connect
65	gnd_colpc	Supply Pixel Array Ground
66	vdd_pix	Supply Pixel Array Supply
67	gnd_colpc	Supply Pixel Array Ground
68	vdd_pix	Supply Pixel Array Supply
69	nc	No connect
70	trigger0	CMOS Input Trigger Input #0
71	trigger1	CMOS Input Trigger Input #1
72	nc	No connect
73	nc	No connect
74	nc	No connect
75	nc	No connect
76	nc	No connect
77	trigger2	CMOS Input Trigger Input #0
78	monitor0	CMOS Output Monitor Output #0
79	vdd_33	Supply 3.3 V supply
80	gnd_33	Supply 3.3 V Ground
81	monitor1	CMOS Output Monitor Output #1
82	reset_n	CMOS Input Sensor Reset (Active Low)
83	ss_n	CMOS Input SPI Slave Select.
84	gnd_33	Supply 3.3 V Ground

Selectable Pin−Out

The PYTHON sensor has a built−in possibility to route some of the internal signals to different pads at the side of the chip.

The pin−out is controlled by glob_config in the chip_configuration register, located at address 2. The two possible pin outs in the 84 pin package are listed in Table 37. By default, the 0x3 setting is selected to ensure compatibility of the 84−pin package with the ISP8 foot print. More details on the ISP8 footprint can be found in AND9158.

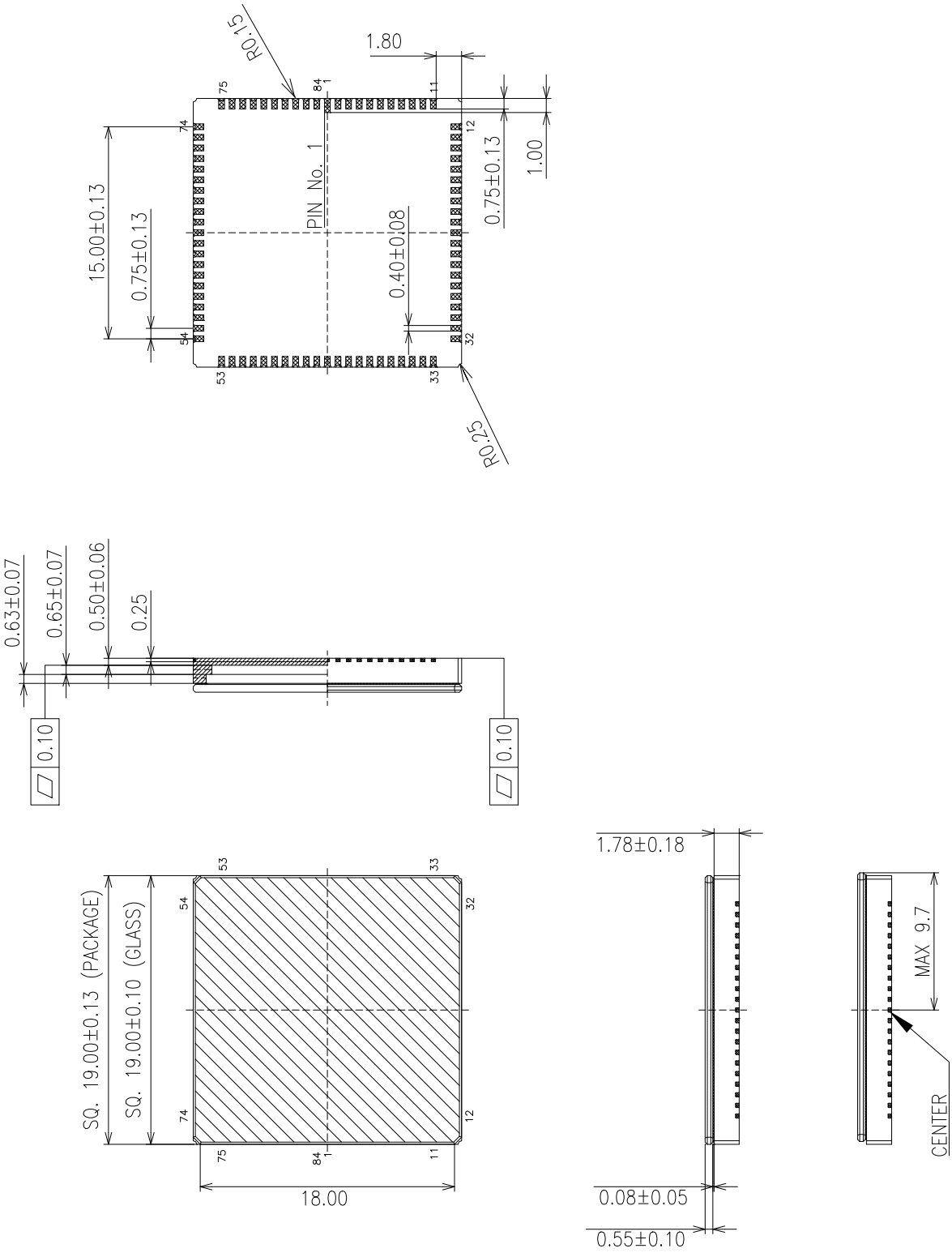
Table 37. OPTIONS FOR PIN−OUT IN THE 84 PIN LCC PACKAGE

Pin Name (84−pin LCC)	Pin Name (84−pin LCC)	Pin No. (84−pin LCC)
glob_config = 0x3	**glob_config = 0x0**	
doutn1	clock_outn	8
doutp1	clock_outp	9
clock_outn	doutn1	14
clock_outp	doutp1	15
syncn	doutn6	29
syncp	doutp6	30
doutn6	syncn	35
doutp6	syncp	36

Mechanical Specification

Parameter	Description	Min	Typ	Max	Units
Die (with Pin 1 to the left center)	Die thickness		725		μm
	Die Size		14.7 x 14.25		mm^2
	Die center, X offset to the center of package	−50	0	50	μm
	Die center, Y offset to the center of the package	−50	0	50	μm
	Die position, tilt to the Die Attach Plane		0		deg
	Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides)		0		deg
	Optical center referenced from the die/package center (X−dir)		−231		μm
	Optical center referenced from the die/package center (Y−dir)		1697		μm
	Distance from bottom of the package to top of the die surface		1.25		mm
	Distance from top of the die surface to top of the glass lid		1.16		mm
Glass Lid Specification	XY size		19 x 19		mm
	Thickness	0.45	0.55	0.65	mm
	Spectral response range	400		1000	nm
	Transmission of glass lid (refer to Figure 52)		92		%
Glass Lid Material	D263 Teco (no coatings on glass)				
Mechanical Shock	JESD22−B104C; Condition G			2000	g
Vibration	JESD22−B103B; Condition 1			2000	Hz
Mounting Profile	Reflow profile according to J−STD−020D.1			260	°C

Package Drawing



NOTE: Unless noted otherwise, all dimensions represent nominal values.

Figure 50. Package Drawing for the 84−pin LCC Package

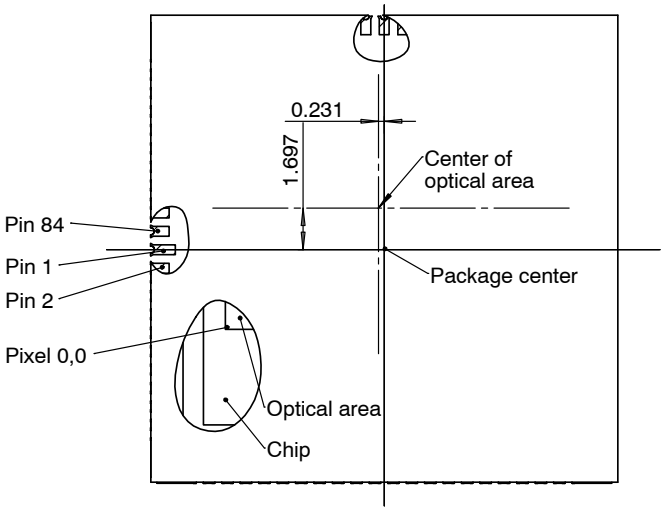
Optical Center Information

The Center of the Die (CD) is the center of the cavity.

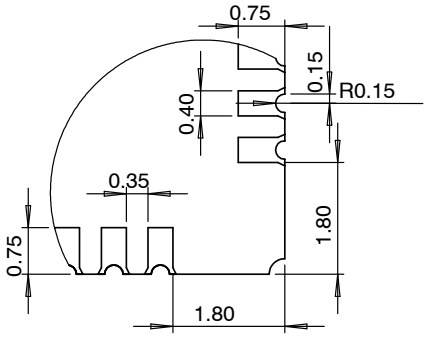
The center of the die is exactly at 50% between the outsides of the two outer seal rings

The center of the cavity is exactly at 50% between the insides of the finger pads.

- Die outer dimensions:
  - B4 is the reference for the Die (0,0) in μm
  - B1 is at (0, 14250) μm
  - B2 is at (14700, 14250) μm
  - B3 is at (14700, 0) μm
- Active Area outer dimensions
  - A1 is the at (881, 13754) μm
  - A2 is at (13356, 13754) μm
  - A3 is at (13356, 3890) μm
  - A4 is at (881, 3890) μm
- Center of the Active Area
  - AA is at (7119, 8822) μm
- Center of the Die
  - CD is at (7350, 7125) μm

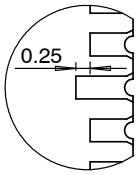


Top View



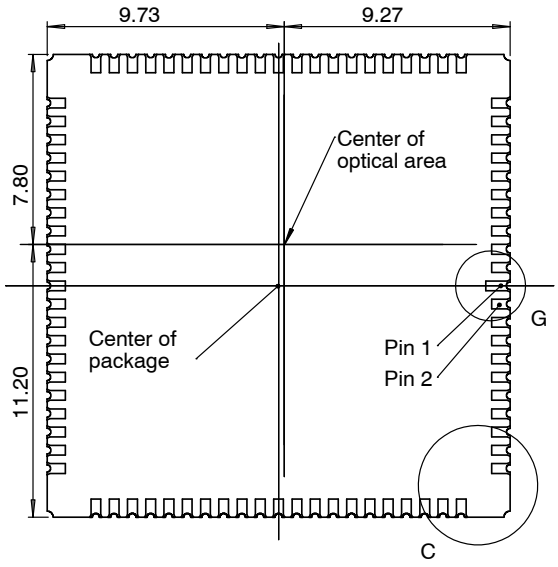
DETAIL C

SCALE 10:1



DETAIL G

SCALE 10:1



Bottom View

NOTE: Unless noted otherwise, all dimensions represent nominal values.

Figure 51. Graphical Representation of the Optical Center

Glass Lid

The PYTHON sensor uses a glass lid without any coatings. Figure 52 shows the transmission characteristics of the glass lid.

As shown in Figure 52, no infrared attenuating color filter glass is used. A filter must be provided in the optical path when color devices are used (source: http://www.pgo−online.com).

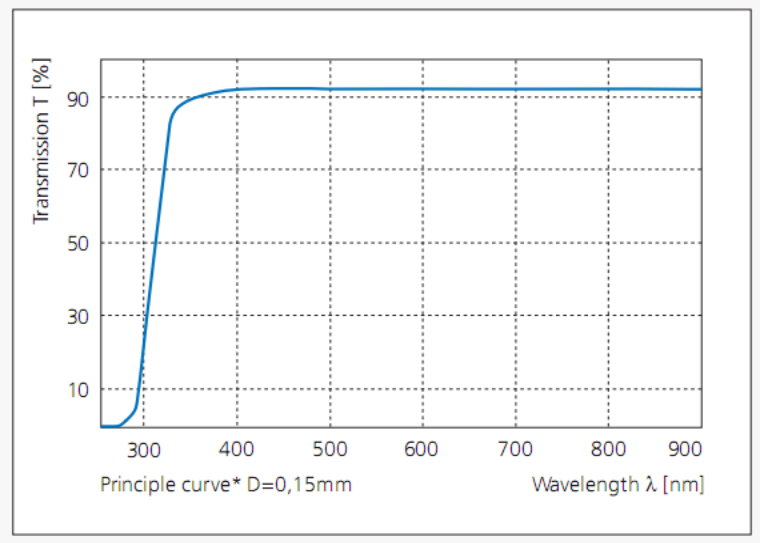


Figure 52. Transmission Characteristics of the Glass Lid

SPECIFICATIONS AND USEFUL REFERENCES

Specifications, Application Notes and useful resources can be accessed via customer login account at MyON – CISP Extranet.
https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do

Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

Product Application Notes

AND9158: PYTHON ISP8 Solution Ref Board Design Considerations

AND5001: Sync Codes in the PYTHON Family

Acceptance Criteria Specification

The Product Acceptance Criteria ACSPYTHON5000 is available at MyON- CISP Extranet. This document contains the criteria to which the PYTHON sensors are tested prior to being shipped.

Return Material Authorization (RMA)

Refer to the ON Semiconductor RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

ACRONYMS

Acronym	Description
ADC	Analog−to−Digital Converter
AFE	Analog Front End
BL	Black pixel data
CDM	Charged Device Model
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital−to−Analog Converter
DDR	Double Data Rate
DNL	Differential Non−Llinearity
DS	Double Sampling
DSNU	Dark Signal Non−Uniformity
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
FE	Frame End
FF	Fill Factor
FOT	Frame Overhead Time
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
FPS	Frame per Second
FS	Frame Start
HBM	Human Body Model
IMG	Image data (regular pixel data)
INL	Integral Non−Linearity

Acronym	Description
IP	Intellectual Property
LE	Line End
LS	Line Start
LSB	least significant bit
LVDS	Low−Voltage Differential Signaling
MSB	most significant bit
PGA	Programmable Gain Amplifier
PLS	Parasitic Light Sensitivity
PRBS	Pseudo−Random Binary Sequence
PRNU	Photo Response Non−Uniformity
QE	Quantum Efficiency
RGB	Red−Green−Blue
RMA	Return Material Authorization
rms	Root Mean Square
ROI	Region of Interest
ROT	Row Overhead Time
S/H	Sample and Hold
SNR	Signal−to−Noise Ratio
SPI	Serial Peripheral Interface
TIA	Telecommunications Industry Association
T_J	Junction temperature
TR	Training pattern
% RH	Percent Relative Humidity

GLOSSARY

conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
CFA	Color filter array. The materials deposited on top of pixels that selectively transmit color.
DNL	Differential non−linearity (for ADCs)
DSNU	Dark signal non−uniformity. This parameter characterizes the degree of non−uniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill−factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
INL	Integral nonlinearity (for ADCs)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m^2 = 1/683 W/m^2)
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo−response non−uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. ”Soft” reset occurs when the reset transistor is operated below the threshold. ”Hard” reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal−to−noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.

PUBLICATION ORDERING INFORMATION

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ON Semiconductor Website: **www.onsemi.com**

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