


"Half-Bridge" IGBT INT-A-PAK (Ultrafast Speed IGBT), 75 A



INT-A-PAK

FEATURES

- Generation 4 IGBT technology
- Ultrafast: Optimized for high speed 8 kHz to 40 kHz in hard switching, > 200 kHz in resonant mode
- Very low conduction and switching losses
- HEXFRED® antiparallel diodes with ultrasoft recovery
- Industry standard package
- UL approved file E78996 
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level


RoHS
COMPLIANT

PRODUCT SUMMARY	
V_{CES}	1200 V
I_C DC	110 A
$V_{CE(on)}$ at 75 A, 25 °C	2.5 V

BENEFITS

- Increased operating efficiency
- Direct mounting to heatsink
- Performance optimized for power conversion: UPS, SMPS, welding
- Lower EMI, requires less snubbing

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		1200	V
Continuous collector current	I_C	$T_C = 25\text{ °C}$	110	A
		$T_C = 76\text{ °C}$	75	
Pulsed collector current	I_{CM}	Repetitive rating; $V_{GE} = 20\text{ V}$, pulse width limited by maximum junction temperature	150	
Peak switching current See fig. 17	I_{LM}		150	
Peak diode forward current	I_{FM}		150	V
Gate to emitter voltage	V_{GE}		± 20	
RMS isolation voltage	V_{ISOL}	Any terminal to case, $t = 1\text{ minute}$	2500	
Maximum power dissipation	P_D	$T_C = 25\text{ °C}$	390	W
		$T_C = 85\text{ °C}$	200	
Operating junction temperature range	T_J		- 40 to + 150	°C
Storage temperature range	T_{Stg}		- 40 to + 125	

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ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector to emitter breakdown voltage	V _{(BR)CES}	V _{GE} = 0 V, I _C = 1 mA	1200	-	-	V
Collector to emitter voltage	V _{CE(on)}	V _{GE} = 15 V, I _C = 75 A	-	2.5	3.7	
		I _C = 75 A, V _{GE} = 15 V, T _J = 125 °C	-	2.25	3.3	
Gate threshold voltage	V _{GE(th)}	V _{CE} = 6.0 V, I _C = 750 μA	3.0	4.5	6.0	
Temperature coefficient of threshold voltage	ΔV _{GE(th)/ΔT_J}		-	- 14	-	mV/°C
Forward transconductance	g _{fe}	V _{CE} = 25 V, I _C = 75 A Pulse width 50 μs, single shot	-	107	-	S
Collector to emitter leaking current	I _{CES}	V _{GE} = 0 V, V _{CE} = 1200 V	-	0.03	1.0	mA
		V _{GE} = 0 V, V _{CE} = 1200 V, T _J = 125 °C	-	4.3	10	
Diode forward voltage	V _F	V _{GE} = 0 V, I _F = 75 A	-	3	3.6	V
		I _F = 75 A, V _{GE} = 0 V, T _J = 125 °C	-	2.83	3.3	
Gate to emitter leakage current	I _{GES}	V _{GE} = ± 20 V	-	-	250	nA

SWITCHING CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total gate charge (turn-on)	Q _g	V _{CC} = 400 V I _C = 85 A	-	570	854	nC
Gate to emitter charge (turn-on)	Q _{ge}		-	96	144	
Gate to collector charge (turn-on)	Q _{gc}		-	189	283	
Turn-on delay time	t _{d(on)}	R _{g1} = 15 Ω	-	437	-	ns
Rise time	t _r	R _{g2} = 0 Ω	-	60	-	
Turn-off delay time	t _{d(off)}	I _C = 75 A	-	395	-	
Fall time	t _f	V _{CC} = 720 V	-	245	-	mJ
Turn-on switching energy	E _{on}	V _{GE} = ± 15 V	-	5	-	
Turn-off switching energy	E _{off} ⁽¹⁾	Inductor load	-	3	-	
Total switching energy	E _{ts} ⁽¹⁾	T _J = 25 °C	-	8	-	ns
Turn-on delay time	t _{d(on)}	R _{g1} = 15 Ω	-	453	-	
Rise time	t _r	R _{g2} = 0 Ω	-	70	-	
Turn-off delay time	t _{d(off)}	I _C = 75 A	-	415	-	mJ
Fall time	t _f	V _{CC} = 720 V	-	661	-	
Turn-on switching energy	E _{on}	V _{GE} = ± 15 V	-	8	-	
Turn-off switching energy	E _{off} ⁽¹⁾	Inductor load	-	11	-	pF
Total switching energy	E _{ts} ⁽¹⁾	T _J = 125 °C	-	19	32	
Input capacitance	C _{ies}	V _{GE} = 0 V	-	12 815	-	
Output capacitance	C _{oes}	V _{CC} = 30 V	-	570	-	ns
Reverse transfer capacitance	C _{res}	f = 1 MHz	-	110	-	
Diode reverse recovery time	t _{rr}	R _{g1} = 15 Ω	-	174	-	
Diode peak reverse current	I _{rr}	R _{g2} = 0 Ω	-	107	-	A
Diode recovery charge	Q _{rr}	I _C = 75 A	-	9367	-	nC
Diode peak rate of fall of recovery during t _b	dl _(rec) /dt	V _{CC} = 720 V dl/dt = 1300 A/μs	-	1491	-	A/μs

Note

⁽¹⁾ Repetitive rating; V_{GE} = 20 V, pulse width limited by maximum junction temperature

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Thermal resistance, junction to case	R _{thJC}	IGBT	-	0.32	°C/W
		Diode	-	0.35	
Thermal resistance, case to sink per module	R _{thCS}		0.1	-	
Mounting torque		case to heatsink	-	4.0	Nm
		case to terminal 1, 2 and 3	For screws M5 x 0.8	-	
Weight of module			200	-	g

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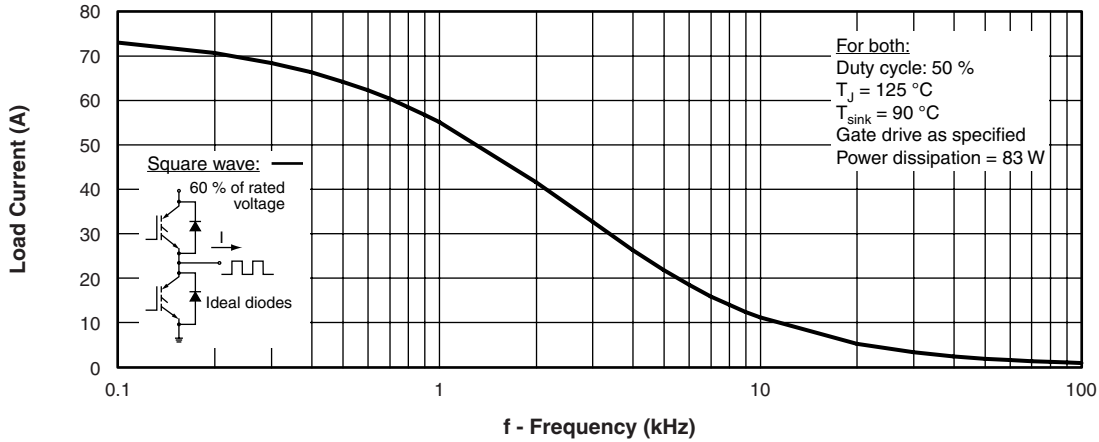


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

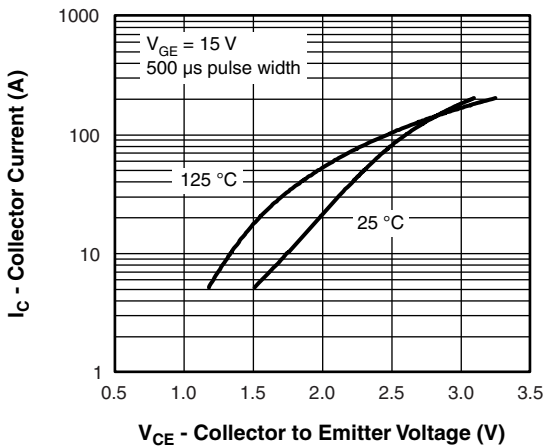


Fig. 2 - Typical Output Characteristics

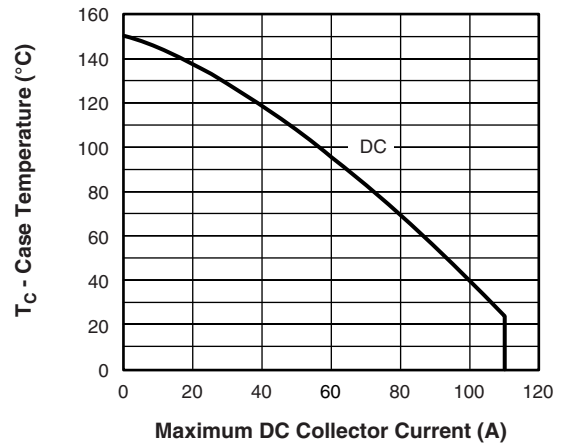


Fig. 4 - Case Temperature vs. Maximum Collector Current

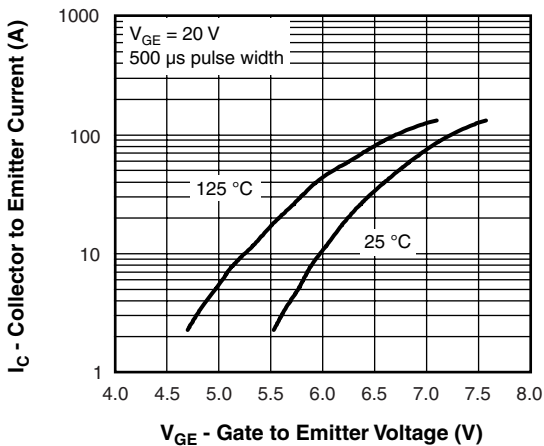


Fig. 3 - Typical Transfer Characteristics

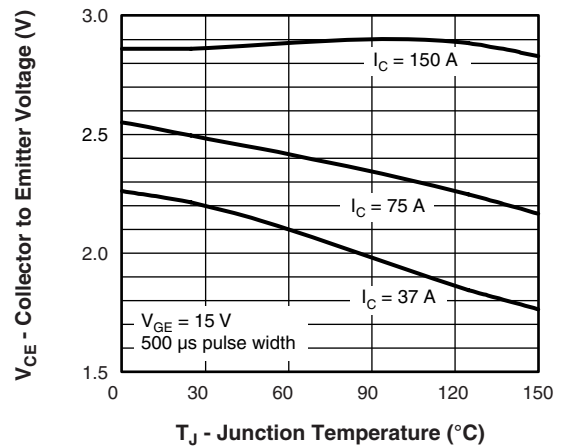


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

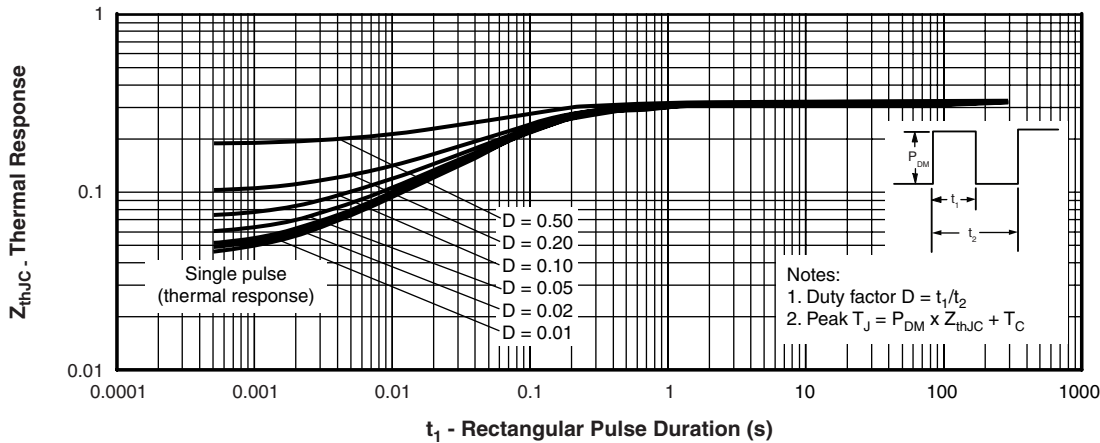


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

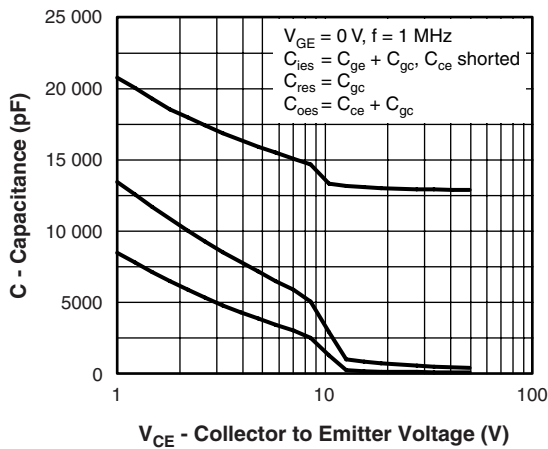


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

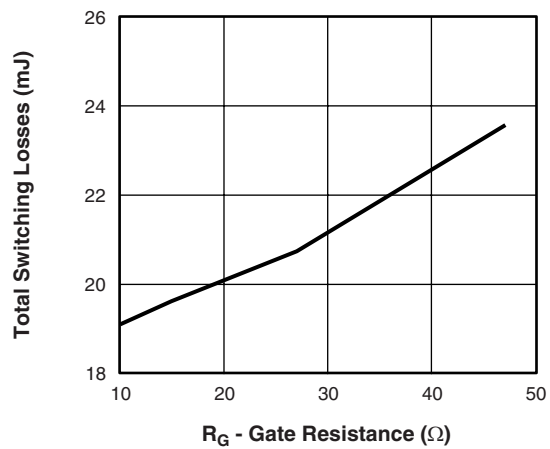


Fig. 9 - Typical Switching Losses vs. Gate Resistance

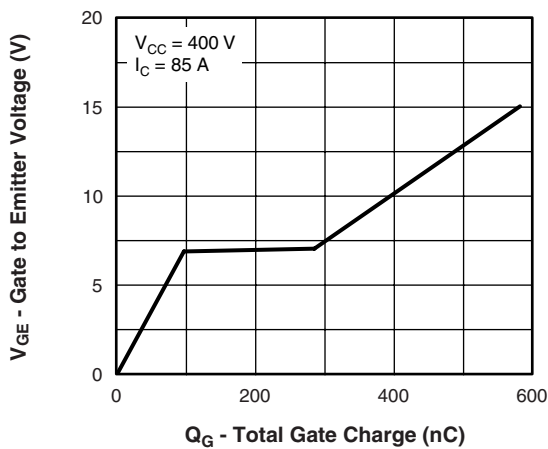


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

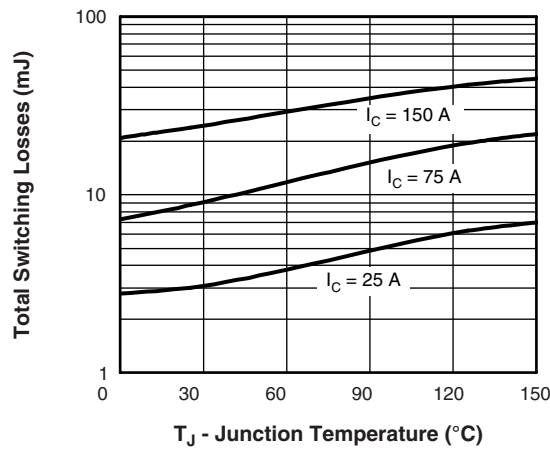


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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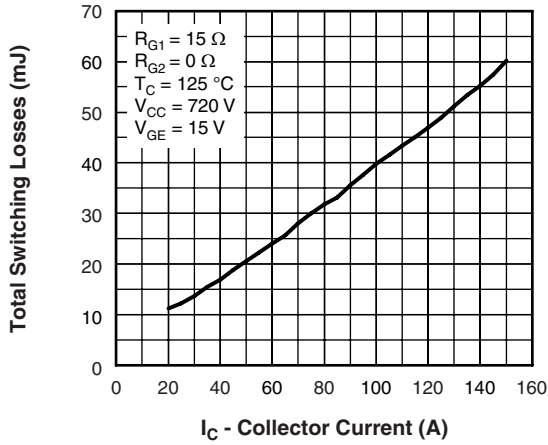


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

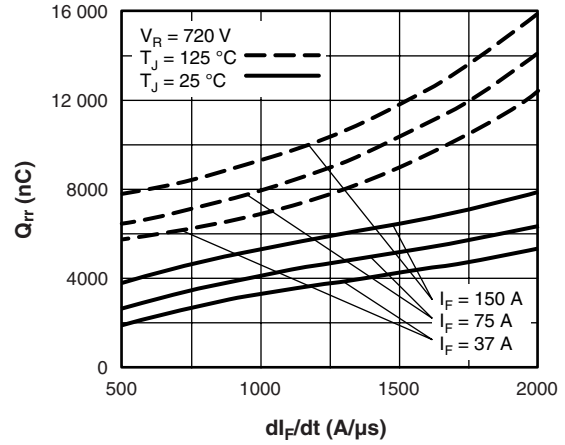


Fig. 14 - Typical Stored Charge vs. di_F/dt

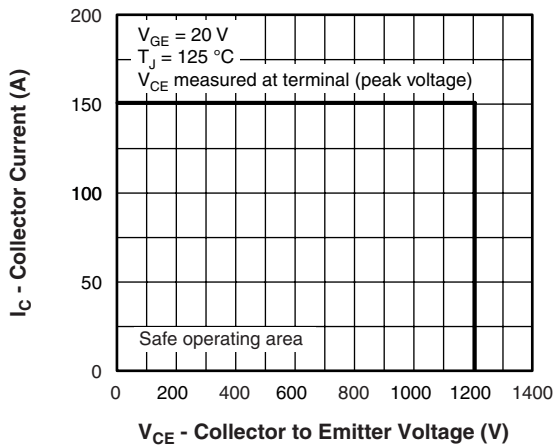


Fig. 12 - Reverse Bias SOA

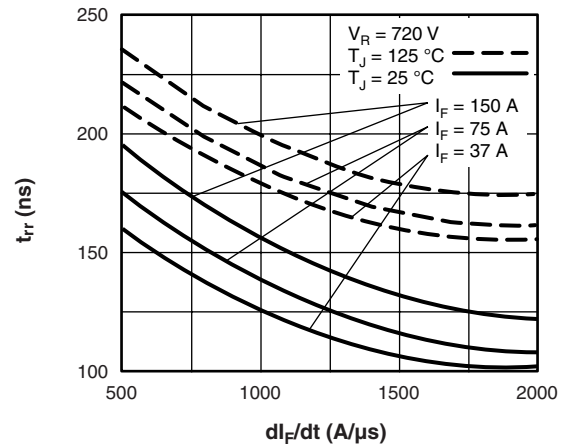


Fig. 15 - Typical Reverse Recovery Time vs. di_F/dt

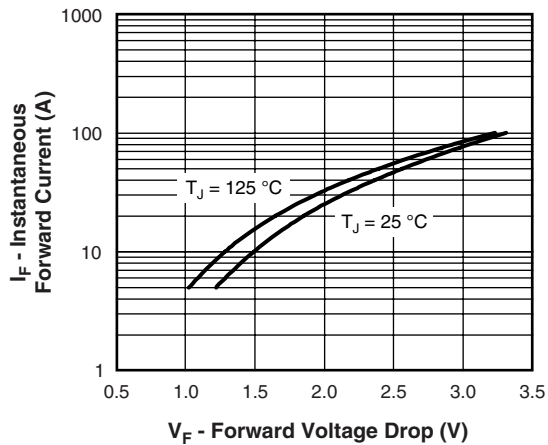


Fig. 13 - Typical Forward Voltage Drop vs. Instantaneous Forward Current

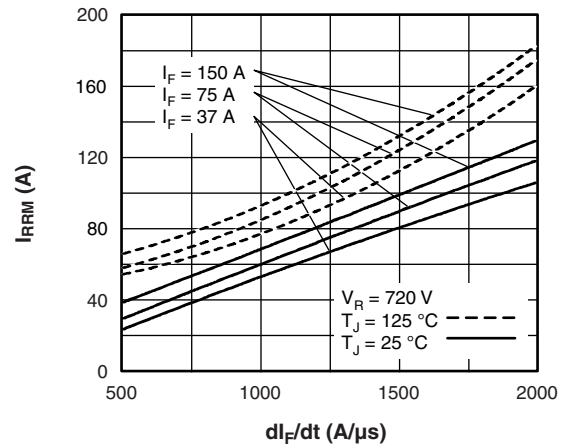


Fig. 16 - Typical Recovery Current vs. di_F/dt

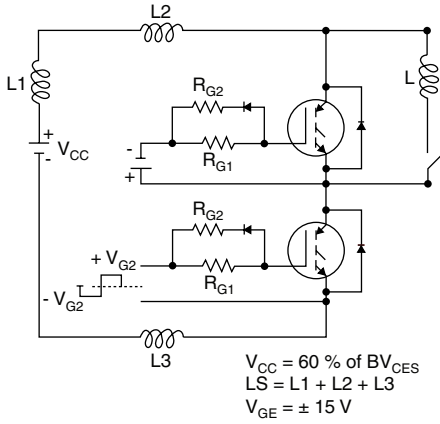


Fig. 17a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

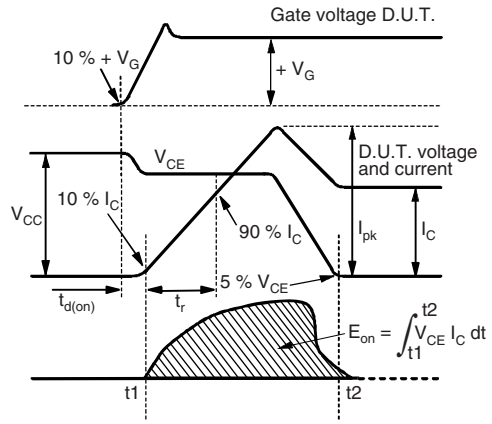


Fig. 17c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

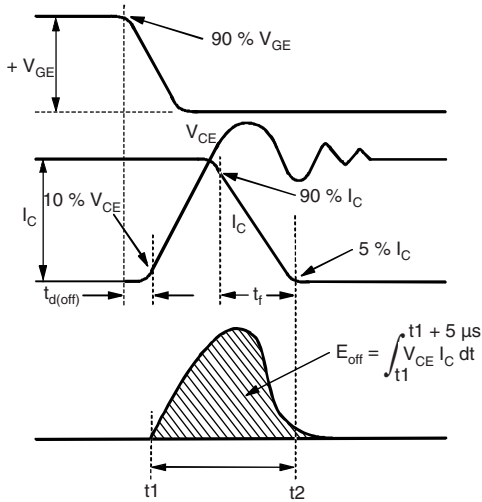


Fig. 17b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

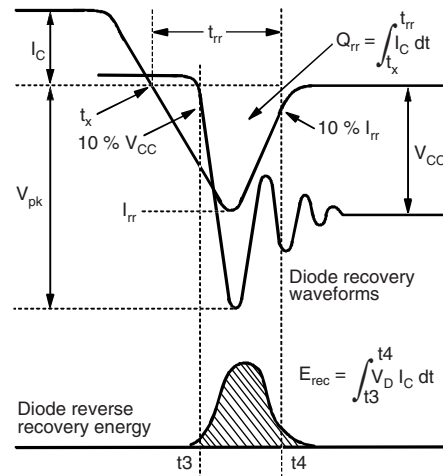


Fig. 17d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

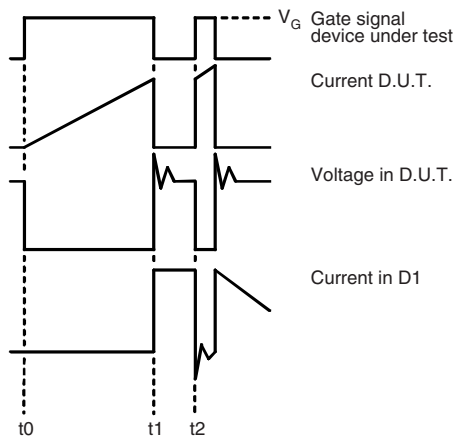
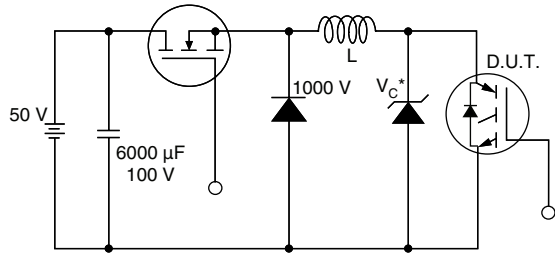


Fig. 17e - Macro Waveforms for Figure 18a's Test Circuit



* Driver same type as D.U.T.; $V_C = 80\%$ of V_{CE} (max)
Note: Due to the 50 V power supply, pulse width and inductor will increase to obtain rated I_d

Fig. 18 - Clamped Inductive Load Test Circuit

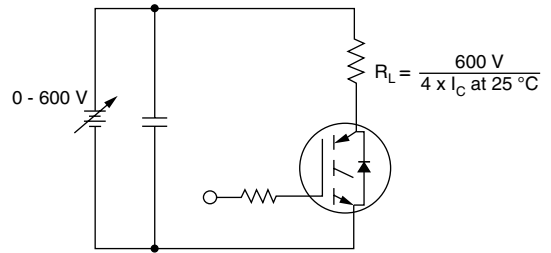


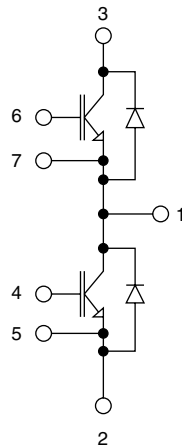
Fig. 19 - Pulsed Collector Current Test Circuit

ORDERING INFORMATION TABLE

Device code	G	A	75	T	S	120	U	PbF
	①	②	③	④	⑤	⑥	⑦	⑧

- 1** - Insulated gate bipolar transistor (IGBT)
- 2** - Generation 4, IGBT silicon, DBC construction
- 3** - Current rating (75 = 75 A)
- 4** - Circuit configuration (T = Half-bridge)
- 5** - Package indicator (INT-A-PAK)
- 6** - Voltage rating (120 = 1200 V)
- 7** - Speed/type (U = Ultrafast)
- 8** - PbF = Lead (Pb)-free

CIRCUIT CONFIGURATION

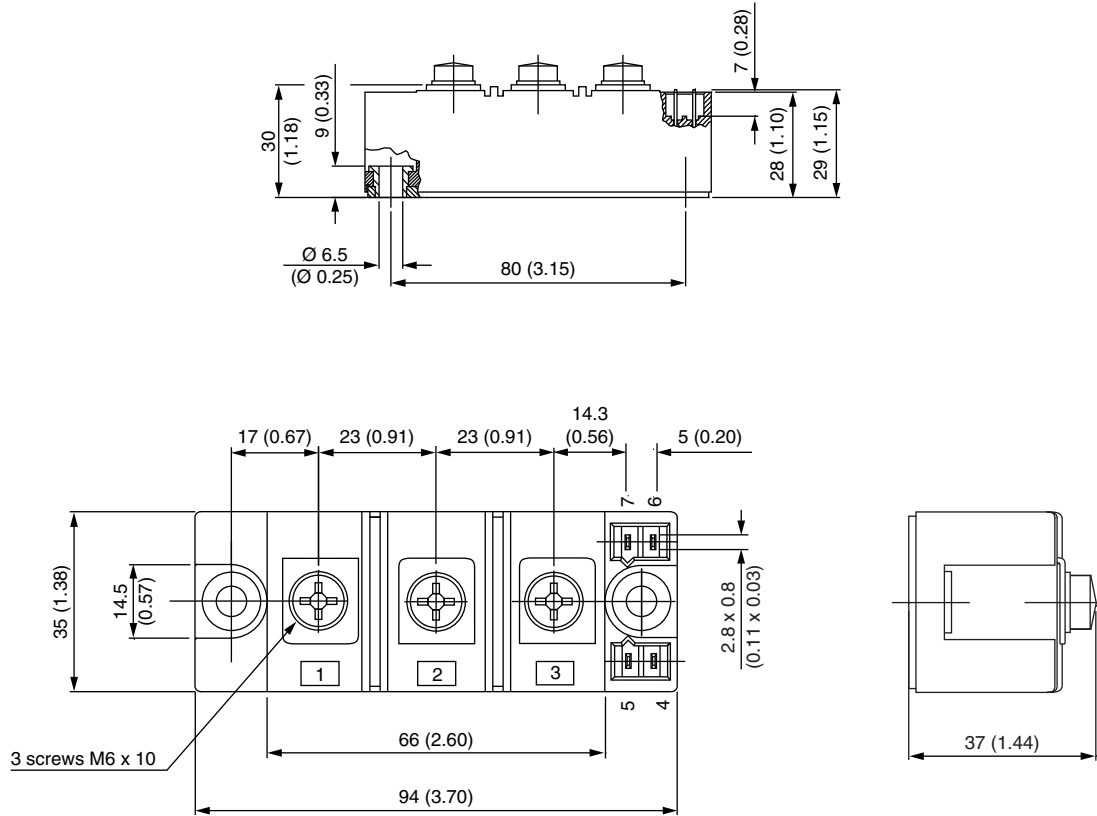


LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95173
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INT-A-PAK IGBT

DIMENSIONS in millimeters (inches)





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