19-0014; Rev 2; 7/96

MAXIM

# High-Voltage, Fault-Protected Analog Multiplexers



## General Description

The MAX388 8-channel single-ended (1-of-8) and the MAX389 4-channel differential (2-of-8) multiplexers (muxes) with internal data latches use a high-voltage series N-channel, P-channel, N-channel structure that significantly improves fault protection over previous devices. If power is removed with input voltages still applied, all channels turn off, allowing only a few nanoamperes of input leakage current. This protects the mux and output circuitry, as well as the signal sources connected to the channel inputs.

When an overvoltage signal up to ±100V (typically ±110V) is applied to an analog input or output, the channel turns off. To further protect output circuitry from on-channel overvoltage, outputs are clamped to less than the power-supply voltage. Since there is no increase in supply current during fault conditions, power dissipation does not increase. The MAX388/MAX389 withstand full overvoltage on any combination of channels, including all channels simultaneously.

All channel selection and control inputs are TTL and CMOS compatible. And, break-before-make switch operation is guaranteed.

## Applications

Data-Acquisition Systems

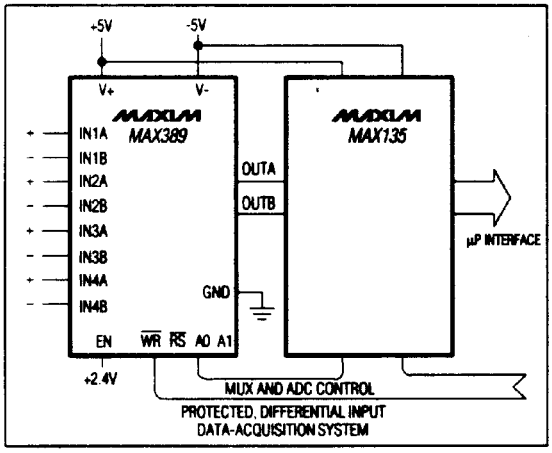
Industrial Process Control Systems

Avionics Test Equipment

Signal Routing Between Systems

Computer-Controlled Analog Data Logging

## Typical Operating Circuit




## Features

- ♦ Fault and Overvoltage Protection
- ♦ Fail-Safe with Power Loss (No Latchup)
- ♦ Break-Before-Make Switching
- ♦ All Channels Off when Power Off
- ♦ Internal Data Latches
- ♦ TTL and CMOS Compatible
- ♦ Operates from ±4.5V to ±18V Supplies
- ♦ On-Channels Turn Off during Overvoltage
- ♦ Nanoamperes Leakage in Overvoltage

## Ordering Information

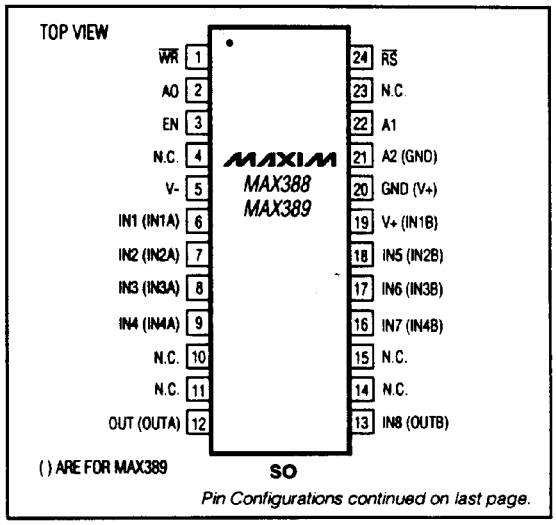
| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| MAX388CPN | 0°C to +70°C | 18 Plastic DIP |
| MAX388CJN | 0°C to +70°C | 18 CERDIP |
| MAX388CWG | 0°C to +70°C | 24 SO |
| MAX388C/D | 0°C to +70°C | Dice* |
| MAX388EPN | -40°C to +85°C | 18 Plastic DIP |
| MAX388EJN | -40°C to +85°C | 18 CERDIP |
| MAX388EWG | -40°C to +85°C | 24 SO |
| MAX388MJN | -55°C to +125°C | 18 CERDIP** |

*Ordering Information continued on last page.*

*Contact factory for dice specifications.

**Contact factory for availability and processing to MIL-STD1 883.

## Pin Configurations




*Pin Configurations continued on last page.*



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# High-Voltage, Fault-Protected Analog Multiplexers

## ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44V
V+ to GND ..... 22V
V- to GND ..... -22V
EN, $\overline{WR}$, $\overline{RS}$, A0-A2 ..... V+ + 4V to V- - 4V
Analog Input with V+ = 15V, V- = -15V ..... ±100V
Analog Input with V+ = V- = 0V ..... ±115V
Continuous Current, IN or OUT ..... 20mA
Peak Current, IN or OUT (Note 1) ..... 40mA

**Note 1:** Pulsed at 1ms, 10% maximum duty cycle.

Continuous Power Dissipation
24-Pin SO (derate 11.76mW/°C above +70°C ..... 941mW
18-Pin Plastic DIP (derate 11.1mW/°C above +70°C) .. 889mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) ..... 842mW
Operating Temperature Ranges
MAX38_C_ _ ..... 0°C to +70°C
MAX38_E_ _ ..... -40°C to +85°C
MAX38_MJN ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, GND = $\overline{WR}$ = 0V, $\overline{RS}$ = +2.4V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | | C, E SUFFIXES MIN | C, E SUFFIXES TYP | C, E SUFFIXES MAX | M SUFFIX MIN | M SUFFIX TYP | M SUFFIX MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Analog Signal Range | $V_{ANALOG}$ | (Note 4) | | | -15 | | 15 | -15 | | 15 | V |
| Drain-Source On Resistance | $r_{DS(ON)}$ | $V_D$ = ±10V, $V_{AL}$ = 0.8V, $I_S$ = 100µA, $V_{AH}$ = 2.4V | | | | 2.0 | 3.0 | | 2.0 | 3.0 | kΩ |
| | | | | $T_{MAX}$ | | 3.0 | 4.0 | | 3.0 | 4.0 | |
| Greatest Change in $r_{DS(ON)}$ Between Channels | $\Delta r_{DS(ON)}$ | -10V < VS < 10V | | | | 10 | | | 10 | | % |
| Source-Off Leakage Current (Note 2) | $I_{IN(OFF)}$ | $V_{EN}$ = 0.8V, $V_{IN}$ = ±10V, $V_{OUT}$ = ±10V | | | | 0.03 | ±1.00 | | 0.03 | ±0.50 | nA |
| | | | | $T_{MAX}$ | | | ±50 | | | ±50 | |
| Drain-Off Leakage Current (Note 2) | $I_{OUT(OFF)}$ | $V_{EN}$ = 0.8V, $V_{IN}$ = ±10V, $V_{OUT}$ = ∓10V | MAX388 | | | 0.1 | ±2.0 | | 0.1 | ±1.0 | nA |
| | | | | $T_{MAX}$ | | | ±200 | | | ±200 | |
| | | | MAX389 | | | | ±2.0 | | | ±1.0 | |
| | | | | $T_{MAX}$ | | | ±100 | | | ±100 | |
| Drain-On Leakage Current (Note 2) | $I_{OUT(ON)}$ | $V_{EN}$ = $V_{AH}$ = 2.4V, $V_{OUT}$ = $V_{IN}$ = ±10V, $V_{AL}$ = 0.8V | MAX388 | | | | ±20 | | | ±20 | nA |
| | | | | $T_{MAX}$ | | | ±600 | | | ±1000 | |
| | | | MAX389 | | | | ±20 | | | ±20 | |
| | | | | $T_{MAX}$ | | | ±300 | | | ±600 | |
| **LOGIC INPUT** | | | | | | | | | | | |
| Logic Input Current (Input Voltage High) | $I_{AH}$ | $V_A$ = 2.4V (Note 3) | | | | | ±1 | | | ±1 | µA |
| | | $V_A$ = 14V (Note 3) | | | | | ±1 | | | ±1 | |
| Logic Input Current (Input Voltage Low) | $I_{AL}$ | $V_{EN}$ = 0V or 2.4V, $V_A$ = $\overline{RS}$ = $\overline{WR}$ = 0V | | | | | ±1 | | | ±1 | µA |
| **FAULT** | | | | | | | | | | | |
| Output Leakage Current with Overvoltage | $I_{OUT(OFF)}$ | $V_{OUT}$ = 0V, $V_{IN}$ = ±60V, (Note 5) | | | | | ±0.05 | | | ±0.02 | µA |
| | | | | $T_{MAX}$ | | | 20 | | | 10 | µA |
| Input Leakage Current with Overvoltage | $I_{IN(OFF)}$ | $V_{IN}$ = ±60V, $V_{OUT}$ = ±10V, (Note 5) | | | | | 40 | | | 25 | µA |
| Input Leakage Current with Power Supplies Off | $I_{IN(OFF)}$ | $V_{IN}$ = ±100V, $V_{EN}$ = $V_{OUT}$ = 0V, A0 = A1 = A2 = 0V or 5V | | | | | 20 | | | 10 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = $\overline{WR}$ = 0V, $\overline{RS}$ = +2.4V, $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | C, E SUFFIXES MIN | C, E SUFFIXES TYP | C, E SUFFIXES MAX | M SUFFIX MIN | M SUFFIX TYP | M SUFFIX MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| **DYNAMIC** | | | | | | | | | | |
| Multiplexer Switching Time | $t_{TRANS}$ | Figure 2 | | | 0.5 | 1.0 | | 0.5 | 1.0 | µs |
| Break-Before-Make Interval | $t_{OPEN}$ | Figure 3 | | | 0.2 | | | 0.2 | | µs |
| Enable or Write Turn-On Time | $t_{ON(EN)}$ $t_{ON(\overline{WR})}$ | Figures 4 and 5 | | | 1.0 | 1.5 | | 1.0 | 1.5 | µs |
| Enable or Write Turn-Off Time | $t_{OFF(EN)}$ $t_{OFF(\overline{WR})}$ | Figures 4 and 6 | | | 0.4 | 1.0 | | 0.4 | 1.0 | µs |
| Charge Injection | Q | Figure 7, Tables 1a and 1b | | | 55 | | | 55 | | pC |
| Off Isolation | OIRR | $V_{EN}$ = 0V, $R_L$ = 1kΩ, $C_L$ = 15pF, $V_{IN}$ = 7$V_{RMS}$, f = 100kHz | | | 68 | | | 68 | | dB |
| Logic Input Capacitance with Switch Off | $C_{IN}$ | f = 1MHz | | | 5 | | | 5 | | pF |
| Input Capacitance with Switch Off | $C_{S(OFF)}$ | VEN = 0V, $V_{IN}$ = 0V, f = 140kHz | | | 5 | | | 5 | | pF |
| Output Capacitance with Switch Off | $C_{D(OFF)}$ | $V_{EN}$ = 0V, f = 140kHz, $V_{OUT}$ = 0V | MAX388 | | 25 | | | 25 | | pF |
| | | | MAX389 | | 12 | | | 12 | | |
| $\overline{WR}$ Pulse Width | $t_{WW}$ | Figure 1 | | 300 | | | 300 | | | ns |
| Ax, EN Data Valid to $\overline{WR}$ | $t_{DW}$ | Setup time, Figure 1 | | 210 | | | 180 | | | ns |
| Ax, EN Data Valid after $\overline{WR}$ | $t_{WD}$ | Hold time, Figure 1 | | 30 | | | 10 | 0 | | ns |
| $\overline{RS}$ Pulse Width | $t_{RS}$ | $V_{IN}$ = 5V, Figure 1 | | 500 | | | 300 | | | ns |
| **SUPPLY** | | | | | | | | | | |
| Supply Range | | (Note 6) | | ±4.5 | | ±18.0 | ±4.5 | | ±18.0 | V |
| Positive Supply Current | I+ | $V_{EN}$ = 2.4V, $V_A$ = 0V or 5V | | | 1.0 | 2.0 | | 1.0 | 2.0 | mA |
| Negative Supply Current | I- | | | | 1.2 | 2.5 | | 1.2 | 2.5 | |

**Note 2:** Leakage currents at $T_{MIN}$ guaranteed, but not tested.

**Note 3:** Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

**Note 4:** When the analog signal exceeds +13.5V or -12V, the blocking action of Maxim's gate structure operates. Only leakage currents flow, and the channel on resistance rises.

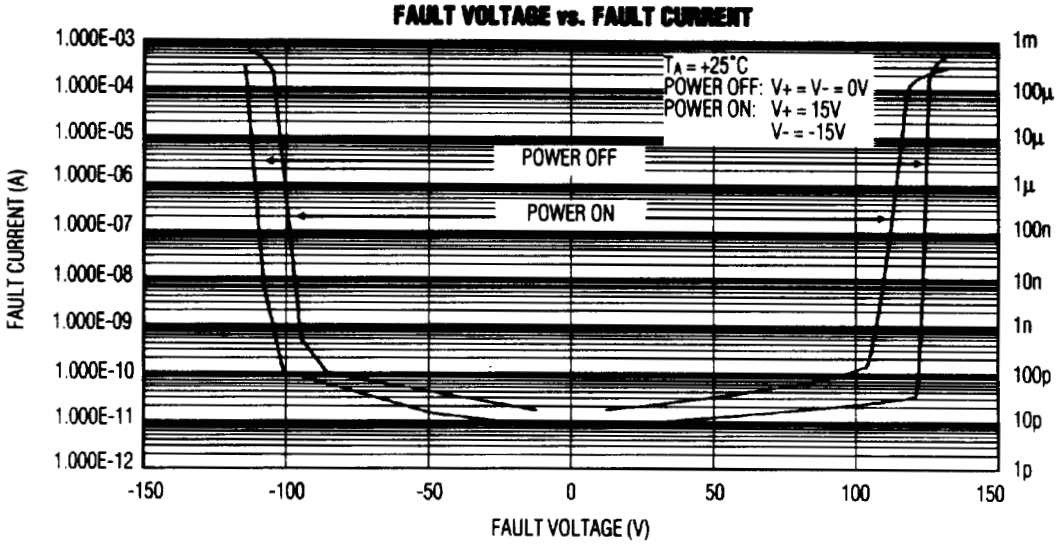
**Note 5:** The value shown is the steady-state value. The transient leakage is typically 50µA. *See Detailed Description.*

**Note 6:** Electrical characteristics such as $r_{DS(ON)}$ will change when power supplies other than ±15V are used.

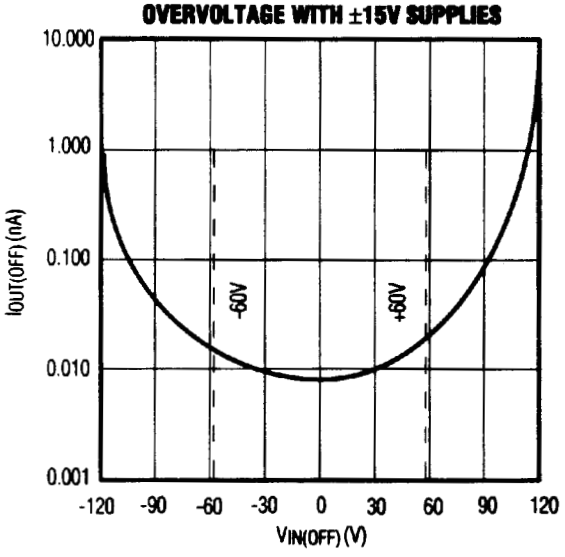
# High-Voltage, Fault-Protected Analog Multiplexers

## Typical Operating Characteristics

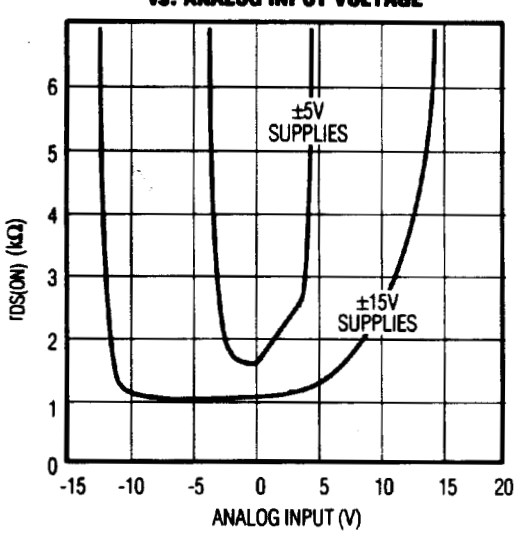
**FAULT VOLTAGE vs. FAULT CURRENT**




**OUTPUT LEAKAGE vs. OFF-CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES**




**$r_{DS(ON)}$ vs. ANALOG INPUT VOLTAGE**



## Detailed Description

### Fault-Protection Circuitry

The MAX388/MAX389 are fully fault-protected for continuous input voltages up to ±100V, whether or not the V+ and V- power supplies are present (±115V with power off). These muxes use a series FET* switching scheme that protects the mux output from overvoltage while limiting the input current to sub-microamp levels. Figures 7 and 8 show input leakage-current levels during overvoltage (Figure 7) and with power off (Figure 8).

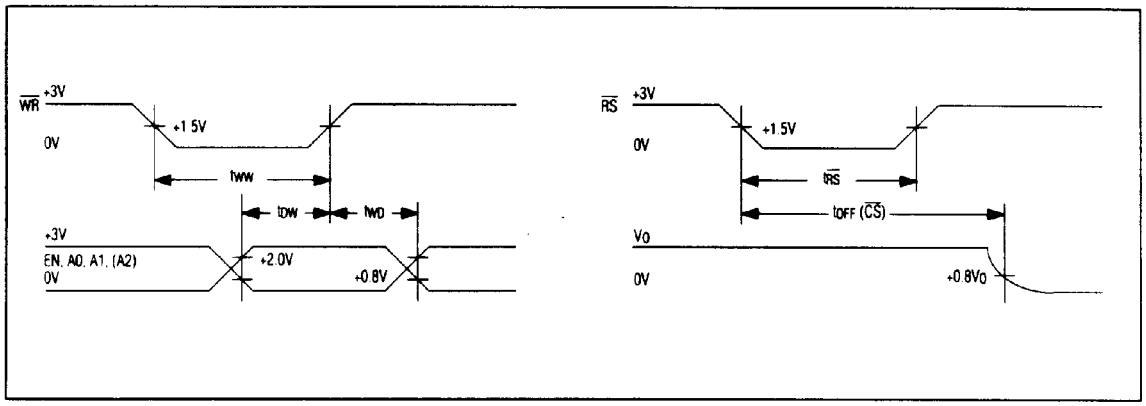



*Figure 1. MAX388/MAX389 Typical Timing Diagrams*

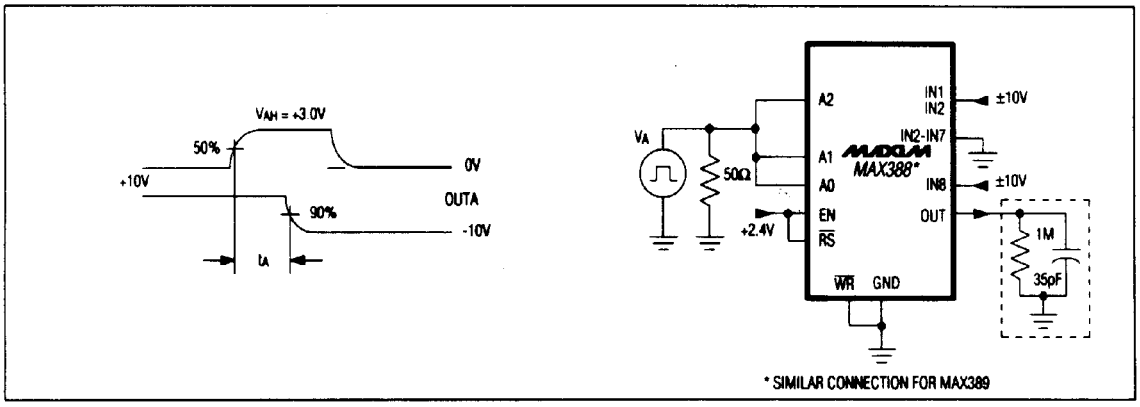



*Figure 2. Access Time vs. Logic Level (High)*

# High-Voltage, Fault-Protected Analog Multiplexers

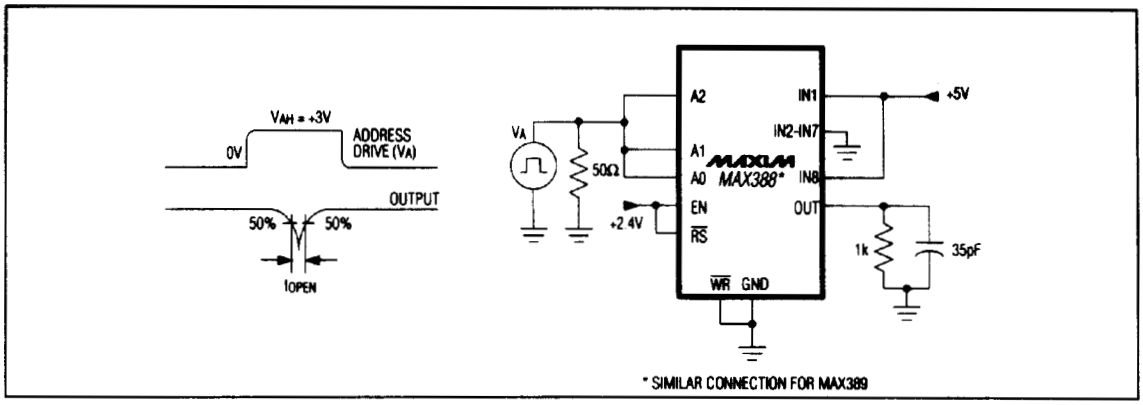



*Figure 3. Break-Before-Make Delay ($t_{OPEN}$)*

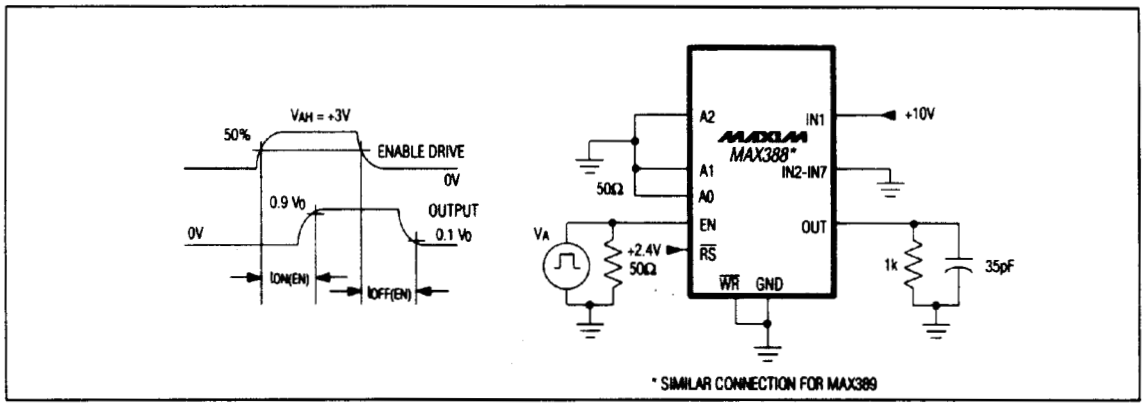



*Figure 4. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)*

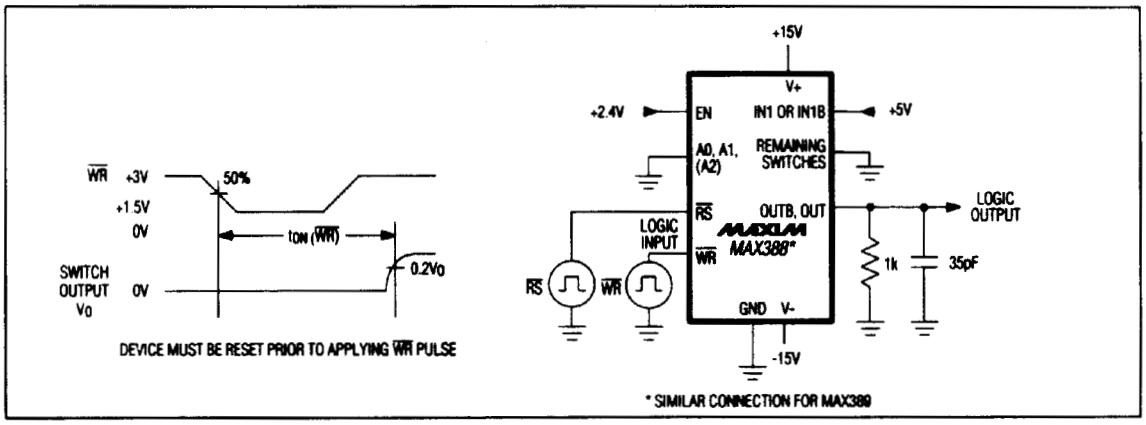



*Figure 5. Write Turn-On Time ($t_{ON(\overline{WR})}$)*

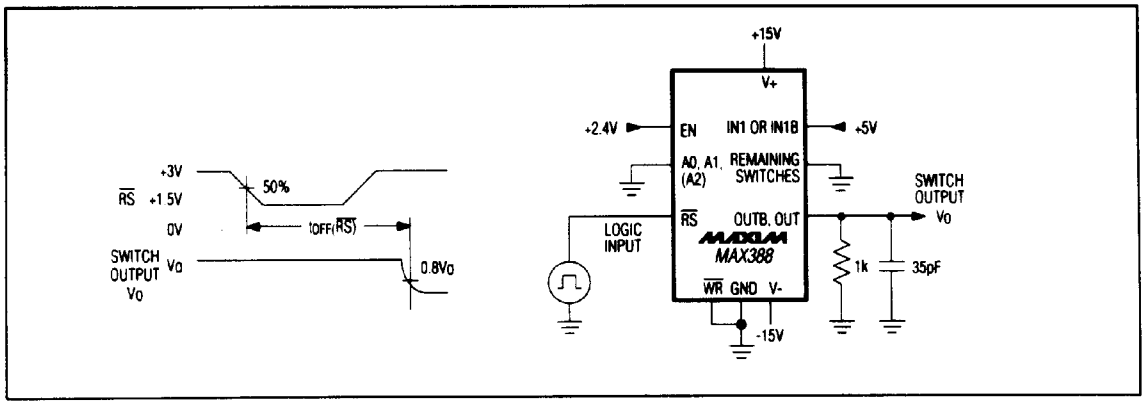



*Figure 6. Reset Turn-Off Time ($t_{OFF(\overline{RS})}$)*

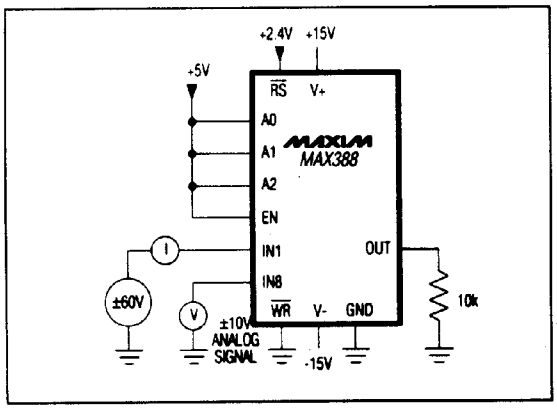



*Figure 7. Input Leakage Current (Overvoltage)*

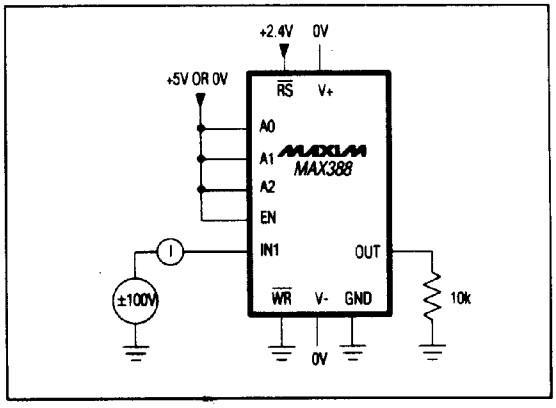



*Figure 8. Input Leakage Current (Power Supplies Off)*

Figures 9 and 10 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -100V input, N-channel FET Q1 is turned on by the +100V gate-to-source voltage. However, the P-channel device Q2 with a $V_{GS}$ of +100V turns off, thereby preventing the input signal from reaching the output. If the input voltage is +100V, Q1 has a negative $V_{GS}$, which turns it off. Similarly, with overvoltage on the output, only sub-microamp leakage currents flow from the output back to the input, since overvoltages turn off either Q1 or Q2.

Figure 11 shows an off channel with V+ and V- present. As with Figures 9 and 10, either an N-channel or a P-channel device will be off for any input voltage from -100V to +100V. The leakage current with negative overvoltages immediately drops to a few nanoamps at +25°C. The fault current for positive overvoltages is initially 40µA to 50µA, decaying over a few seconds to the nanoamp level. The time constant of this decay is due to stored charge on internal nodes and does not compromise fault-protection.

Figure 12 shows an on channel with V+ and V- present. With input voltages less than ±10V, all three FETs are on, and the input signal appears at the output. If the input voltage exceeds V+ minus the N-channel threshold voltage ($V_{TN}$), the N-channel FET will turn off. Since $V_{TN}$ is typically 1.5V and the P-channel threshold voltage ($V_{TP}$) is typically 3V, the muxes' output swing is limited to approximately -12V to +13.5V with ±15V supplies.

# High-Voltage, Fault-Protected Analog Multiplexers

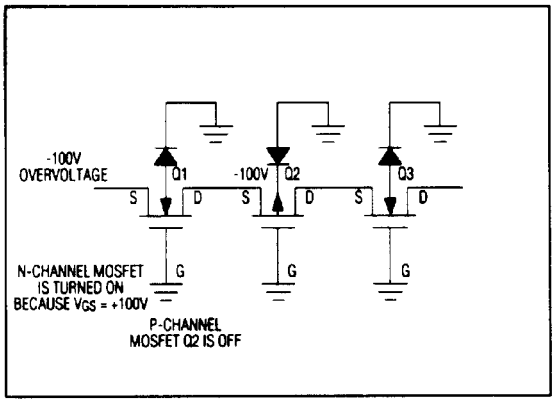



*Figure 9. -100V Overvoltage with Mux Power Off*

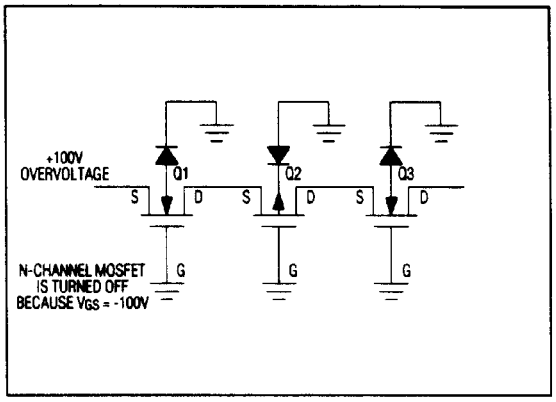



*Figure 10. +100V Overvoltage with Mux Power Off*

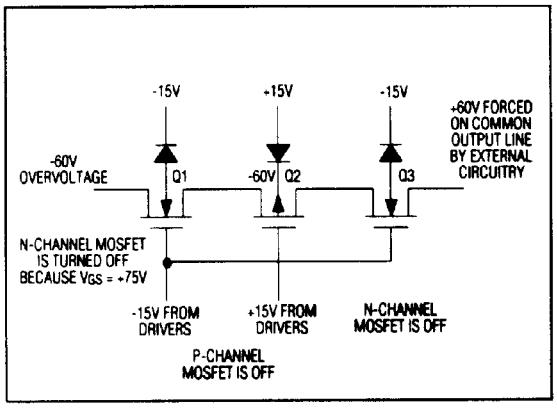



*Figure 11. Off-Channel Overvoltage (-60V) with Mux Power On*

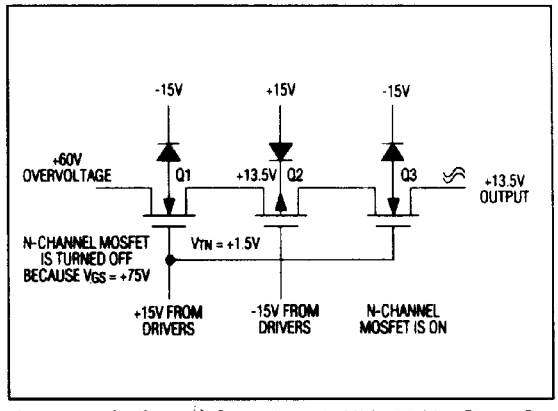



*Figure 12. On-Channel Overvoltage (+60V) with Mux Power On*

The *Typical Operating Characteristics* graphs show typical fault leakage vs. fault voltage curves. The MAX388/MAX389 muxes perform well up to the ±115V maximum rating, providing an additional safety margin.

### Switching Characteristics and Charge Injection

MAX388/MAX389 channel-to-channel switching time is typically 600ns, including approximately 200ns of break-before-make delay. This delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data-acquisition system (Figure 13), the dominant delay is not the MAX388 mux switching time, but the settling time of the following amplifiers and sample-and-hold (S/H). Another limiting factor is the RC time constant formed by the mux $r_{DS(ON)}$ plus the signal source impedance times the load capacitance on the mux output. Even with low signal-source impedances, 100pF capacitance on the mux output approximately doubles the settling time to 0.01% accuracy.

Tables 2a and 2b show typical charge injection levels vs. power-supply voltage and analog input voltages. Note: Since channels are well matched, differential charge injection for the MAX389 is typically less than 5pC. Charge injection that occurs during switching creates a voltage transient with a magnitude inversely proportional to mux output capacitance.

**Table 1a. MAX388 Truth Table**

| A2 | A1 | A0 | EN | $\overline{WR}$ | $\overline{RS}$ | ON SWITCH |
|---|---|---|---|---|---|---|
| **Latching** | | | | | | |
| X | X | X | X | ↓ | 1 | Maintains previous switch condition |
| **Reset** | | | | | | |
| X | X | X | X | X | 0 | NONE (latches cleared) |
| **Transparent Operation** | | | | | | |
| X | X | X | 0 | 0 | 1 | NONE |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 0 | 1 | 4 |
| 1 | 0 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 0 | 1 | 8 |

**Table 1b. MAX389 Truth Table**

| A1 | A0 | EN | $\overline{WR}$ | $\overline{RS}$ | ON SWITCH |
|---|---|---|---|---|---|
| **Latching** | | | | | |
| X | X | X | ↓ | 1 | Maintains previous switch condition |
| **Reset** | | | | | |
| X | X | X | X | 0 | NONE (latches cleared) |
| **Transparent Operation** | | | | | |
| X | X | 0 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 0 | 1 | 4 |

**NOTE:** Logic "1" : $V_{AH} \geq 2.4V$, Logic "0" : $V_{AL} \leq 0.8V$

### *Operation from Supply Voltages Other than ±15V*

The main limitation of supply voltages other than ±15V is a reduction in output signal range. The MAX388 limits the output voltage to typically 1.5V below V+ and 3V above V-. Output swing is limited to +3.5V to -2V when operating from ±5V. The *Typical Operating Characteristics* graphs show typical $r_{DS(ON)}$ for ±15V, ±10V, and ±5V supplies. Operation is guaranteed for ±4.5V to ±18V supplies. Switching delays increase by a factor of two or more at ±5V, but break-before-make operation is preserved.

The MAX388/MAX389 may be powered from a single +9V to +22V supply, as well as from unbalanced supplies such as +15V and -5V. Connect V- to 0V when operating with a +9V to +22V single supply. The digital threshold remains approximately 1.6V above GND, and analog characteristics (such as $r_{DS(ON)}$) are determined by total voltage difference between V+ and V-. This means the MAX388/MAX389 operate with standard TTL logic levels, even with ±5V power supplies.

**Table 2a. MAX388 Charge Injection**

| Supply Voltage (V) | Analog Input Level (V) | Injected Charge (pC) |
|---|---|---|
| ±5 | 1.7<br>0.0<br>-1.7 | 100<br>70<br>45 |
| ±10 | 5.0<br>0.0<br>-5.0 | 200<br>130<br>60 |
| ±15 | 10.0<br>0.0<br>-10.0 | 500<br>180<br>50 |

Test Conditions: $C_L$ = 1000pF on mux output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, A1 = A2 = 0V, A0 is toggled at 2kHz rate between 0V and 3V. +100pC of charge creates a +100mV step when injected into a 1000pF load capacitance.

# High-Voltage, Fault-Protected Analog Multiplexers

**Table 2b. MAX389 Charge Injection**

| Supply Voltage (V) | Analog Input Level (V) | Injected Charge (pC) | | |
|---|---|---|---|---|
| | | OUTA | OUTB | Differential A-B |
| ±5 | 1.7 | 105 | 107 | -2 |
| | 0.0 | 73 | 74 | -1 |
| | -1.7 | 48 | 50 | -2 |
| ±10 | 5.0 | 215 | 220 | -5 |
| | 0.0 | 135 | 139 | -4 |
| | -5.0 | 62 | 63 | -1 |
| ±15 | 10.0 | 525 | 530 | -5 |
| | 0.0 | 180 | 185 | -5 |
| | -10.0 | 55 | 55 | 0 |

Test Conditions: $C_L$ = 1000pF on OUTA and OUTB; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A1 = 0V, A0 is toggled from 0V to 3V at a 2kHz rate.

### Digital-Interface Levels

The typical digital threshold of both the address lines and the Enable (EN) input is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with a 0.8V to 2.4V TTL logic swing over the entire temperature range. The digital threshold is relatively independent of the supply voltages, typically moving from 1.6V to 1.5V as the power supplies are reduced from ±15V to ±5V. In all cases, digital thresholds are referenced to GND.

The digital inputs can also be driven with CMOS logic levels swinging from either V+ to V- or from V+ to GND. Digital input current is just a few nanoamps leakage at all input voltage levels, with a guaranteed maximum of 1µA. The digital inputs are protected from ESD by a 30V zener diode between the input and V+, and can be driven ±4V beyond the supplies without drawing excessive current.

### Operation as Demultiplexers

The MAX388/MAX389 function as demultiplexers when an input is applied to the Output (OUT) pin, and channel inputs are used as outputs. Break-before-make operation and full fault protection are provided when operating as demultiplexers, unlike first-generation fault-protected muxes.

**Table 3a. Typical Off-Isolation Rejection Ratio**

| Frequency (Hz) | 100k | 500k | 1M |
|---|---|---|---|
| One Channel Driven (dB) | 74 | 72 | 66 |
| All Channels Driven (dB) | 64 | 48 | 44 |

Test Conditions: $V_{IN}$ = $20V_{p-p}$ at the tabulated frequency, $R_L$ = 1.5k between OUT and GND, EN = 0V.

$$OIRR = 20\log \frac{20V}{V_{OUT}}$$

**Table 3b. Typical Crosstalk Rejection Ratio**

| Frequency (Hz) | 100k | 500k | 1M |
|---|---|---|---|
| $F_L$ = 1.5k (dB) | 70 | 68 | 64 |
| $R_L$ = 10k (dB) | 62 | 46 | 42 |

Test Conditions: Specified $R_L$ connected from OUT to Ground, EN = +5V, A0 = A1 = A2 = +5V (channel 1 selected). 20Vp-p at the tabulated frequency is applied to channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

### Leakage, Crosstalk, and Isolation

At DC and low frequencies, channel-to-channel crosstalk is caused by variation in output leakage currents as the off-channel input voltages are varied. The MAX388 ouput leakage varies only a few picoamps as all seven off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX388 output ($r_{DS(ON)}$ plus the input-signal source resistance), since the load driven by the MAX388 is usually a high impedance. For a signal source impedance of 10kΩ or lower, DC crosstalk exceeds 120dB.

Tables 3a and 3b show typical AC crosstalk and off-isolation performance. Digital feedthrough is masked by analog charge injection when the output is enabled. When the output is disabled, digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GND and V- pins. The guard formed by these lines is continued onto the MAX388/MAX389 die to provide over 100dB isolation between the digital and analog sections at f = 100kHz.

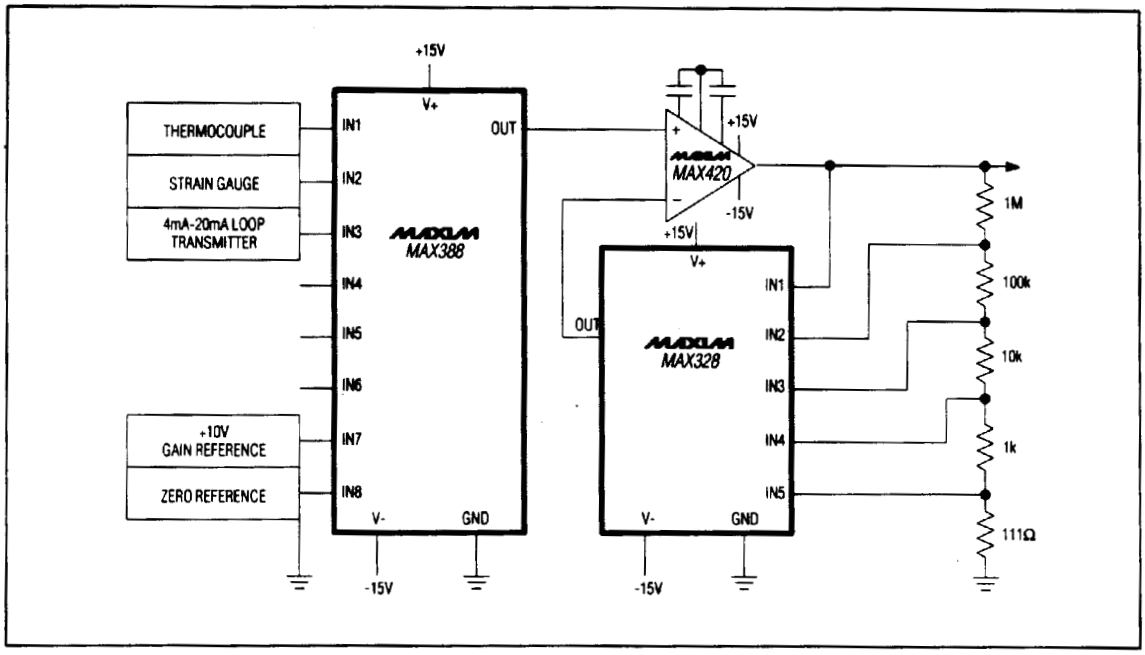



*Figure 13. Typical Data-Acquisition Front End*

## Applications Information

Figure 13 shows a typical data-acquisition system incorporating the MAX388. Since the mux is driving a high-impedance input, the error is a function of the mux on resistance ($r_{DS(ON)}$) times the leakage current ($I_{OUT(ON)}$) and the amplifier bias current ($I_{BIAS}$):

$$V_{ERR} = [r_{DS(ON)}]\,[I_{OUT(ON)} + I_{BIAS}(MAX420)]$$
$$= (3k\Omega)\,(2nA + 30pA)$$
$$= 6.1\mu V \text{ maximum error}$$

In most cases, this error is low enough that preamplification of input signals is not needed, even with very low-level signals, such as 40µV/°C from type J thermocouples.

In systems with fewer than eight inputs, an unused channel can be connected to the system ground reference point for software-zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data-acquisition system as well.

A MAX420 precision op amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed 5µV unadjusted MAX420 offset voltage maintains high-signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data-acquisition system, normally an S/H and an ADC. Since the gain-changing mux is not connected to external sensors and this point in the circuit does not require fault protection, the MAX328 low-leakage mux works well here.

Input switching, however, needs fault protection to provide the protection and isolation required for most data-acquisition inputs. Since external signal sources may continue to supply voltage when the system power is off, non-fault-protected muxes, or even first-generation fault-protected devices, allow many milliamps of fault current to flow from outside sources into the mux.

The MAX388/MAX389 eliminate these problems by limiting output voltage to safe levels (with or without power applied) and by turning all channels off when power is removed. Consequently, only sub-microamp fault currents are maintained for continuous input levels up to ±100V with power supplies off.

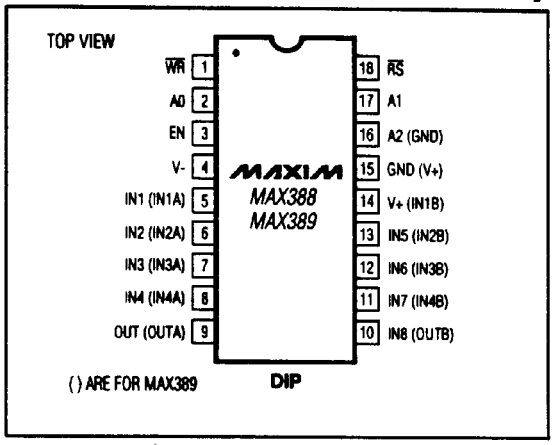
# High-Voltage, Fault-Protected Analog Multiplexers

## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| MAX389CPN | 0°C to +70°C | 18 Plastic DIP |
| MAX389CJN | 0°C to +70°C | 18 CERDIP |
| MAX389CWG | 0°C to +70°C | 24 SO |
| MAX389C/D | 0°C to +70°C | Dice* |
| MAX389EPN | -40°C to +85°C | 18 Plastic DIP |
| MAX389EJN | -40°C to +85°C | 18 CERDIP |
| MAX389EWG | -55°C to +125°C | 24 SO |
| MAX389MJN | -55°C to +125°C | 18 CERDIP** |

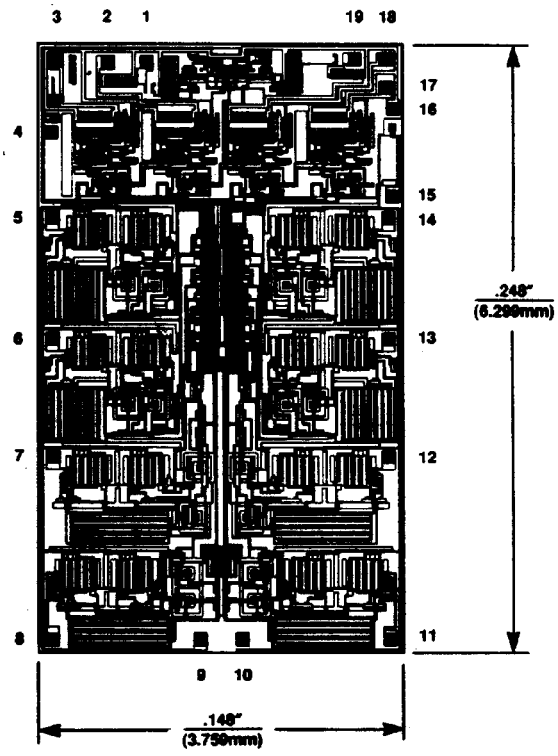
*Contact factory for dice specifications.
**Contact factory for availability and processing to MIL-STD-883.

## Pin Configurations (continued)




## Chip Topography

| DIE PAD # | MAX388 | MAX389 |
|---|---|---|
| 1 | $\overline{WR}$ | $\overline{WR}$ |
| 2 | A0 | A0 |
| 3 | EN | EN |
| 4 | V- | V- |
| 5 | IN1 | IN1A |
| 6 | IN2 | IN2A |
| 7 | IN3 | IN3A |
| 8 | IN4 | IN4A |
| 9 | OUT | OUTA |
| 10 | N.C. | OUTB |
| 11 | IN8 | IN4B |
| 12 | IN7 | IN3B |
| 13 | IN6 | IN2B |
| 14 | IN5 | IN1B |
| 15 | V+ | V+ |
| 16 | GND | GND |
| 17 | A2 | N.C. |
| 18 | A1 | A1 |
| 19 | $\overline{RS}$ | $\overline{RS}$ |

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