

**μPG2250T5N-EVAL-A**

**Evaluation Board**

- Circuit Description
- Performance data
- Circuit schematic and assembly drawing

## Circuit Description

The circuit schematic and assembly drawing are shown on the last two pages.

### Matching and Bias Circuits

The inductor L1 is for input matching and should be placed close to the device.

The output matching is realized mainly with the capacitor C6. C6 can be placed as close as possible to the device without much sacrifice of the performance when the layout space is tight. On the other hand the output power can be increased by a fraction of dB by moving C6 away from the device. The trace length between C6 and the device on this evaluation board is about 100 mil. Because of the gradual change in its width, the effect of this section of trace cannot be simply represented by a set of parameters of transmission line impedance and electrical length. It is recommended that the designer leave some space for tuning on this trace length in the initial prototype board layout if an optimal output power is desirable.

The uPG2250T5N has three gain stages, each being biased by an external voltage supply. The DC feed lines are not completely isolated from the RF path on the chip, and as a result care needs to be taken in the board layout for these DC lines.

The inductor L2 on the Vdd1 line provides the DC feed for the first stage and is part of the inter-stage matching between stage 1 and 2 as well. The value of this inductor may need to be adjusted on the application board to have the optimized performance. Generally it should be placed close to the device and immediately followed by the capacitor C2 as shown in the assembly drawing of this evalboard.

The length of trace TL1 on the Vdd2 line has significant impact on the output power and the value shown in the schematic should be used in the application board layout.

The inductor L3 is for the last stage DC feed and functions as an RF choke. Its value and location are not critical.

The three shunt capacitors on the DC lines (C2, C8 and C9) provide a low RF impedance at their respective locations. Their value should be in the range of 10 to 30pF. These low RF impedance spots adequately isolate the RF circuit from the rest of DC feed lines beyond the point of shunt capacitors. This arrangement is particularly beneficial in transferring the evaluation circuit to the end products because the RF characteristic of a DC feed line usually cannot be well controlled in a practical board design. The other three 0.01uF capacitors, C1, C3 and C5, are general bypass capacitors and the user can select their values and locations according the design requirements.

### PCB Material

The PCB is Getek two layer board. The board thickness is 28mil.

# Typical Performance Data

Test Conditions:

$f=2.45\text{GHz}$ ;  $P_{in}=-5\text{dBm}$ ;  $V_{cont}=1.8\text{V}$

For  $V_{DD1,2,3}=1.8\text{V}$

**Quiescent current  $I_{dsq}$ : 55mA;**

**Output Power  $P_{out}$ : 21dBm;**

**Supply Current  $I_{DD}$ : 130mA;**

**Efficiency PAE: 55%;**

For  $V_{DD1,2,3}=3\text{V}$

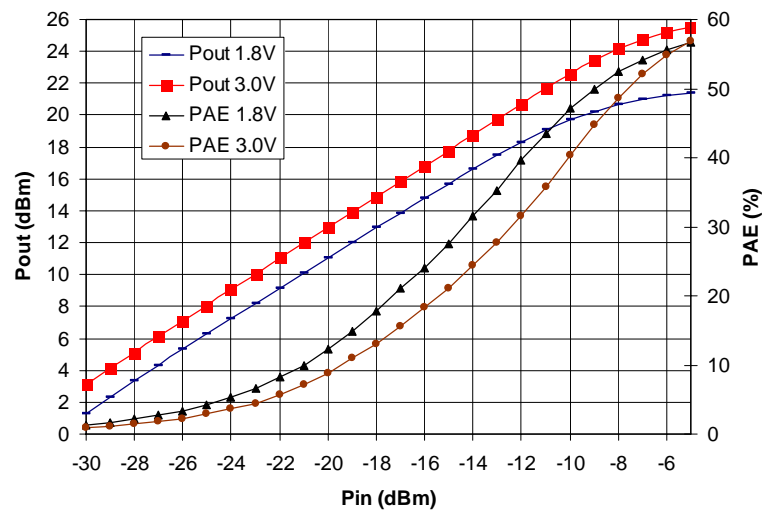
**Quiescent current  $I_{dsq}$ : 80mA;**

**Output Power  $P_{out}$ : 25dBm;**

**Supply Current  $I_{DD}$ : 200mA;**

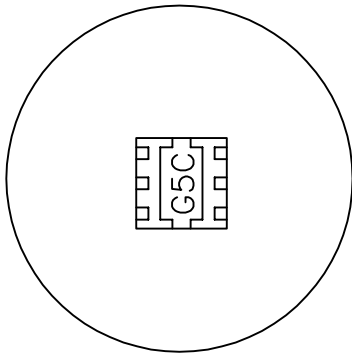
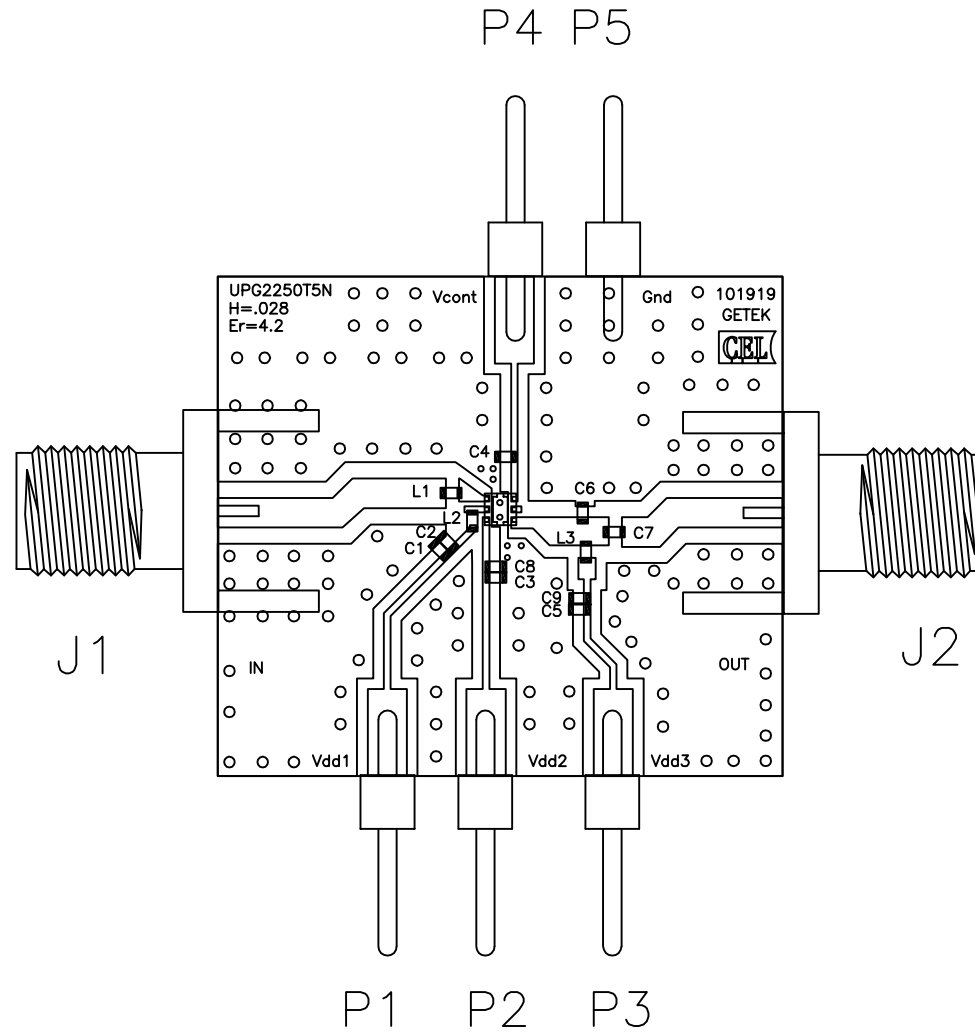
**Efficiency PAE: 55%;**

$P_{out}$  and PAE vs  $P_{in}$  are shown in the following plot.





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



APPROVALS		CALIFORNIA EASTERN LABS 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054		
Designed by:	BMU	01/03/2007	TITLE:	
Designed by:	BMU	01/03/2007	UPG2250T5N-EVAL-A	
Checked by:			ASSEMBLY_DRAWING	
Project Engineer:			SIZE	FSCM NO.
Quality Control:			C	DWG NO.
				AD-101919
				REV
				—

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