

For air-conditioner fan motor

# 3-Phase Brushless Fan Motor Controller

## BD62014AFS

### ● General Description

This controller synthesizes the optimal driving signal from hall sensor signals, and outputs the synthesized signal to control the external level shifter and power transistor. The replacement is also easy because of its pin compatibility with BD62011AFS and BD62012AFS. This controller provides optimum motor drive for a wide variety of applications, and enables motor unit standardization.

### ● Features

- 180° sinusoidal commutation logic
- PWM control (Upper and lower arm switching)
- Phase control supported from 0° to +40° at 1° intervals
- Rotational direction switch
- FG signal output with pulse number switch (4 or 12)
- VREG output (5V/30mA)
- Protection circuits provided: OCP, TSD, UVLO, MLP and the external fault input (FIB)

### ● Applications

- Air conditioners; air cleaners; water pumps; dishwashers; washing machines
- General OA equipment

### ● Key Specifications

- Supply voltage range: 10V to 18V
- Duty control voltage range: 1.1V to 4.4V
- Phase control range: 0° to 40°
- Operating temperature: -40°C to 110°C
- Junction Temperature: +150°C
- Power dissipation: 1.0W

### ● Package

SSOP-A24

W (Typ.) x D (Typ.) x H (Max.)  
10.00 mm x 7.80 mm x 2.10 mm



### ● Typical Application Circuit

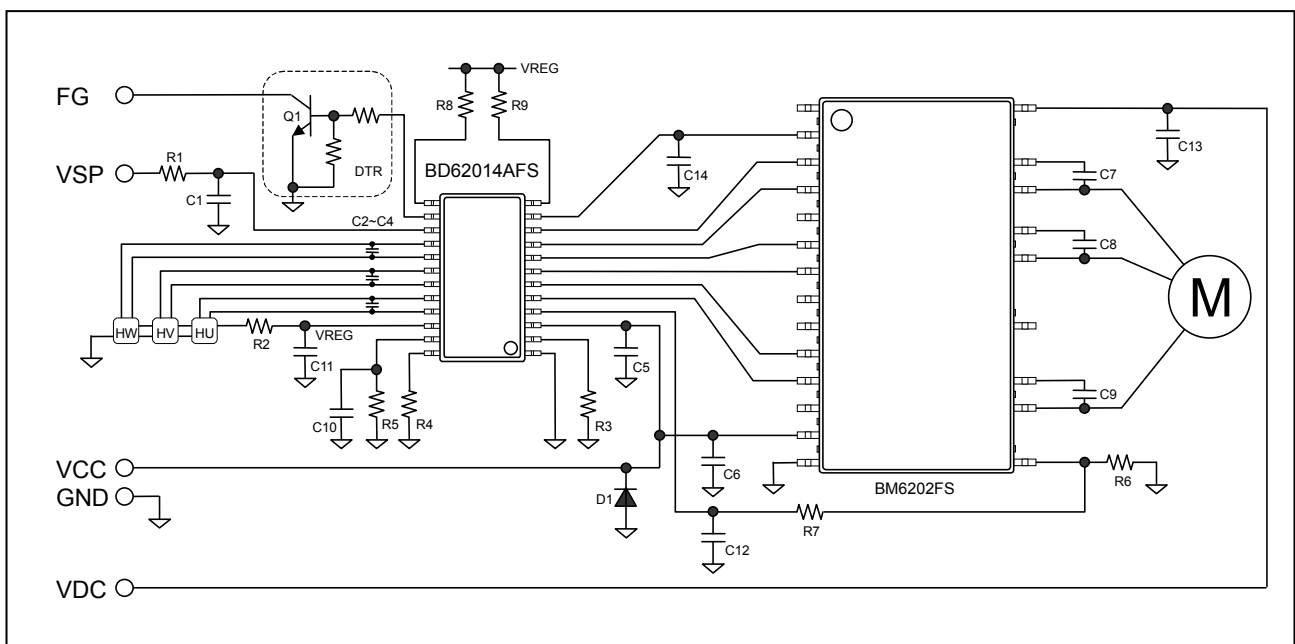


Figure 1. Application circuit example - BD62014AFS & BM6202FS

● Block Diagram and Pin Configuration

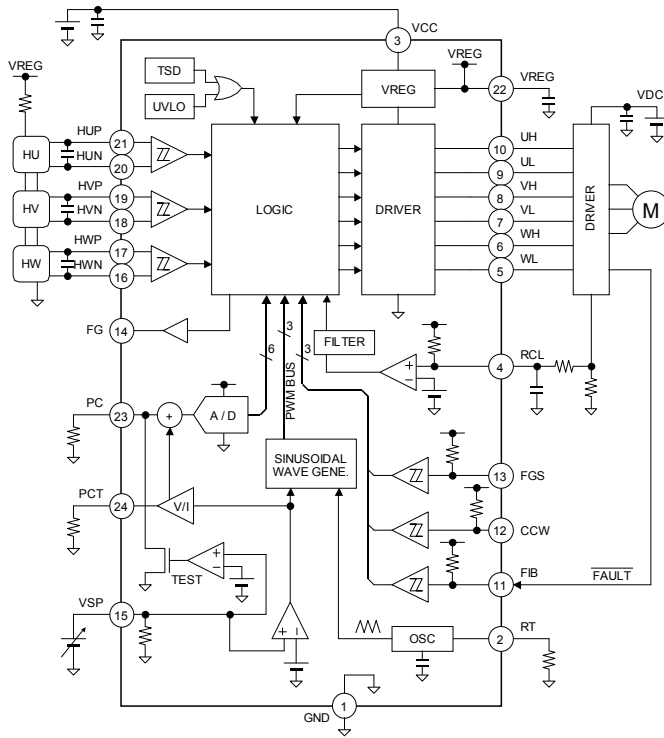


Figure 2. Block diagram

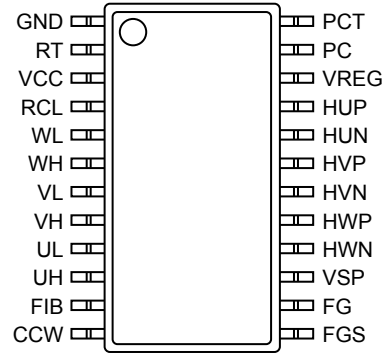


Figure 3. Pin configuration

● Pin Descriptions

| Pin | Name | Function                          | Pin | Name | Function                       |
|-----|------|-----------------------------------|-----|------|--------------------------------|
| 1   | GND  | Signal ground                     | 24  | PCT  | VSP offset voltage output pin  |
| 2   | RT   | Carrier frequency setting pin     | 23  | PC   | Phase control input pin        |
| 3   | VCC  | Power supply                      | 22  | VREG | Regulator output               |
| 4   | RCL  | Over current sense pin            | 21  | HUP  | Hall input pin phase U+        |
| 5   | WL   | Low side driver output phase W    | 20  | HUN  | Hall input pin phase U-        |
| 6   | WH   | High side driver output phase W   | 19  | HVP  | Hall input pin phase V+        |
| 7   | VL   | Low side driver output phase V    | 18  | HVN  | Hall input pin phase V-        |
| 8   | VH   | High side driver output phase V   | 17  | HWP  | Hall input pin phase W+        |
| 9   | UL   | Low side driver output phase U    | 16  | HWN  | Hall input pin phase W-        |
| 10  | UH   | High side driver output phase U   | 15  | VSP  | Duty control voltage input pin |
| 11  | FIB  | External fault input (Low active) | 14  | FG   | FG signal output               |
| 12  | CCW  | Direction switch (H:CCW)          | 13  | FGS  | FG pulse # switch (H:12, L:4)  |

## ● Functional Descriptions

### 1) Commutation logic

When the hall cycle is about 5-Hz or less (e.g. when the motor starts up), the commutation mode is 120° square wave drive with upper and lower switching (no lead angle). The controller monitors the hall cycle, and switches to 180° sinusoidal commutation drive when the hall cycle reaches or exceeds about 5-Hz over four consecutive cycles. Refer to the timing charts in figures 7 and 8.

Table 1. 120° commutation (Six-state) truth table (CW)

| HU | HV | HW | UH  | VH  | WH  | UL                      | VL                      | WL                      |
|----|----|----|-----|-----|-----|-------------------------|-------------------------|-------------------------|
| H  | L  | H  | L   | PWM | L   | H                       | $\overline{\text{PWM}}$ | L                       |
| H  | L  | L  | L   | L   | PWM | H                       | L                       | $\overline{\text{PWM}}$ |
| H  | H  | L  | L   | L   | PWM | L                       | H                       | $\overline{\text{PWM}}$ |
| L  | H  | L  | PWM | L   | L   | $\overline{\text{PWM}}$ | H                       | L                       |
| L  | H  | H  | PWM | L   | L   | $\overline{\text{PWM}}$ | L                       | H                       |
| L  | L  | H  | L   | PWM | L   | L                       | $\overline{\text{PWM}}$ | H                       |

### 2) Duty control

The switching duty can be controlled by forcing DC voltage with value from  $V_{SPMIN}$  to  $V_{SPMAX}$  to the VSP pin. When the VSP voltage is higher than  $V_{SPTST}$ , the controller forces PC pin voltage to ground (Testing mode, maximum duty and no lead angle). The VSP pin is pulled down internally by a 200 kΩ resistor. Therefore, note the impedance when setting the VSP voltage with a resistance voltage divider.

### 3) Carrier frequency setting

The carrier frequency setting can be freely adjusted by connecting an external resistor between the RT pin and ground. The RT pin is biased to a constant voltage, which determines the charge current to the internal capacitor. Carrier frequencies can be set within a range from about 16 kHz to 50 kHz. Refer to the formula to the right.

$$F_{OSC} [\text{kHz}] = \frac{400}{R_T [\text{k}\Omega]}$$

### 4) FG signal output

The number of FG output pulses can be switched in accordance with the number of poles and the rotational speed of the motor. The FG signal is output from the FG pin. The 12-pulse signal is generated from the three hall signals (exclusive NOR), and the 4-pulse signal is the same as hall U signal. It is recommended to pull up FGS pin to VREG voltage when malfunctioning because of the noise.

| FGS | No. of pulse |
|-----|--------------|
| H   | 12           |
| L   | 4            |

### 5) Direction of motor rotation setting

The direction of rotation may be switched by the CCW pin. When CCW pin is "H" or open, the motor rotates at CCW direction. When the real direction is different from the setting, the commutation mode is 120° square wave drive (no lead angle). It is recommended to pull up CCW pin to VREG voltage when malfunctioning because of the noise.

| CCW | Direction |
|-----|-----------|
| H   | CCW       |
| L   | CW        |

### 6) Hall signal comparator

The hall comparator provides voltage hysteresis to prevent noise malfunctions. The bias current to the hall elements should be set to the input voltage amplitude from the element, at a value higher than the minimum input voltage,  $V_{HALLMIN}$ . We recommend connecting a ceramic capacitor with value from 100 pF to 0.01 μF, between the differential input pins of the hall comparator. Note that the bias to hall elements must be set within the common mode input voltage range  $V_{HALLCM}$ .

### 7) Output duty pulse width limiter

Pulse width duty is controlled during PWM switching in order to ensure the operation of external power transistor. The controller doesn't output pulse of less than  $T_{MIN}$  (0.8 $\mu$ s minimum). Dead time is forcibly provided to prevent external power transistors to turn-on simultaneously in upper and lower side in driver output (for example, UH and UL) of each arm. This will not overlap the minimum time  $T_{DT}$  (1.6 $\mu$ s minimum). Because of this, the maximum duty of 120° square wave drive at start up is 90% (typical).

### 8) Phase control setting

The driving signal phase can be advanced to the hall signal for phase control. The lead angle is set by forcing DC voltage to the PC pin. The input voltage is converted digitally by a 6-bit A/D converter, in which internal VREG voltage is assumed to be full-scale, and the converted data is processed by a logic circuit. The lead angle can be set from 0° to +40° at 1° intervals, and updated fourth hall cycle of phase W falling edge. Phase control function only operates at sinusoidal commutation mode. However, the controller forces PC pin voltage to ground (no lead angle) during testing mode. The VSP offset voltage (Figure 29) is buffered to PCT pin, to connect an external resistor between PCT pin and ground. The internal bias current is determined by PCT voltage and the resistor value -  $V_{PCT} / R_{PCT}$  -, and mixed to PC pin. As a result, the lead angle setting is followed with the duty control voltage, and the performance of the motor can be improved. Please select the  $R_{PCT}$  value from 50 k $\Omega$  to 200 k $\Omega$  in the range on the basis of 100 k $\Omega$ , because the PCT pin current capability is a 100  $\mu$ A or less.

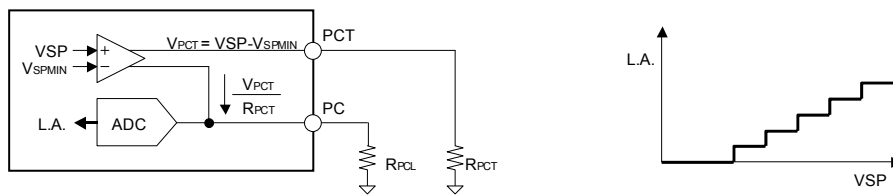


Figure 4. Phase control setting example 1

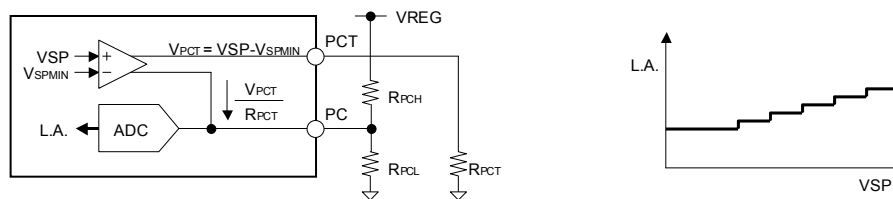


Figure 5. Phase control setting example 2

### 9) Overcurrent protection (OCP) circuit

The over current protection circuit can be activated by connecting a low value resistor for current detection between the external output stage ground and the controller IC ground. When the RCL pin voltage reaches or surpasses the threshold value, the controller forces all the upper switching arm inputs low (UH, VH, WH = L, L, L), thus initiating the overcurrent protection operation. When the RCL pin voltage swings below the ground, it is recommended to insert a resistor - 1.5 k $\Omega$  or more - between RCL pin and current detection resistor to prevent malfunction. Since this protection circuit is not a latch type, it returns to normal operation - synchronizing with the carrier frequency - once the RCL pin voltage falls below the threshold voltage. A filter is built into the overcurrent detection circuit to prevent malfunctions, and does not activate when a short pulse of less than  $T_{RCL}$  is present at the input.

### 10) Under voltage lock out (UVLO) circuit

To secure the lowest power supply voltage necessary to operate the controller, and to prevent under voltage malfunctions, an UVLO circuit is built into this controller. When the power supply voltage falls to  $V_{UVL}$  or below, the controller forces all driver outputs low. When the voltage rises to  $V_{UVH}$  or above, the UVLO circuit ends the lock out operation and returns the chip to normal operation.

The voltage monitor circuit (4.0V nominal) is built-in for the VREG voltage. Therefore, the UVLO circuit does not release operation when the VREG voltage rising is delayed behind the VCC voltage rising even if VCC voltage becomes  $V_{UVH}$  or more.

**11) Thermal shutdown (TSD) circuit**

The TSD circuit operates when the junction temperature of the controller exceeds the preset temperature (175°C nominal). At this time, the controller forces all driver outputs low. Since thermal hysteresis is provided in the TSD circuit, the chip returns to normal operation when the junction temperature falls below the preset temperature (150°C nominal). The TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation in the presence of extreme heat. Do not continue to use the IC after the TSD circuit is activated, and do not use the IC in an environment where activation of the circuit is assumed.

**12) Motor lock protection (MLP) circuit**

When the controller detects the motor locking during fixed time of 4 seconds nominal when each edge of the hall signal doesn't input either, the controller forces all driver outputs low under a fixed time 20 seconds nominal, and self-returns to normal operation. This circuit is enabled if the voltage force to VSP is over the duty minimum voltage  $V_{SPMIN}$ , and note that the motor cannot start up when the controller doesn't detect the motor rotation by the minimum duty control.

**13) External fault signal input pin (FIB pin, low active)**

The FIB pin can force all controller driver outputs low at any time. The FIB pin is pulled up to VREG internally by a 100 kΩ resistor. Therefore, an open drain output can be connected directly. It is recommended to pull up FIB pin to VREG voltage when this function is not used or malfunctioning because of the noise.

**14) Hall signal wrong input detection**

Hall element abnormalities may cause incorrect inputs that vary from the normal logic. When all hall input signals go high or low, the hall signal wrong input detection circuit forces all driver outputs low. And when the controller detects the abnormal hall signals continuously for four times or more motor rotation, the controller forces all driver outputs low and latches the state. It is released if the duty control voltage VSP is forced to ground level once.

**15) Internal voltage regulator**

The internal voltage regulator VREG is output for the bias of the hall element and the phase control setting. However, when using the VREG function, be aware of the  $I_{OMAX}$  value. If a capacitor is connected to the ground in order to stabilize output, a value of 1 μF or more should be used. In this case, be sure to confirm that there is no oscillation in the output.

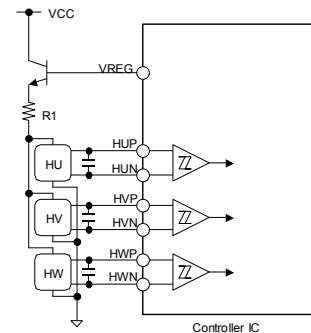


Figure 6. VREG output pin application example

● Timing Charts (CW)

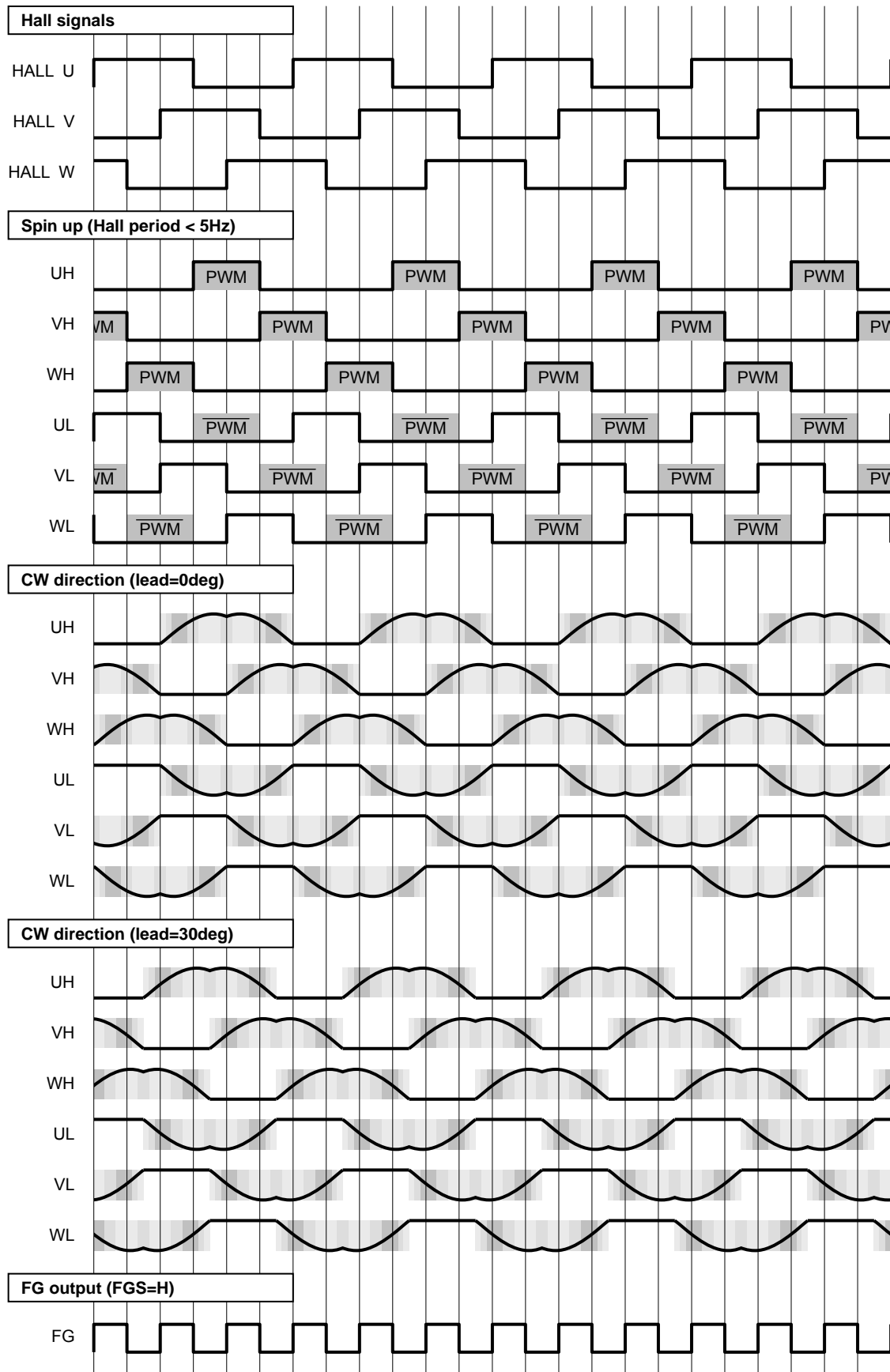


Figure 7. BD62014AFS (Clockwise) timing charts

● Timing Charts (CCW)

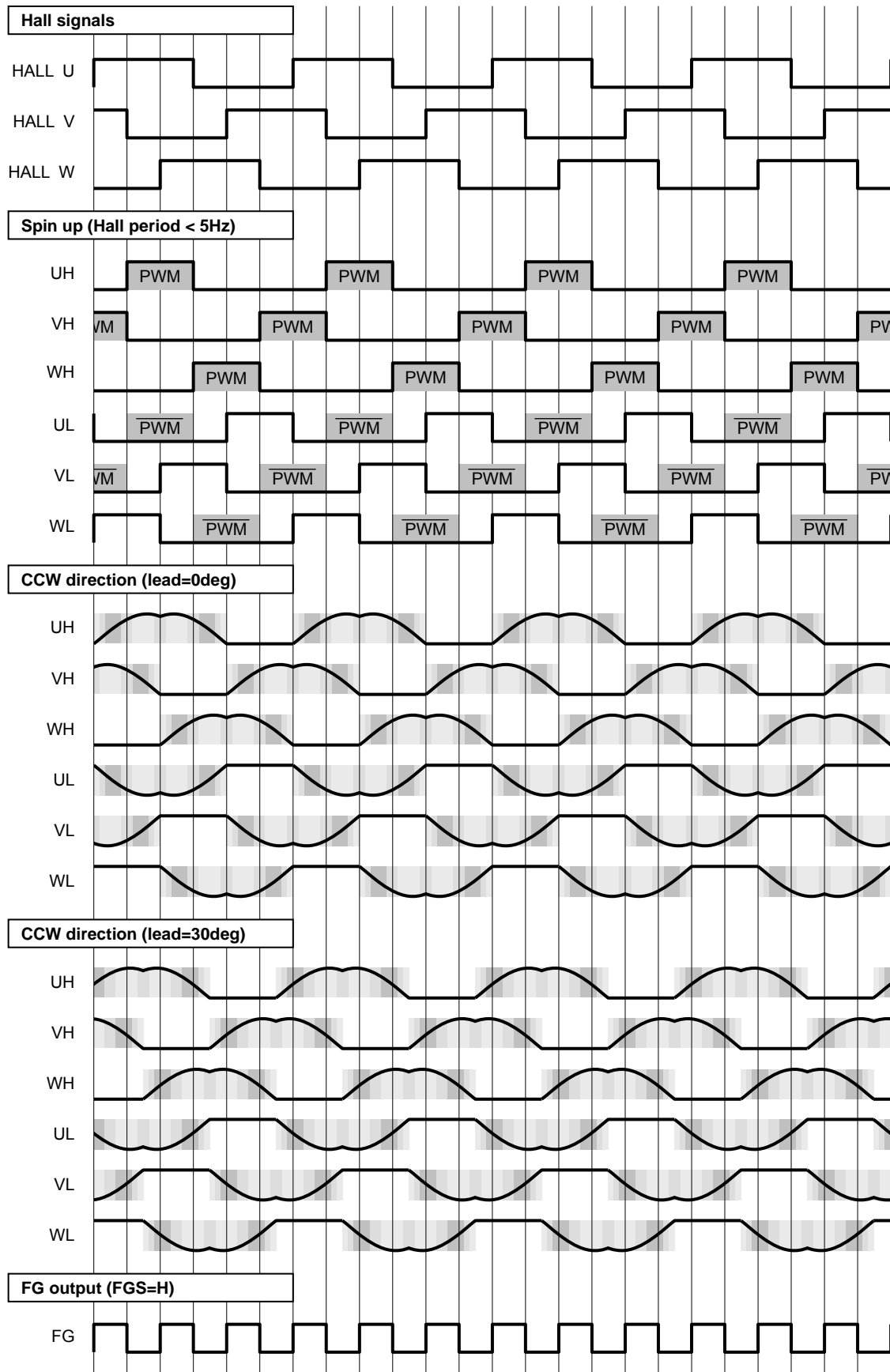


Figure 8. BD62014AFS (Counter clockwise) timing charts

### ● Controller Outputs and Operation Mode Summary

| Conditions        | Detected direction                                  | Forward (CW:U~V~W, CCW:U~W~V)        |   | Reverse (CW:U~W~V, CCW:U~V~W)        |                         |
|-------------------|---|--------------------------------------|---|--------------------------------------|-------------------------|
|                   | Hall sensor period                                  | < 5Hz                                | 5Hz <   | < 5Hz                                | 5Hz <                   |
| Normal operation  | $V_{SP} < V_{SPMIN}$<br>(Duty off)                  | Upper and lower arm off              |   |                                      |                         |
|                   | $V_{SPMIN} < V_{SP} < V_{SPMAX}$<br>(Control range) | 120°<br>Upper and lower<br>switching | 180° sinusoidal<br>Upper and lower switching                    | 120°<br>Upper and lower<br>switching | 120°<br>Upper switching |
|                   | $V_{SPTST} < V_{SP}$<br>(Testing mode)              |                                      | 180° sinusoidal<br>Upper and lower switching<br>(No lead angle) |                                      |                         |
| Protect operation | Overcurrent   | Upper arm off                        |   | Upper and lower arm off              |                         |
|                   | UVLO  | Upper and lower arm off              |   |                                      |                         |
|                   | TSD   |                                      |   |                                      |                         |
|                   | Motor lock  |                                      |   |                                      |                         |
|                   | External input                                      |                                      |   |                                      |                         |
|                   | Hall sensor abnormally                              | Upper and lower arm off and latch    |   |                                      |                         |

\* The controller monitors both edges of three hall sensors for detecting period.

\* Phase control function only operates at sinusoidal commutation mode. However, the controller forces no lead angle during the testing mode.

### ● Absolute Maximum Ratings (Ta=25°C, All voltages are with respect to ground)

| Parameter             | Symbol           | Ratings            | Unit |
|-----------------------|------------------|--------------------|------|
|                       |                  | BD62014AFS         |      |
| Supply voltage        | $V_{CC}$         | 20 <sup>*1</sup>   | V    |
| Duty control voltage  | $V_{SP}$         | -0.3 to 20         | V    |
| All others            | $V_{IO}$         | -0.3 to 5.5        | V    |
| Driver outputs        | $I_{OMAX(OUT)}$  | ±15 <sup>*1</sup>  | mA   |
| Monitor output        | $I_{OMAX(FG)}$   | ±5 <sup>*1</sup>   | mA   |
| VREG outputs          | $I_{OMAX(VREG)}$ | -40 <sup>*1</sup>  | mA   |
| Operating temperature | $T_{OPR}$        | -40 to 110         | °C   |
| Storage temperature   | $T_{STG}$        | -55 to 150         | °C   |
| Power dissipation     | $P_d$            | 1.00 <sup>*2</sup> | W    |
| Junction temperature  | $T_{jmax}$       | 150                | °C   |

\*1 Do not, however, exceed  $P_d$  or ASO.

\*2 Mounted on a 70mm x 70mm x 1.6mm FR4 glass-epoxy board with less than 3% copper foil. Derated at 8mW/°C above 25°C.

### ● Operating Conditions (Ta=25°C)

| Parameter      | Symbol   | BD62014AFS | Unit |
|----------------|----------|------------|------|
| Supply voltage | $V_{CC}$ | 10 to 18   | V    |



● **Electrical Characteristics** (Unless otherwise specified, Ta=25°C and VCC=15V)

| Parameter  | Symbol               | Limits                 |                        |                       | Unit              | Conditions                            |
|--|----------------------|------------------------|------------------------|-----------------------|-------------------|---------------------------------------|
|  |                      | Min.                   | Typ.                   | Max.                  |                   |                                       |
| <b>Power supply</b>  |                      |                        |                        |                       |                   |                                       |
| Supply current   | I <sub>CC</sub>      | 2.0                    | 2.8                    | 5.0                   | mA                |                                       |
| VREG voltage   | V <sub>REG</sub>     | 4.5                    | 5.0                    | 5.5                   | V                 | I <sub>O</sub> =-30mA                 |
| <b>Driver outputs</b>  |                      |                        |                        |                       |                   |                                       |
| Output high voltage  | V <sub>OH</sub>      | V <sub>REG</sub> -0.60 | V <sub>REG</sub> -0.20 | V <sub>REG</sub>      | V                 | I <sub>O</sub> =-5mA                  |
| Output low voltage   | V <sub>OL</sub>      | 0                      | 0.14                   | 0.60                  | V                 | I <sub>O</sub> =5mA                   |
| Dead time  | T <sub>DT</sub>      | 1.6                    | 2.0                    | 2.4                   | μs                |                                       |
| Minimum pulse width  | T <sub>MIN</sub>     | 0.8                    | 1.0                    | 1.2                   | μs                |                                       |
| <b>Hall comparators</b>                                      |                      |                        |                        |                       |                   |                                       |
| Input bias current   | I <sub>HALL</sub>    | -2.0                   | -0.1                   | 2.0                   | μA                | V <sub>IN</sub> =0V                   |
| Common mode input  | V <sub>HALLCM</sub>  | 0                      | -                      | V <sub>REG</sub> -1.5 | V                 |                                       |
| Minimum input level  | V <sub>HALLMIN</sub> | 50                     | -                      | -                     | mV <sub>p-p</sub> |                                       |
| Hysteresis voltage P   | V <sub>HALLHY+</sub> | 5                      | 13                     | 23                    | mV                |                                       |
| Hysteresis voltage N   | V <sub>HALLHY-</sub> | -23                    | -13                    | -5                    | mV                |                                       |
| <b>Duty control</b>  |                      |                        |                        |                       |                   |                                       |
| Input bias current   | I <sub>SP</sub>      | 15                     | 25                     | 35                    | μA                | V <sub>IN</sub> =5V                   |
| Duty minimum voltage   | V <sub>SPMIN</sub>   | 0.8                    | 1.1                    | 1.4                   | V                 |                                       |
| Duty maximum voltage   | V <sub>SPMAX</sub>   | 4.1                    | 4.4                    | 4.7                   | V                 |                                       |
| Testing mode range   | V <sub>SPTST</sub>   | 8.2                    | -                      | 18                    | V                 |                                       |
| Minimum output duty  | D <sub>MIN</sub>     | 1.2                    | 1.8                    | 2.4                   | %                 | F <sub>OSC</sub> =18kHz               |
| Maximum output duty  | D <sub>MAX</sub>     | -                      | 100                    | -                     | %                 | F <sub>OSC</sub> =18kHz               |
| <b>Mode switch and the external input - FGS, CCW and FIB</b> |                      |                        |                        |                       |                   |                                       |
| Input bias current   | I <sub>IN</sub>      | -70                    | -50                    | -30                   | μA                | V <sub>IN</sub> =0V                   |
| Input high voltage   | V <sub>INH</sub>     | 3                      | -                      | V <sub>REG</sub>      | V                 |                                       |
| Input low voltage  | V <sub>INL</sub>     | 0                      | -                      | 1                     | V                 |                                       |
| Hysteresis voltage   | V <sub>INHY</sub>    | 0.2                    | 0.5                    | 0.8                   | V                 |                                       |
| <b>Monitor output - FG</b>                                   |                      |                        |                        |                       |                   |                                       |
| Output high voltage  | V <sub>MONH</sub>    | V <sub>REG</sub> -0.40 | V <sub>REG</sub> -0.08 | V <sub>REG</sub>      | V                 | I <sub>O</sub> =-2mA                  |
| Output low voltage   | V <sub>MONL</sub>    | 0                      | 0.06                   | 0.40                  | V                 | I <sub>O</sub> =2mA                   |
| <b>Overcurrent protection</b>                                |                      |                        |                        |                       |                   |                                       |
| Input bias current   | I <sub>RCL</sub>     | -30                    | -20                    | -10                   | μA                | V <sub>IN</sub> =0V                   |
| Threshold voltage  | V <sub>RCL</sub>     | 0.48                   | 0.50                   | 0.52                  | V                 |                                       |
| Noise masking time   | T <sub>RCL</sub>     | 0.8                    | 1.0                    | 1.2                   | μs                |                                       |
| <b>Phase control</b>   |                      |                        |                        |                       |                   |                                       |
| Minimum lead angle   | P <sub>MIN</sub>     | -                      | 0                      | 1                     | deg               | V <sub>PC</sub> =0V                   |
| Maximum lead angle   | P <sub>MAX</sub>     | 39                     | 40                     | -                     | deg               | V <sub>PC</sub> =2/3·V <sub>REG</sub> |
| <b>Carrier frequency oscillator</b>                          |                      |                        |                        |                       |                   |                                       |
| Carrier frequency  | F <sub>OSC</sub>     | 16                     | 18                     | 20                    | kHz               | R <sub>T</sub> =22kΩ                  |
| <b>Under voltage lock out</b>                                |                      |                        |                        |                       |                   |                                       |
| Release voltage  | V <sub>UVH</sub>     | 8.5                    | 9.0                    | 9.5                   | V                 |                                       |
| Lockout voltage  | V <sub>UVL</sub>     | 7.5                    | 8.0                    | 8.5                   | V                 |                                       |
| Hysteresis voltage   | V <sub>UVHY</sub>    | 0.5                    | 1.0                    | 1.5                   | V                 |                                       |

● Typical Performance Curves (Reference data)

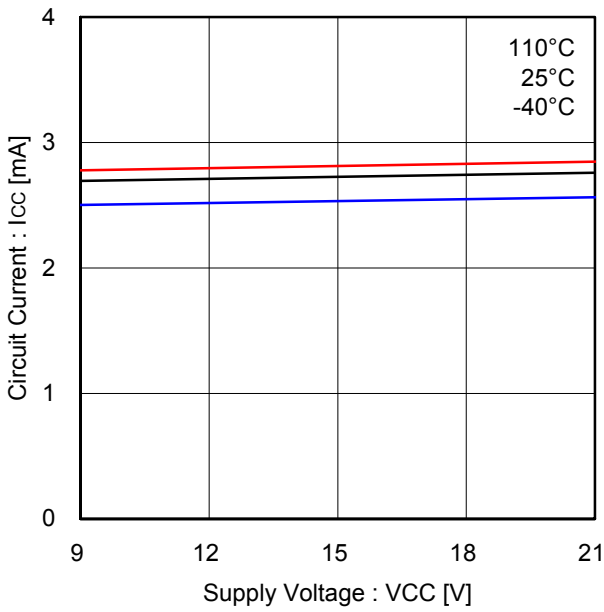


Figure 9. Circuit current

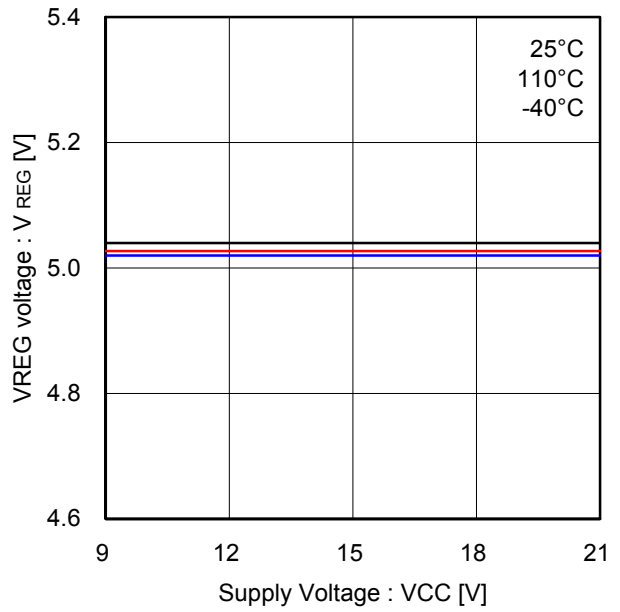


Figure 10. VREG - VCC

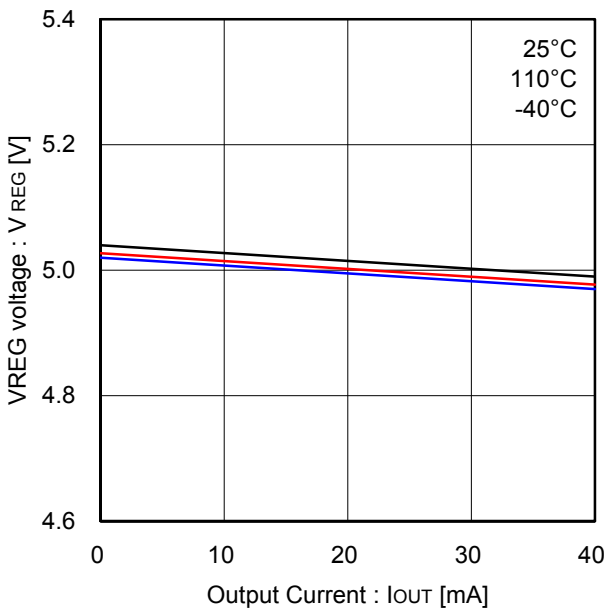


Figure 11. VREG drive capability

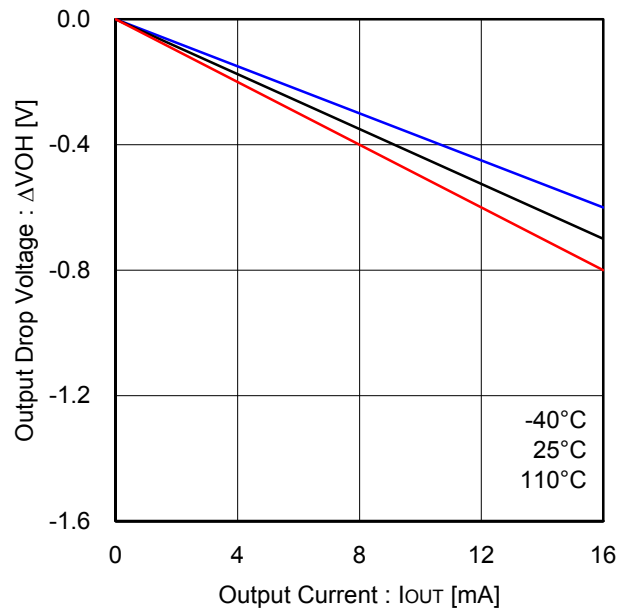


Figure 12. High side output voltage (XH, XL)

● Typical Performance Curves (Reference data) - Continued

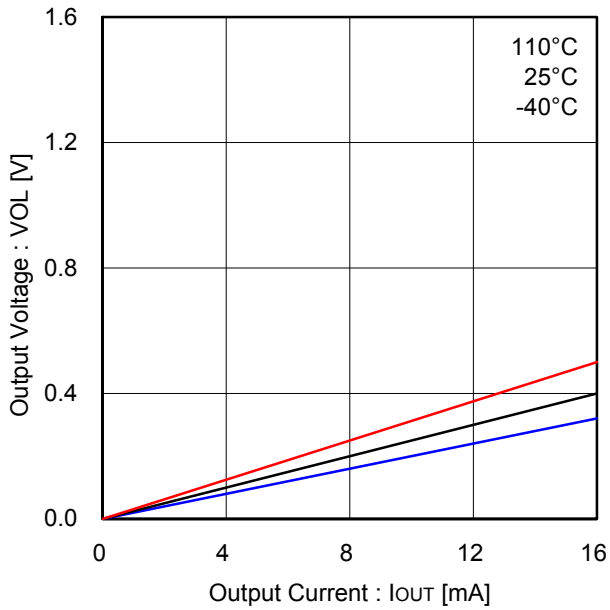


Figure 13. Low side output voltage (XH, XL)

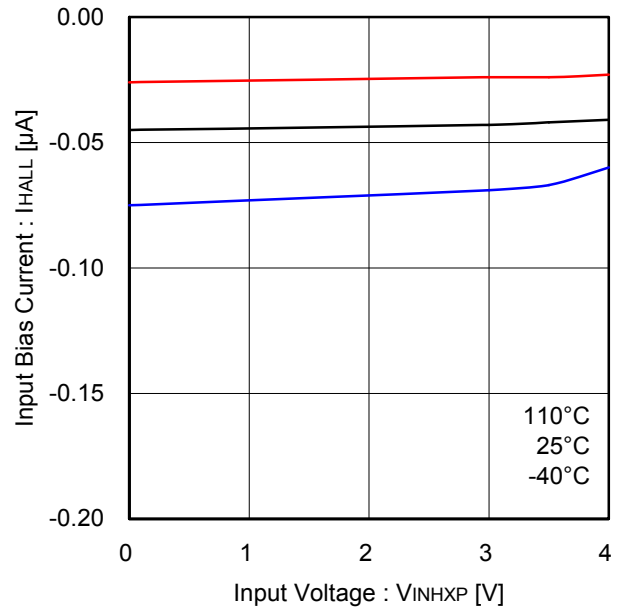


Figure 14. Hall comparator input bias current (HXP, HXN)

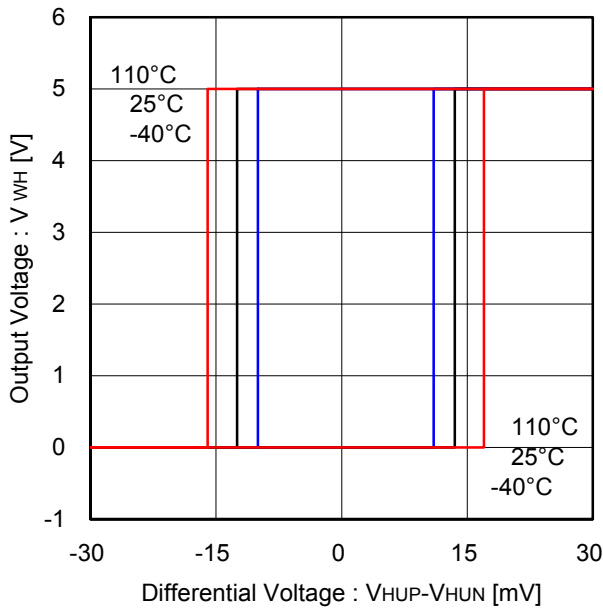


Figure 15. Hall comparator hysteresis voltage

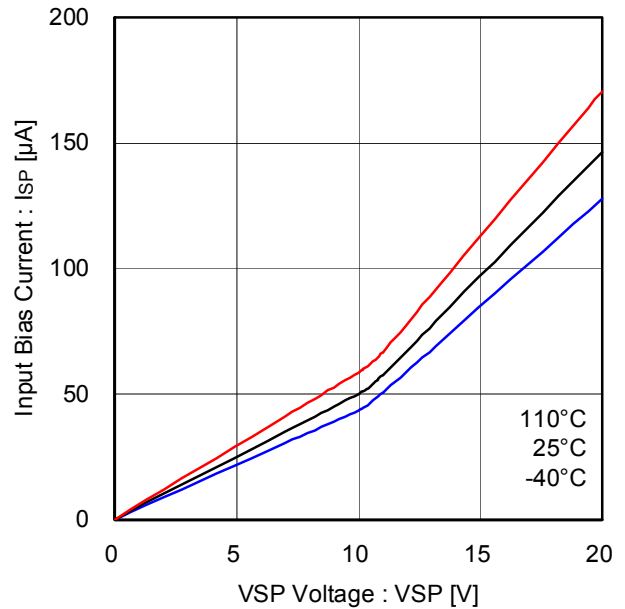


Figure 16. VSP input bias current

● Typical Performance Curves (Reference data) - Continued

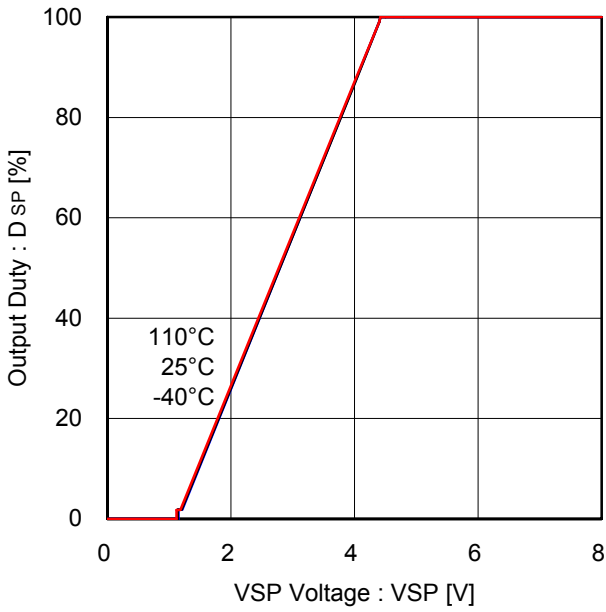


Figure 17. Output duty - VSP voltage

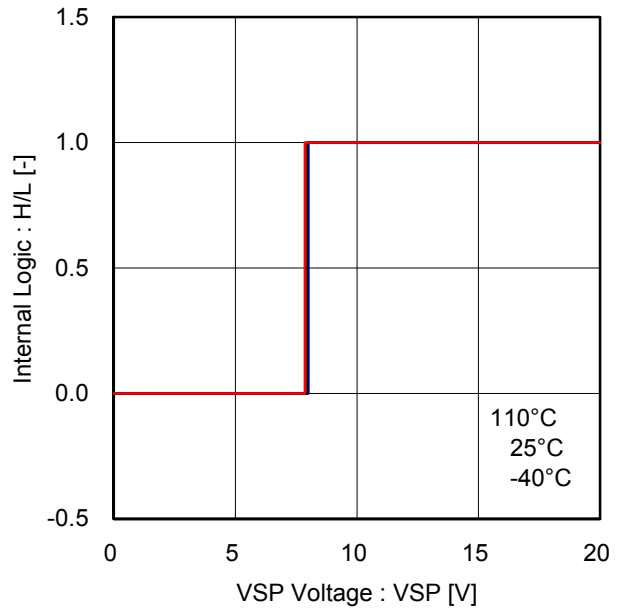


Figure 18. Testing mode threshold voltage

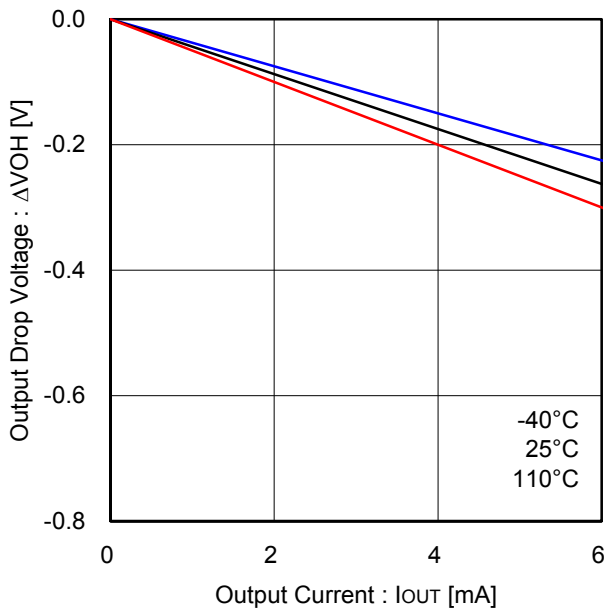


Figure 19. High side output voltage (FG)

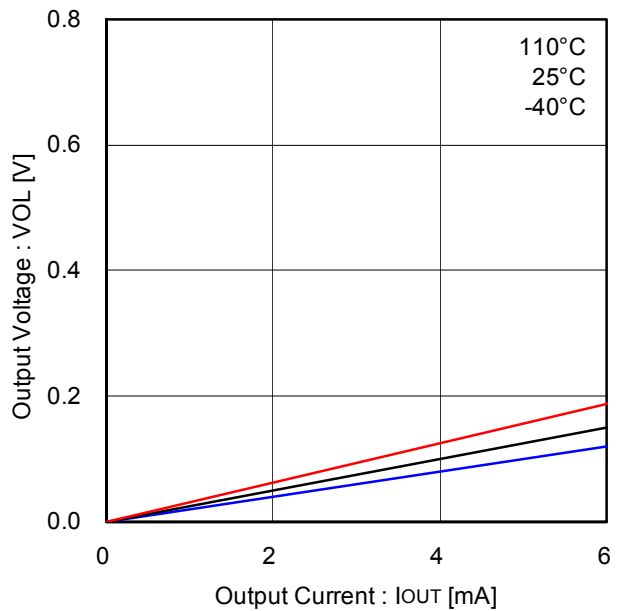


Figure 20. Low side output voltage (FG)

● Typical Performance Curves (Reference data) - Continued

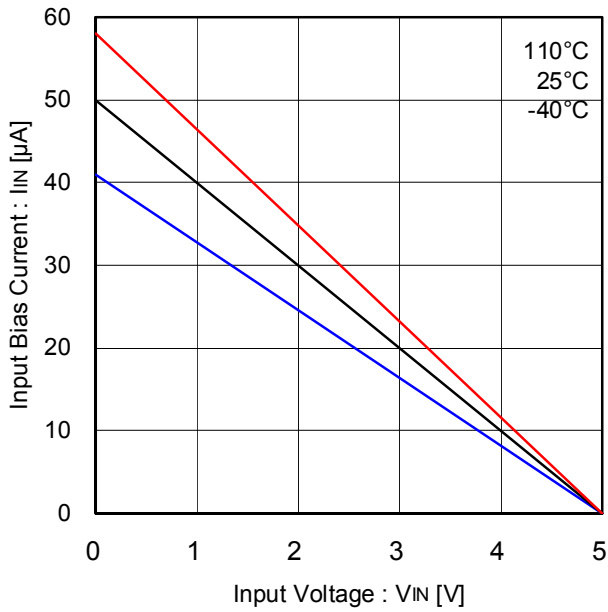


Figure 21. Input bias current (CCW, FIB)

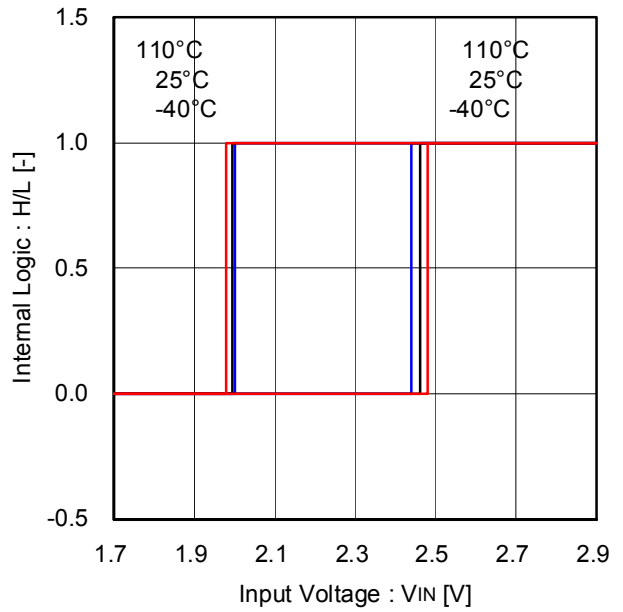


Figure 22. Input threshold voltage (CCW, FIB)

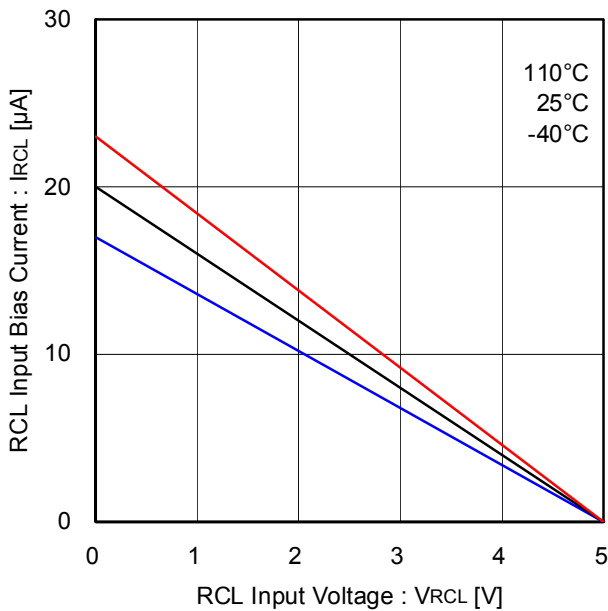


Figure 23. RCL input bias current

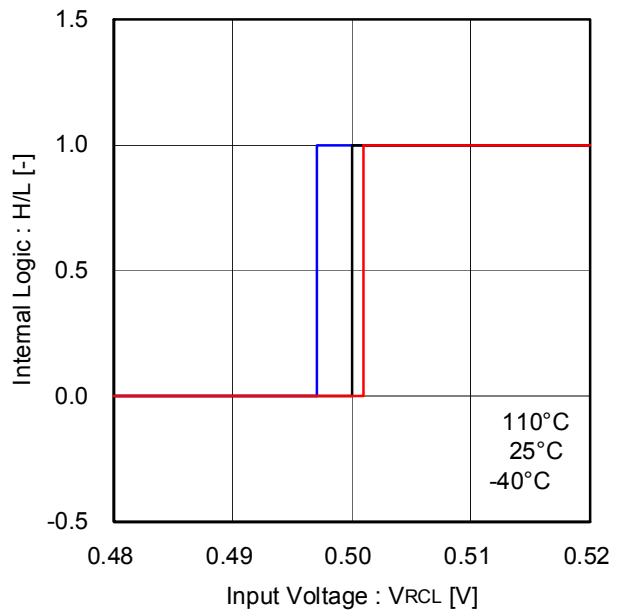


Figure 24. RCL input threshold voltage

● Typical Performance Curves (Reference data) - Continued

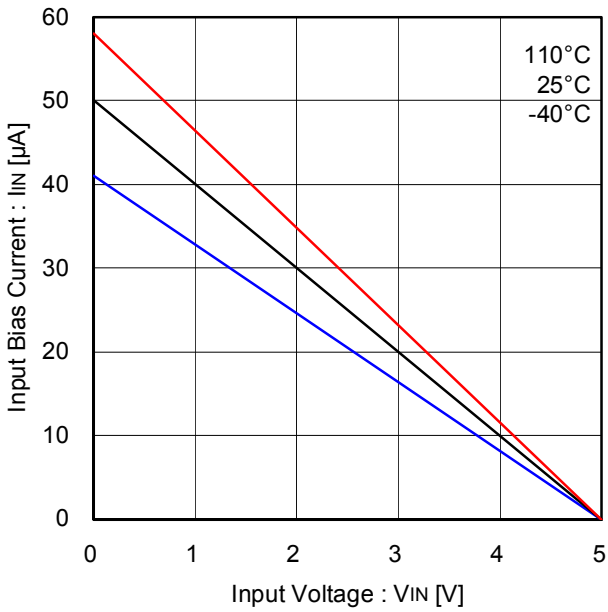


Figure 25. Input bias current (FGS)

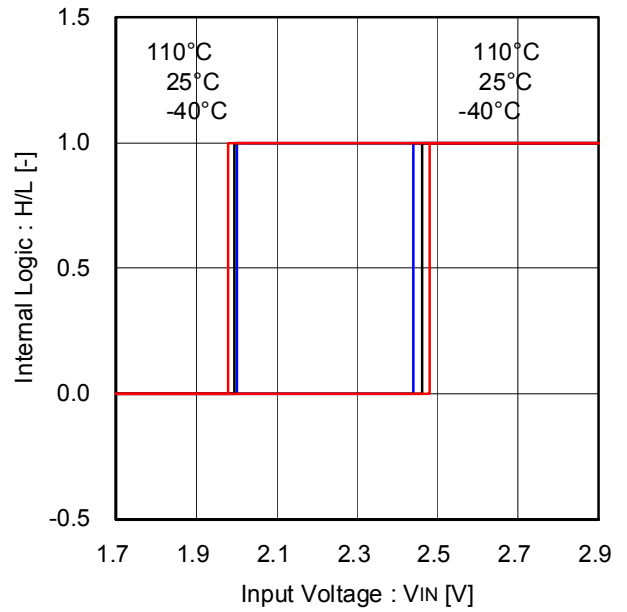


Figure 26. Input threshold voltage (FGS)

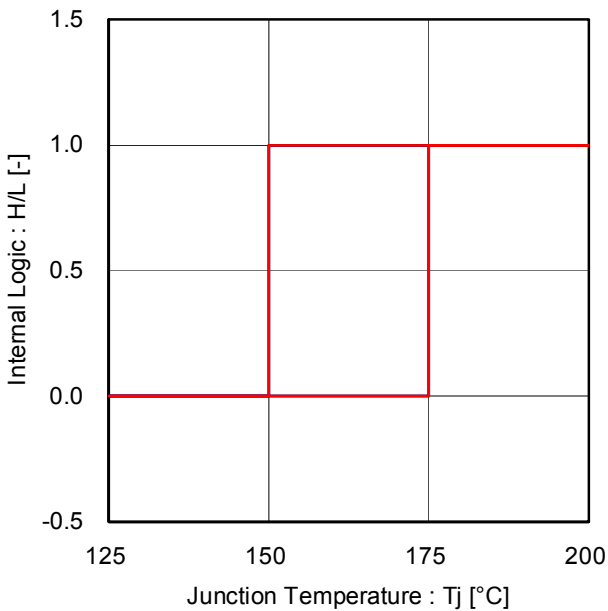


Figure 27. Thermal shut down

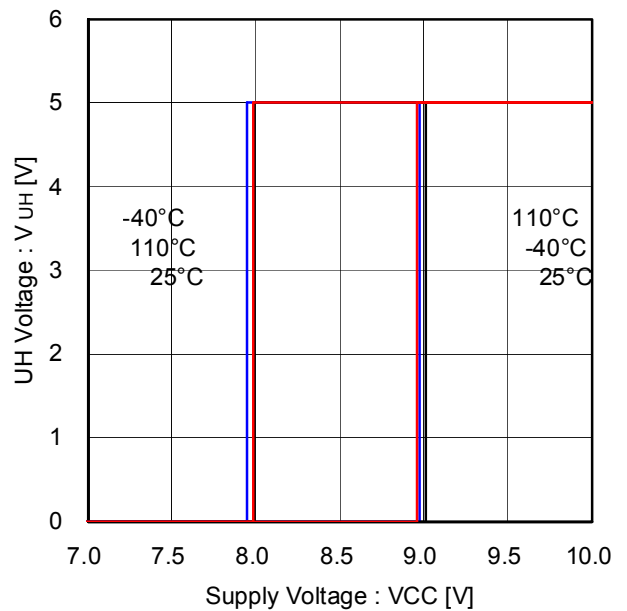


Figure 28. Under voltage lock out (VCC)

● Typical Performance Curves (Reference data) - Continued

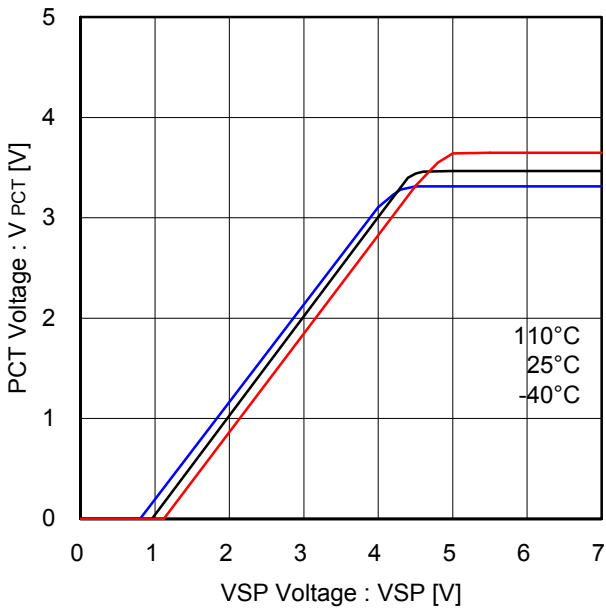


Figure 29. VSP - PCT offset voltage

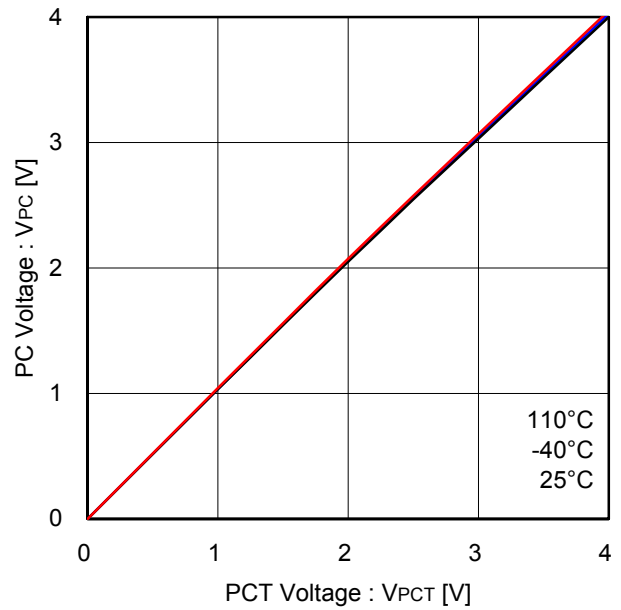


Figure 30. PCT - PC linearity  
( $R_{PCT}=R_{PC}=100k\Omega$ )

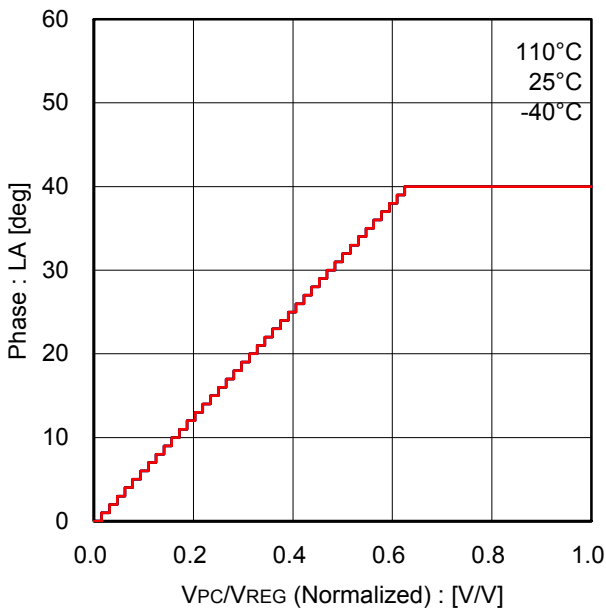


Figure 31. PC voltage normalized - Lead angle

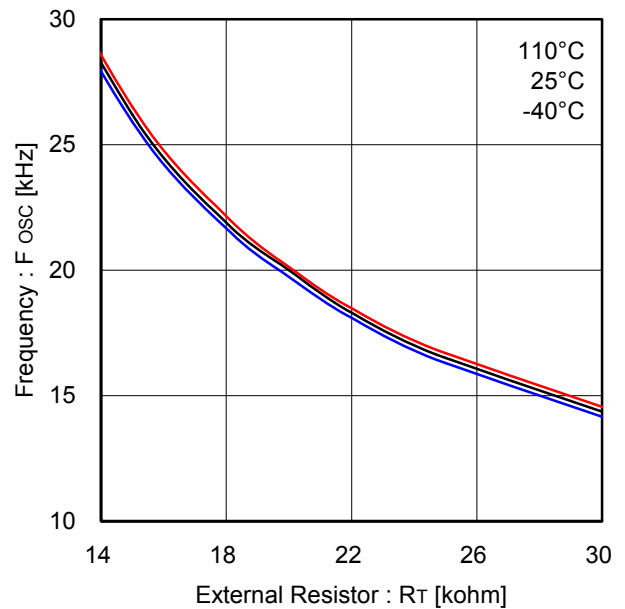


Figure 32. Carrier frequency -  $R_T$

● Application Circuit Example

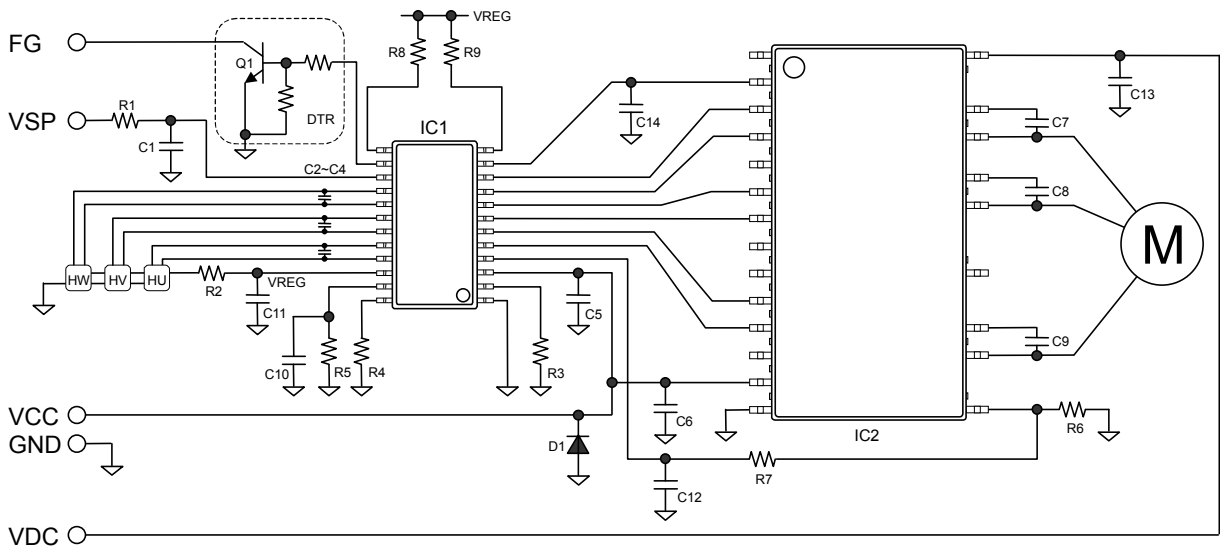


Figure 33. Application circuit example (180° sinusoidal commutation driver)

Parts list

| Parts | Value | Manufacturer | Type               | Parts | Value  | Ratings | Type          |
|-------|-------|--------------|--------------------|-------|--------|---------|---------------|
| IC1   | -     | ROHM         | BD62014AFS         | C1    | 0.1μF  | 50V     | Ceramic       |
| IC2   | -     | ROHM         | BM6202FS           | C2-4  | 2200pF | 50V     | Ceramic       |
| R1    | 1kΩ   | ROHM         | MCR18EZPF1001      | C5    | 10 μF  | 50V     | Ceramic       |
| R2    | 150Ω  | ROHM         | MCR18EZPJ151       | C6    | 10 μF  | 50V     | Ceramic       |
| R3    | 22kΩ  | ROHM         | MCR18EZPF2202      | C7-9  | 1μF    | 50V     | Ceramic       |
| R4    | 100kΩ | ROHM         | MCR18EZPF1003      | C10   | 0.1μF  | 50V     | Ceramic       |
| R5    | 51kΩ  | ROHM         | MCR18EZPF5102      | C11   | 1μF    | 50V     | Ceramic       |
| R6    | 0.5Ω  | ROHM         | MCR50JZHFL1R50 x 3 | C12   | 100pF  | 50V     | Ceramic       |
| R7    | 10kΩ  | ROHM         | MCR18EZPF1002      | C13   | 0.1μF  | 630V    | Ceramic       |
| R8    | 0Ω    | ROHM         | MCR18EZPJ000       | C14   | 0.1μF  | 50V     | Ceramic       |
| R9    | 0Ω    | ROHM         | MCR18EZPJ000       | HX    | -      | -       | Hall elements |
| Q1    | -     | ROHM         | DTC124EUA          |       |        |         |               |
| D1    | -     | ROHM         | KDZ20B             |       |        |         |               |



● Interfaces

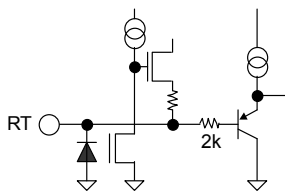


Figure 34. RT

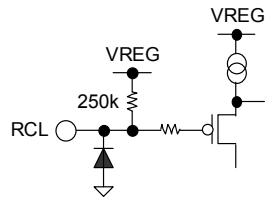


Figure 35. RCL

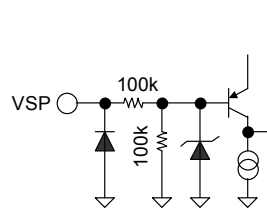


Figure 36. VSP

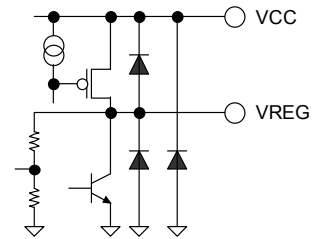


Figure 37. VREG, VCC

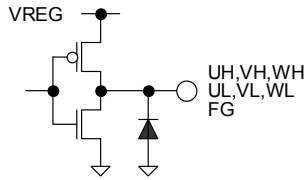


Figure 38. XH, XL, FG

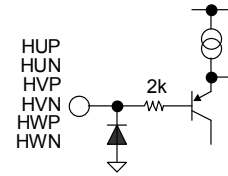


Figure 39. HXP, HXN

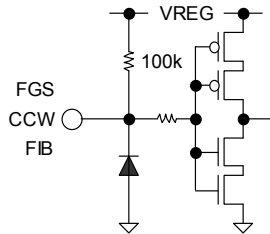


Figure 40. FGS, CCW, FIB

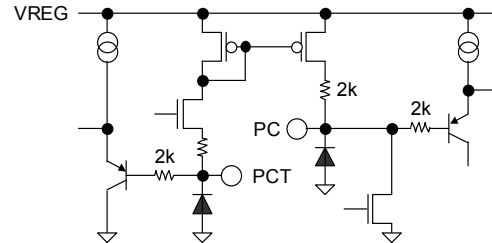


Figure 41. PC, PCT

## ● Notes for Use

### 1) Absolute maximum ratings

Devices may be destroyed when supply voltage or operating temperature exceeds the absolute maximum rating. Because the cause of this damage cannot be identified as, for example, a short circuit or an open circuit, it is important to consider circuit protection measures, such as adding fuses, if any value in excess of absolute maximum ratings is to be implemented.

### 2) Electrical potential at GND

Keep the GND terminal to the minimum potential under any operating condition. In addition, check to determine whether there is any terminal that provides voltage below GND, including the voltage during transient phenomena. However, note that even if the voltage does not fall below GND in any other operating condition, it can still swing below GND potential when the motor generates back electromotive force at the RCL terminal. The chip layout in this product is designed to avoid this sort of electrical potential problem, but pulling excessive current may still result in malfunctions. Therefore, it is necessary to observe operation closely to conclusively confirm that there is no problem in actual operation. If there are small signal GND and high current GND, it is recommended to separate the patterns for the high current GND and the small signal GND and provide a proper grounding to the reference point of the set not to affect the voltage at the small signal GND with the change in voltage due to resistance component of pattern wiring and high current. Also for GND wiring pattern of the component externally connected, pay special attention not to cause undesirable change to it.

### 3) Driver outputs

The high voltage semiconductor generally driven by this product is connected to the next stage via the controller. If any special mode in excess of absolute maximum ratings is to be implemented with this product or its application circuits, it is important to take physical safety measures, such as providing voltage-clamping diodes or fuses.

### 4) Thermal design

Use a thermal design that allows sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

### 5) Inter-pin shorts and mounting errors

Take caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together. Also, connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply lines, such as establishing an external diode between the power supply and the IC power supply pin.

### 6) Operation in strong electromagnetic fields

Using this product in strong electromagnetic fields may cause IC malfunctions. Take extreme caution with electromagnetic fields.

### 7) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a low impedance pin subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

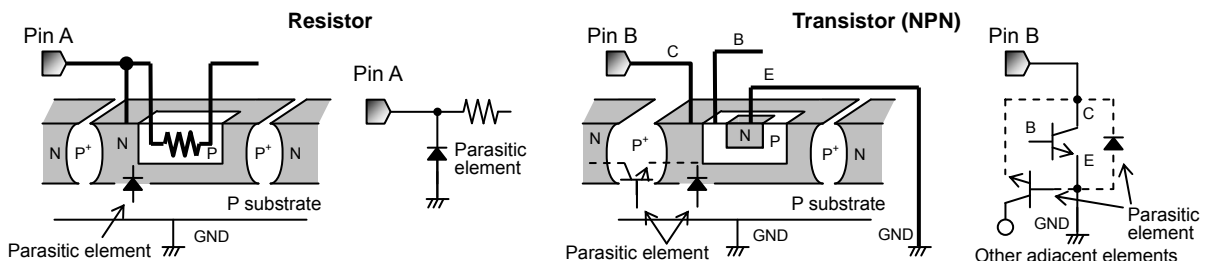
### 8) Regarding the input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements, in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

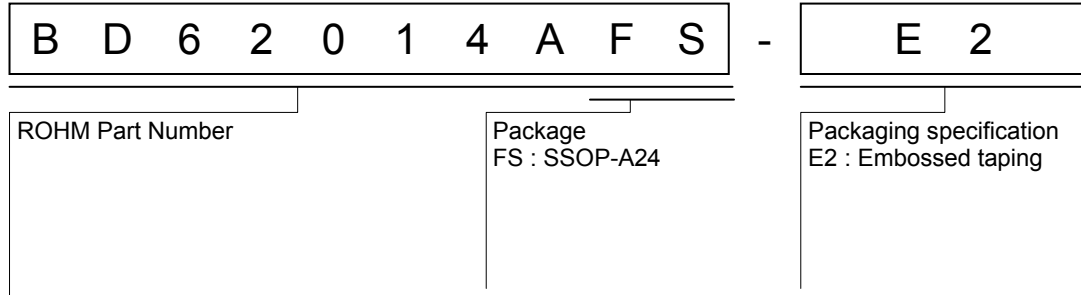
When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, as well as operating malfunctions and physical damage. Therefore, do not use methods by which parasitic diodes operate, such as applying a voltage lower than the GND (P substrate) voltage to an input pin.



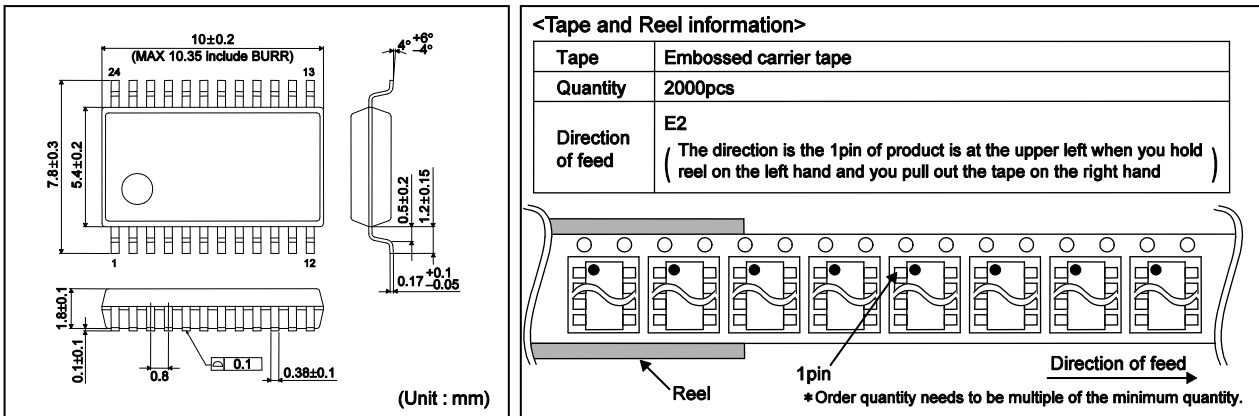
Appendix: Example of monolithic IC structure

● Ordering Information

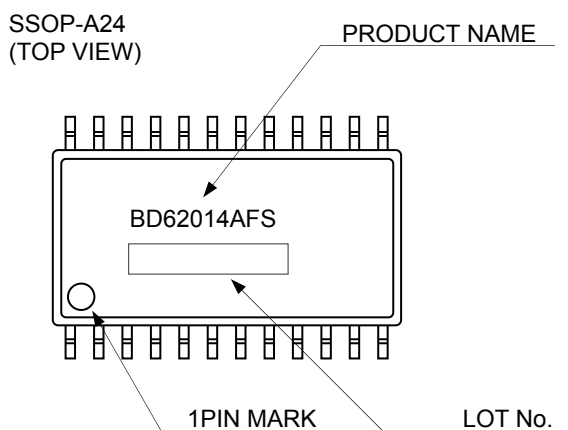


● Physical Dimension, Tape and Reel Information

**SSOP-A24**



● Marking Diagram



● Revision History

| Date        | Revision | Changes                      |
|-------------|----------|------------------------------|
| 18.DEC.2015 | 001      | New release                  |
| 03.JUN.2016 | 002      | Correct some misdescriptions |

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|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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  - Sealing or coating our Products with resin or other coating materials
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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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For details, please refer to ROHM Mounting specification

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  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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