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**EVB-LAN9355  
Evaluation Board  
User's Guide**

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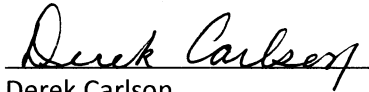
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VP Development Tools



Date

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## Preface

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For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

## INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9355. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [The Microchip Web Site](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

## DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9355 Evaluation Board as a development tool for the LAN9355 three-port 10/100 managed Ethernet switch. The manual layout is as follows:

- **Chapter 1. “Overview”** – Shows a brief description of the EVB-LAN9355 Evaluation Board.
- **Chapter 2. “Getting Started”** – Includes instructions on how to get started with the EVB-LAN9355 Evaluation Board.
- **Chapter 3. “Board Configuration”** – Provides information about the EVB-LAN9355 Evaluation Board battery charging features.
- **Appendix A. “EVB-LAN9355 Evaluation Board”** – This appendix shows the EVB-LAN9355 Evaluation Board.
- **Appendix B. “EVB-LAN9355 Evaluation Board Schematics”** – This appendix shows the EVB-LAN9355 Evaluation Board schematics.
- **Appendix C. “Bill of Materials (BOM)”** – This appendix includes the EVB-LAN9355 Evaluation Board Bill of Materials (BOM).

## CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

### DOCUMENTATION CONVENTIONS

| Description                                      | Represents  | Examples  |
|--|---|---|
| <b>Arial font:</b>                               |   |   |
| Italic characters                                | Referenced books  | <i>MPLAB® IDE User's Guide</i>                              |
|  | Emphasized text   | ...is the <i>only</i> compiler...                           |
| Initial caps                                     | A window  | the Output window   |
|  | A dialog  | the Settings dialog   |
|  | A menu selection  | select Enable Programmer                                    |
| Quotes   | A field name in a window or dialog  | "Save project before build"                                 |
| Underlined, italic text with right angle bracket | A menu path   | <u>File</u> > <i>Save</i>                                   |
| Bold characters                                  | A dialog button   | Click <b>OK</b>   |
|  | A tab   | Click the <b>Power</b> tab                                  |
| N'Rnnnn  | A number in verilog format, where N is the total number of digits, R is the radix and n is a digit. | 4'b0010, 2'hF1  |
| Text in angle brackets < >                       | A key on the keyboard   | Press <Enter>, <F1>   |
| <b>Courier New font:</b>                         |   |   |
| Plain Courier New                                | Sample source code  | #define START   |
|  | Filenames   | autoexec.bat  |
|  | File paths  | c:\mcc18\h  |
|  | Keywords  | _asm, _endasm, static                                       |
|  | Command-line options  | -Opa+, -Opa-  |
|  | Bit values  | 0, 1  |
|  | Constants   | 0xFF, 'A'   |
| Italic Courier New                               | A variable argument   | <i>file.o</i> , where <i>file</i> can be any valid filename |
| Square brackets [ ]                              | Optional arguments  | mcc18 [options] <i>file</i> [options]                       |
| Curly brackets and pipe character: {   }         | Choice of mutually exclusive arguments; an OR selection   | errorlevel {0 1}  |
| Ellipses...                                      | Replaces repeated text  | var_name [, var_name...]                                    |
|  | Represents code supplied by user  | void main (void)<br>{ ...<br>}                              |



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- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:

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### **DOCUMENT REVISION HISTORY**

#### **Revision A (July 2015)**

- Initial Release of this Document.

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## Chapter 1. Overview

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### 1.1 INTRODUCTION

The LAN9355 is a fully featured, three-port 10/100 managed Ethernet switch designed for industrial and embedded applications where performance, flexibility, ease of integration and system cost control are required.

The LAN9355 combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and serial management. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hard-ware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks.

The LAN9355 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

100BASE-FX is supported via an external fiber transceiver and cable diagnostics (open and length) is included on the internal twisted pair copper interface.

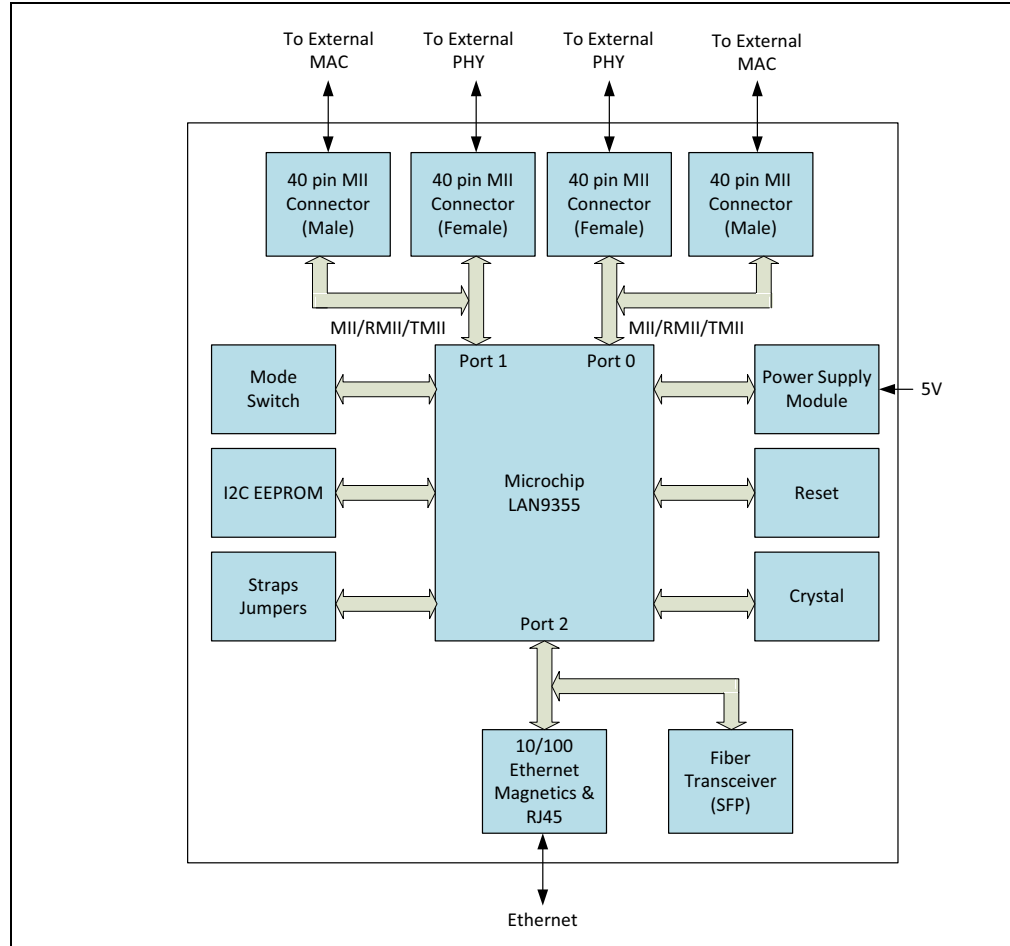
The EVB-LAN9355 is an Evaluation Board (EVB) that utilizes the LAN9355 to provide a fully-functional three-port Ethernet switch with Dual MII/RMII/TurboMII. The EVB9355 provides one fully integrated MAC/PHY internet ports (Ports 2) via on-board RJ45 connectors. Port 0 and Port 1 provides two MII port connectors which support the following:

- An external Dual MII/RMII/Turbo MII –Capable MAC (with LAN9355 in PHY mode), via the on-board 40-pin male MII connector
- An external Dual MII/RMII/Turbo MII –Capable PHY (with LAN9355 in MAC mode), via the on-board 40-pin female MII connector

Power is supplied to the board via a +5V external wall mount power supply.

The EVB-LAN9355 includes a 64K x 8 I2C EEPROM that may be used to automatically load configuration settings from the EEPROM into the device at reset. An I2C host adapter interface header (10-pin, 2x5) is provided to simplify I2C based configuration. A simplified block diagram of the EVB LAN9355 can be seen in [Figure 1-1](#).

**FIGURE 1-1: EVB-LAN9355 BLOCK DIAGRAM**



**1.1.1 References**

Concepts and material available in the following documents may be helpful when reading this document. Visit [www.microchip.com](http://www.microchip.com) for the latest documentation.

| Document                               | Location  |
|--|---|
| LAN9355 datasheet                      | Visit <a href="http://www.microchip.com">www.microchip.com</a>  |
| AN8-13 Suggested Magnetics             | <a href="http://www.microchip.com/wwwAppNotes/AppNotes.aspx?appnote=en562793">http://www.microchip.com/wwwAppNotes/AppNotes.aspx?appnote=en562793</a> |
| EVB-LAN9355 Evaluation Board Schematic | Visit <a href="http://www.microchip.com">www.microchip.com</a>  |

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### 1.1.2 Terms and Abbreviations

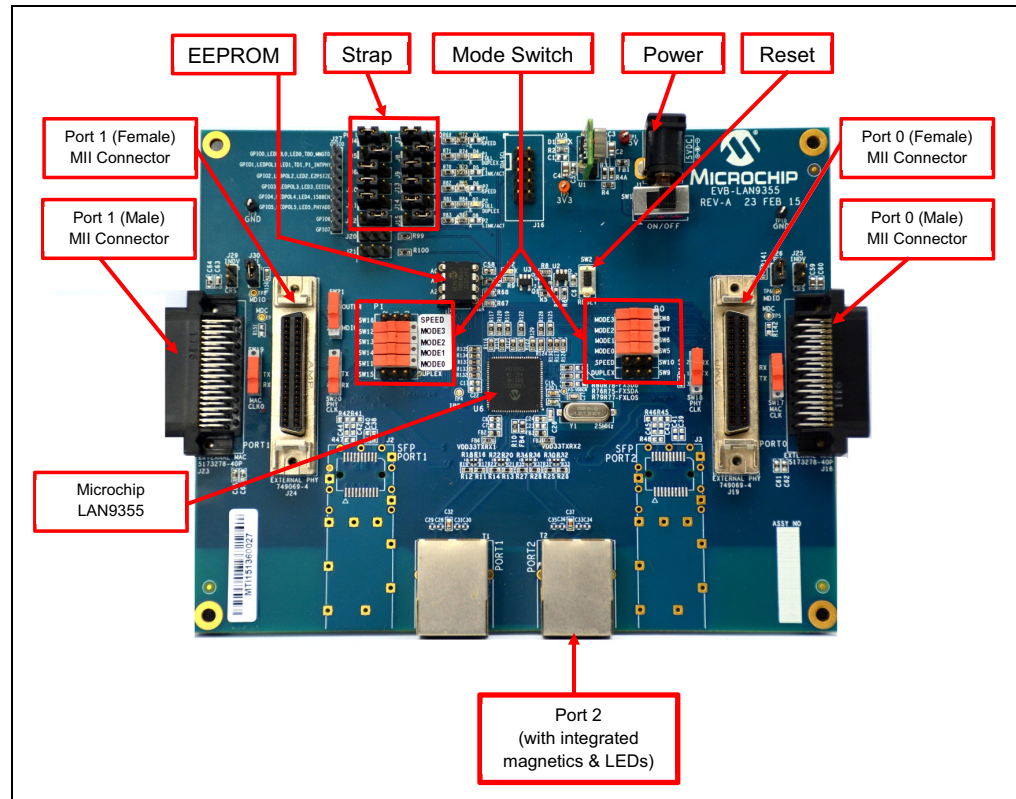
- **EVB** - Evaluation Board
- **DNP** - Do Not Populate
- **100BASE-TX** - 100 Mbps Fast Ethernet, IEEE802.3u Compliant
- **GPIO** - General Purpose I/O
- **MII** - Media Independent Interface
- **RMII** - Reduced Media Independent Interface
- **EEE** - Energy-Efficient Ethernet
- **SFP** - Small Form-factor Pluggable
- **SFF** - Small Form Factor
- **SMI** - Serial Management Interface

## Chapter 2. Board Details

### 2.1 BOARD DETAILS

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the EVB-LAN9355 is shown in Figure 2-1.

**FIGURE 2-1: LAN9355 BOARD REV-A**



#### 2.1.1 Power

DC 5V is applied through (J1) DC Socket, powered by a +5V external wall adapter switch (SW1) need to be ON position for the 5V to reach the 3.3V regulator. Glowing of Green LED (D1) indicates successful generation of 3.3V o/p. This Power is supplied to the LAN9355 and it has internal 1.2 V regulator which supplies power to the internal core logic.

#### 2.1.2 Power-on Reset

A power-on reset occurs whenever power is initially applied to the LAN9355 or if the power is removed and reapplied to the LAN9355. This event resets all circuitry within the LAN9355. After initial power-on, the LAN9355 can be reset by pressing the reset switch (SW2). The reset LED D2 will assert (red) when the LAN9355 is in reset condition.

For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

### **2.1.3 Clock**

The LAN9355 requires a fixed-frequency 25 MHz clock ( $\pm 50$  ppm) source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25 MHz crystal to the OSCI and OSCO pins. Optionally, this clock can be provided by driving the OSCI input pin with a single-ended 25 MHz clock source.

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## Chapter 3. Board Configuration

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### 3.1 STRAP OPTIONS

The following tables describe the default settings and jumper descriptions for the EVB-LAN9355. These defaults are the recommended configurations for evaluation of the LAN9355. These settings may be changed as needed, however, any deviation from the defaults settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

#### 3.1.1 Jumpers J4:J15

Jumpers J4 through J15 set various functions of the LAN9355. They can also be used as GPIOs, LED drivers. When used as LED drivers, as they are on the EVB-LAN9355, they are connected a specific way to set the strap value to a “1”, and another way to set the strap value to a “0”. Figure 3-1 illustrates the schematics connections with the D3 circuit as a pull-up, and the D4 circuit as a pull-down. To illuminate D3, the LAN9355 will drive the cathode of the D3 low. To illuminate D4, the LAN9355 will drive the cathode of the D4 high.

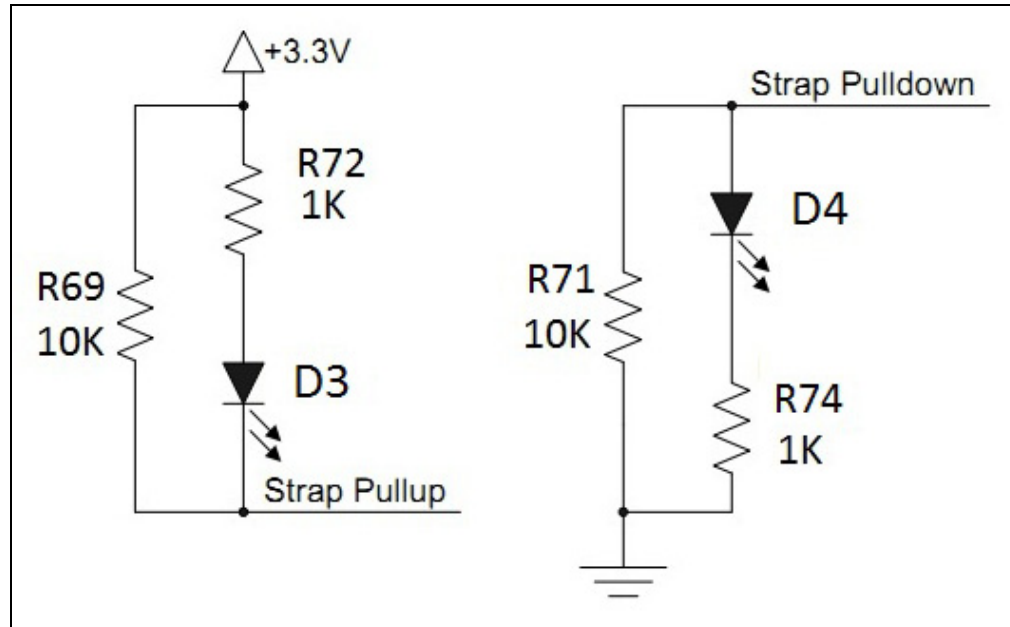
The J4 - J15 jumpers must be configured in pairs to identical settings in order to realize the D3 circuit or the D4 circuit. The pairings are as follows:

- J4 & J7
- J6 & J9
- J5 & J8
- J11 & J14
- J10 & J13
- J12 & J15

The following subsections detail the jumper pair settings, their associated strap settings, and the functional effects of setting the straps. All strap values are read during power-up and on the rising edge of nRST signal. Once the strap value is set, the LAN9355 will drive the LED's high or low for illumination according the strap value. For other designs which may use these pins as GPIOs refer to LAN9355 datasheet for additional information. In those cases, internal default straps must be changed by an I2C or SMI master or through EEPROM fields.



**FIGURE 3-1: LED STRAP CIRCUIT**



**3.1.1.1 GPIO/LED POL/LED CONFIGURATIONS:**

GPIO/LED POL/LED configuration straps are used to configure the default polarity of LEDs, GPIOs through jumpers as shown below in Table 3-1.

**TABLE 3-1: GPIO/LED POL/LED CONFIGURATIONS**

| Header    | Pin Settings | Signal Name                | Strap Value | Description                         |
|-----------|--------------|----------------------------|-------------|-------------------------------------|
| J4 & J7   | 1-2(default) | LEDPOL0<br>/GPIO0<br>/LED0 | 1           | The LED (D3) is set as active LOW.  |
|           | 2-3          |                            | 0           | The LED (D3) is set as active HIGH. |
| J5 & J8   | 1-2(default) | LEDPOL1<br>/GPIO1<br>/LED1 | 1           | The LED (D4) is set as active LOW.  |
|           | 2-3          |                            | 0           | The LED (D4) is set as active HIGH. |
| J6 & J9   | 1-2(default) | LEDPOL2<br>/GPIO2<br>/LED2 | 1           | The LED (D5) is set as active LOW.  |
|           | 2-3          |                            | 0           | The LED (D5) is set as active HIGH. |
| J10 & J13 | 1-2(default) | LEDPOL3<br>/GPIO3<br>/LED3 | 1           | The LED (D6) is set as active LOW.  |
|           | 2-3          |                            | 0           | The LED (D6) is set as active HIGH. |

**TABLE 3-1: GPIO/LED POL/LED CONFIGURATIONS (CONTINUED)**

| Header    | Pin Settings | Signal Name                | Strap Value | Description                         |
|-----------|--------------|----------------------------|-------------|-------------------------------------|
| J11 & J14 | 1-2(default) | LEDPOL4<br>/GPIO4<br>/LED4 | 1           | The LED (D7) is set as active LOW.  |
|           | 2 -3         |                            | 0           | The LED (D7) is set as active HIGH. |
| J12 & J15 | 1-2(default) | LEDPOL5<br>/GPIO5<br>/LED5 | 1           | The LED (D8) is set as active LOW.  |
|           | 2 -3         |                            | 0           | The LED (D8) is set as active HIGH. |

**3.1.1.2 SERIAL MANAGEMENT MODE CONFIGURATION**

Serial Management Mode selection strap (MNGT0) is used to configure the default value of the Serial Management Mode Strap hard-strap (serial\_mngt\_mode\_strap) through jumpers as shown below in Table 3-2.

**TABLE 3-2: SERIAL MANAGEMENT MODE CONFIGURATION**

| Header  | Pin Settings  | serial_mngt_mode_strap | Description      |
|---------|---------------|------------------------|------------------|
| J4 & J7 | 2-3           | 0                      | SMI Managed Mode |
| J4 & J7 | 1-2 (default) | 1                      | I2C Managed Mode |

**3.1.1.3 EEPROM SIZE CONFIGURATION:**

The EEPROM size configuration strap (J6 & J9) determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)\_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)\_24C512 as shown below in Table 3-3.

**TABLE 3-3: EEPROM SIZE CONFIGURATION**

| Header  | Pin Settings  | eprom_size_strap Value | Description   |
|---------|---------------|------------------------|---|
| J6 & J9 | 1-2 (default) | 1                      | EEPROM size = 32K bits (4k x 8) through 512K bits (64K x 8) |
|         | 2 -3          | 0                      | EEPROM size = 1K bits (128 x 8) through 16K bits (2K x 8)   |

**3.1.1.4 ENERGY-EFFICIENT ETHERNET CONFIGURATION**

EEEEEE\_ENEN configuration strap is used to configure the default value of the EEE Enable 2-1 soft-straps (EEE\_enable\_strap\_[2:1]) through jumpers as shown below in Table 3-4.

**Note:** “EEE\_enable\_strap\_1” strap is used for the LAN9355 when in Port 1 internal PHY mode.

**TABLE 3-4: EEE\_EN CONFIGURATION**

| Header    | Pin Settings | EEE_enable_strap_[2:1] Value | Description |
|-----------|--------------|------------------------------|-------------|
| J10 & J13 | 1-2(default) | 1                            | EEE Enable  |
|           | 2-3          | 0                            | EEE Disable |

**3.1.1.5 1588 ENABLE CONFIGURATION**

Energy Efficient Ethernet configuration strap is used to configure the default value of the 1588 Enable soft-strap (1588\_enable\_strap) through jumpers as shown below in Table 3-5.

**TABLE 3-5: 1588 ENABLE CONFIGURATION**

| Header    | Pin Settings  | 1588_enable_strap Value | Description  |
|-----------|---------------|-------------------------|--------------|
| J11 & J14 | 1-2 (default) | 1                       | 1588 Enable  |
|           | 2-3           | 0                       | 1588 Disable |

**3.1.1.6 PHY ADDRESS CONFIGURATION**

PHY Address selection strap is used to configure the default value of the Switch PHY Address Select soft-strap (phy\_addr\_sel\_strap) through jumpers as shown below in Table 3-6.

**TABLE 3-6: PHY ADDRESSING**

| Header    | Pin Settings  | PHY_ADDR_SEL_STRAP Value | VIRTUAL PHY 0 AND 1 DEFAULT ADDRESS VALUE | PHY A DEFAULT ADDRESS VALUE | PHY B DEFAULT ADDRESS VALUE |
|-----------|---------------|--------------------------|---|-----------------------------|-----------------------------|
| J12 & J15 | 1-2           | 1                        | 1   | 2                           | 3                           |
|           | 2-3 (default) | 0                        | 0   | 1                           | 2                           |

**3.1.2 GPIO 6 & GPIO 7 Input and Output Configurations**

GPIO 6 & 7 configuration straps are used to configure the default input value of the GPIO 6 and 7 through jumpers as shown below in Table 3-7 and Table 3-8.

**TABLE 3-7: GPIO 6 & 7 INPUT CONFIGURATION**

| Header | Pin Settings | Input | Signal Name |
|--------|--------------|-------|-------------|
| J20    | 1-2          | 1     | GPIO6       |
|        | 2-3          | 0     |             |
| J21    | 1-2          | 1     | GPIO7       |
|        | 2-3          | 0     |             |

**TABLE 3-8: GPIO 6 & 7 OUTPUT CONFIGURATION**

| Header | Pin | Output    | Signal Name |
|--------|-----|-----------|-------------|
| J20    | 2   | Push Pull | GPIO6       |
| J21    | 2   | Push Pull | GPIO7       |

**Note:** By default, the jumpers settings for J20 & J21 will be OPEN.

### 3.1.3 Link Partner Duplex/Speed Configurations

The “duplex\_strap\_0” strap from SW9 is used to determine the link partners duplex ability when in Port 0 MII MAC and RMII MAC modes.

The “speed\_strap\_0” strap from SW10 is used to determine the link partners speed ability and to determine the parallel detect speed when in Port 0 MII MAC and RMII MAC modes, as shown below in Table 3-9.

**TABLE 3-9: EMULATED LINK PARTNER DEFAULT ADVERTISED ABILITY FOR PORT 0**

| SW9<br>(P0_DUPLEX) | SW10<br>(P0_SPEED) | duplex_strap_0 | speed_strap_0 | ADVERTISED<br>LINK PARTNER<br>ABILITY       |
|--------------------|--------------------|----------------|---------------|---|
| 1-2                | 1-3                | 1              | 0             | 10BASE-T<br>full-duplex<br>(0010)           |
| 1-2                | 1-2                | 1              | 1             | 100BASE-X<br>full-duplex<br>(1000)          |
| 1-3                | 1-3                | 0              | 0             | 10BASE-T<br>half-duplex<br>(0001) (Default) |
| 1-3                | 1-2                | 0              | 1             | 100BASE-X<br>half-duplex<br>(0100)          |

**Note:** For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

The “duplex\_strap\_1” strap from SW15 is used to determine the link partners duplex ability when in Port 1 MII MAC and RMII MAC modes.

The “speed\_strap\_1” strap from SW16 is used to determine the link partners speed ability and to determine the parallel detect speed when in Port 1 MII MAC and RMII MAC modes, as shown below in Table 3-10.

**TABLE 3-10: EMULATED LINK PARTNER DEFAULT ADVERTISED ABILITY FOR PORT 1**

| SW15<br>(P1_DUPLEX) | SW16<br>(P1_SPEED) | duplex_strap_0 | speed_strap_0 | ADVERTISED<br>LINK PARTNER<br>ABILITY       |
|---------------------|--------------------|----------------|---------------|---|
| 1-2                 | 1-3                | 1              | 0             | 10BASE-T<br>full-duplex<br>(0010)           |
| 1-2                 | 1-2                | 1              | 1             | 100BASE-X<br>full-duplex<br>(1000)          |
| 1-3                 | 1-3                | 0              | 0             | 10BASE-T<br>half-duplex<br>(0001) (Default) |
| 1-3                 | 1-2                | 0              | 1             | 100BASE-X<br>half-duplex<br>(0100)          |

**Note:** For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

**3.1.4 Port 0/Port 1 Mode Configurations**

Port 0 Mode configuration straps (SW5, SW6, SW7 & SW8) are used to configure the hard-straps such as Switch Port 0 Mode Strap (P0\_mode\_strap[1:0]), Switch Port 0 RMII Clock Direction Strap (P0\_rmii\_clock\_dir\_strap) and Switch Port 0 Clock Strength Strap (P0\_clock\_strength\_strap) as shown below in Table 3-11.

**TABLE 3-11: PORT 0 MODE STRAP MAPPING**

| P0_MODE3 (SW8) | P0_MODE2 (SW7) | P0_MODE1 (SW6) | P0_MODE0 (SW5) | MODE                    |
|----------------|----------------|----------------|----------------|-------------------------|
| 1-3            | 1-3            | X              | X              | MII MAC (default)       |
| 1-3            | 1-2            | 1-3            | X              | MII PHY                 |
| 1-3            | 1-2            | 1-2            | 1-3            | Turbo MII PHY 12 ma     |
| 1-3            | 1-2            | 1-2            | 1-2            | Turbo MII PHY 16 ma     |
| 1-2            | 1-3            | 1-3            | X              | RMII MAC clock in       |
| 1-2            | 1-3            | 1-2            | 1-3            | RMII MAC clock out 12ma |
| 1-2            | 1-3            | 1-2            | 1-2            | RMII MAC clock out 16ma |
| 1-2            | 1-2            | 1-3            | X              | RMII PHY clock in       |
| 1-2            | 1-2            | 1-2            | 1-3            | RMII PHY clock out 12ma |
| 1-2            | 1-2            | 1-2            | 1-2            | RMII PHY clock out 16ma |

**Note:** For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

Port 1 Mode configuration straps (SW11, SW14, SW13 & SW12) are used to configure the hard-straps such as Switch Port 1 Mode Strap (P1\_mode\_strap[1:0]), Switch Port 1 RMII Clock Direction Strap (P1\_rmii\_clock\_dir\_strap) and Switch Port 1 Clock Strength Strap (P1\_clock\_strength\_strap) as shown below in Table 3-12.

**TABLE 3-12: PORT 1 MODE STRAP MAPPING**

| P1_INTPHY (J5 & J8) | P1_MODE3 (SW12) | P1_MODE2 (SW13) | P1_MODE1 (SW14) | P1_MODE0 (SW11) | MODE                    |
|---------------------|-----------------|-----------------|-----------------|-----------------|-------------------------|
| 2-3                 | 1-3             | 1-3             | X               | X               | MII MAC (default)       |
| 2-3                 | 1-3             | 1-2             | 1-3             | X               | MII PHY                 |
| 2-3                 | 1-3             | 1-2             | 1-2             | 1-3             | Turbo MII PHY 12 ma     |
| 2-3                 | 1-3             | 1-2             | 1-2             | 1-2             | Turbo MII PHY 16 ma     |
| 2-3                 | 1-2             | 1-3             | 1-3             | X               | RMII MAC clock in       |
| 2-3                 | 1-2             | 1-3             | 1-2             | 1-3             | RMII MAC clock out 12ma |
| 2-3                 | 1-2             | 1-3             | 1-2             | 1-2             | RMII MAC clock out 16ma |
| 2-3                 | 1-2             | 1-2             | 1-3             | X               | RMII PHY clock in       |
| 2-3                 | 1-2             | 1-2             | 1-2             | 1-3             | RMII PHY clock out 12ma |
| 2-3                 | 1-2             | 1-2             | 1-2             | 1-2             | RMII PHY clock out 16ma |
| 1-2                 | X               | X               | X               | X               | Internal PHY            |

**Note:** For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

### 3.1.5 RMII RX Clock Configurations

When LAN9355 is in MAC/PHY mode the reference clock routed either through TX or RX Clock as shown in Table 3-13.

**TABLE 3-13: RX CLOCK CONFIGURATIONS FOR PORT 0**

| Switch Settings      | DESCRIPTION                        | Mode     |
|----------------------|------------------------------------|----------|
| SW19 (1-3) (Default) | TX Clock used as a Reference Clock | RMII MAC |
| SW19 (1-2)           | RX Clock used as a Reference Clock | RMII MAC |
| SW20 (1-3) (Default) | Reference clock used as a TX clock | RMII PHY |
| SW20 (1-2)           | Reference clock used as a RX clock | RMII PHY |

### 3.1.6 GPIO Header

J27 connector is used for GPIO header. Respective pin details are given below in Table 3-14.

**TABLE 3-14: PIN NAMES FOR GPIO HEADER**

| Signal Name | Pin Number |
|-------------|------------|
| GPIO0       | J27.1      |
| GPIO1       | J27.2      |
| GPIO2       | J27.3      |
| GPIO3       | J27.4      |
| GPIO4       | J27.5      |
| GPIO5       | J27.6      |
| GPIO6       | J27.7      |
| GPIO7       | J27.8      |

### 3.1.7 I2C Aardvark® Header

J16 connector is used for I2C Aardvark header. Respective pin details are given below in Table 3-15.

**TABLE 3-15: PIN NAMES FOR I2C AARDVARK HEADER**

| Signal Name | Pin Number     |
|-------------|----------------|
| I2C2_SCL    | J16.1          |
| I2C2_SDA    | J16.3          |
| GND         | J16.2 & J16.10 |

### 3.1.8 Copper and Fiber Mode Selections

The LAN9355 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFF) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) in SFP mode. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resistor assembly options must to be configured.

**Note:** Vendor part number for SFP Transceiver: Finisar/FTLF1217P2.

### 3.1.8.1 COPPER MODE

The EVB-LAN9355 is set to Copper Mode by default. Table 3-16 details the required strap resistors settings for Copper Mode operation.

**TABLE 3-16: COPPER MODE STRAP RESISTORS**

| Resistors      | Signal Names | Description   |
|----------------|--------------|---|
| R79 (10K)      | FXLOSEN      | Copper twisted pair for ports A and B further determined by FXSDENA and FXSDENB |
| R76, R80 (10K) | FXSDA/FXSDB  | Configures Port 0 and Port 1 to Copper Mode                                     |

**Note:** R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-17 must be assembled for Copper Mode operation.

**TABLE 3-17: COPPER MODE SIGNAL ROUTING RESISTORS**

| Resistors          | Description                   |
|--------------------|-------------------------------|
| R17, R19, R21, R23 | Port 0 Copper mode is Enabled |
| R31, R33, R35, R37 | Port 1 Copper mode is Enabled |

**Note:** R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

### 3.1.8.2 FIBER MODE

The LAN9355 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resistors must be configured.

**Note:** Copper Mode related resistors must be DNP while Fiber Mode is active (See **Section 3.1.8.1 “Copper Mode”**).

Table 3-18 details the required strap resistor settings for Fiber Mode operation.

**TABLE 3-18: FIBER MODE STRAP RESISTORS**

| Resistors      | Description                                       |
|----------------|---|
| R77 (10K)      | Configures Port 0 & 1 to FX_LOS Mode              |
| R75, R78 (10K) | Configures Port 0 & 1 to Fiber mode, respectively |

**Note:** R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-19 must be assembled for Fiber Mode operation.

**TABLE 3-19: FIBER MODE SIGNAL ROUTING RESISTORS**

| Resistors          | Description               |
|--------------------|---------------------------|
| R16, R18, R20, R22 | Port 0 Fiber mode Enabled |
| R30, R32, R34, R36 | Port 1 Fiber mode Enabled |

**Note:** R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

### 3.1.8.3 FX-LOS FIBER MODE STRAP

FX-LOS strap details are shown in Table 3-20. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

**TABLE 3-20: FX-LOS MODE STRAP SETTINGS**

| R77 (10K) | R79 (10K) | Reference Voltage (v) | Function  |
|-----------|-----------|-----------------------|---|
| Populate  | DNP       | 3.3                   | A level above 2V selects FX-LOS for Port 0 and Port 1   |
| Populate  | Populate  | 1.5                   | A level of 1.5V selects FX-LOS for Port 0 and FX-SD / Copper twisted pair for Port 1, further determined by FXSDB |
| DNP       | Populate  | 0 (Default)           | A level of 0V selects FX-SD / Copper twisted pair for Ports 0 and 1, further determined by FXSDA, FXSDB           |

**Note:** The above strap details describe the LAN9355 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

## 3.2 LEDS

Table 3-21 describes the different LED references and their corresponding colors and indications.

**TABLE 3-21: LEDS**

| Reference | Color | Indication                     |
|-----------|-------|--------------------------------|
| D1        | Green | 3.3V Power active              |
| D2        | Red   | LAN9355 is in reset condition  |
| D4        | Green | Full-duplex / Collision Port 1 |
| D6        | Green | Full-duplex / Collision Port 2 |

**Note:** Assumes the LED\_FUN field of the LED\_CFG register is 00b.

## 3.3 TEST POINTS

Table 3-22 describes the different test points and their corresponding connections.

**TABLE 3-22: TEST POINTS**

| Test Points | Description                  | Connection |
|-------------|------------------------------|------------|
| TP1         | Single pin populated 5V      | 5V_EXT     |
| TP2         | Single pin populated 3V3     | 3V3        |
| TP3         | Single pin unpopulated VDDCR | VDDCR      |



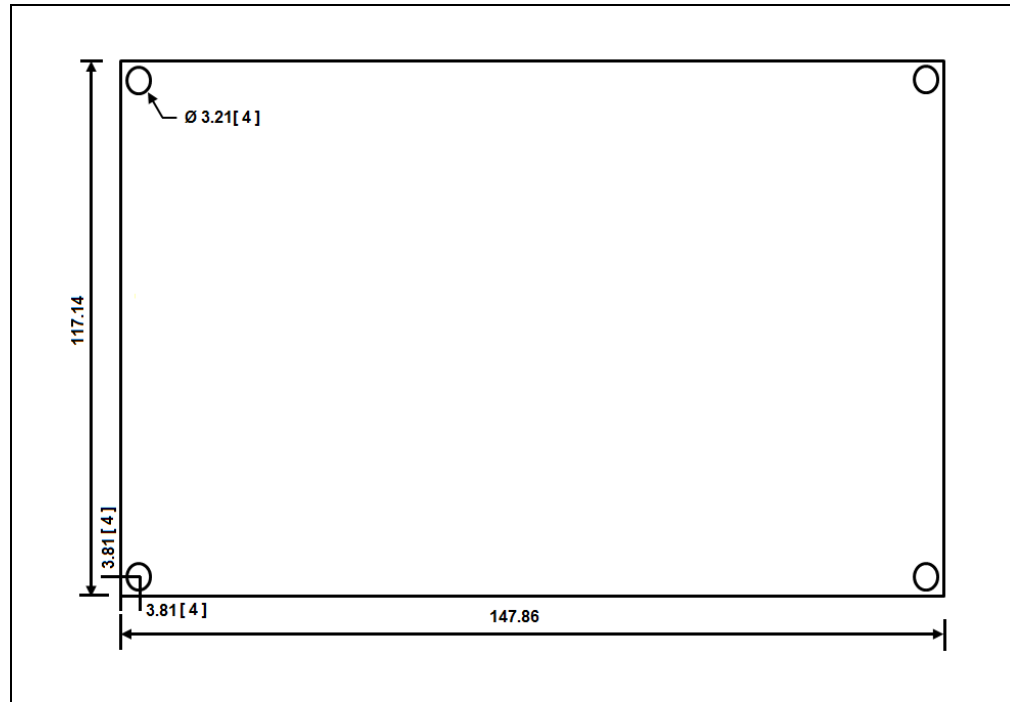
**TABLE 3-22: TEST POINTS**

| Test Points | Description                    | Connection |
|-------------|--------------------------------|------------|
| TP4         | Single pin unpopulated IRQ     | IRQ        |
| TP5         | Single pin unpopulated P0_MDC  | P0_MDC     |
| TP6         | Single pin unpopulated P0_MDIO | P0_MDIO    |
| TP7         | Single pin unpopulated P1_MDC  | P1_MDC     |
| TP8         | Single pin unpopulated P1_MDIO | P1_MDIO    |
| TP9         | Single pin populated GND       | GND        |
| TP10        | Single pin populated GND       | GND        |

## 3.4 MECHANICALS

Figure 3-2 displays details for EVB-LAN9355 mechanical dimensions. Dimensions are in mm.

**FIGURE 3-2: LAN9355 EVB MECHANICAL DIMENSIONS**

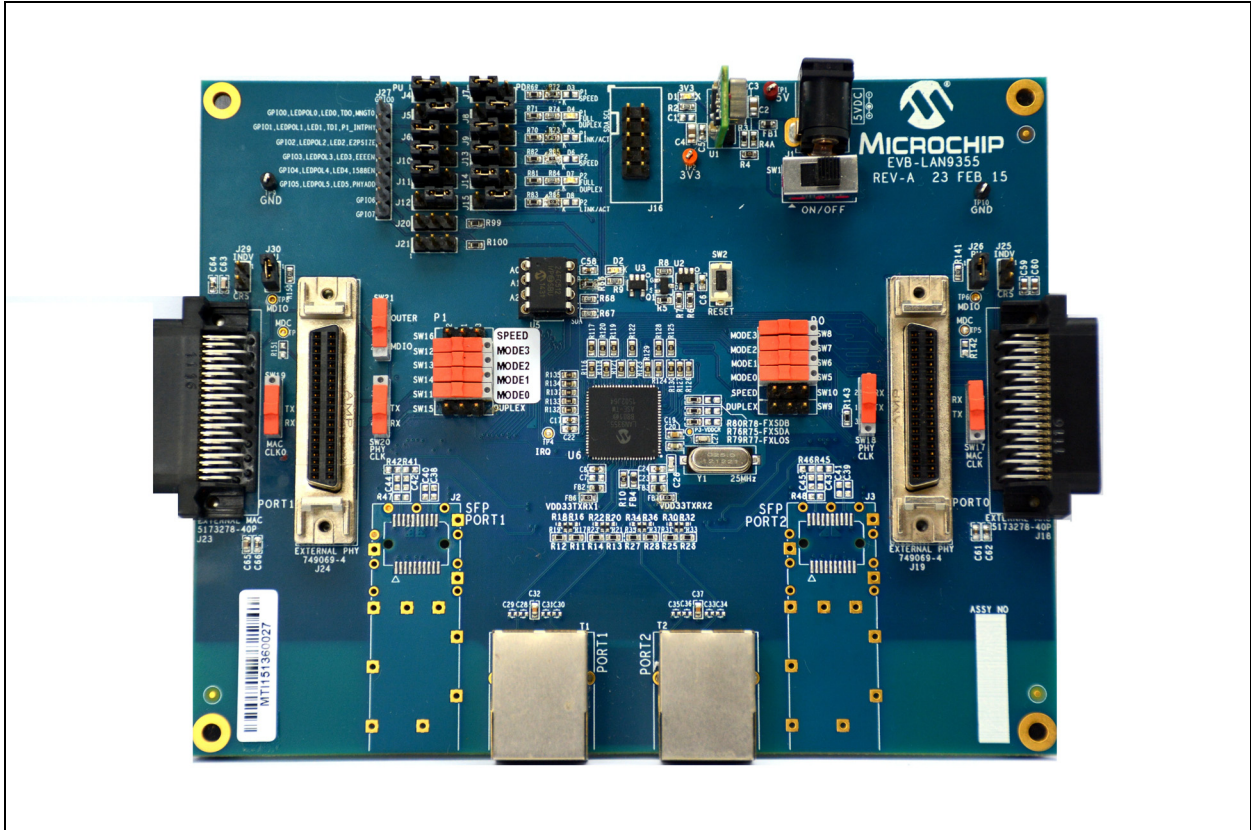


**Appendix A. EVB-LAN9355 Evaluation Board**

**A.1 INTRODUCTION**

This appendix shows the EVB-LAN9355 Evaluation Board.

**FIGURE A-1: EVB-LAN9355 EVALUATION BOARD**





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## **Appendix B. EVB-LAN9355 Evaluation Board Schematics**

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### **B.1 INTRODUCTION**

This appendix shows the EVB-LAN9355 Evaluation Board Schematics.

FIGURE B-1: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 1

### EVB-LAN9355 Block Diagram

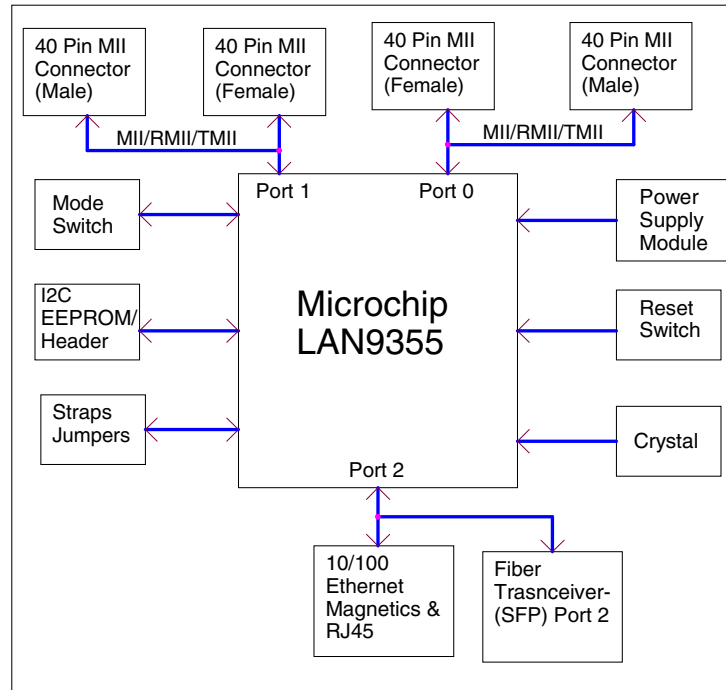


FIGURE B-2: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 2

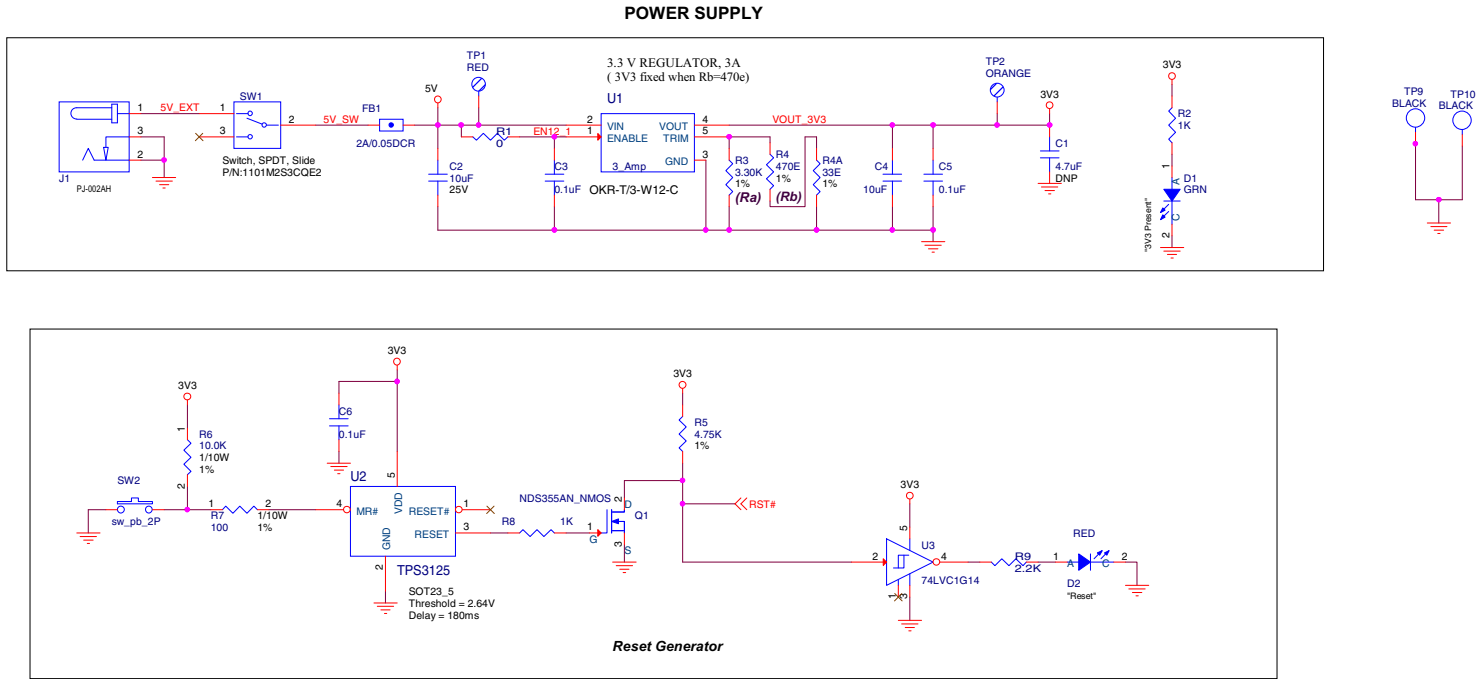
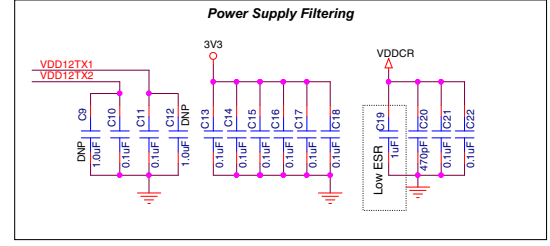
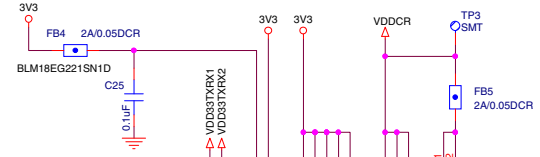
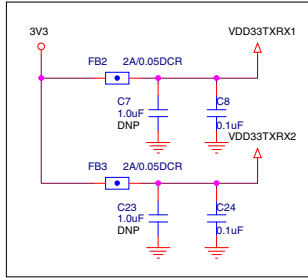


FIGURE B-3: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 3



Note: OSCVSS need to connect to Chip grd.

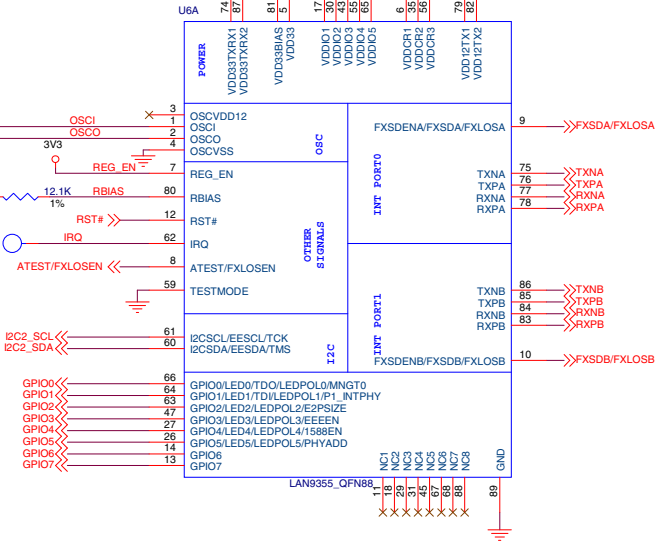
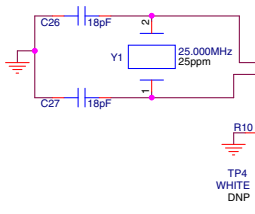


FIGURE B-4: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 4

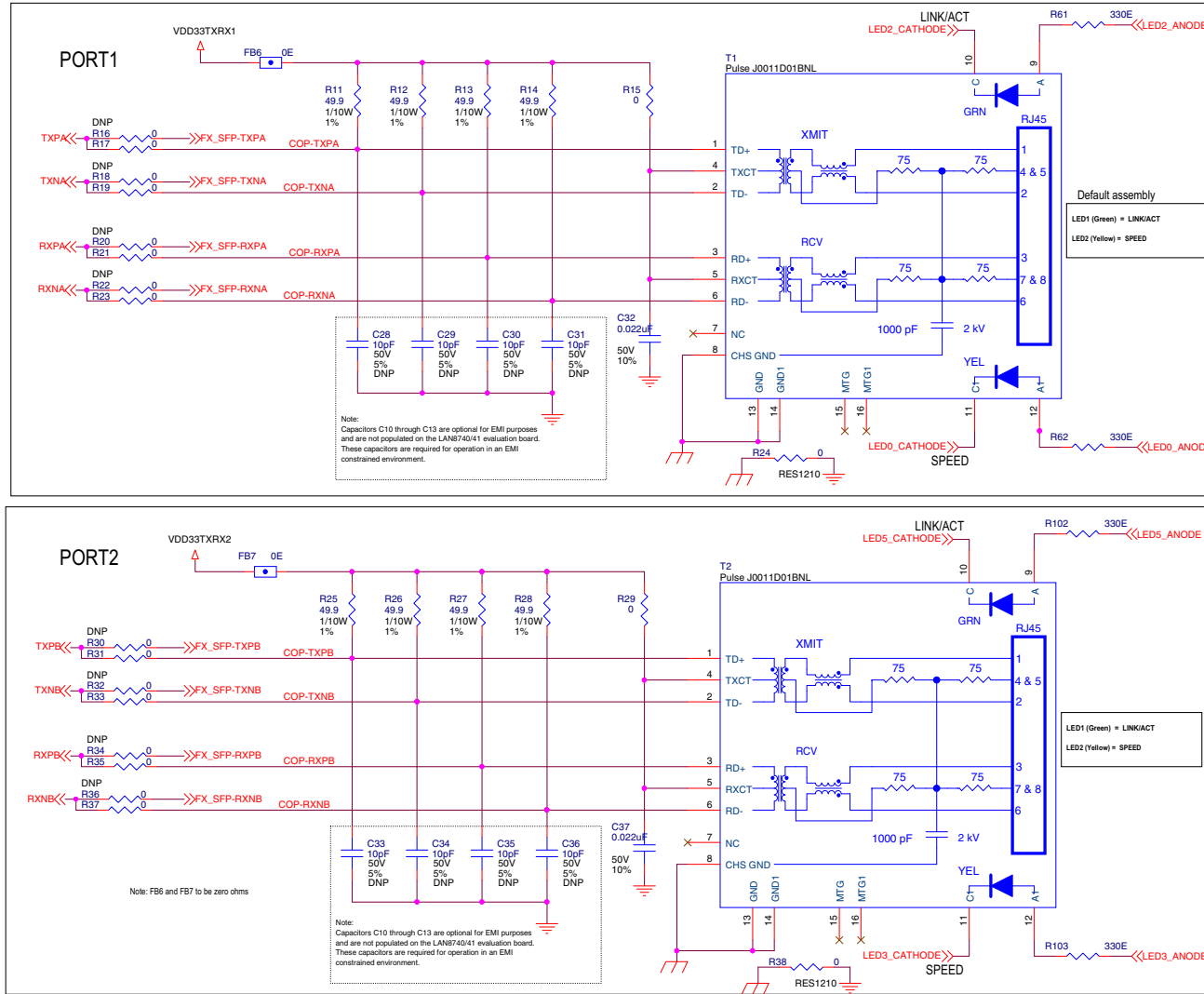
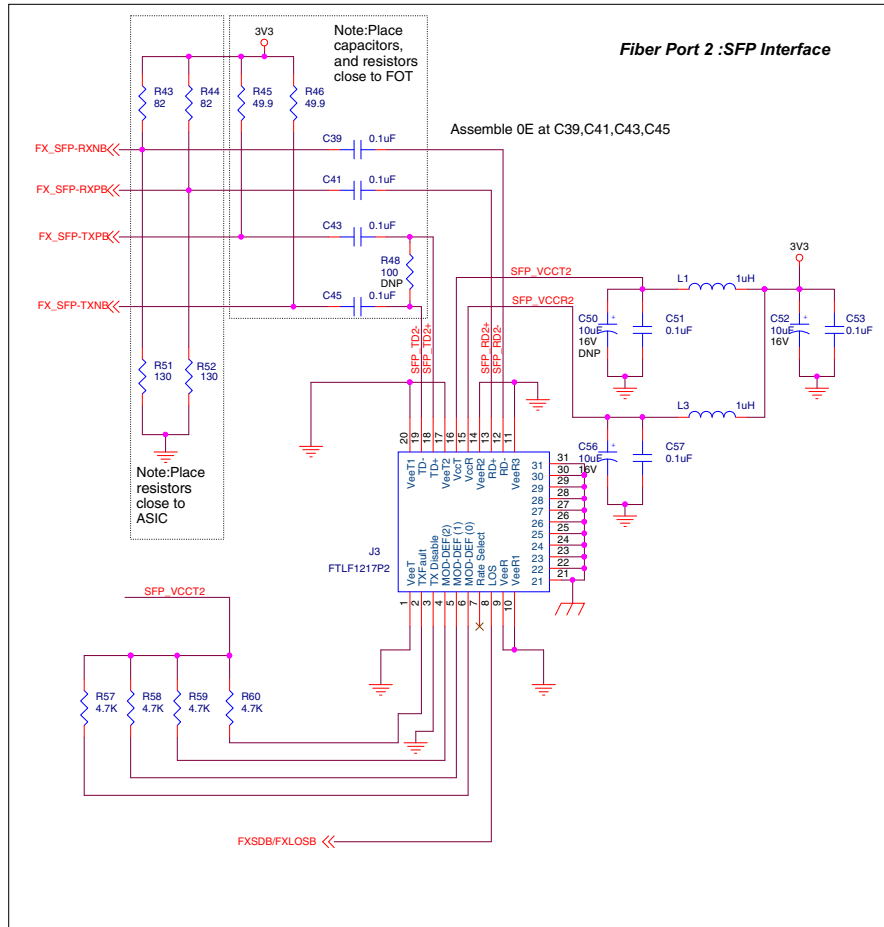
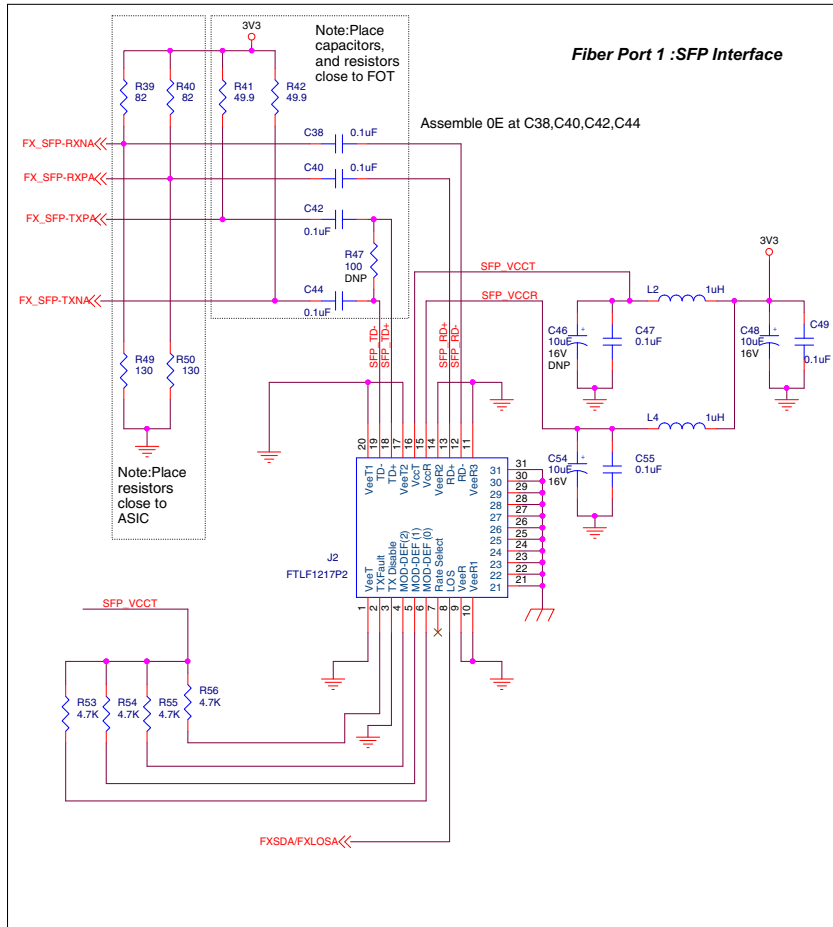


FIGURE B-5: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 5



Note: Fiber mode related components are Not Populated on EVB (Default)



**FIGURE B-6: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 6**

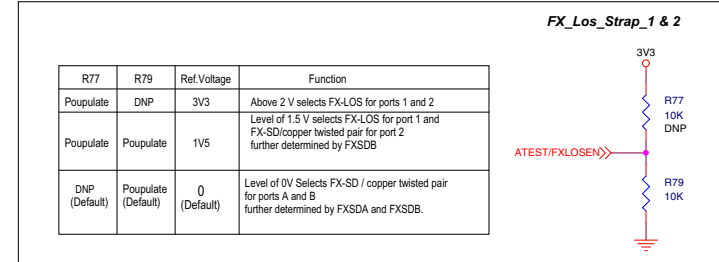
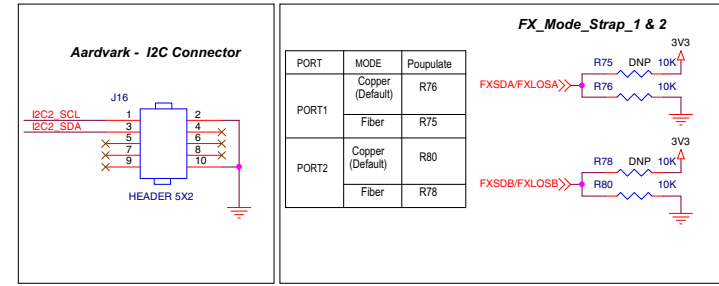
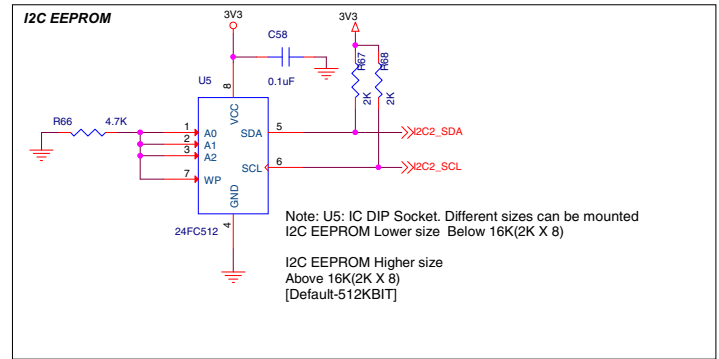
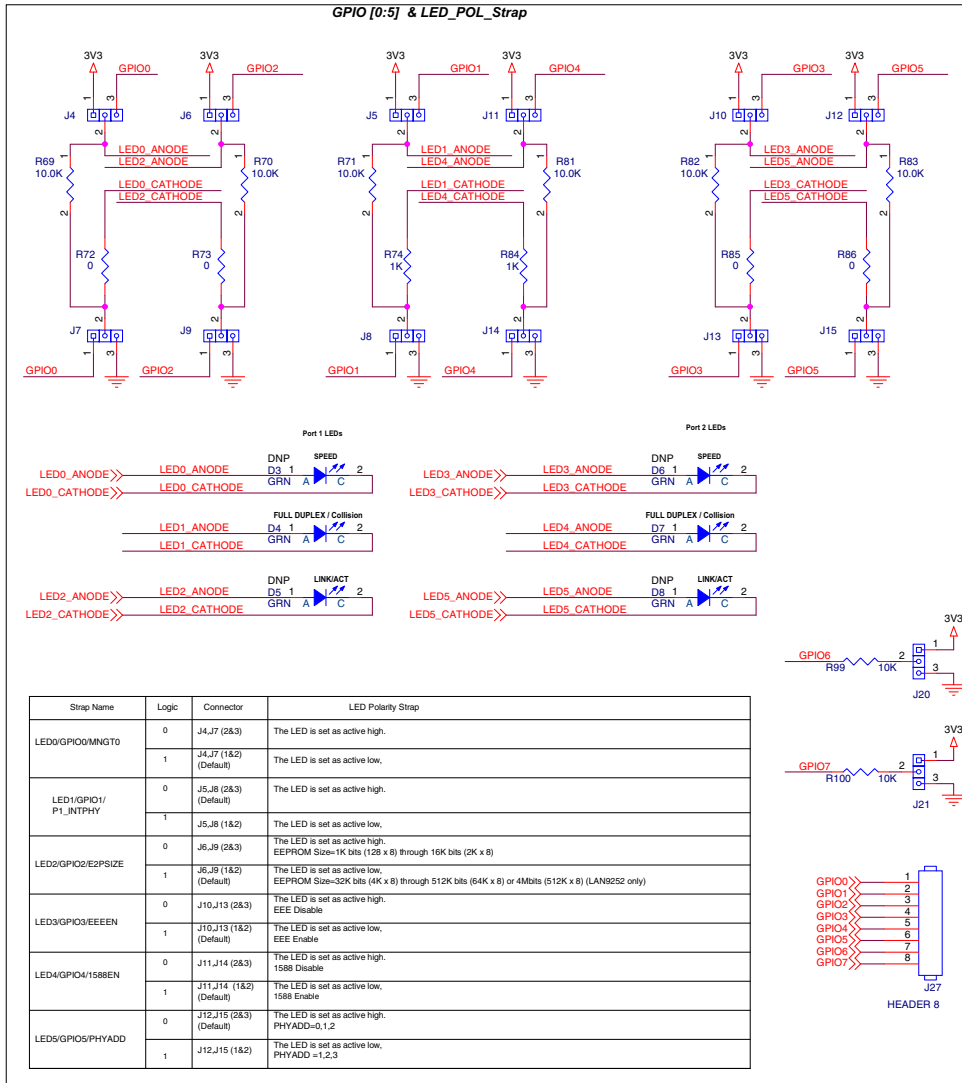
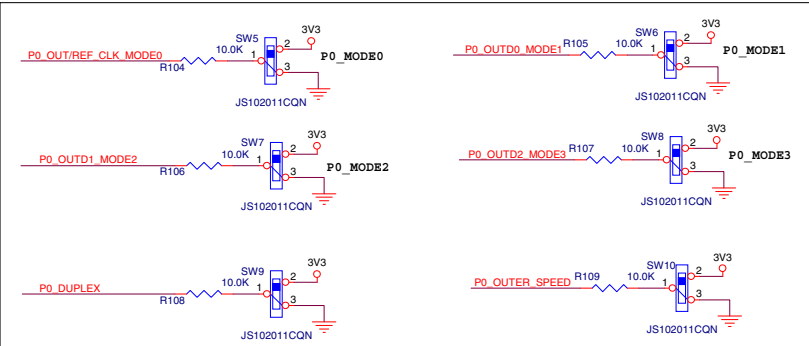


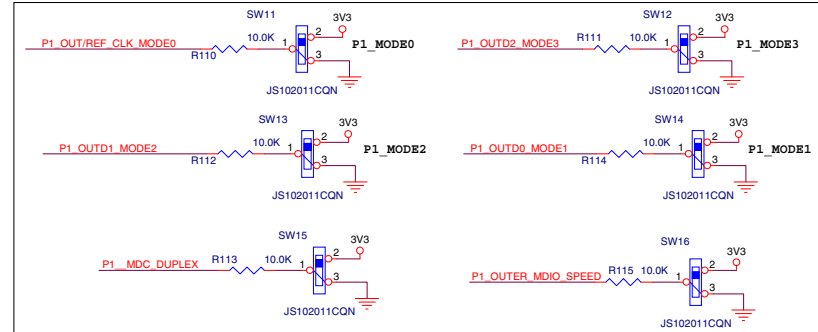
FIGURE B-7: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 7



Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .

PORT 0 MODE STRAP MAPPING

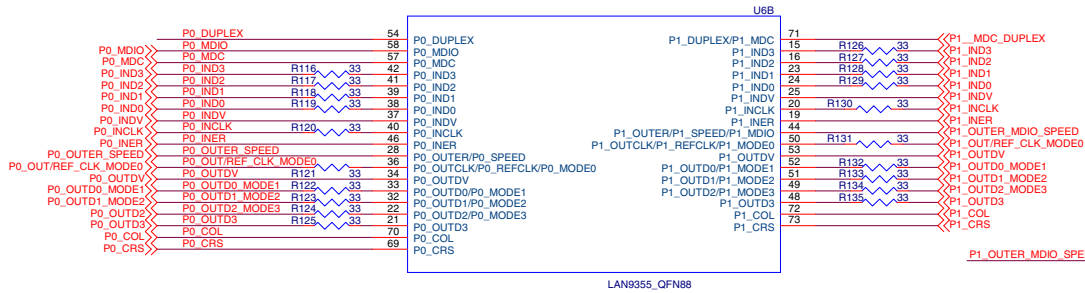
| P1_INTPHY (J5 & J8) | P0_MODE3 (SW9) | P0_MODE2 (SW7) | P0_MODE1 (SW6) | P0_MODE0 (SW5) | Port 0 Mode             |
|---------------------|----------------|----------------|----------------|----------------|-------------------------|
| x                   | 0              | 0              | x              | x              | MII MAC (Default)       |
| x                   | 0              | 1              | 0              | x              | MII PHY                 |
| x                   | 0              | 1              | 1              | 0              | Turbo MII PHY 12 ma     |
| x                   | 0              | 1              | 1              | 1              | Turbo MII PHY 16 ma     |
| x                   | 1              | 0              | 0              | x              | RMII MAC clock in       |
| x                   | 1              | 0              | 1              | 0              | RMII MAC clock out 12ma |
| x                   | 1              | 0              | 1              | 1              | RMII MAC clock out 16ma |
| x                   | 1              | 1              | 0              | x              | RMII PHY clock in       |
| x                   | 1              | 1              | 1              | 0              | RMII PHY clock out 12ma |
| x                   | 1              | 1              | 1              | 1              | RMII PHY clock out 16ma |



Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .

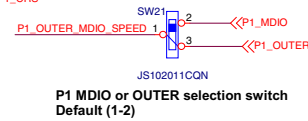
PORT 1 MODE STRAP MAPPING

| P1_INTPHY (J5 & J8) | P1_MODE3 (SW12) | P1_MODE2 (SW13) | P1_MODE1 (SW14) | P1_MODE0 (SW11) | Port 1 Mode             |
|---------------------|-----------------|-----------------|-----------------|-----------------|-------------------------|
| 0                   | 0               | 0               | x               | x               | MII MAC (Default)       |
| 0                   | 0               | 1               | 0               | x               | MII PHY                 |
| 0                   | 0               | 1               | 1               | 0               | Turbo MII PHY 12 ma     |
| 0                   | 0               | 1               | 1               | 1               | Turbo MII PHY 16 ma     |
| 0                   | 1               | 0               | 0               | x               | RMII MAC clock in       |
| 0                   | 1               | 0               | 1               | 0               | RMII MAC clock out 12ma |
| 0                   | 1               | 0               | 1               | 1               | RMII MAC clock out 16ma |
| 0                   | 1               | 1               | 0               | x               | RMII PHY clock in       |
| 0                   | 1               | 1               | 1               | 0               | RMII PHY clock out 12ma |
| 0                   | 1               | 1               | 1               | 1               | RMII PHY clock out 16ma |
| 1                   | x               | x               | x               | x               | Internal PHY            |



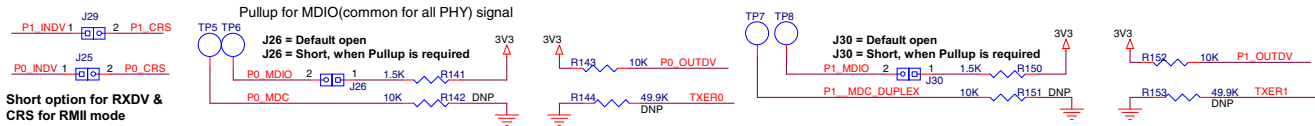
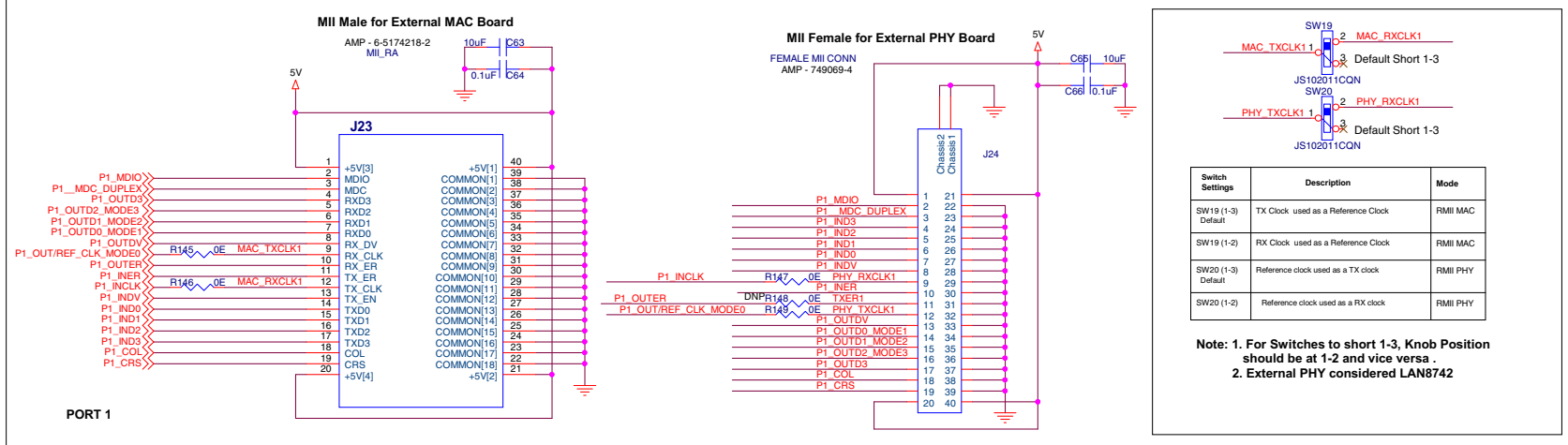
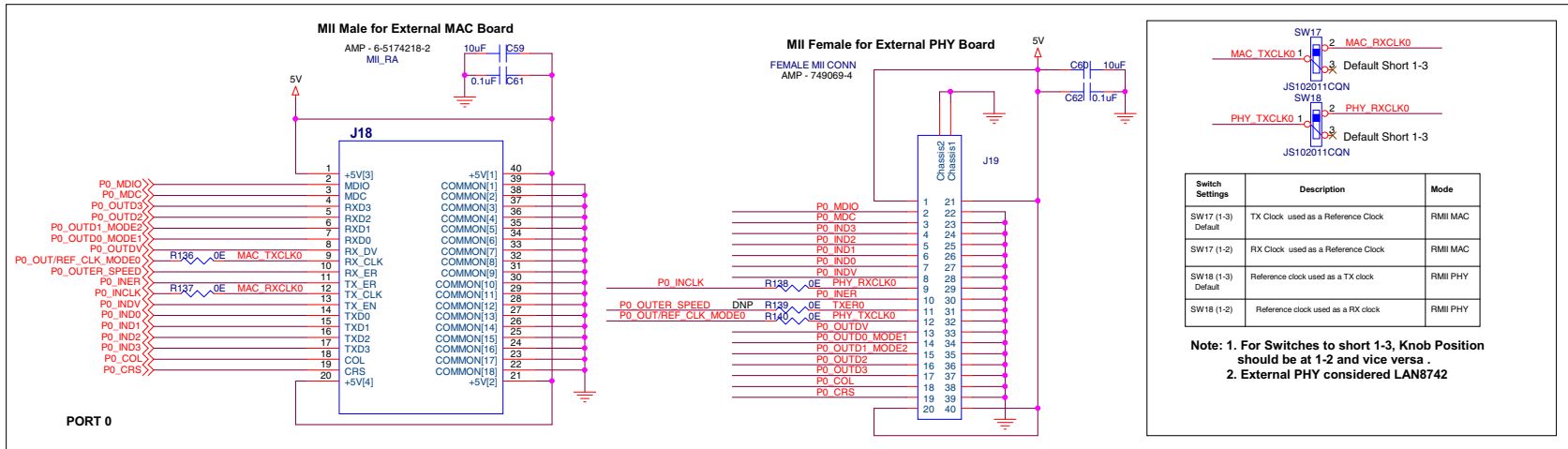
Emulated Link Partner Default Advertised Ability

| SW9 (P0_DUPLEX) / SW15 (P1_DUPLEX) | SW10 (P0_SPEED) / SW16 (P1_SPEED) | ADVERTISED LINK PARTNER ABILITY (Bits 8,7,6,5) |
|------------------------------------|-----------------------------------|--|
| 1                                  | 0                                 | 10BASE-T full-duplex (0010)                    |
| 1                                  | 1                                 | 100BASE-X full-duplex (1000) (Default)         |
| 0                                  | 0                                 | 10BASE-T half-duplex (0001)                    |
| 0                                  | 1                                 | 100BASE-X half-duplex (0100)                   |



P1 MDIO or OUTER selection switch Default (1-2)

FIGURE B-8: EVB-LAN9355 EVALUATION BOARD SCHEMATIC 8





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## **Appendix C. Bill of Materials (BOM)**

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### **C.1 INTRODUCTION**

This appendix includes the EVB-LAN9355 Evaluation Board Bill of Materials (BOM).

Configuration: One internal copper mode with higher size EEPROM (24FC512)

**TABLE C-1: EVB-LAN9355 EVALUATION BOARD BILL OF MATERIALS**

| Item | Qty | Reference Designator(s)   | Part                      | PCB Footprint             | Manufacturer      | Manufacturer Part Number |
|------|-----|---|---------------------------|---------------------------|-------------------|--------------------------|
| 1    | 2   | C2,C4   | 10uF                      | CAP0805                   | Murata            | GRM21BR61E106KA73L       |
| 2    | 21  | C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17,C18,C21,C22,C24,C25,C58,C61,C62,C64,C66 | 0.1uF                     | CAP0603                   | Murata            | GRM155R61E104KA7D        |
| 3    | 1   | C19   | 1uF                       | CAP0603                   | Murata            | GRM188R61C105KA93D       |
| 4    | 1   | C20   | 470pF                     | CAP0603                   | Murata            | GRM033R71E471KA01D       |
| 5    | 2   | C26,C27   | 18pF                      | CAP0603                   | Murata            | GRM1885C1H180JA01D       |
| 6    | 2   | C32,C37   | 0.022uF                   | CAP0603                   | Kemet             | C0603C223K5RACTU         |
| 7    | 4   | C59,C60,C63,C65   | 10uF                      | CAP0603                   | TDK               | C1608X5R0J106K080AB      |
| 8    | 3   | D1,D4,D7  | GRN                       | LED0603                   | Würth electronics | 150 060 GS7 500 0        |
| 9    | 1   | D2  | RED                       | LED0603                   | Würth electronics | 150 060 RS7 500 0        |
| 10   | 5   | FB1,FB2,FB3,FB4,FB5   | 2A/0.05DCR                | RES0603                   | Murata            | BLM18EG221SN1D           |
| 11   | 1   | J1  | SKT_P-WR_2R0mm_4A_THRU_RA | th_conn_pwrjack_dc-210_rt | Cui Stack         | PJ-002AH                 |
| 12   | 18  | J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15,J20,J21,J28,J29,J30,J31               | HDR_1x3                   | TH_CONN_1X3P              | FCI               | 68000-103HLF             |
| 13   | 1   | J16   | HEADER 5X2                | th_conn_2x5p_BOX          | FCI               | 67997-210HLF             |
| 14   | 2   | J18,J23   | MII_RA                    | TH_CON-N_TE-5173278_40P   | TE                | 5173278-2-ND             |
| 15   | 2   | J19,J24   | FEMALE MII CONN           | TH_CONN_MII-749069-4      | TE                | 749069-4-ND              |
| 16   | 4   | J22,J25,J26,J32   | CONN_2P                   | th_conn_1x2p              | FCI               | 68000-102HLF             |
| 17   | 1   | J27   | HEADER 8                  | TH_CONN_1X8P              | FCI               | 68000-108HLF             |
| 18   | 1   | Q1  | NDS355AN_NMOS             | soT23-NDS                 | Fairchild         | NDS355AN                 |
| 19   | 17  | R1,R15,R29,R136,R137,R138,R140,R145,R146,R147,R149, FB6,FB7, R72,R73,R85,R86    | 0E                        | RES0603                   | Panasonic         | ERJ-3GEY0R00V            |
| 20   | 4   | R2,R8,R74,R84   | 1K                        | RES0603                   | Panasonic         | ERJ-3GEYJ102V            |
| 21   | 1   | R3  | 3.30K                     | RES0603                   | Yageo America     | 9C06031A3301FKHFT        |
| 22   | 1   | R4  | 470E                      | RES0603                   | BOURNS            | CR0603-FX-4700ELF        |
| 23   | 1   | R4A   | 33E                       | RES0603                   | BOURNS            | CR0603-FX-33R0ELF        |
| 24   | 1   | R5  | 4.75K                     | RES0603                   | Panasonic         | ERJ-3EKF4751V            |

**TABLE C-1: EVB-LAN9355 EVALUATION BOARD BILL OF MATERIALS (CONTINUED)**

| Item | Qty | Reference Designator(s)   | Part                | PCB Footprint            | Manufacturer             | Manufacturer Part Number  |
|------|-----|---|---------------------|--------------------------|--------------------------|---------------------------|
| 25   | 26  | R6,R69,R70,R71,R81,R82,R83,R76,R79,R80,R99,R100,R143,R152,R104,R105,R106,R107,R108,R109,R110,R111,R112,R113,R114,R115 | 10.0K               | RES0603                  | Panasonic                | ERJ-3EKF1002V             |
| 26   | 1   | R7  | 100E                | RES0603                  | Panasonic                | ERJ-3EKF1000V             |
| 27   | 1   | R9  | 2.2K                | RES0603                  | Panasonic                | ERJ-3GEYJ222V             |
| 28   | 1   | R10   | 12.1K               | RES0603                  | Rohm                     | MCR01MZPF1202             |
| 29   | 8   | R11,R12,R13,R14,R25,R26,R27,R28   | 49.9E               | RES0603                  | Yageo America            | 9C06031A49R9FKHFT         |
| 30   | 8   | R17,R19,R21,R23,R31,R33,R35,R37   | 0E                  | RES0402                  | Panasonic                | ERJ-2GE0R00X              |
| 31   | 2   | R24,R38   | 0E                  | RES1210                  | Vishay                   | CRCW12100000Z0EA          |
| 32   | 4   | R61,R62,R102,R103   | 330E                | RES0603                  | Panasonic                | ERJ-3GEYJ331V             |
| 33   | 2   | R67,R68   | 2K                  | RES0603                  | Panasonic                | ERJ-3GEYJ202V             |
| 34   | 20  | R116,R117,R118,R119,R120,R121,R122,R123,R124,R125,R126,R127,R128,R129,R130,R131,R132,R133,R134,R135                   | 33E                 | RES0603                  | Bourns Inc.              | CR0603-JW-330ELF          |
| 35   | 2   | R141,R150   | 1.5K                | RES0603                  | Panasonic                | ERJ-3GEYJ152V             |
| 36   | 1   | SW1   | SW-SPDT-SLIDE       | sw_ck_1101m2s3cq2        | C&K                      | 1101M2S3CQE2              |
| 37   | 1   | SW2   | sw_pb_2P            | sw_pb_2P                 | Panasonic                | EVQ-PJU04K                |
| 38   | 13  | SW5,SW6,SW7,SW8,SW9,SW10,SW11,SW12,SW13,SW14,SW15,SW16,SW17   | JS102011CQN         | TH_SW_SPST_3P_10x2p5     | Würth electronics        | 450301014042              |
| 39   | 1   | TP1   | RED                 | TH_TP_60D40              | Keystone                 | 5000                      |
| 40   | 1   | TP2   | ORANGE              | TH_TP_60D40              | Keystone                 | 5003                      |
| 41   | 2   | TP9,TP10  | BLACK               | TH_TP_60D40              | Keystone                 | 5001                      |
| 42   | 2   | T1,T2   | Pulse - J0011D01BNL | th_conn_pulse_rj45_j0026 | Pulse Electronics        | 553-1483-ND               |
| 43   | 1   | U1  | 3_Amp               | TH_DC-DC_VERT_5PIN_P67   | Murata                   | OKR-T/3-W12-C             |
| 44   | 1   | U2  | TPS3125             | SOT23_5                  | TI                       | TPS3125L30DBVR            |
| 45   | 1   | U3  | 74LVC1G14           | SOT23_5                  | TI                       | SN74LVC1G14DCKR           |
| 46   | 1   | U5  | Round Base          | IC_DIP8_300              | Assmann                  | AR08-HZL-TT-R             |
| 47   | 1   | U5  | 24FC512             | IC_DIP8_300              | Microchip                | 24FC512-I/P               |
| 48   | 1   | U6  | LAN9355_QFN88       | IC_QFN88                 | Microchip                | LAN9355                   |
| 49   | 1   | Y1  | 25.000MHz           | XTAL_HCM49               | Cardinal Components Inc. | CSM1Z-A5B2C5-40-25.0D18-F |

**NOTES:**



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