2300 MHz to 2900 MHz Balanced Mixer, LO Buffer and RF Balun

Data Sheet **ADL5363**

FEATURES

RF frequency range of 2300 MHz to 2900 MHz
IF frequency range of dc to 450 MHz
Power conversion loss: 7.7 dB
SSB noise figure of 7.6 dB
Input IP3 of 31 dBm
Typical LO drive of 0 dBm
Single-ended, 50 Ω RF and LO input ports
High isolation SPDT LO input switch
Single-supply operation: 3.3 V to 5 V
Exposed pad, 5 mm × 5 mm 20-lead LFCSP
1500 V HBM/1250 V FICDM ESD performance

APPLICATIONS

Cellular base station receivers
Transmit observation receivers
Radio link downconverters

GENERAL DESCRIPTION

The ADL5363 uses a highly linear, doubly balanced passive mixer core along with integrated RF and local oscillator (LO) balancing circuitry to allow for single-ended operation. The ADL5363 incorporates an RF balun to provide optimal performance over a 2300 MHz to 2900 MHz input frequency range. The balanced passive mixer arrangement provides good LO-to-RF leakage, typically better than −30 dBm, and excellent intermodulation performance. The balanced mixer core also provides extremely high input linearity, allowing the device to be used in demanding cellular applications where in-band blocking signals might otherwise result in the degradation of dynamic performance.

FUNCTIONAL BLOCK DIAGRAM

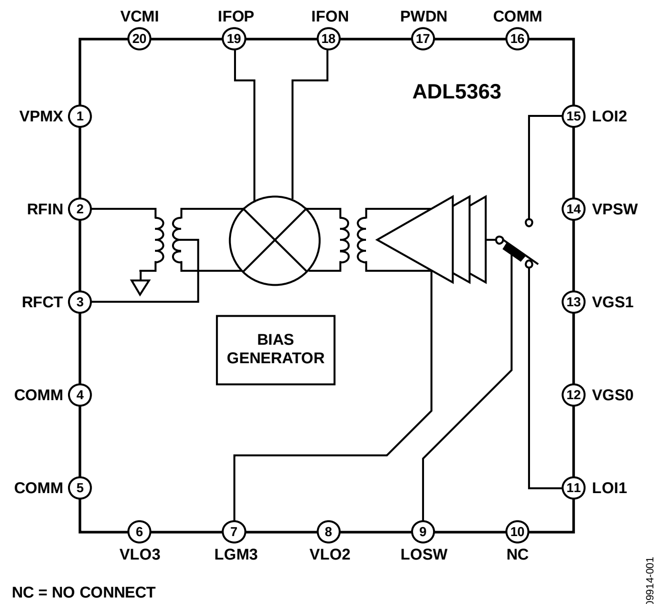

Figure 1.

The ADL5363 provides two switched LO paths that can be used in TDD applications where it is desirable to rapidly switch between two local oscillators. LO current can be externally set using a resistor to minimize dc current commensurate with the desired level of performance. For low voltage applications, the ADL5363 is capable of operation at voltages down to 3.3 V with substantially reduced current. For low voltage operation, an additional logic pin is provided to power down (<200 µA) the circuit when desired.

The ADL5363 is fabricated using a BiCMOS high performance IC process. The device is available in a 5 mm × 5 mm, 20-lead LFCSP and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Table 1. Passive Mixers

RF Frequency (MHz)	Single Mixer	Single Mixer and IF Amp	Dual Mixer and IF Amp
500 to 1700	ADL5367	ADL5357	ADL5358
1200 to 2500	ADL5365	ADL5355	ADL5356
2300 to 2900	ADL5363	ADL5353	ADL5354

Rev. A **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

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7/10—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, Z_O = 50 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		16		dB
Input Impedance			50		Ω
RF Frequency Range		2300		2900	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		33||-0.3		Ω||pF
IF Frequency Range		dc		450	MHz
DC Bias Voltage[1]	Externally generated	3.3	5.0	5.5	V
LO INTERFACE					
LO Power		−6	0	+10	dBm
Return Loss			15		dB
Input Impedance			50		Ω
LO Frequency Range		2330		3350	MHz
POWER-DOWN (PWDN) INTERFACE[2]					
PWDN Threshold			1.0		V
Logic 0 Level				0.4	V
Logic 1 Level		1.4			V
PWDN Response Time	Device enabled, IF output to 90% of its final level		160		ns
	Device disabled, supply current <5 mA		220		ns
PWDN Input Bias Current	Device enabled		0.0		µA
	Device disabled		70		µA

[1] Apply the supply voltage from the external circuit through the choke inductors.
[2] The PWDN function is intended for use with V_S ≤ 3.6 V only.

5 V PERFORMANCE

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and PCB loss		7.7		dB
SSB Noise Figure			7.6		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 2534.5 MHz, f_{RF2} = 2535.5 MHz, f_{LO} = 2738 MHz, each RF tone at 0 dBm		31		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 2535 MHz, f_{RF2} = 2585 MHz, f_{LO} = 2738 MHz, each RF tone at 0 dBm		62		dBm
Input 1 dB Compression Point (IP1dB)[1]	Exceeding 20 dBm RF power results in damage to the device		25		dBm
LO-to-IF Leakage	Unfiltered IF output		−22		dBm
LO-to-RF Leakage			−32		dBm
RF-to-IF Isolation			−44		dBc
IF/2 Spurious	−10 dBm input power		−61		dBc
IF/3 Spurious	−10 dBm input power		−70		dBc
POWER SUPPLY					
Positive Supply Voltage		4.5	5	5.5	V
Quiescent Current	V_S = 5 V		100		mA

[1] Exceeding 20 dBm RF power results in damage to the device.

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 60 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and PCB loss		7.4		dB
SSB Noise Figure			6.8		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 2534.5 MHz, f_{RF2} = 2535.5 MHz, f_{LO} = 2738 MHz, each RF tone at 0 dBm		26		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 2535 MHz, f_{RF2} = 2585 MHz, f_{LO} = 2738 MHz, each RF tone at 0 dBm		56		dBm
POWER SUPPLY					
Positive Supply Voltage			3.3		V
Quiescent Current	V_S = 5 V		60		mA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	20 dBm
LO Input Level	13 dBm
IFOP, IFON Bias Voltage	6.0 V
VGS0, VGS1, LOSW, PWDN	5.5 V
Internal Power Dissipation	0.5 W
Thermal Resistance, θ_{JA}	25°C/W
Temperature	
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

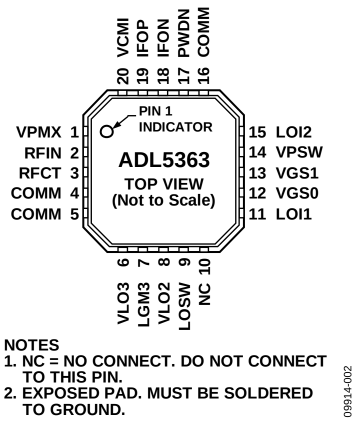

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPMX	Positive Supply Voltage.
2	RFIN	RF Input. Must be ac-coupled.
3	RFCT	RF Balun Center Tap (AC Ground).
4, 5,16	COMM	Device Common (DC Ground).
6, 8	VLO3, VLO2	Positive Supply Voltages for LO Amplifier.
7	LGM3	LO Amplifier Bias Control.
9	LOSW	LO Switch. LOI1 selected for 0 V, and LOI2 selected for 3 V.
10	NC	No Connect.
11, 15	LOI1, LOI2	LO Inputs. Must be ac-coupled.
12, 13	VGS0, VGS1	Mixer Gate Bias Controls. 3 V logic. Ground these pins for nominal setting.
14	VPSW	Positive Supply Voltage for LO Switch.
17	PWDN	Power Down. Connect this pin to ground for normal operation and connect this pin to 3.0 V for disable mode.
18, 19	IFON, IFOP	Differential IF Outputs.
20	VCMI	No Connect. This pin can be grounded.
	EPAD (EP)	Exposed pad. Must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V PERFORMANCE

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

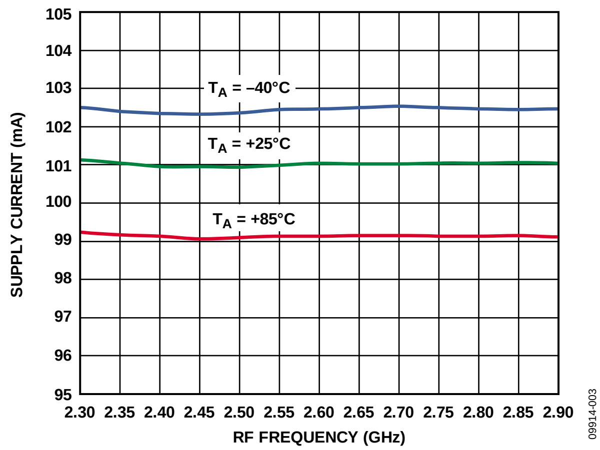

Figure 3. Supply Current vs. RF Frequency

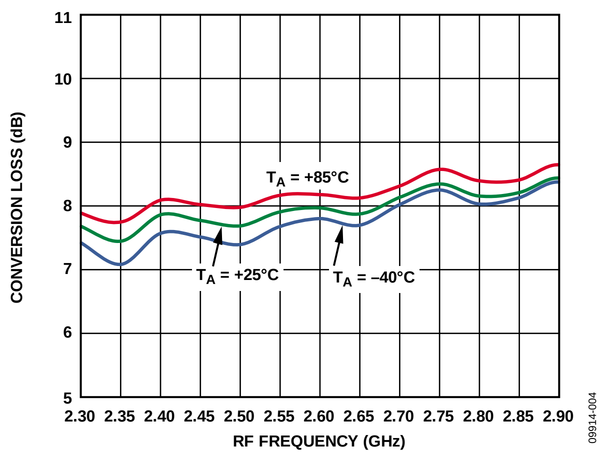

Figure 4. Power Conversion Loss vs. RF Frequency

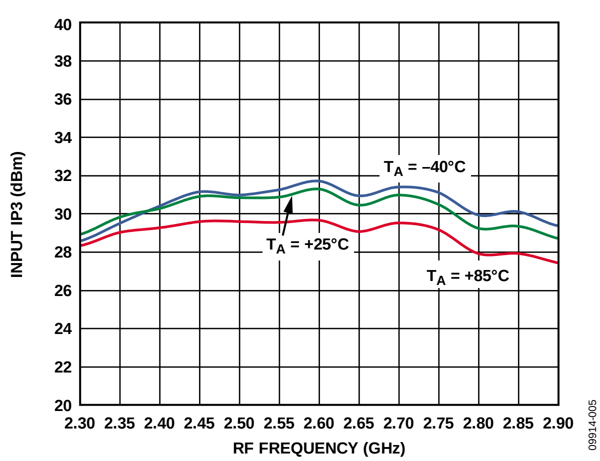

Figure 5. Input IP3 vs. RF Frequency

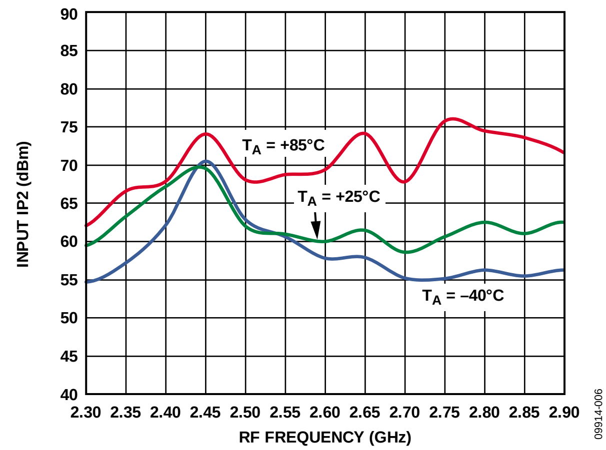

Figure 6. Input IP2 vs. RF Frequency

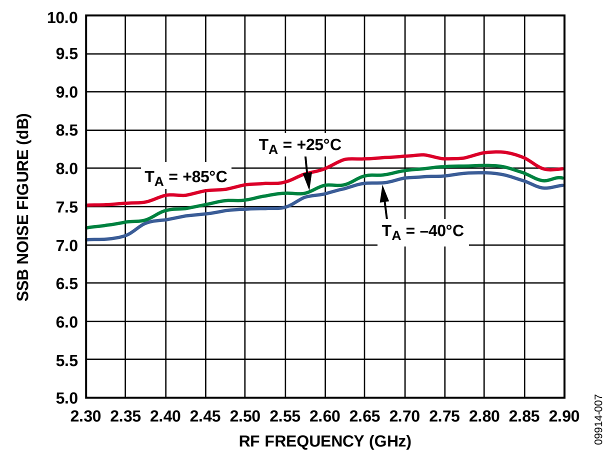

Figure 7. SSB Noise Figure vs. RF Frequency

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

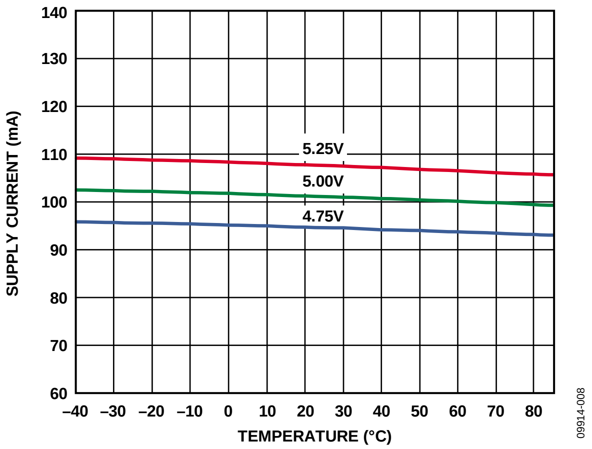

Figure 8. Supply Current vs. Temperature

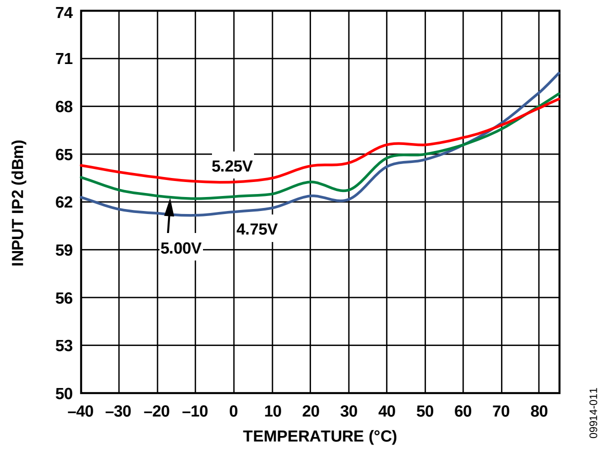

Figure 11. Input IP2 vs. Temperature

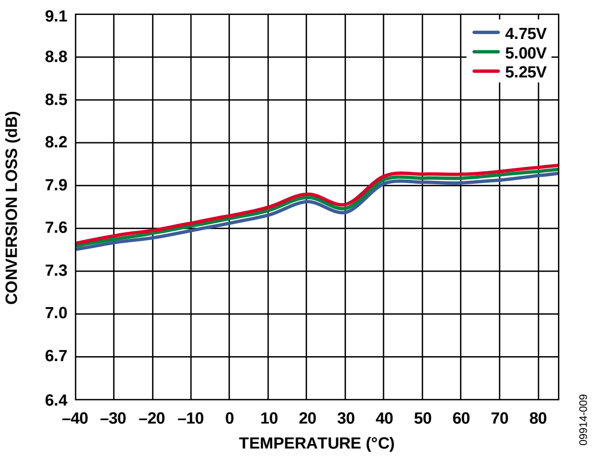

Figure 9. Power Conversion Loss vs. Temperature

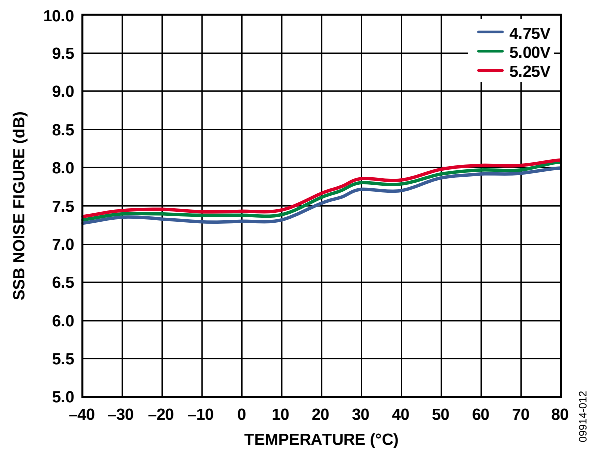

Figure 12. SSB Noise Figure vs. Temperature

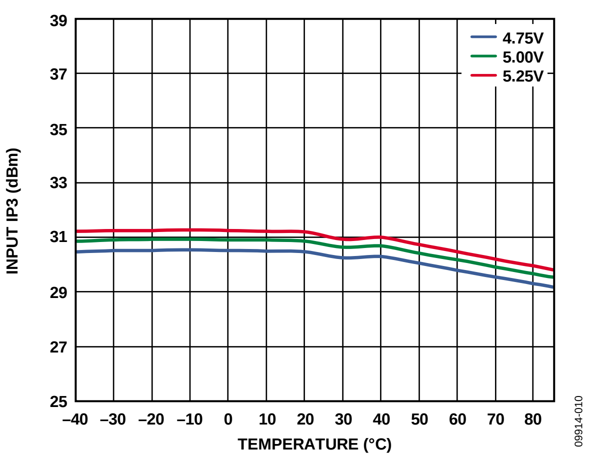

Figure 10. Input IP3 vs. Temperature

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

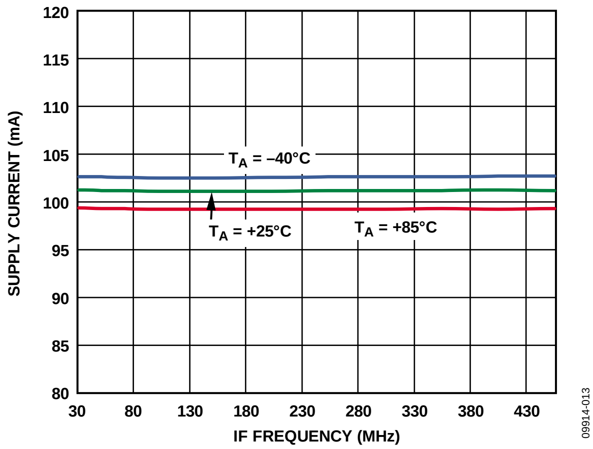

Figure 13. Supply Current vs. IF Frequency

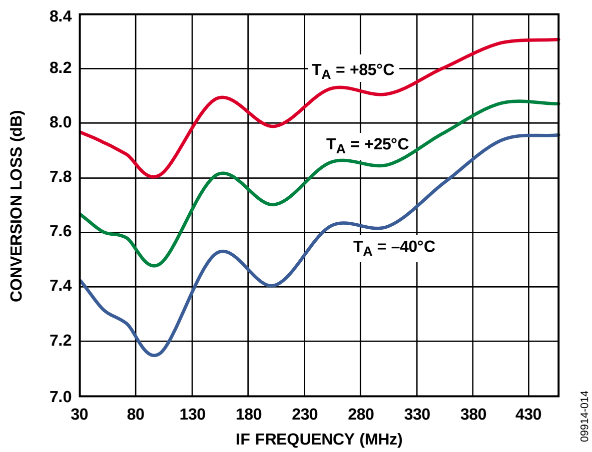

Figure 14. Power Conversion Loss vs. IF Frequency

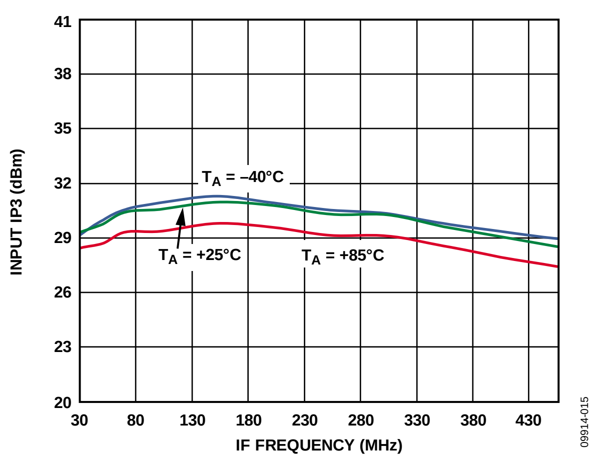

Figure 15. Input IP3 vs. IF Frequency

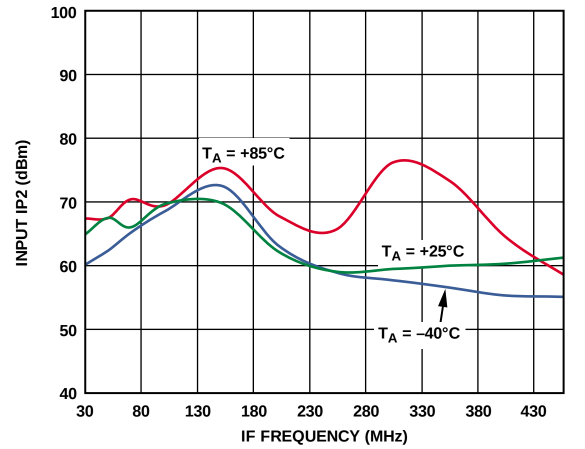

Figure 16. Input IP2 vs. IF Frequency

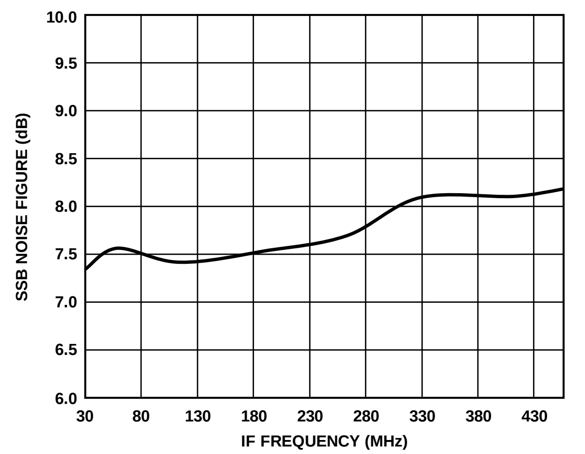

Figure 17. SSB Noise Figure vs. IF Frequency

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

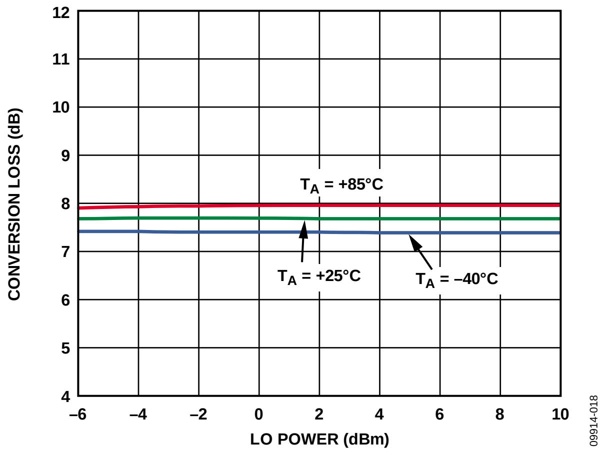

Figure 18. Power Conversion Loss vs. LO Power

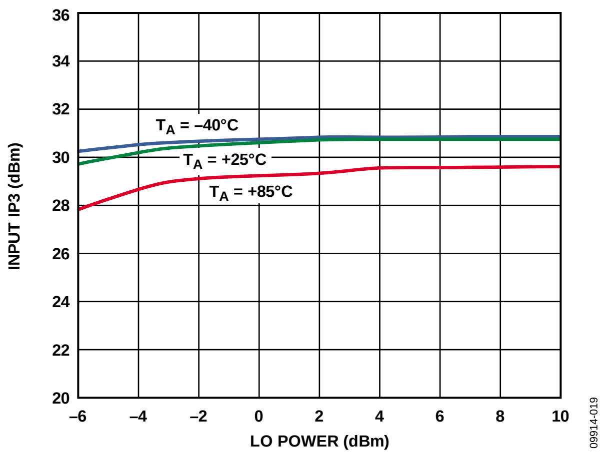

Figure 19. Input IP3 vs. LO Power

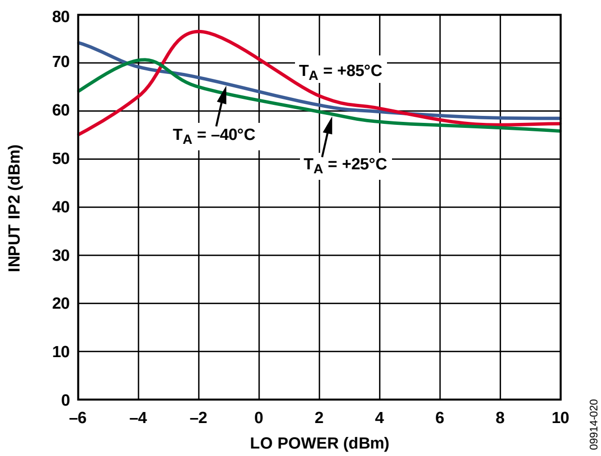

Figure 20. Input IP2 vs. LO Power

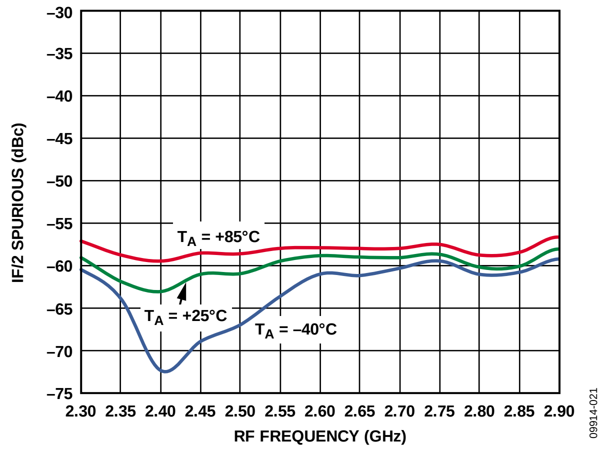

Figure 21. IF/2 Spurious vs. RF Frequency

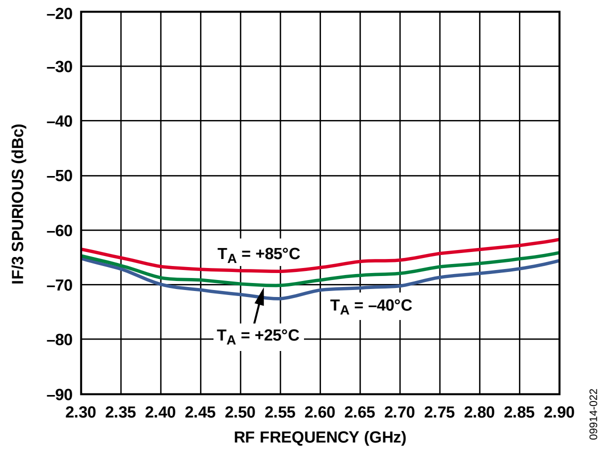

Figure 22. IF/3 Spurious vs. RF Frequency

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

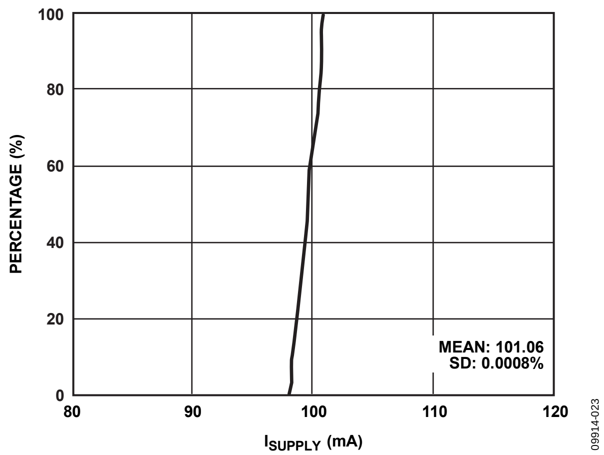

Figure 23. Supply Current Distribution

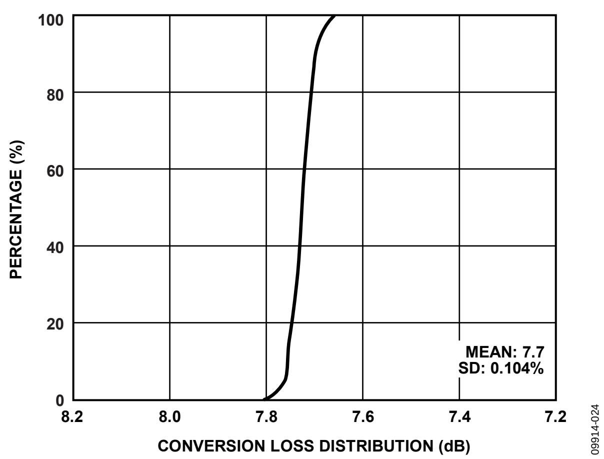

Figure 24.Conversion Loss Distribution

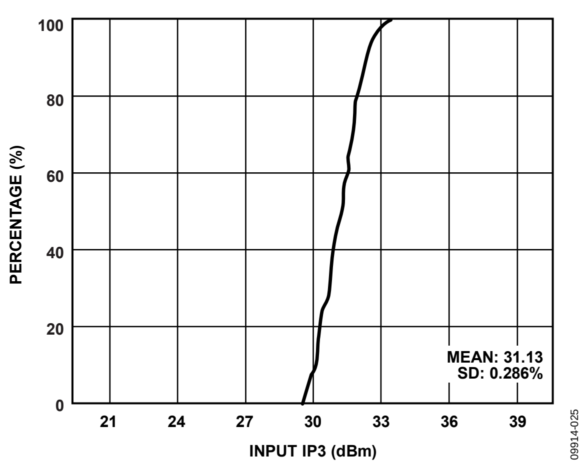

Figure 25. Input IP3 Distribution

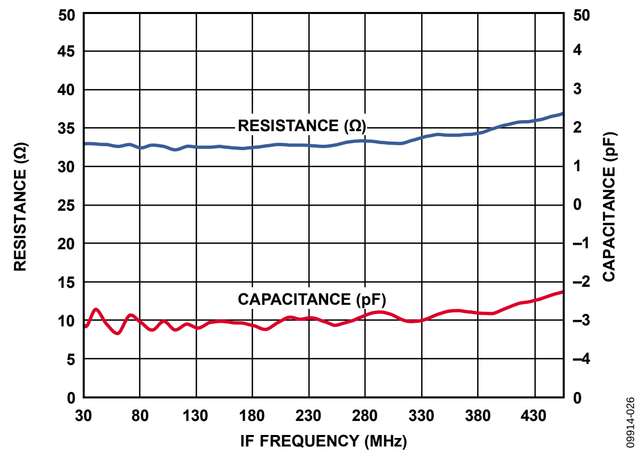

Figure 26. IF Output Impedance (R Parallel, C Equivalent)

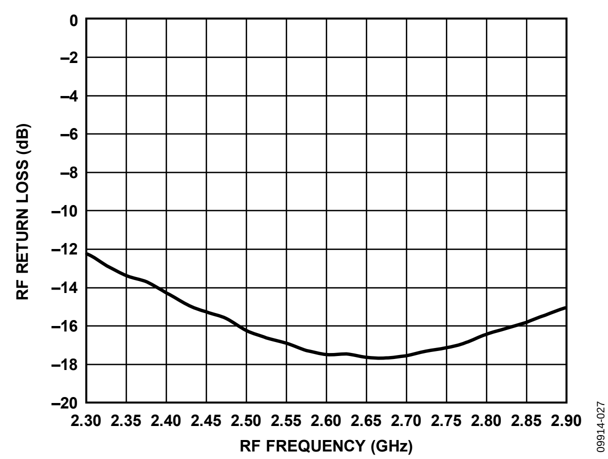

Figure 27. RF Port Return Loss, Fixed IF

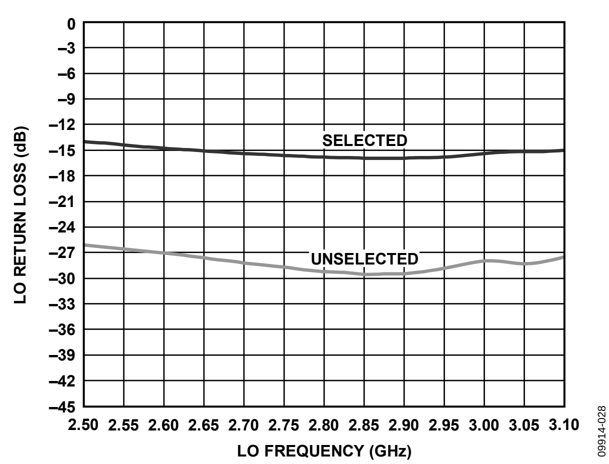

Figure 28. LO Return Loss, Selected and Unselected

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

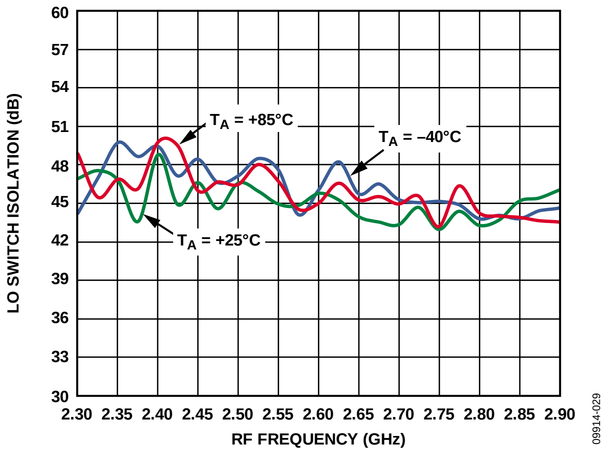

Figure 29. LO Switch Isolation vs. RF Frequency

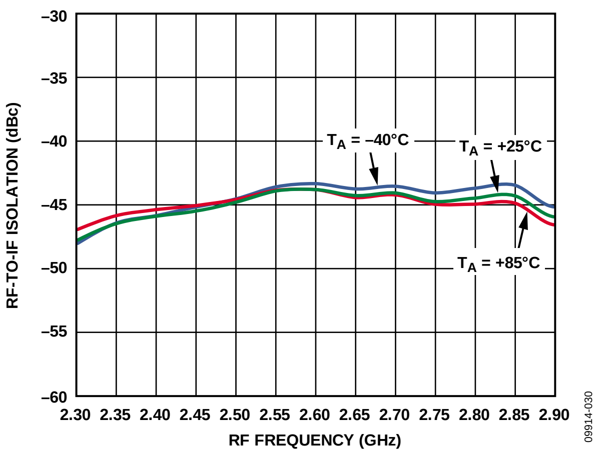

Figure 30. RF-to-IF Isolation vs. RF Frequency

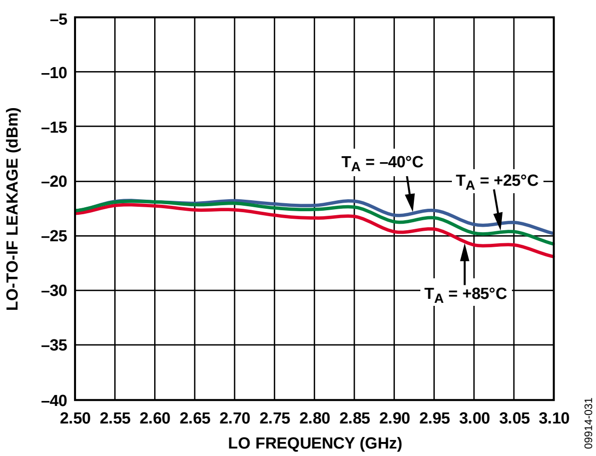

Figure 31. LO-to-IF Leakage vs. LO Frequency

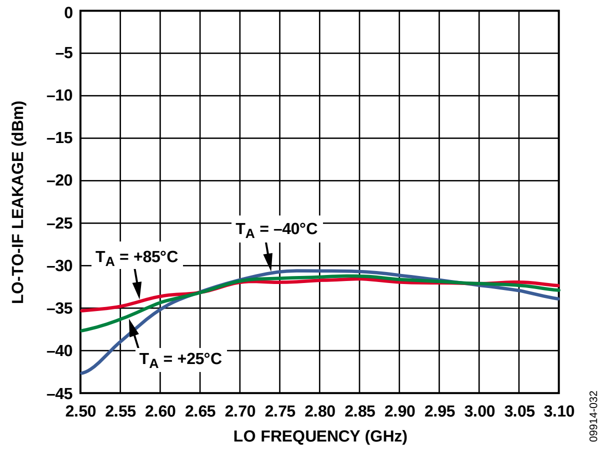

Figure 32. LO-to-RF Leakage vs. LO Frequency

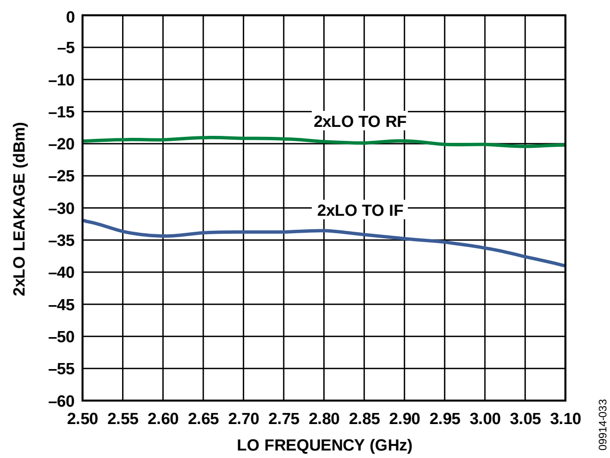

Figure 33. 2LO Leakage vs. LO Frequency

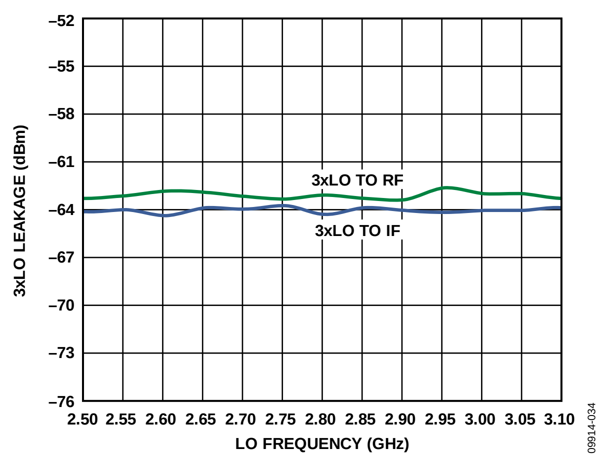

Figure 34. 3LO Leakage vs. LO Frequency

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

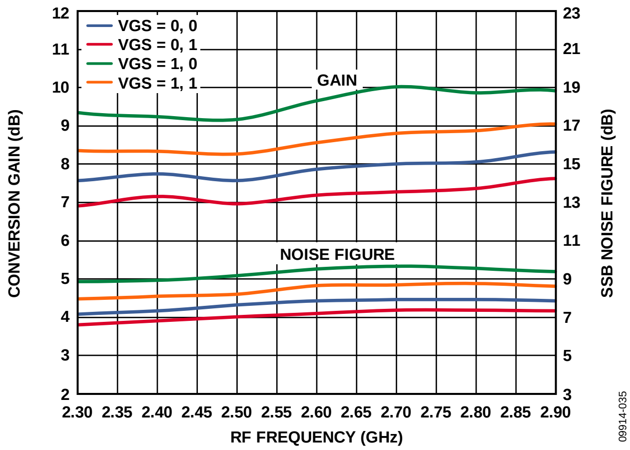

Figure 35. Power Conversion Loss and SSB Noise Figure vs. RF Frequency

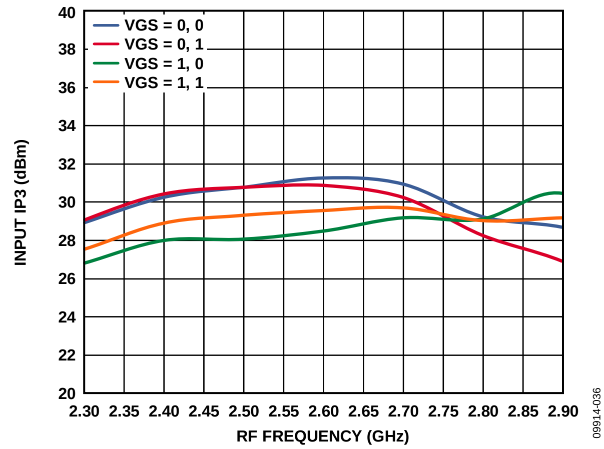

Figure 36. Input IP3 vs. RF Frequency

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 60 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

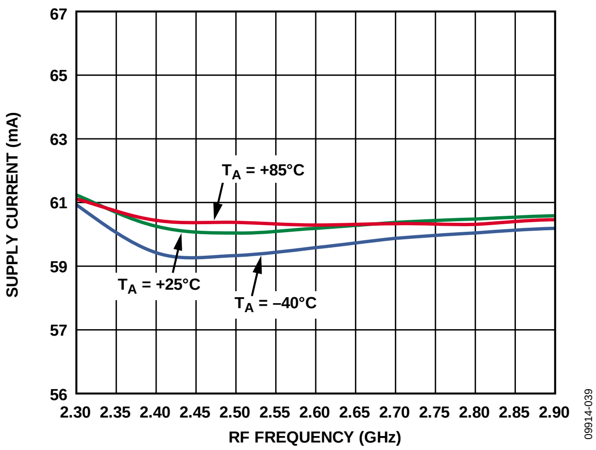

Figure 37. Supply Current vs. RF Frequency at 3.3 V

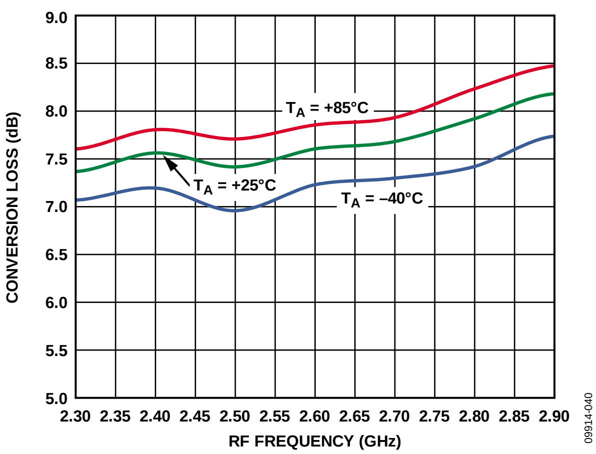

Figure 38. Power Conversion Loss vs. RF Frequency at 3.3 V

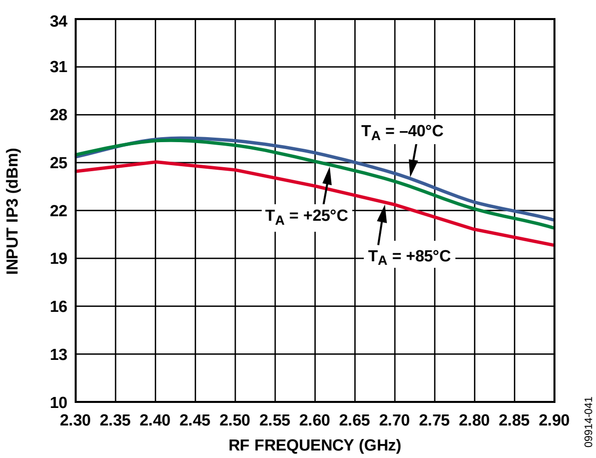

Figure 39. Input IP3 vs. RF Frequency at 3.3 V

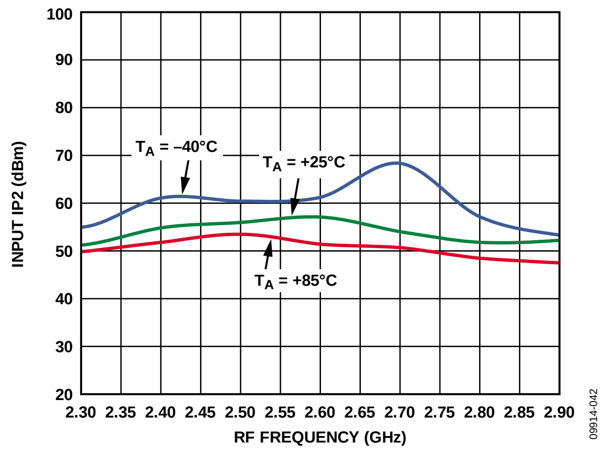

Figure 40. Input IP2 vs. RF Frequency at 3.3 V

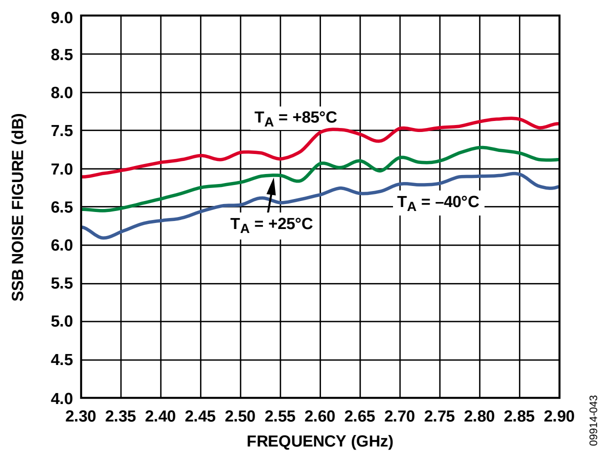

Figure 41. SSB Noise Figure vs. RF Frequency at 3.3 V

UPCONVERSION

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

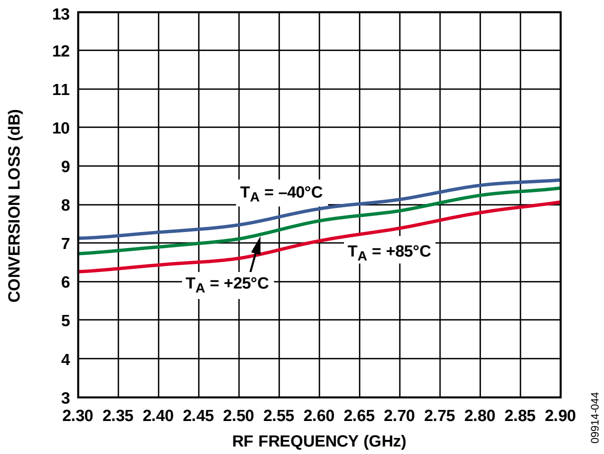

Figure 42. Power Conversion Loss vs. RF Frequency, V_S = 5 V, Upconversion

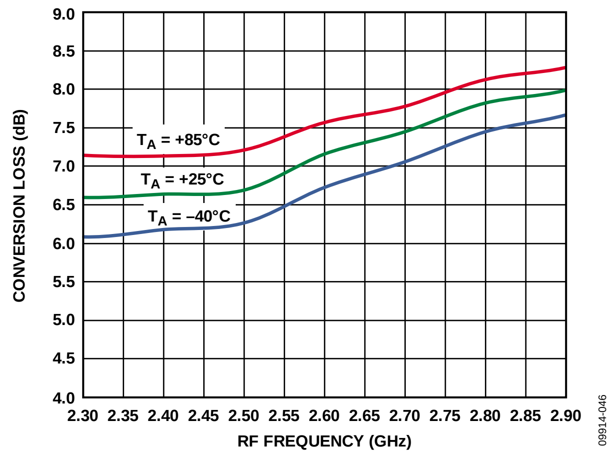

Figure 44. Power Conversion Loss vs. RF Frequency at 3.3 V, Upconversion

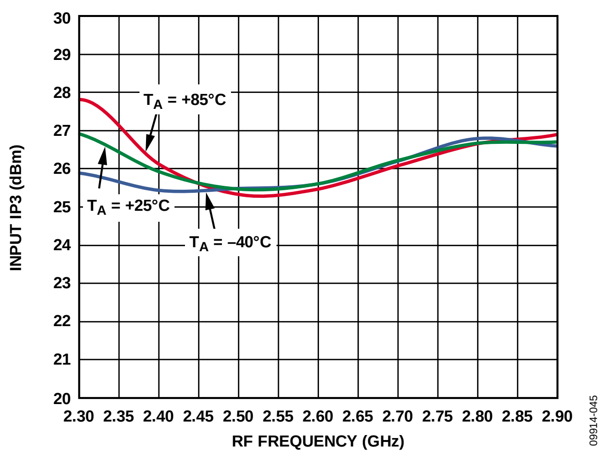

Figure 43. Input IP3 vs. RF Frequency, V_S = 5 V, Upconversion

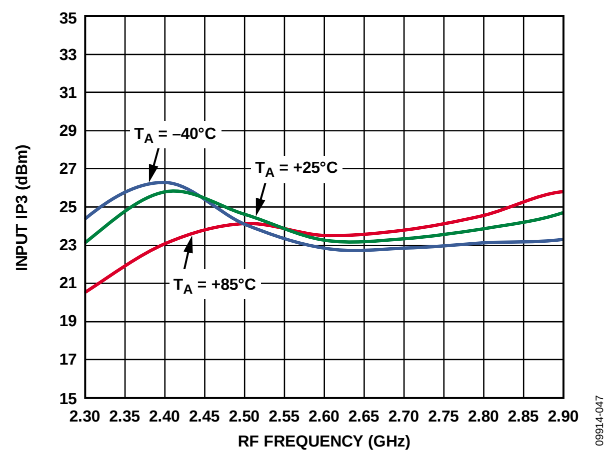

Figure 45. Input IP3 vs. RF Frequency at 3.3 V, Upconversion

SPURIOUS PERFORMANCE

($N \times f_{RF}$) − ($M \times f_{LO}$) spur measurements were made using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = −100 dBm.

5 V Performance

V_S = 5 V, I_S = 100 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−10.9	−28.3	−44.5												
	1	−42.2	0.0	−49.3	−31.2	−49.8											
	2	−75.8	−76.5	−64.6	−78.4	−78.5	−94.7										
	3	<−100	−83.0	<−100	−73.5	−90.9	−89.8	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

3.3 V Performance

V_S = 3.3 V, I_S = 56 mA, T_A = 25°C, f_{RF} = 2535 MHz, f_{LO} = 2738 MHz, LO power = 0 dBm, RF power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−16.9	−35.1	−61.4												
	1	−41.9	0.0	−49.1	−30.4	−52.6											
	2	−72.3	−80.3	−62.7	−68.5	−71.9	<−100										
	3	−94.6	−71.6	<−100	−61.2	−92.7	−75.1	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15																<−100

CIRCUIT DESCRIPTION

The ADL5363 consists of two primary components: the radio frequency (RF) subsystem and the local oscillator (LO) subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

The RF subsystem consists of an integrated, low loss RF balun, passive MOSFET mixer, sum termination network.

The LO subsystem consists of an SPDT-terminated FET switch and a three-stage limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input.

A block diagram of the device is shown in Figure 46.

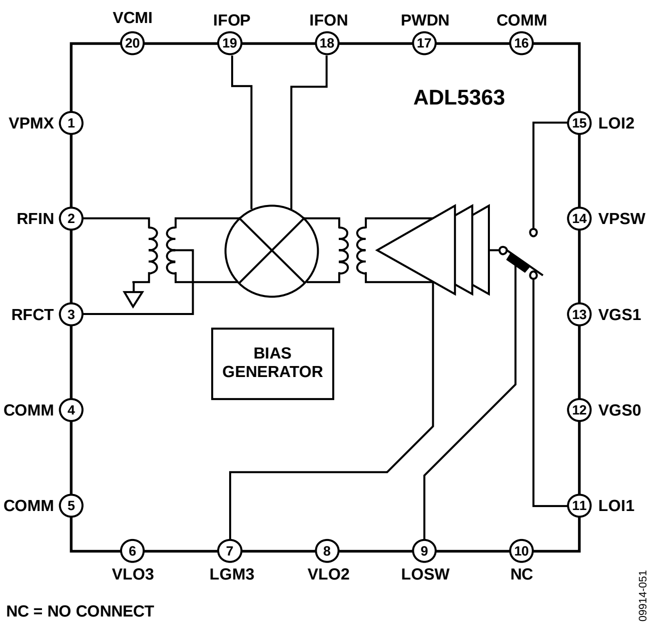

Figure 46. Simplified Schematic

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a low loss (<1 dB) unbalanced-to-balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended that a blocking capacitor be used to avoid running excessive dc current through the part. The RF balun can easily support an RF input frequency range of 2300 MHz to 2900 MHz.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

As the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all the idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the IF output. This termination is accomplished by the addition of a sum network between the IF output and the mixer.

The IP3 performance can be optimized by adjusting the supply current with an external resistor. Figure 37 and 38 illustrate how the bias resistor affects the performance with a 5 V supply. Additionally, dc current can be saved by increasing either or both resistors. It is permissible to reduce the dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the part. (Note that no performance enhancement is obtained by reducing the value of these resistors and excessive dc power dissipation may result.)

LO SUBSYSTEM

The ADL5363 has two LO inputs permitting multiple synthesizers to be rapidly switched with extremely short switching times (<40 ns) for frequency agile applications. The two inputs are applied to a high isolation SPDT switch that provides a constant input impedance, regardless of whether the port is selected, to avoid pulling the LO sources. This multiple section switch also ensures high isolation to the off input, minimizing any leakage from the unwanted LO input that may result in undesired IF responses.

The single-ended LO input is converted to a fixed amplitude differential signal using a multistage, limiting LO amplifier. This results in consistent performance over a range of LO input power. Optimum performance is achieved from −6 dBm to +10 dBm, but the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. The bandwidth of the intermodulation performance is somewhat influenced by the current in the LO amplifier chain. For dc current sensitive applications, it is permissible to reduce the current in the LO amplifier by raising the value of the external bias control resistor. For dc current critical applications, the LO chain can operate with a supply voltage as low as 3.3 V, resulting in substantial dc power savings.

In addition, when operating with supply voltages below 3.6 V, the ADL5363 has a power-down mode that permits the dc current to drop to <200 µA.

All of the logic inputs are designed to work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V. All logic inputs are high impedance up to Logic 1 levels of 3.3 V. At levels exceeding 3.3 V, protection circuitry permits operation up to 5.5 V, although a small bias current is drawn.

All pins, including the RF pins, are ESD protected and have been tested up to a level of 1500 V HBM and 1250 V CDM.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5363 mixer is designed to downconvert radio frequencies (RF) primarily between 2300 MHz and 2900 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz. Figure 47 depicts the basic connections of the mixer. To prevent nonzero dc voltages from damaging the RF balun or LO input circuit, ac-couple the RF and LO input ports. The RFIN matching network consists of a series 1.5 pF capacitor and a shunt 12 nH inductor to provide the optimized RF input return loss for the desired frequency band.

IF PORT

The real part of the output impedance is approximately 50 Ω, as seen in Figure 26, which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion loss that is approximately the same as the power conversion loss, as shown in Table 3.

MIXER VGS CONTROL DAC

The ADL5363 features two logic control pins, VGS0 (Pin 12) and VGS1 (Pin 13), that allow programmability for internal gate-to-source voltages for optimizing mixer performance over desired frequency bands. The evaluation board defaults both VGS0 and VGS1 to ground.

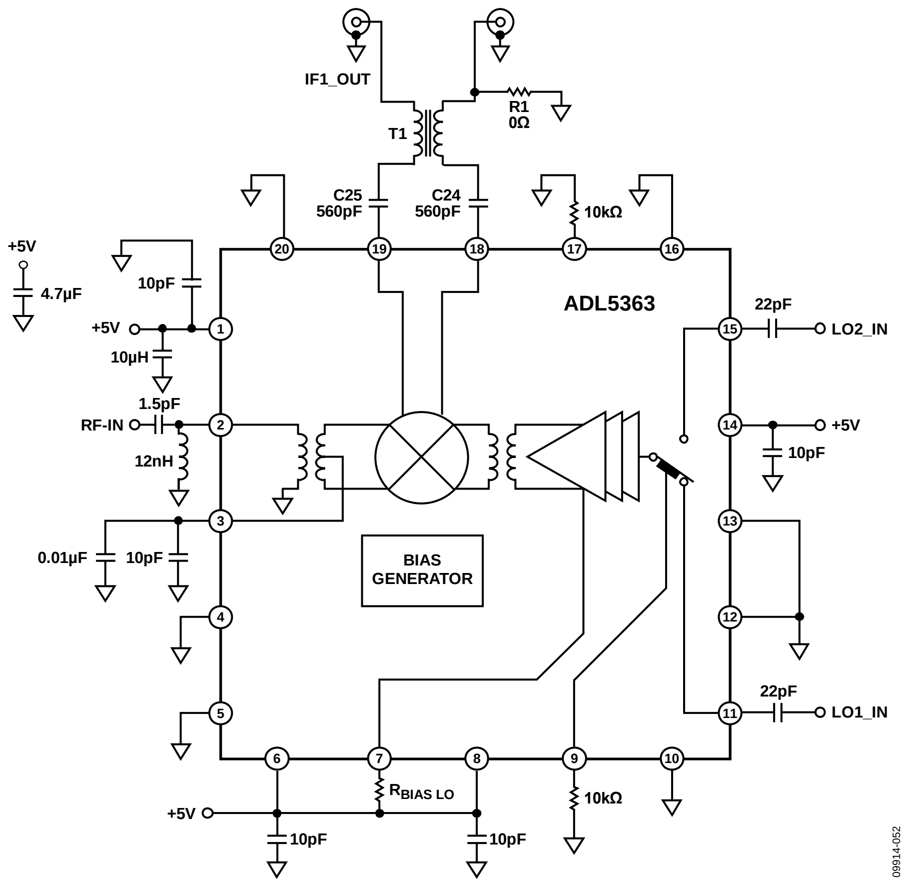

Figure 47. Typical Application Circuit

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers. The standard evaluation board schematic is shown in Figure 48. The evaluation board is fabricated using Rogers® RO3003 material. Table 7 describes the various configuration options of the evaluation board. Evaluation board layout is shown in Figure 49 to Figure 52.

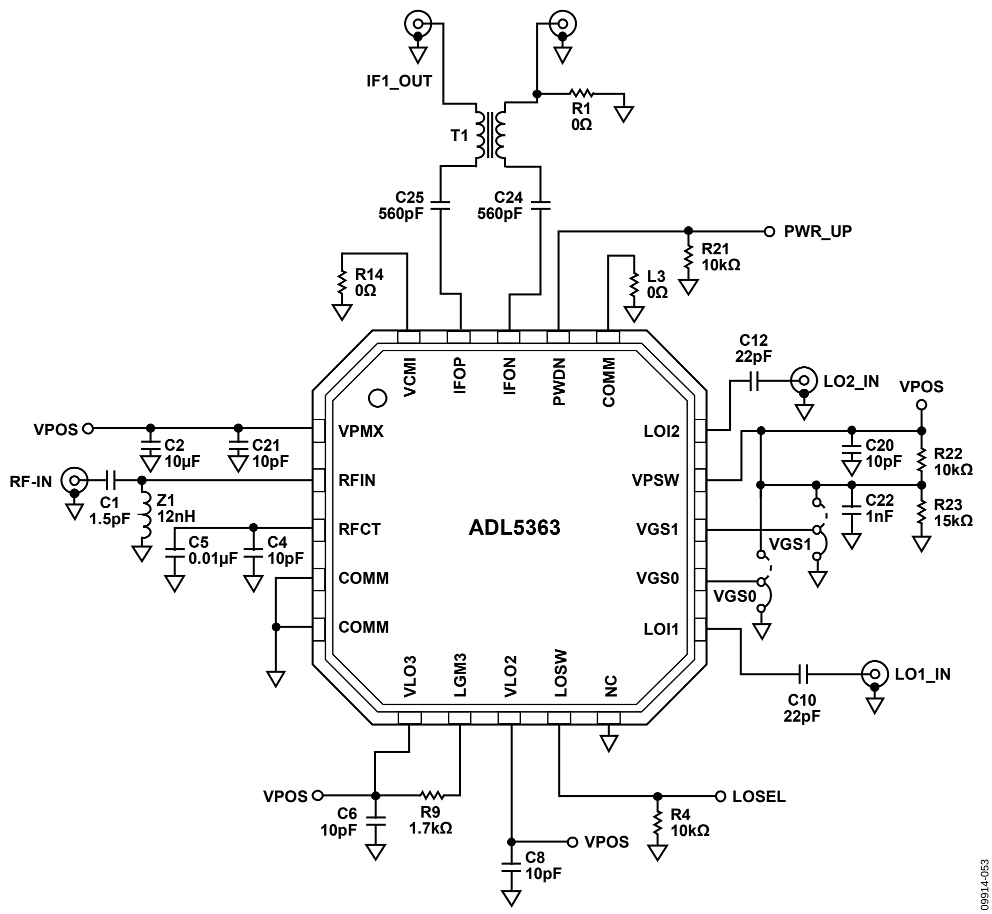

Figure 48. Evaluation Board Schematic

Table 7. Evaluation Board Configuration

Components	Function	Description	Default Conditions
C2, C6, C8, C20, C21	Power supply decoupling	Power Supply Decoupling. Nominal supply decoupling consists of a 10 μF capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C2 = 10 μF (size 0603), C6, C8, C20, C21 = 10 pF (size 0402)
C1, C4, C5, Z1	RF input interface	RF Input Interface. The input channels are ac-coupled through C1. C4 and C5 provide bypassing for the center taps of the RF input baluns.	C1 = 1.5 pF (size 0402), C4 = 10 pF (size 0402), C5 = 0.01 μF (size 0402) Z1= 12 nH (size 0402)
T1, R1, C24, C25	IF output interface	IF Output Interface. T1 is a 1:1 impedance transformer used to provide a single-ended IF output interface. Remove R1 for balanced output operation. C24 and C25 are used to block the dc bias at the IF ports.	T1 = TC1-1-13M+ (Mini-Circuits), R1 = 0 Ω (size 0402), C24, C25 = 560 pF (size 0402)
C10, C12, R4	LO interface	LO Interface. C10 and C12 provide ac coupling for the LO1_IN and LO2_IN local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R4 provides a pull-down to ensure that LO1_IN is enabled when the LOSEL test point is logic low. LO2_IN is enabled when LOSEL is pulled to logic high.	C10, C12 = 22 pF (size 0402), R4 = 10 kΩ (size 0402)
R21	PWDN interface	PWDN Interface. R21 pulls the PWDN logic low and enables the device. The PWR_UP test point allows the PWDN interface to be exercised using the an external logic generator. Grounding the PWDN pin for nominal operation is allowed. Using the PWDN pin when supply voltages exceed 3.3 V is not allowed.	R21 = 10 kΩ (size 0402)
C22, L3, R9, R14, R22, R23, VGS0, VGS1	Bias control	Bias Control. R22 and R23 form a voltage divider to provide 3 V for logic control, bypassed to ground through C22. VGS0 and VGS1 jumpers provide programmability at the VGS0 and VGS1 pins. It is recommended to pull these two pins to ground for nominal operation. R9 sets the bias point for the internal LO buffers.	C22 = 1 nF (size 0402), L3 = 0 Ω (size 0603), R9 = 1.7 kΩ (size 0402), R14 = 0 Ω (size 0402), R22 = 10 kΩ (size 0402), R23 = 15 kΩ (size 0402), VGS0 = VGS1 = 3-pin shunt

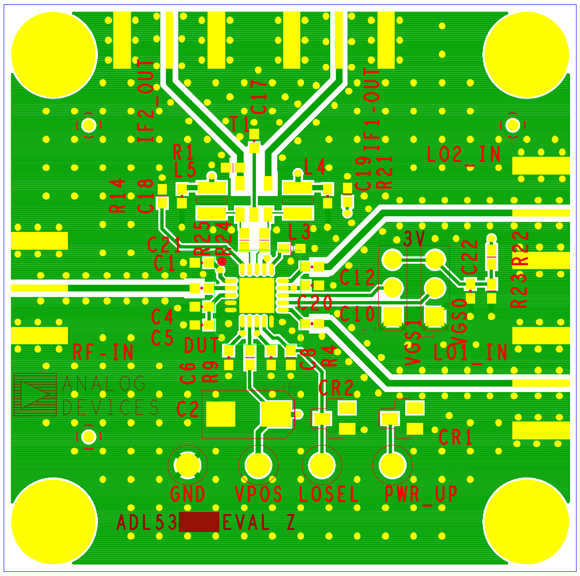

Figure 49. Evaluation Board Top Layer

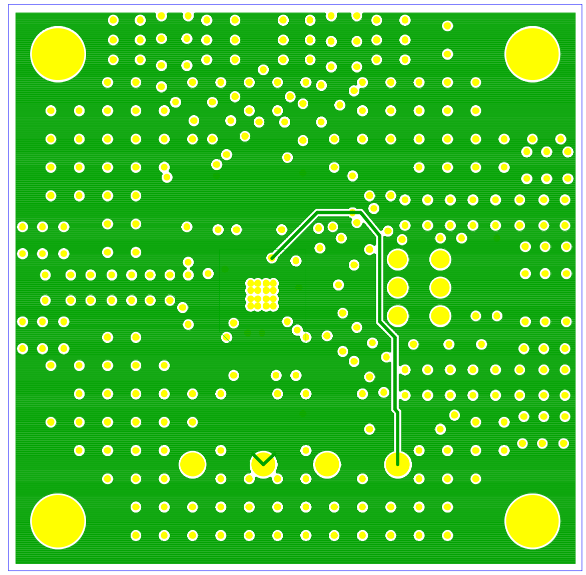

Figure 51. Evaluation Board Power Plane, Internal Layer 2

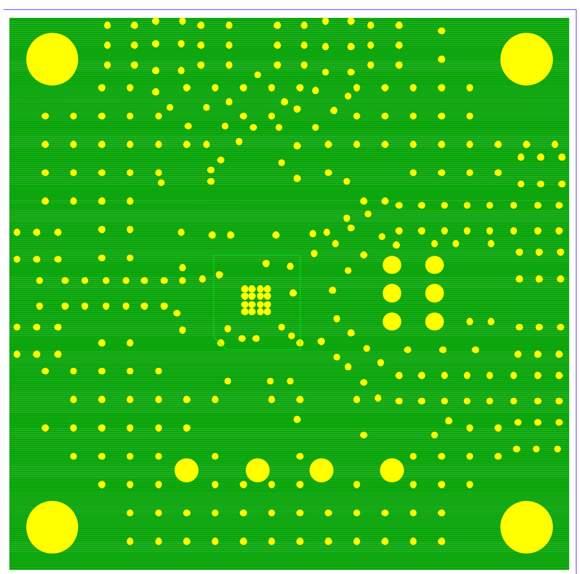

Figure 50. Evaluation Board Ground Plane, Internal Layer 1

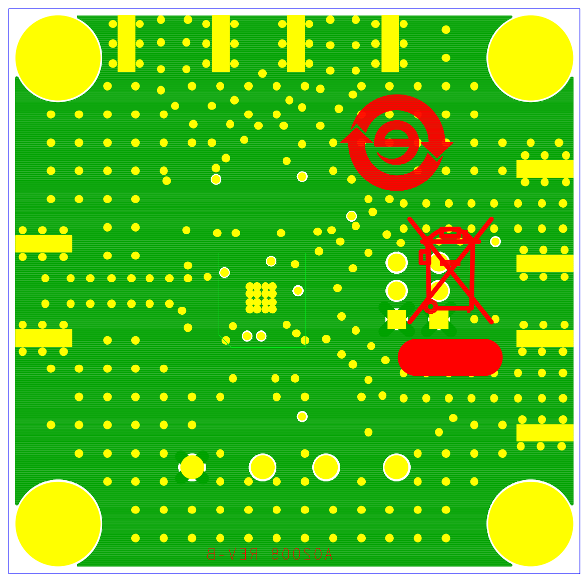

Figure 52. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

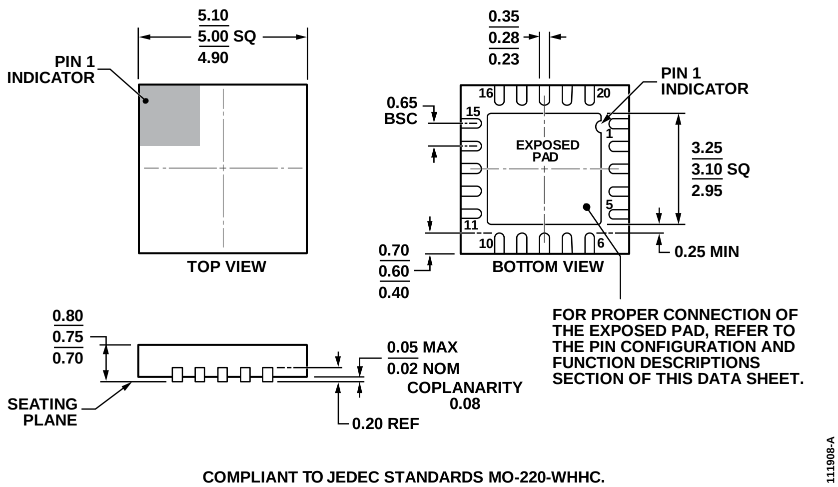

Figure 53. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-20-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5363ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 7" Tape and Reel	CP-20-9	1,500
ADL5363-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.

NOTES

D09914-0-2/15(A)

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