

# High Speed, Low Cost, Triple Op Amp

# ADA4861-3

#### FEATURES

High speed 730 MHz, -3 dB bandwidth 625 V/μs slew rate 13 ns settling time to 0.5% Wide supply range: 5 V to 12 V Low power: 6 mA/amplifier 0.1 dB flatness: 100 MHz Differential gain: 0.01% Differential phase: 0.02° Low voltage offset: 100 μV (typical) High output current: 25 mA Power down

#### **APPLICATIONS**

Consumer video Professional video Broadband video ADC buffers Active filters

#### **GENERAL DESCRIPTION**

The ADA4861-3 is a low cost, high speed, current feedback, triple op amp that provides excellent overall performance. The 730 MHz, -3 dB bandwidth, and 625 V/µs slew rate make this amplifier well suited for many high speed applications. With its combination of low price, excellent differential gain (0.01%), differential phase (0.02°), and 0.1 dB flatness out to 100 MHz, this amplifier is ideal for both consumer and professional video applications.

The ADA4861-3 is designed to operate on supply voltages as low as +5 V and up to  $\pm$ 5 V using only 6 mA/amplifier of supply current. To further reduce power consumption, each amplifier is equipped with a power-down feature that lowers the supply current to 0.3 mA/amplifier when not being used.

The ADA4861-3 is available in a 14-lead SOIC\_N package and is designed to work over the extended temperature range of  $-40^{\circ}$ C to  $+105^{\circ}$ C.

#### **PIN CONFIGURATION**





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### **REVISION HISTORY**

3/06—Rev 0 to Rev. A	
Changes to 20 MHz Active Low-Pass Filter Section	. 13
Changes to Figure 48 and Figure 49	13

10/05—Revision 0: Initial Version

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### **SPECIFICATIONS**

 $V_S = +5 V$  (@  $T_A = 25^{\circ}C$ , G = +2,  $R_L = 150 \Omega$ ,  $C_L = 4 pF$ , unless otherwise noted); for G = +2,  $R_F = R_G = 301 \Omega$ ; and for G = +1,  $R_F = 499 \Omega$ .

Parameter	Conditions	Min	Тур	Max	Unit
DYNAMIC PERFORMANCE			-76		
-3 dB Bandwidth	$V_0 = 0.2 V p - p$		350		MHz
	$V_0 = 2 V p p$		145		MHz
	$G = +1 V_0 = 0.2 V \text{ p-p}$		560		MHz
Bandwidth for 0.1 dB Elatness	$V_0 = 2 V p - p$		85		MHz
+Slew Rate (Rising Edge)	$V_0 = 2V p p$		590		V/us
-Slew Rate (Falling Edge)	$V_0 = 2V p p$		480		V/µs
Settling Time to 0.5% (Rise/Fall)	$V_0 = 2V p p$		12/13		v/µs
	vo – 2 v step		12/13		115
Harmonic Distortion HD2/HD2	$f_{r} = 1 M H_{T} V_{r} = 2 V p p$		01/ 00		dPc
Harmonic Distortion HD2/HD3	$f_c = 1 \text{ MHz}, v_c = 2 \text{ V } p \text{ -} p$		-01/-09		
	$I_{C} = 5 I_{V} I_{H} Z, v_{O} = 2 v p - p$		-09/-70		
Input Voltage Noise			3.8 1 7/5 5		
	I = 100  kHz, +IN/-IN		1.//5.5		ра/унг
Differential Gain			0.02		%
Differential Phase			0.03		Degrees
All-Hostile Crosstalk	Amplifier 1 and Amplifier 2 driven,		-65		dВ
DC REDEODMANCE	Ampliner 5 output measured, I – T MHZ				
		12	0.0	. 10	m)/
Input Offset Voltage		-13	-0.9	+13	mv 
+Input Bias Current		-2	-0.8	+1	μΑ
		-8	+2.3	+13	μΑ
		400	620		KL2
INPUT CHARACTERISTICS					
Input Resistance	+IN		14		MΩ
	-IN		85		Ω
Input Capacitance	+IN		1.5		р⊦
Input Common-Mode Voltage Range	G = +1		1.2 to 3.8		V
Common-Mode Rejection Ratio	$V_{CM} = 2 V \text{ to } 3 V$	-54	-56.5		dB
POWER-DOWN PINS					
Input Voltage	Enabled		0.6		V
	Power down		1.8		V
Bias Current	Enabled		-3		μΑ
	Power down		115		μΑ
Turn-On Time			200		ns
Turn-Off Time			3.5		μs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	$V_{IN} = +2.25 \text{ V to } -0.25 \text{ V}$		55/100		ns
Output Voltage Swing	$R_L = 150 \Omega$	1.2 to 3.8	1.1 to 3.9		V
	$R_L = 1 \ k\Omega$	0.9 to 4.1	0.85 to 4.15		V
Short-Circuit Current	Sinking and sourcing		65		mA
POWER SUPPLY					
Operating Range		5		12	V
Total Quiescent Current	Enabled	12.5	16.1	18.5	mA
Quiescent Current/Amplifier	POWER DOWN pins = $+V_s$		0.2	0.33	mA
Power Supply Rejection Ratio					
+PSR	$+V_{s} = 4 V \text{ to } 6 V, -V_{s} = 0 V$	-60	-64		dB

 $V_{S} = \pm 5 V (@ T_{A} = 25^{\circ}C, G = +2, R_{L} = 150 \Omega, C_{L} = 4 pF, unless otherwise noted); for G = +2, R_{F} = R_{G} = 301 \Omega; and for G = +1, R_{F} = 499 \Omega.$ 

### Table 2.

Parameter	Conditions	Min	Тур	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_0 = 0.2 V p - p$		370		MHz
	$V_0 = 2 V p - p$		210		MHz
	$G = +1, V_0 = 0.2 V p-p$		730		MHz
Bandwidth for 0.1 dB Flatness	$V_0 = 2 V p - p$		100		MHz
+Slew Rate (Rising Edge)	$V_0 = 2 V p - p$		910		V/µs
–Slew Rate (Falling Edge)	$V_0 = 2 V p - p$		680		V/µs
Settling Time to 0.5% (Rise/Fall)	$V_0 = 2 V \text{ step}$		12/13		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion HD2/HD3	$f_{c} = 1 \text{ MHz}, V_{o} = 2 \text{ V p-p}$		-85/-99		dBc
Harmonic Distortion HD2/HD3	$f_{c} = 5 \text{ MHz}, V_{o} = 2 \text{ V p-p}$		-73/-86		dBc
Input Voltage Noise	f = 100 kHz		3.8		nV/√Hz
Input Current Noise	f = 100  kHz, +IN/-IN		1.7/5.5		pA/√Hz
Differential Gain			0.01		%
Differential Phase			0.02		Degrees
All-Hostile Crosstalk	Amplifier 1 and Amplifier 2 driven,		-65		dB
	Amplifier 3 output measured, $f = 1 MHz$				
DC PERFORMANCE					
Input Offset Voltage		-13	-0.1	+13	mV
+Input Bias Current		-2	-0.7	+1	μΑ
–Input Bias Current		-8	+2.9	+13	μA
Open-Loop Transresistance		500	720		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+IN		15		MΩ
	-IN		90		Ω
Input Capacitance	+IN		1.5		рF
Input Common-Mode Voltage Range	G = +1		-3.7 to +3.7		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2 V$	-55	-58		dB
POWER-DOWN PINS					
Input Voltage	Enabled		-4.4		V
	Power down		-3.2		V
Bias Current	Enabled		-3		μA
	Power down		250		μA
Turn-On Time			200		ns
Turn-Off Time			3.5		μs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	$V_{IN} = \pm 3.0 \text{ V}$		30/90		ns
Output Voltage Swing	$R_L = 150 \Omega$	±2	-3.1 to +3.65		V
	$R_L = 1 \ k\Omega$	±3.9	±4.05		V
Short-Circuit Current	Sinking and sourcing		100		mA
POWER SUPPLY					
Operating Range		5		12	V
Total Quiescent Current	Enabled	13.5	17.9	20.5	mA
Quiescent Current/Amplifier	POWER DOWN pins = +Vs		0.3	0.5	mA
Power Supply Rejection Ratio					
+PSR	$+V_{s} = 4 V \text{ to } 6 V, -V_{s} = -5 V$	-63	-66		dB
–PSR	$+V_s = 5 V$ , $-V_s = -4 V$ to $-6 V$ , POWER DOWN pins = $-V_s$	-59	-62		dB

### **ABSOLUTE MAXIMUM RATINGS**

Table 3.

1 4010 01	
Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_{s} + 1 V to + V_{s} - 1 V$
Differential Input Voltage	±Vs
Storage Temperature	–65°C to +125°C
Operating Temperature Range	-40°C to +105°C
Lead Temperature	JEDEC J-STD-20
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### THERMAL RESISTANCE

 $\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for device soldered in circuit board for surface-mount packages.

#### Table 4. Thermal Resistance

Package Type	θ <sub>JA</sub>	Unit
14-lead SOIC_N	90	°C/W

#### **Maximum Power Dissipation**

The maximum safe power dissipation for the ADA4861-3 is limited by the associated rise in junction temperature ( $T_I$ ) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality. The power dissipated in the package  $(P_D)$  is the sum of the quiescent power dissipation and the power dissipated in the die due to the amplifiers' drive at the output. The quiescent power is the voltage between the supply pins  $(V_s)$  times the quiescent current  $(I_s)$ .

 $P_D$  = Quiescent Power + (Total Drive Power – Load Power)

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages should be considered.

Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . In addition, more metal directly in contact with the package leads and through holes under the device reduces  $\theta_{JA}$ .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 14-lead SOIC\_N (90°C/W) on a JEDEC standard 4-layer board.  $\theta_{JA}$  values are approximations.



Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

#### **ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



### **TYPICAL PERFORMANCE CHARACTERISTICS**

 $R_L = 150 \Omega$  and  $C_L = 4 pF$ , unless otherwise noted.



Figure 4. Small Signal Frequency Response for Various Gains



Figure 5. Large Signal Frequency Response for Various Gains



Figure 6. Large Signal 0.1 dB Flatness



Figure 7. Small Signal Frequency Response for Various Gains



Figure 8. Large Signal Frequency Response for Various Gains



Figure 9. Large Signal Frequency Response for Various Output Levels



Figure 10. Small Signal Frequency Response vs. R<sub>F</sub>



Figure 11. Harmonic Distortion vs. Frequency



Figure 12. Harmonic Distortion vs. Frequency



Figure 13. Large Signal Frequency Response vs. R<sub>F</sub>



Figure 14. Harmonic Distortion vs. Frequency



Figure 15. Harmonic Distortion vs. Frequency



Figure 16. Small Signal Transient Response for Various Supplies



Figure 17. Small Signal Transient Response for Various Capacitor Loads



Figure 18. Small Signal Transient Response for Various Capacitor Loads



Figure 19. Small Signal Transient Response for Various Supplies



Figure 20. Small Signal Transient Response for Various Capacitor Loads



Figure 21. Small Signal Transient Response for Various Capacitor Loads



Figure 22. Large Signal Transient Response for Various Supplies



Figure 23. Large Signal Transient Response for Various Capacitor Loads



Figure 24. Large Signal Transient Response for Various Capacitor Loads



Figure 25. Large Signal Transient Response for Various Supplies



Figure 26. Large Signal Transient Response for Various Capacitor Loads



Figure 27. Large Signal Transient Response for Various Capacitor Loads



Figure 28. Slew Rate vs. Input Voltage



Figure 29. Slew Rate vs. Input Voltage



Figure 30. Settling Time Rising Edge











Figure 33. Settling Time Falling Edge



Figure 34. Transimpedance and Phase vs. Frequency







Figure 36. Output Overdrive Recovery







Figure 38. Common-Mode Rejection vs. Frequency



Figure 39. Output Overdrive Recovery



Figure 40. Input Voltage Noise vs. Frequency



Figure 41. Total Supply Current vs. Supply Voltage



Figure 42. Input Vos vs. Common-Mode Voltage



Figure 43. Input Current Noise vs. Frequency



Figure 44. Total Supply Current at Various Supplies vs. Temperature



Figure 45. Input Bias Current vs. Output Voltage

### APPLICATIONS GAIN CONFIGURATIONS

Unlike conventional voltage feedback amplifiers, the feedback resistor has a direct impact on the closed-loop bandwidth and stability of the current feedback op amp circuit. Reducing the resistance below the recommended value can make the amplifier response peak and even become unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth. Table 5 provides a convenient reference for quickly determining the feedback and gain set resistor values and bandwidth for common gain configurations.

Gain	R <sub>F</sub> (Ω)	R <sub>G</sub> (Ω)	–3 dB SS BW (MHz)	Large Signal 0.1 dB Flatness
+1	499	N/A	730	90
-1	301	301	350	60
+2	301	301	370	100
+5	200	49.9	180	30
+10	200	22.1	80	15

<sup>1</sup>Conditions:  $V_S = \pm 5 V$ ,  $T_A = 25^{\circ}C$ ,  $R_L = 150 \Omega$ .

Figure 46 and Figure 47 show the typical noninverting and inverting configurations and recommended bypass capacitor values.



Figure 47. Inverting Gain

### **20 MHz ACTIVE LOW-PASS FILTER**

The ADA4861-3 triple amplifier lends itself to higher order active filters. Figure 48 shows a 28 MHz, 6-pole, Sallen-Key low-pass filter.



Figure 48. 28 MHz, 6-Pole Low-Pass Filter

The filter has a gain of approximately 23 dB and flat frequency response out to 22 MHz. This type of filter is commonly used at the output of a video DAC as a reconstruction filter. The frequency response of the filter is shown in Figure 49.



Figure 49. 20 MHz Low-Pass Filter Frequency Response

### **RGB VIDEO DRIVER**

Figure 50 shows a typical RGB driver application using bipolar supplies. The gain of the amplifier is set at +2, where  $R_F = R_G = 301 \Omega$ . The amplifier inputs are terminated with shunt 75  $\Omega$  resistors, and the outputs have series 75  $\Omega$  resistors for proper video matching. In Figure 50, the POWER-DOWN pins are not shown connected to any signal source for simplicity. If the power-down function is not used, it is recommended that the power-down pins be tied to the negative supply and not be left floating (not connected).

For applications that require a fixed gain of +2, consider using the ADA4862-3 with integrated  $R_F$  and  $R_G$ . The ADA4862-3 is another high performance triple current feedback amplifier that can simplify design and reduce board area.





#### **DRIVING TWO VIDEO LOADS**

In applications that require two video loads be driven simultaneously, the ADA4861-3 can deliver. Figure 51 shows the ADA4861-3 configured with dual video loads. Figure 52 shows the dual video load 0.1 dB bandwidth performance.



Figure 51. Video Driver Schematic for Two Video Loads



Figure 52. Large Signal Frequency Response for Various Supplies,  $R_L = 75 \Omega$ 

#### **POWER-DOWN PINS**

The ADA4861-3 is equipped with three independent POWER DOWN pins, one for each amplifier. This allows the user the ability to reduce the quiescent supply current when an amplifier is inactive. The power-down threshold levels are derived from the voltage applied to the  $-V_S$  pin. When used in single-supply applications, this is especially useful with conventional logic levels. The amplifier is powered down when the voltage applied to the POWER DOWN pins is greater than  $-V_S + 1$  V. In a single-supply application, this is > +1 V (that is, 0 V + 1 V), in a  $\pm 5$  V supply application, the voltage is > -4 V. The amplifier is enabled whenever the POWER DOWN pins are left either open or the voltage on the POWER DOWN pins is lower than 1 V above  $-V_S$ . If the POWER DOWN pins are not used, it is best to connect them to the negative supply.

#### SINGLE-SUPPLY OPERATION

The ADA4861-3 can also be operated from a single power supply. Figure 53 shows the schematic for a single 5 V supply video driver. The input signal is ac-coupled into the amplifier via C1. Resistor R2 and Resistor R4 establish the input midsupply reference for the amplifier. Capacitor C5 prevents constant current from being drawn through the gain set resistor and enables the ADA4861-3 at dc to provide unity gain to the input midsupply voltage, thereby establishing the output voltage dc operating point. Capacitor C6 is the output coupling capacitor. For more information on single-supply operation of op amps, see www.analog.com/library/analogDialogue/archives/35-02/avoiding/.



Figure 53. Single-Supply Video Driver Schematic

#### POWER SUPPLY BYPASSING

Careful attention must be paid to bypassing the power supply pins of the ADA4861-3. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 2.2  $\mu$ F to 47  $\mu$ F capacitor located in proximity to the ADA4861-3 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, 0.1  $\mu$ F MLCC decoupling capacitors should be located as close to each of the power supply pins as is physically possible, no more than 1/8 inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

### LAYOUT

As is the case with all high-speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. The ADA4861-3 can operate at up to 730 MHz; therefore, proper RF design techniques must be employed. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near and under the input and output pins reduces stray capacitance. Signal lines connecting the feedback and gain resistors should be kept as short as possible to minimize the inductance and stray capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) through the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than 1 inch) is recommended. For more information on high speed board layout, go to: www.analog.com and www.analog.com/library/analogDialogue/archives/39-09/layout.html.

### **OUTLINE DIMENSIONS**



Narrow Body (R-14) Dimensions shown in millimeters and (inches)

#### **ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4861-3YRZ <sup>1</sup>	–40°C to +105°C	14-Lead SOIC_N	R-14	1
ADA4861-3YRZ-RL1	–40°C to +105°C	14-Lead SOIC_N	R-14	2,500
ADA4861-3YRZ-RL71	–40°C to +105°C	14-Lead SOIC_N	R-14	1,000

 $^{1}$  Z = Pb-free part.

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![](_page_15_Picture_8.jpeg)

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![](_page_16_Picture_0.jpeg)

![](_page_16_Picture_2.jpeg)

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