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April 2014

FDMB2307NZ

Dual Common Drain N-Channel PowerTrench® MOSFET 20 V, 9.7 A, 16.5 m Ω

Features

- Max $r_{S1S2(on)} = 16.5 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 8 \text{ A}$
- Max $r_{S1S2(on)} = 18 \text{ m}\Omega$ at $V_{GS} = 4.2 \text{ V}$, $I_D = 7.4 \text{ A}$
- Max $r_{S1S2(on)} = 21 \text{ m}\Omega$ at $V_{GS} = 3.1 \text{ V}$, $I_D = 7 \text{ A}$
- Max $r_{S1S2(on)} = 24 \text{ m}\Omega$ at $V_{GS} = 2.5 \text{ V}$, $I_D = 6.7 \text{ A}$
- Low Profile 0.8 mm maximum in the new package MicroFET 2x3 mm
- HBM ESD protection level > 2 kV (Note 3)
- RoHS Compliant

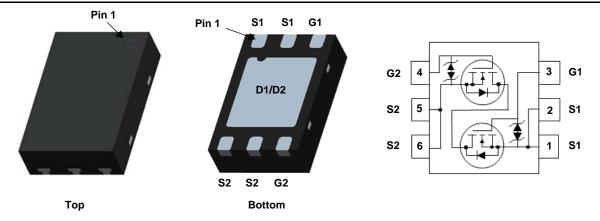


General Description

This device is designed specifically as a single package solution for Li-lon battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art MicroFET Leadframe, the FDMB2307NZ minimizes both PCB space and $r_{\rm S1S2(on)}.$

Application

■ Li-Ion Battery Pack



MLP 2x3

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{S1S2}	Source1 to Source2 Voltage			20	V
V _{GS}	Gate to Source Voltage		(Note 4)	±12	V
1	Source1 to Source2 Current -Continuous	T _A = 25°C	(Note 1a)	9.7	Δ.
IS1S2	-Pulsed			40	— A
Б	Power Dissipation	T _A = 25 °C	(Note 1a)	2.2	10/
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1b)	0.8	W
T _J , T _{STG}	Operating and Storage Junction Temperature	Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(Dual Operation)	(Note 1a)	57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(Dual Operation)	(Note 1b)	161	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
307	FDMB2307NZ	MLP 2x3	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	octeristics					
I _{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V _{S1S2} = 16 V, V _{GS} = 0 V			1	μА
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 12 V, V _{S1S2} = 0 V			10	μΑ

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = 250 \mu A$	0.6	1	1.5	V
	$V_{GS} = 4.5 \text{ V}, I_{S1S2} = 8 \text{ A}$	10.5	13.5	16.5		
	V _{GS} = 4.2 V, I _{S1S2} = 7.4 A	11	14	18		
	V _{GS} = 3.1 V, I _{S1S2} = 7 A	11.5	16	21	mΩ	
'S1S2(on)	3132(011)	V _{GS} = 2.5 V, I _{S1S2} = 6.7 A	12	18	24	11152
		$V_{GS} = 4.5 \text{ V}, I_{S1S2} = 8 \text{ A},$ $T_{J} = 125 ^{\circ}\text{C}$	11	20	29	
9 _{FS}	Forward Transconductance	V _{S1S2} = 5 V, I _{S1S2} = 8 A		41		S

Dynamic Characteristics

C _{iss}	Input Capacitance		V 40.V V 0.V		1760	2640	pF
C _{oss}			$V_{S1S2} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		229	345	pF
C _{rss}	Reverse Transfer Capacitance		1 – 1 101112		211	320	pF
R_g	Gate Resistance	(Note 5)		0.1	2.6	8	Ω

Switching Characteristics

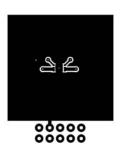
t _{d(on)}	Turn-On Delay Time		12	22	ns
t _r	Rise Time	V _{S1S2} = 10 V, I _{S1S2} = 8 A,	19	34	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	32	51	ns
t _f	Fall Time		9.5	17	ns
Q_g	Total Gate Charge	V _{G1S1} = 0 V to 5 V	20	28	nC
Q_g	Total Gate Charge	$V_{G1S1} = 0 \text{ V to } 4.5 \text{ V}$ $I_{S1S2} = 8 \text{ A},$	18	25	nC
Q_{gs}	Gate1 to Source1 Charge	$V_{G2S2} = 0 \text{ V}$	2.8		nC
Q_{gd}	Gate1 to Source2 "Miller" Charge	V G252 - 0 V	5.3		nC

Source1- Source2 Diode Characteristics

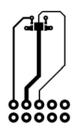
I _{fss}	Maximum Continuous Source1-Source2 Diode Forward Current		8	Α	
V _{fss}	Source1 to Source2 Diode Forward Voltage $V_{G1S 1} = 0 \text{ V}, V_{G2S2} = 4.5 \text{ V}$ $I_{fss} = 8 \text{ A}$	/, (Note 2)	0.8	1.2	V

NOTES

^{1.} R_{BJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a. 57 °C/W when mounted on
 a 1 in² pad of 2 oz copper



b. 161 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- 4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.
- 5. Rg is measured on 100% of the die at wafer level.

Typical Characteristics T_J = 25°C unless otherwise noted

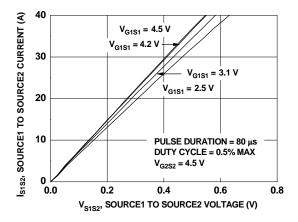


Figure 1. On-Region Characteristics

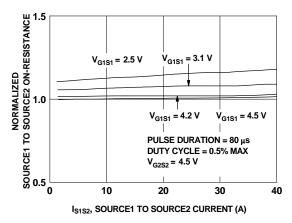


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

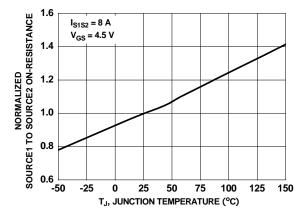


Figure 5. Normalized On Resistance vs Junction Temperature

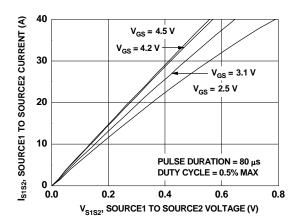


Figure 2. On-Region Characteristics

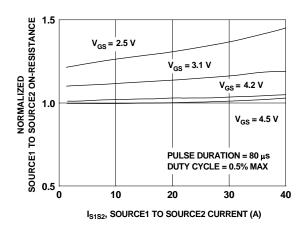


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

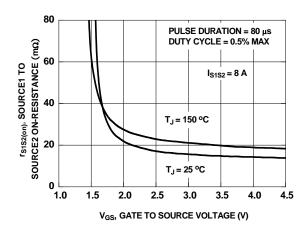


Figure 6. On Resistance vs Gate to Source Voltage

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

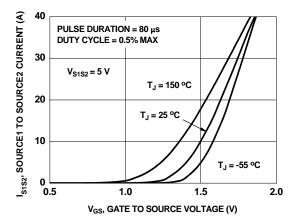


Figure 7. Transfer Characteristics

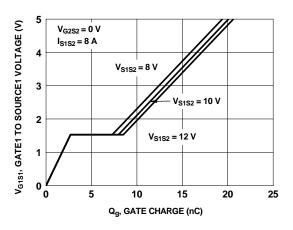


Figure 9. Gate Charge Characteristics

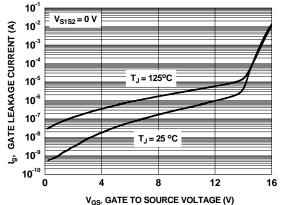


Figure 11. Gate Leakage Current vs **Gate to Source Voltage**

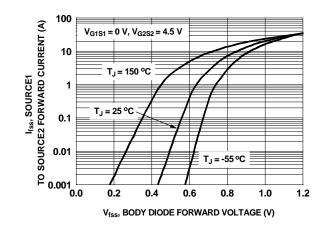


Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current

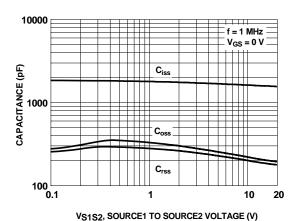


Figure 10. Capacitance vs Source1 to Source2 Voltage

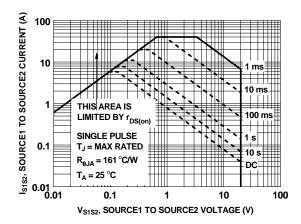


Figure 12. Forward Bias Safe **Operating Area**

Typical Characteristics T_J = 25°C unless otherwise noted

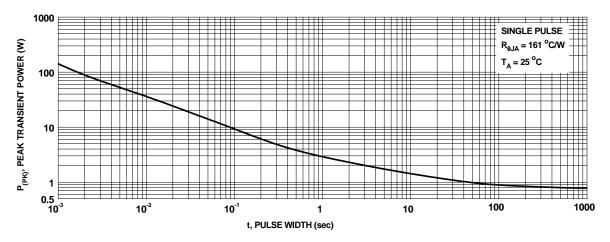


Figure 13. Single Pulse Maximum Power Dissipation

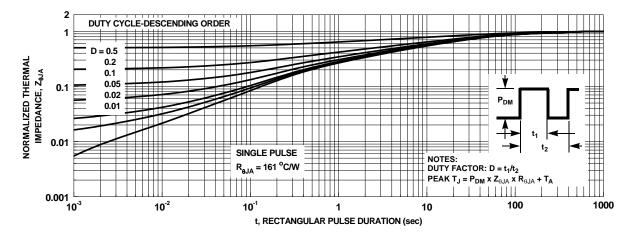
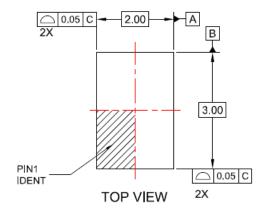
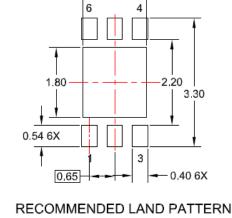


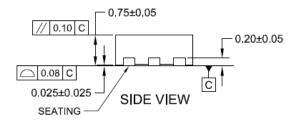
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

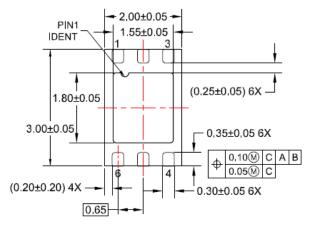
Dimensional Outline and Pad Layout





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BOTTOM VIEW

NOTES:

- A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.
- B. DRAWING FILENAME: MKT-MLP06Qrev3.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009,
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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

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