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FDMS8333L

December 2014

N-Channel PowerTrench[®] MOSFET 40 V, 76 A, 3.1 m Ω

Features

- Max $r_{DS(on)}$ = 3.1 m Ω at V_{GS} = 10 V, I_D = 22 A
- Max $r_{DS(on)}$ = 4.3 m Ω at V_{GS} = 4.5 V, I_D = 19 A
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

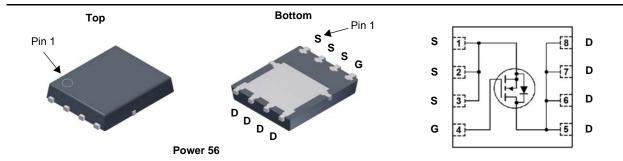


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- OringFET / Load Switching
- Synchronous rectification
- DC-DC Conversion



MOSFET Maximum Ratings TA = 25 °C unless otherwise noted

Symbol	Parameter				Ratings	Units
V _{DS}	Drain to Source V	oltage			40	V
V _{GS}	Gate to Source Vo	oltage			±20	V
I _D	Drain Current	-Continuous	T _C = 25 °C		76	
	-Continuous		T _A = 25 °C	(Note 1a)	22	Α
		-Pulsed		(Note 4)	250	
E _{AS}	Single Pulse Aval	anche Energy		(Note 3)	216	mJ
D	Power Dissipation	l	T _C = 25 °C		69	W
P_{D}	Power Dissipation	1	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Sto	orage Junction Temperat	ure Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8333L	FDMS8333L	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-6		mV/°C
r _{DS(on)}		V _{GS} = 10 V, I _D = 22 A		2.4	3.1	
	Static Drain to Source On Resistance	V _{GS} = 4.5 V, I _D = 19 A		3.3	4.3	mΩ
		V_{GS} = 10 V, I_D = 22 A, T_J = 125 °C		3.6	4.7	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 22 A		120		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V = 20 V V = 0 V		3245	4545	pF
Coss	Output Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		840	1175	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		32	55	pF
R _q	Gate Resistance		0.1	0.7	2.1	Ω

Switching Characteristics

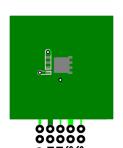
t _{d(on)}	Turn-On Delay Time		14	25	ns
t _r	Rise Time	V _{DD} = 20 V, I _D = 22 A,	4.7	10	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{GEN} = 6 Ω	33	53	ns
t _f	Fall Time		4.2	10	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	46	64	nC
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 20 \text{ V}$,	22	31	nC
Q _{gs}	Gate to Source Charge	I _D = 22 A	8.8		nC
Q_{gd}	Gate to Drain "Miller" Charge		5.5		nC

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.9 \text{ A}$	(Note 2)	0.7	1.2	٧
	Source to Drain Diode 1 of ward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 22 \text{ A}$	(Note 2)	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 22 A, di/dt = 100 A/μs		38	61	ns
Q _{rr}	Reverse Recovery Charge			20	32	nC

Notes:

¹ R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

^{3.} E_{AS} of 216 mJ is based on starting $T_J = 25$ °C; N-ch: L = 3 mH, $I_{AS} = 12$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 38$ A.

^{4.} Pulsed Id limited by junction temperature, td<=100 μ S, please refer to SOA curve for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

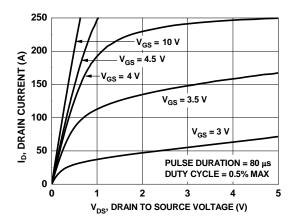


Figure 1. On Region Characteristics

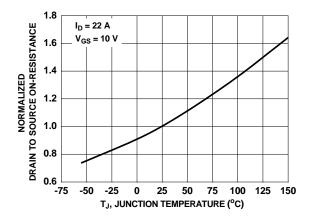


Figure 3. Normalized On Resistance vs Junction Temperature

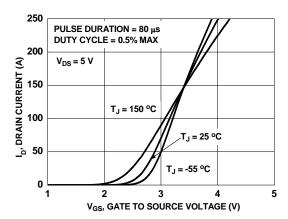


Figure 5. Transfer Characteristics

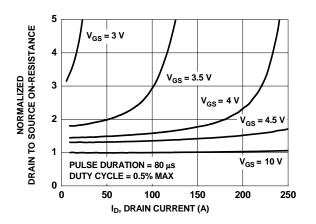


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

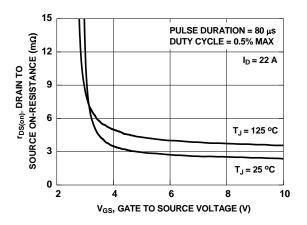


Figure 4. On-Resistance vs Gate to Source Voltage

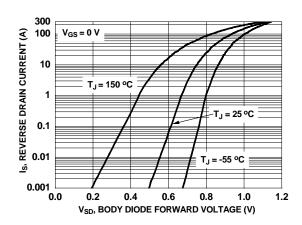


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

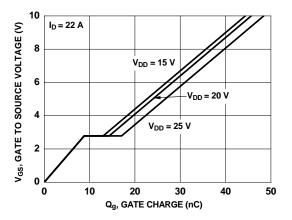


Figure 7. Gate Charge Characteristics

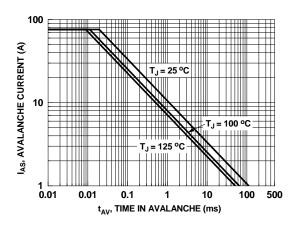


Figure 9. Unclamped Inductive Switching Capability

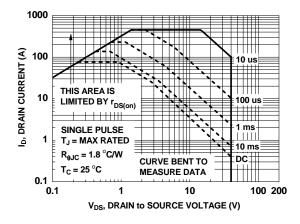


Figure 11. Forward Bias Safe Operating Area

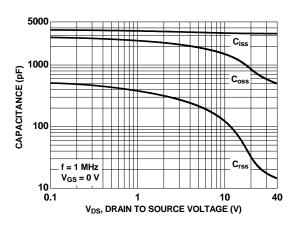


Figure 8. Capacitance vs Drain to Source Voltage

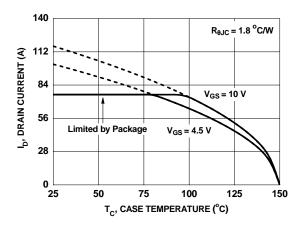


Figure 10. Maximum Continuous Drain Current vs Case Temperature

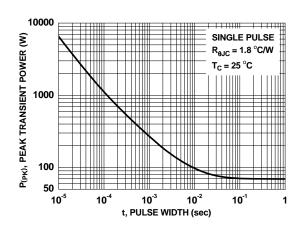


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

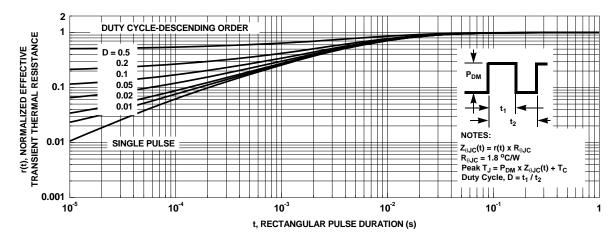


Figure 13. Transient Thermal Response Curve



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