

74HC3G34; 74HCT3G34

Triple buffer gate

Rev. 7 — 11 June 2018

Product data sheet

1 General description

The 74HC3G34; 74HCT3G34 is a triple buffer. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2 Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC3G34: CMOS level
 - For 74HCT3G34: TTL level
- Complies with JEDEC standard no. 7 A
- Symmetrical output impedance
- High noise immunity
- Low-power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC3G34DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74HCT3G34DP					
74HC3G34DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74HCT3G34DC					

nexperia

4 Marking

Table 2. Marking

Type number	Marking code ^[1]
74HC3G34DP	H34
74HCT3G34DP	T34
74HC3G34DC	P34
74HCT3G34DC	U34

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram

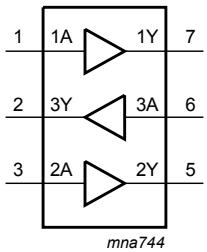


Figure 1. Logic symbol

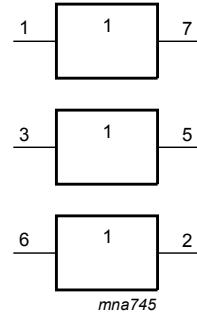


Figure 2. IEC logic symbol

6 Pinning information

6.1 Pinning

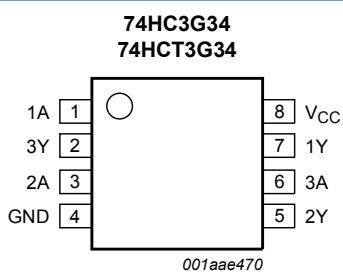


Figure 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
1Y, 2Y, 3Y	7, 5, 2	data output
GND	4	ground (0 V)
V _{CC}	8	supply voltage

7 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	L
H	H

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1]	-	±20 mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±20 mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	quiescent supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	300 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G34			74HCT3G34			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10 Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max		
74HC3G34									
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V	
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V	
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V	
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V	
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V	
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V	
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V	
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V	
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V	
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V	
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V	
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V	
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	µA	

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	per input pin; V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	µA
C _I	input capacitance		-	1.5	-	-	-	pF

74HCT3G34								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	µA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	375	-	410	µA
C _I	input capacitance		-	1.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 5](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC3G34								
t _{pd}	propagation delay	nA to nY; see Figure 4 [2]						
		V _{CC} = 2.0 V	-	29	95	-	125	ns
		V _{CC} = 4.5 V	-	9	19	-	25	ns
		V _{CC} = 6.0 V	-	8	16	-	20	ns
t _t	transition time	nY; see Figure 4 [3]						
		V _{CC} = 2.0 V	-	18	95	-	125	ns
		V _{CC} = 4.5 V	-	6	19	-	25	ns
		V _{CC} = 6.0 V	-	5	16	-	20	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [4]	-	10	-	-	-	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HCT3G34								
t_{pd}	propagation delay	nA to nY; see Figure 4 [2]						
		$V_{CC} = 4.5$ V	-	10	23	-	29	ns
t_t	transition time	nY; $V_{CC} = 4.5$ V; see Figure 4 [3]	-	6	19	-	25	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5$ V [4]	-	9	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{TLH} and t_{TTL} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$

where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

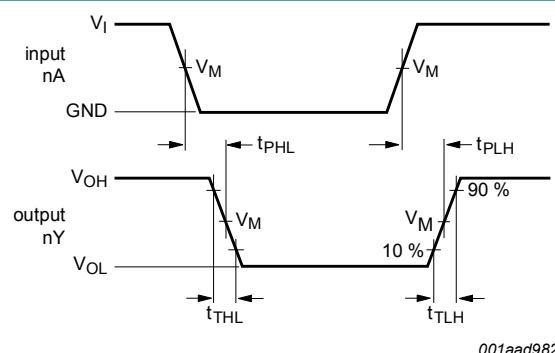
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1 Waveform and test circuit



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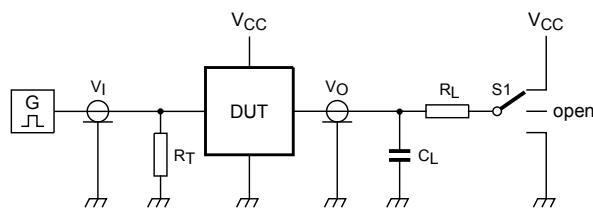
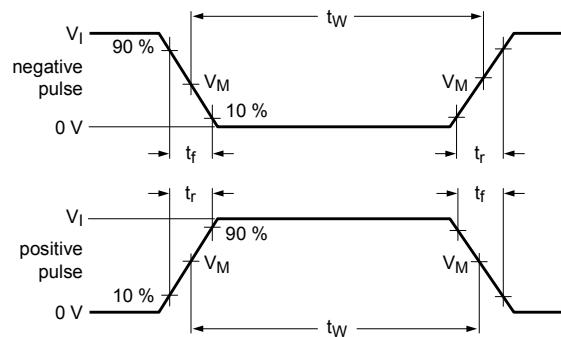
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. Propagation delay data input (nA) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC3G34	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT3G34	1.3 V	1.3 V



001aad983

Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

$S1$ = Test selection switch.

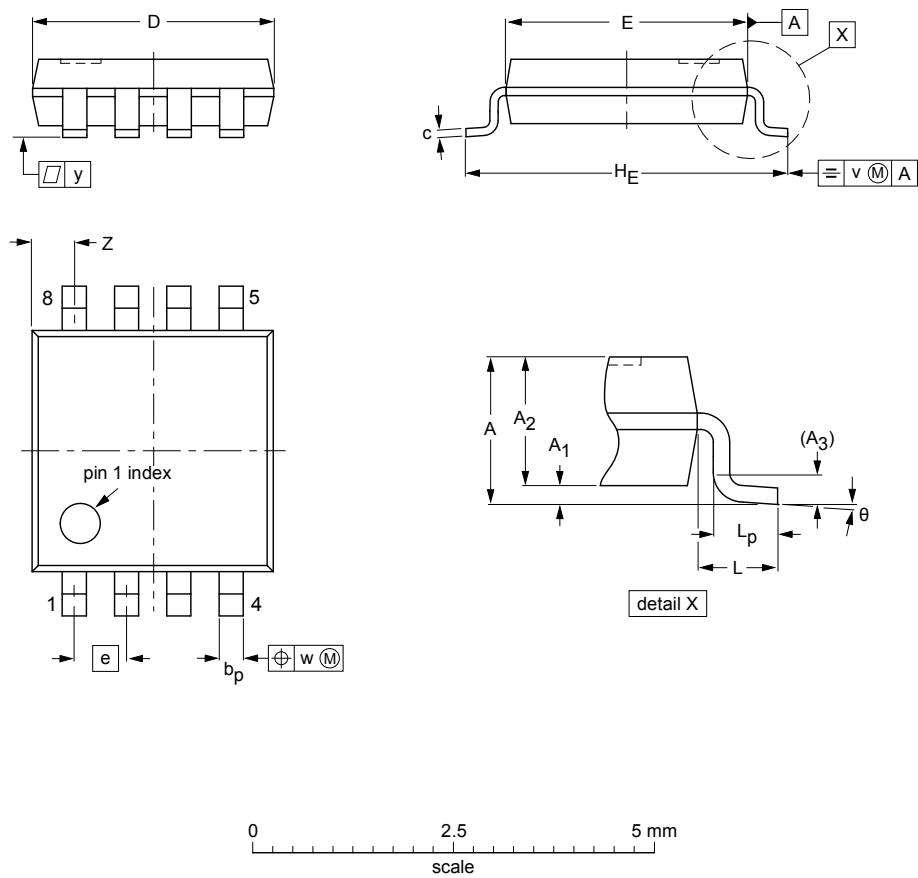
Figure 5. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	
74HC3G34	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	open
74HCT3G34	GND to 3 V	≤ 6 ns	50 pF	1 k Ω	open

12 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

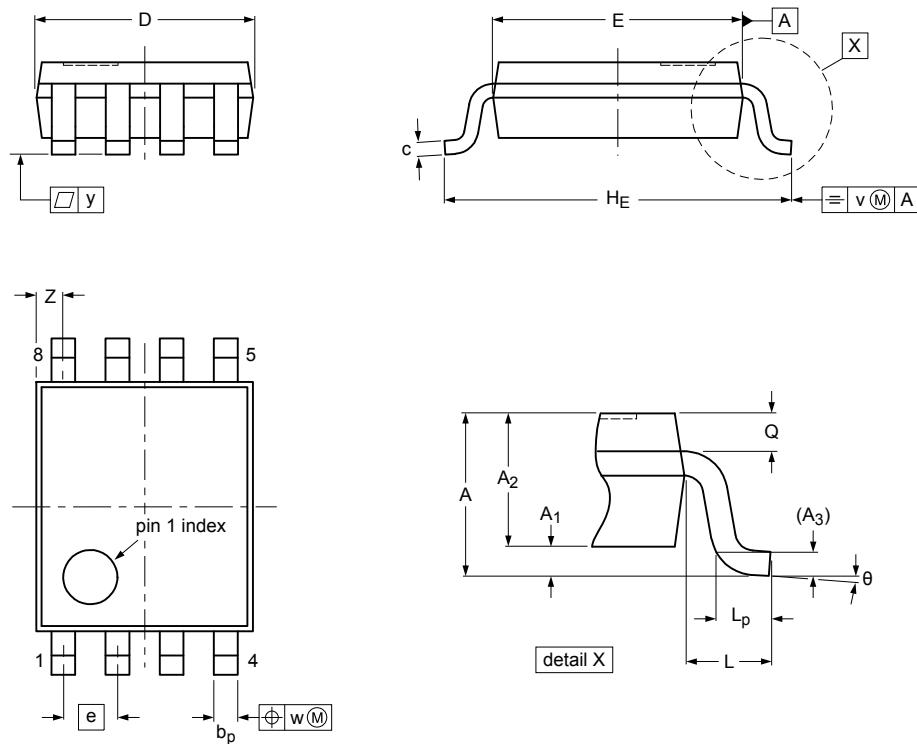
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Figure 6. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	max	0.15	0.85		0.27	0.23	2.1	2.4		3.2	0.40	0.21		0.2	0.08	0.1	0.4	8°
mm	nom	1		0.12					0.5		0.4							
mm	min	0.00	0.60		0.17	0.08	1.9	2.2		3.0	0.15	0.19					0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

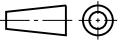
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				-07-06-02- 16-05-31

Figure 7. Package outline SOT765-1 (VSSOP8)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G34 v.7	20180611	Product data sheet	-	74HC_HCT3G34 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC3G34GD and 74HCT3G34GD removed. 			
74HC_HCT3G34 v.6	20131211	Product data sheet	-	74HC_HCT3G34 v.5
Modifications:	<ul style="list-style-type: none"> For type numbers 74HC3G34GD and 74HCT3G34GD XSON8U has changed to XSON8. 			
74HC_HCT3G34 v.5	20090507	Product data sheet	-	74HC_HCT3G34 v.4
74HC_HCT3G34 v.4	20060309	Product data sheet	-	74HC_HCT3G34 v.3
74HC_HCT3G34 v.3	20030519	Product specification	-	74HC_HCT3G34 v.2
74HC_HCT3G34 v.2	20030210	Product specification	-	74HC_HCT3G34 v.1
74HC_HCT3G34 v.1	20031003	Product specification	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ Р В 0015-002 и ЭС РД 009

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