

FEATURES

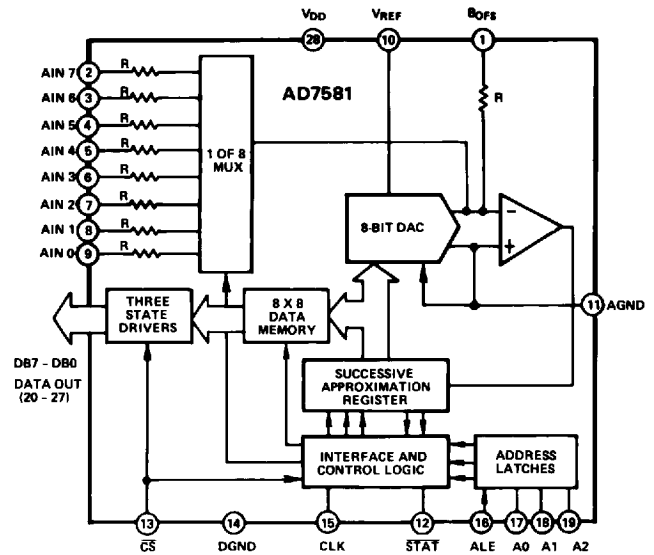
- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to μ P
- Low Cost

GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs ($A_0 - A_2$) with ALE enables the AD7581 to interface with μ P systems which feature either shared or separate address and data buses.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD7581 — SPECIFICATIONS

DC SPECIFICATIONS ($V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Operation, unless otherwise stated.)

Parameter	Version ¹	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AQ	±1 7/8	±1 7/8 max	LSB	
	KN, BQ	±3/4	±3/4 max	LSB	
	LN, CQ	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AQ	±1 7/8	±1 7/8 max	LSB	
	KN, BQ	±7/8	±7/8 max	LSB	
	LN, CQ	±3/4	±3/4 max	LSB	
Offset Error ²	JN, AQ	200	200 max	mV	Adjustable to zero, See Figure 7a.
	KN, BQ	80	80 max	mV	
	LN, CQ	50	50 max	mV	
Gain Error					
Worst Channel	JN, AQ	±3	±6 max	LSB	Adjustable to zero, See Figure 7a. Gain Error Is Measured After Offset Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} Is ±2LSB.
	KN, BQ	±2	±4 max	LSB	
	LN, CQ	±1	±2 max	LSB	
Gain Match Between Channels	JN, AQ	2	3 max	LSB	Adjustable to zero, See Figure 7a.
	KN, BQ	1 1/2	2 max	LSB	
	LN, CQ	1	1 max	LSB	
B_{OFS} Gain Error	All	-2 1/2	-	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (Pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	±5%
At B_{OFS} (Pin 1) ³	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (Pins 2-9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	-10	-10	V	
V_{REF} Range ⁴	All	-5 to -15	-5 to -15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to $+V_{REF}$	0 to $+V_{REF}$	V	See Figure 7 and 8.
Bipolar Mode	All	0 to $-V_{REF}$	0 to $-V_{REF}$	V	See Figure 9
		$-VB_{OFS} \leq VA_{IN} \leq V_{REF} - VB_{OFS}$			
DIGITAL INPUTS					
\overline{CS} (Pin 13), ALE (Pin 16) $A_0 - A_2$ (Pin 17-19), CLK (Pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	$V_{IN} = 0V$, V_{DD}
V_{INL} Logic LOW Input Voltage	All	+1.2	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	
C_{IN} Input Capacitance ⁵	All	4	5 max	pF	
DIGITAL OUTPUTS					
STAT (Pin 12), DB_7 to DB_0 (Pins 20-27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	$I_{SOURCE} = 40\mu A$ $I_{SINK} = 1.6mA$
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	$V_{OUT} = 0V$ to V_{DD}
Floating State Output Capacitance ($DB_7 - DB_0$)	All	5	10 max	pF	
Output Code	All	Unipolar Binary Figure 7 Complementary Binary Figure 8 Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	$f_{CLK} = 1MHz$
I_{DD} - Static	All	3 typ	5 max	mA	
I_{DD} - Dynamic	All	3 typ	8 max	mA	

NOTES

¹Temperature range as follows: JN, KN, LN (0 to +70°C); AQ, BQ, CQ (-25°C to +85°C).

²Typical offset temperature coefficient is ±150μV/°C.

³ $R_{B_{OFS}}/R_{AIN}$ (0-7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a and Figure 9a.

⁴Typical value, not guaranteed or subject to test.

⁵Guaranteed but not tested.

⁶Typical change in B_{OFS} gain from +25°C to T_{min} to T_{max} is ±2LSBs.

Specifications subject to change without notice.

AC SPECIFICATIONS ($V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Operation, unless otherwise stated.)

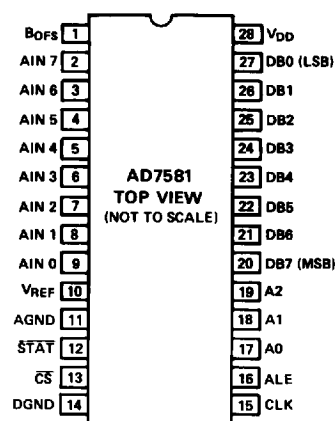
Symbol	Specification	Typical at +25°C	Limit Over Temperature	Units	Conditions
t_H	ALE pulse width	50	80 min	ns	See "Switching Terminology"
t_{ALS}	Address valid to latch set-up time	45	70 min	ns	
t_{ALH}	Address valid to latch hold time	10	20 min	ns	
t_{LCS}	Address latch to \overline{CS} set-up time	10	20 min	ns	
t_{ACC}	\overline{CS} to output propagation delay	200	250 max	ns	$C_L = 100pF$
t_{CW}	\overline{CS} pulse width	250	280 min	ns	
t_{CF}	\overline{CS} to output float propagation delay	50	80 max	ns	
t_{CLZ}	\overline{CS} to low impedance bus	100	150 max	ns	
f_{CLK}	Clock frequency for stated accuracy	1600	1200 max ¹	kHz	

¹ Guaranteed conversion time of 66.6 μ s/channel with 1200kHz clock.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND	+7V
V_{DD} to DGND	+7V
AGND to DGND	-0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 13, 16-19)	-0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to DGND (Pins 12, 20-27)	-0.3V, $V_{DD} + 0.3V$
CLK (Pin 15) Input Voltage to DGND	-0.3V, $V_{DD} + 0.3V$
V_{REF} (Pin 10) to AGND	$\pm 25V$
V_{BOFS} (Pin 1) to AGND	$\pm 17V$
AIN (0-7)(Pin 9-2)	$\pm 17V$
Operating Temperature Range	
Commercial (J, K, L Versions)	0 to +70°C
Industrial (A, B, C Versions)	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package)	
to +75°C	1,000mW
Derate above +75°C by	10mW/°C

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model	Temperature Range	Differential Nonlinearity (LSB)	Package Option*
AD7581JN	0 to +70°C	$\pm 1 \frac{7}{8}$ max	N-28
AD7581KN	0 to +70°C	$\pm 7/8$ max	N-28
AD7581LN	0 to +70°C	$\pm 3/4$ max	N-28
AD7581AQ	-25°C to +85°C	$\pm 1 \frac{7}{8}$ max	Q-28
AD7581BQ	-25°C to +85°C	$\pm 7/8$ max	Q-28
AD7581CQ	-25°C to +85°C	$\pm 3/4$ max	Q-28

NOTE

*N = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

TIMING AND CONTROL OF THE AD7581

CHANNEL SELECTION

Table 1 shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table 1. Channel Selection Truth Table

TIMING AND CONTROL

A typical timing diagram is shown in Figure 3. When CS is HIGH, the three-state data drivers are in the high-impedance state. When CS goes LOW the data drivers switch to the low-impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

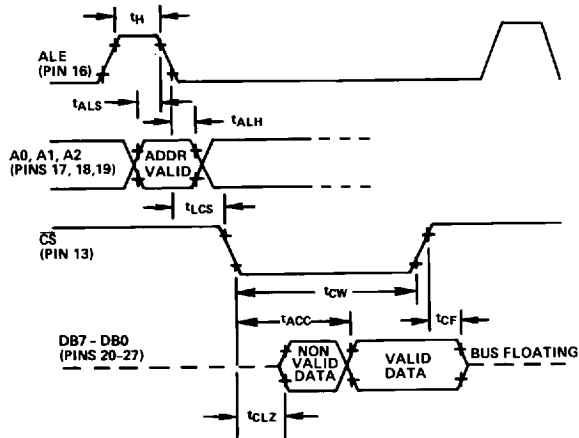


Figure 3. Timing Diagram for the AD7581

SWITCHING TERMINOLOGY

- t_H: ALE pulse width requirement.
- t_{ALH}: Address Valid to latch hold time.
- t_{ALS}: Address Valid to latch set-up time.
- t_{LCS}: Address latch to Chip Select set-up time.
- t_{CW}: Chip Select pulse width requirement.
- t_{ACC}: Chip Select to valid data propagation delay.
- t_{CF}: Chip Select to output data float propagation delay.
- t_{CLZ}: Chip Select to low impedance data bus.

CHANNEL IDENTIFICATION

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The STAT output provides an

identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on a rising edge of a clock pulse and is completed in 200ns. This occurs 6 clock periods before STAT goes low.

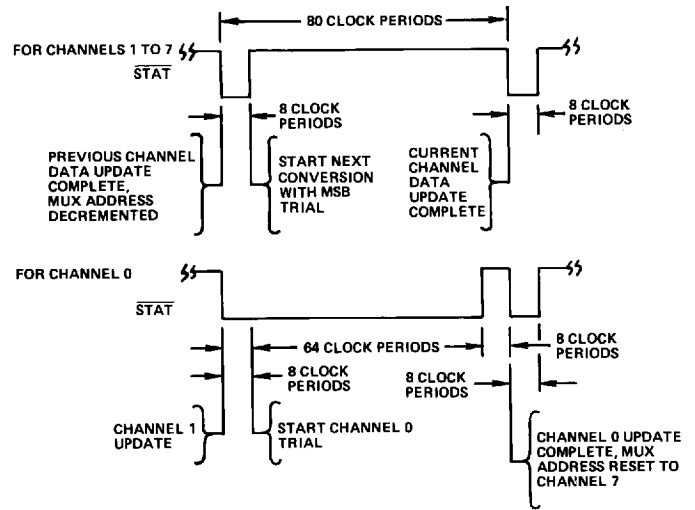


Figure 4. STAT Output for Channel Identification

One simple circuit using the STAT output is shown in Figure 5. The time constant RC is chosen such that X₂ ignores the normal STAT low pulse width (8 clock periods wide) but respond to the much wider STAT low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a 1μs clock period C = 0.022μF, R = 1.8kΩ.

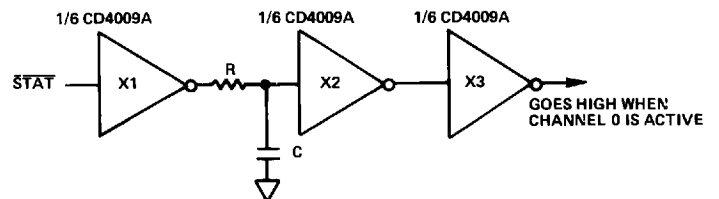


Figure 5. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the STAT output and hence determine channel identity. A simple routine is shown in Figure 6.

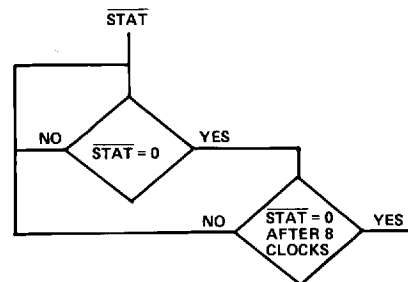


Figure 6. Software Channel Identification

AD7581

OPERATING THE AD7581

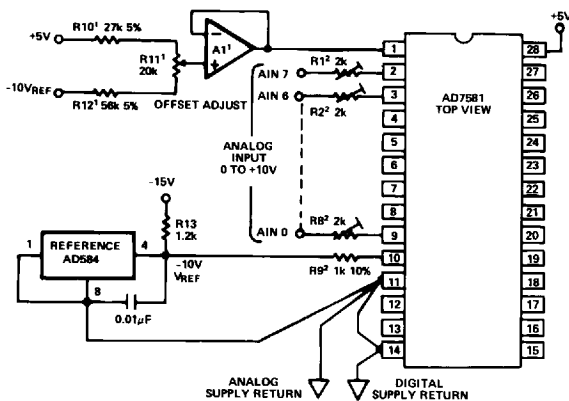
UNIPOLAR BINARY OPERATION

Figures 7a and 7b show the analog circuit connections and typical transfer characteristic for unipolar operation (0V to +10V). An AD584 is used for the -10V reference. Calibration is as follows (device clocked i.e., continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS} . R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS} .

1. Since comparator offset will be the same regardless of which channel is active, take A_0 , A_1 and A_2 LOW and and exercise ALE to latch the address.
2. With $A_{IN 0} = 19.5mV$ ($1/2LSB$) adjust R11, i.e., the offset voltage on B_{OFS} , until $DB_7 - DB_1$ are LOW and DB_0 (LSB) flickers.



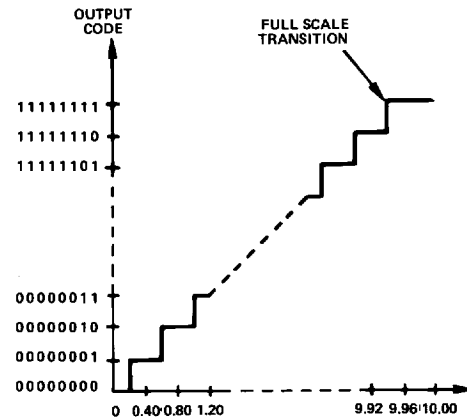
NOTES:
¹ A1, R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED AND B_{OFS} CAN BE TIED TO AGND.
² R1, R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.

Figure 7a. AD7581 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941V ($FS - 3/2LSB$) to all input channels $A_{IN} (0-7)$.
2. Select required channel n via A_0 , A_1 , A_2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION. BIT WEIGHT FOR A -10V REFERENCE IS $\approx 39.1mV$.

Figure 7b. Transfer Characteristic for Unipolar Circuit of Figure 7a

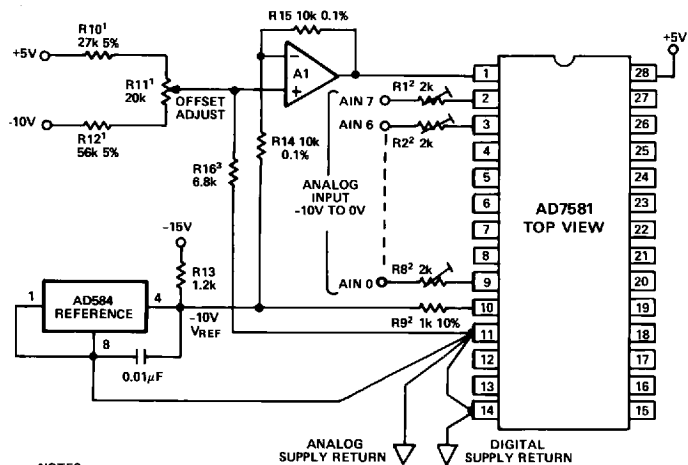
UNIPOLAR (COMPLEMENTARY BINARY) OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar (complementary binary) operation. Calibration is as follows (continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS} . R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS} .

1. Since comparator offset will be the same regardless of which channel is active, take A_0 , A_1 and A_2 LOW and exercise ALE to latch the address.
2. With $A_{IN 0} = -9.98V$ ($-FS + 1/2LSB$) adjust R11, i.e., the offset voltage on B_{OFS} , until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.



NOTES:
¹ R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
² R1 - R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
³ R16/R10/R12 = 5kΩ. IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 5kΩ.

Figure 8a. AD7581 (0V to -10V) Operation (Output Code is Complementary Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

- 1) Apply -58.6mV ($3/2\text{LSB}$) to all input channels A_{IN} (0-7).
- 2) Select required channel n via A_0, A_1, A_2 and exercise ALE to latch the address.
- 3) Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
- 4) Select next channel requiring gain trim and repeat step 2 and 3.

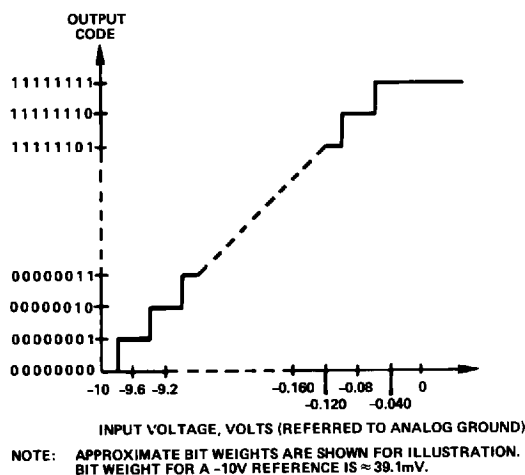


Figure 8b. Transfer Characteristic for Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for $\pm 5\text{V}$ bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFFS} pin.

Calibration is as follows (continuous conversions);

OFFSET:

1. Apply -4.980V ($-FS/2 + 1/2\text{LSB}$) to all input channels A_{IN} (0-7).
2. Trim R11 of the comparator offset circuit until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

1. Apply $+4.941\text{V}$ ($+FS/2 - 3/2\text{LSB}$) to all input channels, A_{IN} (0-7).
2. Select required channel n via A_0, A_1, A_2 , and latch the address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.

4. Select next channel requiring gain trim and repeat steps 2 and 3.
5. Apply -19.5mV to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.

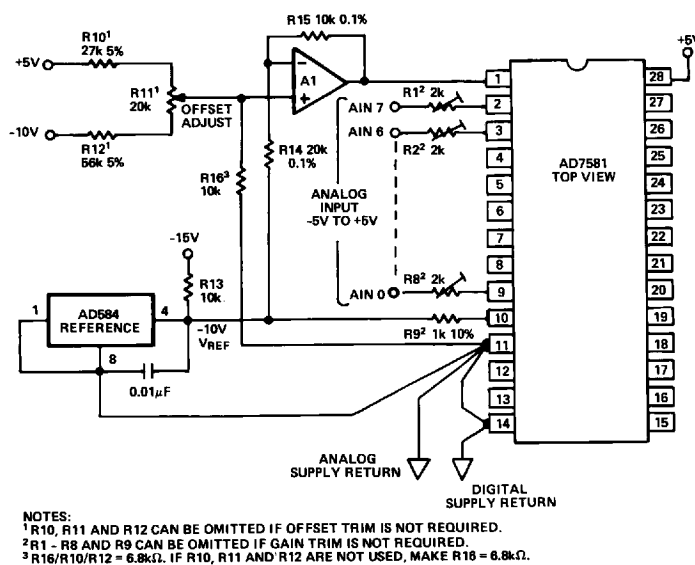


Figure 9a. AD7581 Bipolar (-5V to $+5\text{V}$) Operation (Output Code is Offset Binary)

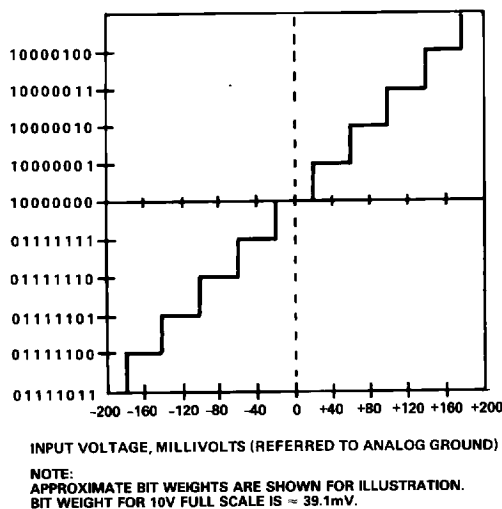


Figure 9b. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

AD7581

INTERFACING THE AD7581

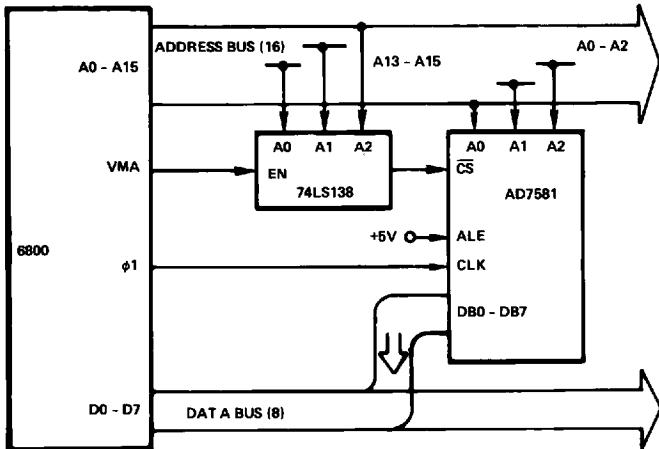


Figure 10. AD7581/6800 Interface

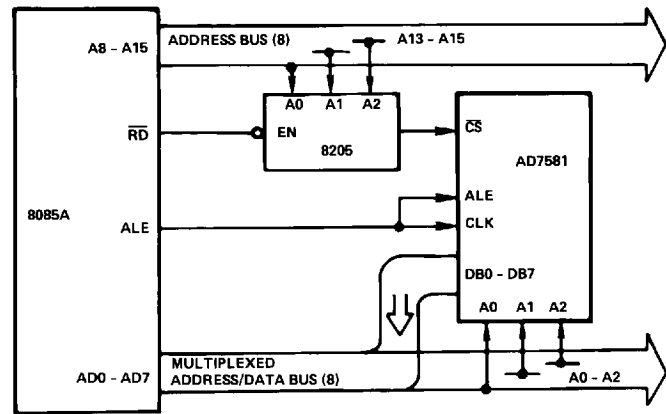


Figure 11. AD7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND

It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7581. In systems where the $A_{GND} - D_{GND}$ intertie is not local, connect back-to-back diodes (1N914 or equivalent) between the AD7581 A_{GND} and D_{GND} pins.

2. LOGIC DEGLITCHING IN μP APPLICATIONS

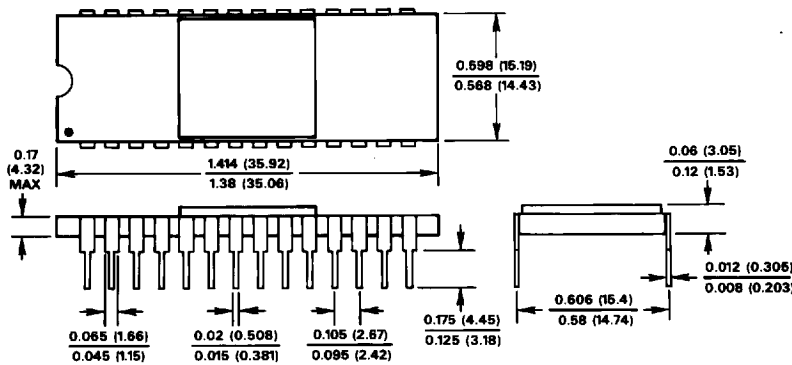
Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7581 \overline{CS} terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with \overline{RD} (8080), \overline{RD} (8085) or VMA (6800).

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

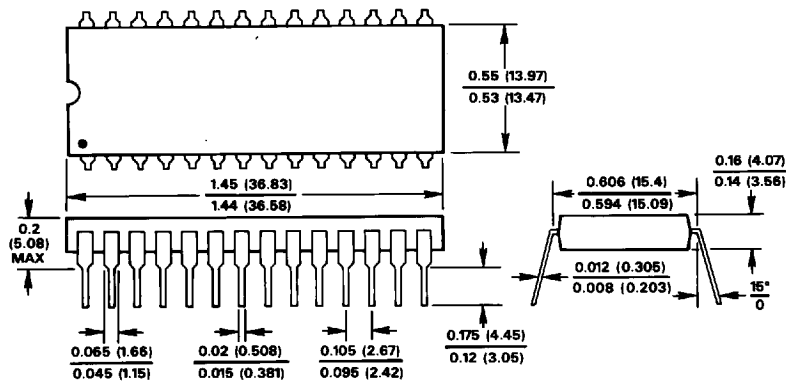
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (D-28)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE
WITH MIL-M-38510 REQUIREMENTS
CAVITY LID IS ELECTRICALLY ISOLATED

28-PIN PLASTIC DIP (N-28)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42

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