# CY91520 Series

# 32-bit FR81S Microcontroller

The CY91520 series is a Cypress 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

**Note**:This series is a composition of the end of the above-mentioned each name of articles of presence, According to Presence of sub-clock, CSV initial value and LVD initial value. Please see "Ordering Information" for details.

## Features

### FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
- General-purpose register : 32 bits × 16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift order etc.
- High-level language support instructions
- Function entry/exit instructions
- Register content multi-load and store instructions
- Bit search instructions
  Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
- Overhead reduction during branch process
- Register interlock function
- Easy assembler writing
- The support at the built-in / instruction level of the multiplier
- Signed 32-bit multiplication: 5 cycles
- Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
  6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

### Peripheral Functions

- Clock generation (equipped with SSCG function)
  - Main oscillation (4 MHz to 16 MHz)
  - Sub oscillation (32 kHz) or none sub oscillation
  - PLL multiplication rate : 1 to 20 times
  - Equipped with a 100 kHz CR oscillator
- Built-in program flash memory capacity
  CY91F522: 256 +64 KB
  CY91F523: 384 + 64 KB
  CY91F524: 512 + 64 KB
  CY91F525: 768 + 64 KB
  CY91F526: 1024 + 64 KB
- Flash memory for built-in data (WorkFlash) 64 KB
- Built-in RAM capacity
  - Main RAM
    CY91F522: 48 KB
    CY91F523: 48 KB
    CY91F524: 64 KB
    CY91F525: 96 KB
    CY91F526: 128 KB
  - Backup RAM 8 KB
- General-purpose ports:
  CY91F52xB 44 sets (No sub oscillation), 42 sets (sub oscillation)
  CY91F52xD 56 sets (No sub oscillation), 54 sets (sub oscillation)
  CY91F52xF 76 sets (No sub oscillation), 74 sets (sub oscillation)
  CY91F52xJ 96 sets (No sub oscillation), 94 sets (sub oscillation)
  CY91F52xK 120 sets (No sub oscillation), 118 sets (sub oscillation)
  CY91F52xL 152 sets (No sub oscillation), 150 sets (sub oscillation)
  Included $I^2C$ open drain corresponding ports:16 sets
- External bus interface
  - 22-bit address, 16-bit data
- DMA Controller
  - Up to 16 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
  - 12-bit resolution : Max. 48 ch (32 ch + 16 ch)
  - Conversion time : 1.4 µs

- D/A converter (R-2R type)
  - 8-bit resolution : 2 ch
- External interrupt input: 8 channels × 2 units total 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
  - 5 V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
    < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer support
    <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
    <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hard assist function
    < $I^2C$ >
  - 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
  - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Standard mode (Max. 100 kbps) / fast mode (Max. 400 kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
  - Transfer speed : Up to 1 Mbps
  - 128-transmission/reception message buffering :
    1 channel (ch.0),
    64-transmission/reception message buffering :
    2 channels (ch.1 and ch.2)
- PPG: 16-bit × Max. 48 channels
  - LED drive output 4 channels 11 ch to 14 ch
  - Reload timer : 16-bit × Max.8 channels
  - Free-run timer :
    16-bit × 3 channels
    32-bit × Max 3 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
  - 8-/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32 kHz) (dual clock products) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
  - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90 nm Technology
- Power supplies
  - 5 V Power supply
  - The internal 1.2 V is generated from 5 V with the voltage step-down circuit

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# 1. Product Lineup

**Product Lineup Comparison 64 Pins**

| | CY91F522B | CY91F523B | CY91F524B | CY91F525B | CY91F526B |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | None | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | None | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 1 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 5 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 4 ch | | | | |
| 16-bit Reload Timer | 7 ch | | | | |
| PPG | 16 bit × 21 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 13 ch (1 unit), 12 bit × 13 ch (1 unit) | | | | |
| D/A converter (8 bit) | 1 ch | | | | |
| Multi-Function Serial Interface | 8 ch*1 | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 44 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| NMI request function | Yes | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V*2 | | | | |
| Package | LQD064 | | | | |

*1: Only channel 5, channel 6 and channel 11 support the $I^2C$ (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Product Lineup Comparison 80 Pins**

| | CY91F522D | CY91F523D | CY91F524D | CY91F525D | CY91F526D |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | None | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | 1 ch | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 2 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 5 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 4 ch | | | | |
| 16-bit Reload Timer | 7 ch | | | | |
| PPG | 16 bit × 27 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 16 ch (1 unit), 12 bit × 16 ch (1 unit) | | | | |
| D/A converter (8 bit) | 1 ch | | | | |
| Multi-Function Serial Interface | 9 ch*1 | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 56 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V *2 | | | | |
| Package | LQH080 | | | | |

*1: Only channel 5, channel 6 and channel 11 support the $I^2C$ (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Product Lineup Comparison 100 Pins**

| | CY91F522F | CY91F523F | CY91F524F | CY91F525F | CY91F526F |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | None | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | 1 ch | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 3 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 6 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 6 ch | | | | |
| 16-bit Reload Timer | 8 ch | | | | |
| PPG | 16 bit × 34 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 21 ch (1 unit), 12 bit × 16 ch (1 unit) | | | | |
| D/A converter (8 bit) | 2 ch | | | | |
| Multi-Function Serial Interface | 12 ch[*1] | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 76 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V[*2] | | | | |
| Package | LQI100 | | | | |

*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Product Lineup Comparison 120 Pins**

| | CY91F522J | CY91F523J | CY91F524J | CY91F525J | CY91F526J |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | None | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | 2 ch | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 3 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 6 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 6 ch | | | | |
| 16-bit Reload Timer | 8 ch | | | | |
| PPG | 16 bit × 38 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 26 ch (1 unit), 12 bit × 16 ch (1 unit) | | | | |
| D/A converter (8 bit) | 2 ch | | | | |
| Multi-Function Serial Interface | 12 ch*1 | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 96 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V *2 | | | | |
| Package | LQM120 | | | | |

*1: Only channel 3 and channel 4 support the $I^2C$ (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the $I^2C$ (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Product Lineup Comparison 144 Pins**

| | CY91F522K | CY91F523K | CY91F524K | CY91F525K | CY91F526K |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | Yes | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | 2 ch | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 3 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 6 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 6 ch | | | | |
| 16-bit Reload Timer | 8 ch | | | | |
| PPG | 16 bit × 44 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit) | | | | |
| D/A converter (8 bit) | 2 ch | | | | |
| Multi-Function Serial Interface | 12 ch[*1] | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 120 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V [*2] | | | | |
| Package | LQS144, LQN144 | | | | |

*1: Only channel 3 and channel 4 support the $I^2C$ (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the $I^2C$ (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Product Lineup Comparison 176 Pins**

| | CY91F522L | CY91F523L | CY91F524L | CY91F525L | CY91F526L |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5 ns (80 MHz) | | | | |
| Flash Capacity (Program) | (256+64) KB | (384+64) KB | (512+64) KB | (768+64) KB | (1024+64) KB |
| Flash Capacity (Data) | 64 KB | | | | |
| RAM Capacity | (48+8) KB | | (64+8) KB | (96+8) KB | (128+8) KB |
| External BUS I/F (22 address/16 data/4 cs) | Yes | | | | |
| DMA Transfer | 16 ch | | | | |
| 16-bit Base Timer | 2 ch | | | | |
| Free-run Timer | 16 bit × 3 ch, 32 bit × 3 ch | | | | |
| Input capture | 16 bit × 4 ch, 32 bit × 6 ch | | | | |
| Output Compare | 16 bit × 6 ch, 32 bit × 6 ch | | | | |
| 16-bit Reload Timer | 8 ch | | | | |
| PPG | 16 bit × 48 ch | | | | |
| Up/down Counter | 2 ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8 ch × 2 units | | | | |
| A/D converter | 12 bit × 32 ch (1 unit), 12 bit × 16 ch (1 unit) | | | | |
| D/A converter (8 bit) | 2 ch | | | | |
| Multi-Function Serial Interface | 12 ch*1 | | | | |
| CAN | 64 msg × 2 ch/128 msg × 1 ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 152 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| NMI request function | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6 ch | | | | |
| Operation guaranteed temperature ($T_A$) | -40 °C to +125 °C | | | | |
| Power supply | 2.7 V to 5.5 V *2 | | | | |
| Package | LQP176 | | | | |

*1: Only channel 3 and channel 4 support the $I^2C$ (fast mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the $I^2C$ (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Table for Clock Supervisor and External Low Voltage Detection Reset Initial Value ON/OFF**

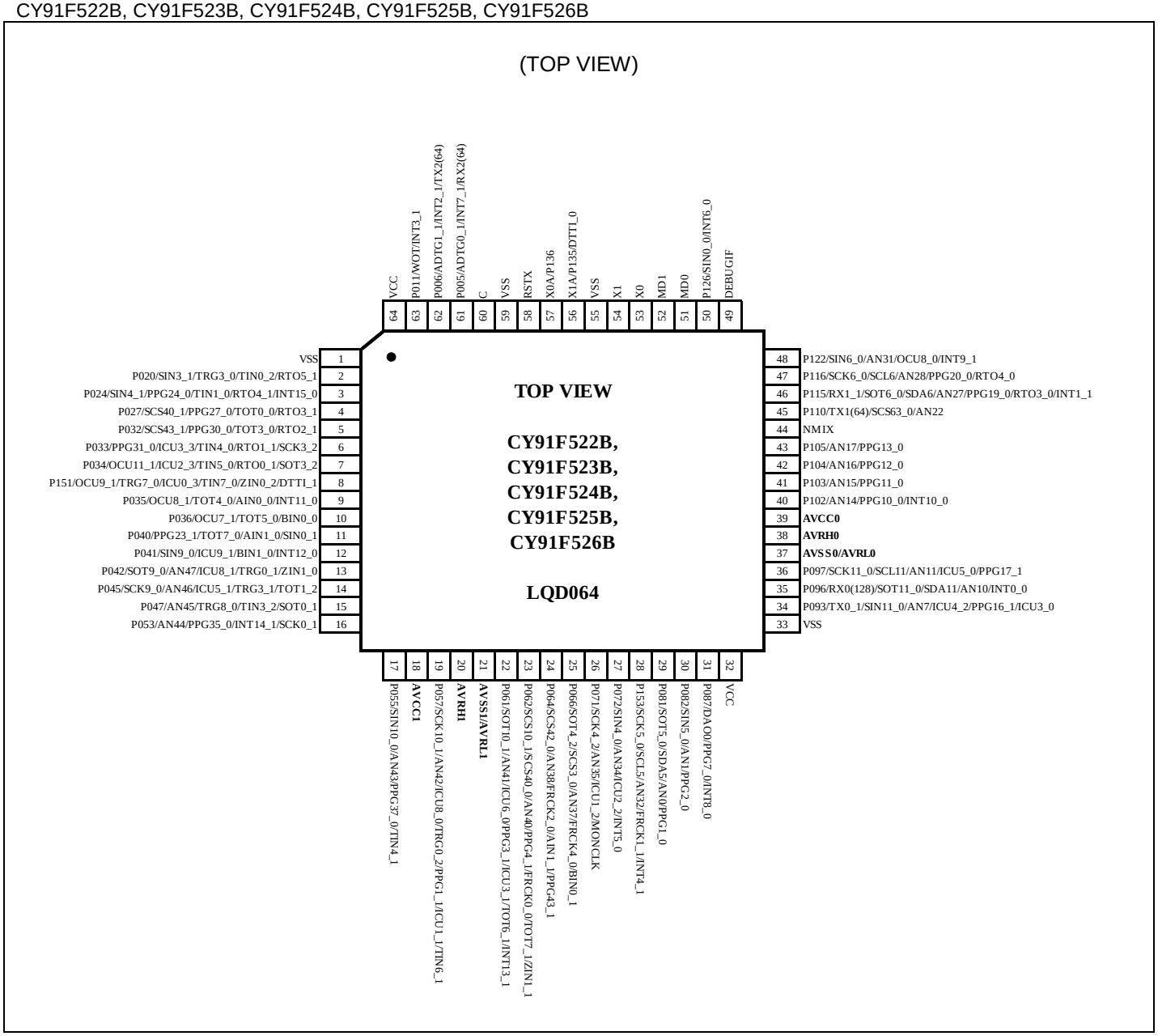
| Clock | CSV Initial Value | LVD Initial Value | Function |
|---|---|---|---|
| single | ON | ON | S |
| | | OFF | U |
| | OFF | ON | H |
| | | OFF | K |
| Dual | ON | ON | W |
| | | OFF | Y |
| | OFF | ON | J |
| | | OFF | L |

```
ＣＹ９１Ｆ５２Ｘ□△○
          ｜｜｜└→Ｒｅｖｉｓｉｏｎ：Ｂ, Ｃ, Ｄ, Ｅ
          ｜｜└──→Ｆｕｎｃｔｉｏｎ：See the table for clock supervisor and external
          ｜｜                      low voltage detection reset initial value ON/OFF.
          ｜└────→ＰＫＧ Ｔｙｐｅ：Ｂ ６４ｐｉｎ
          ｜                      Ｄ ８０ ｐｉｎ
          ｜                      Ｆ １００ ｐｉｎ
          ｜                      Ｊ １２０ ｐｉｎ
          ｜                      Ｋ １４４ ｐｉｎ
          ｜                      Ｌ １７６ ｐｉｎ
          └──────→Ｍｅｍｏｒｙ Ｓｉｚｅ：２ ２５６ＫＢ
                                  ３ ３８４ＫＢ
                                  ４ ５１２ＫＢ
                                  ５ ７６８ＫＢ
                                  ６ １ＭＢ
```

## 2. Pin Assignment

**CY91F52xB**

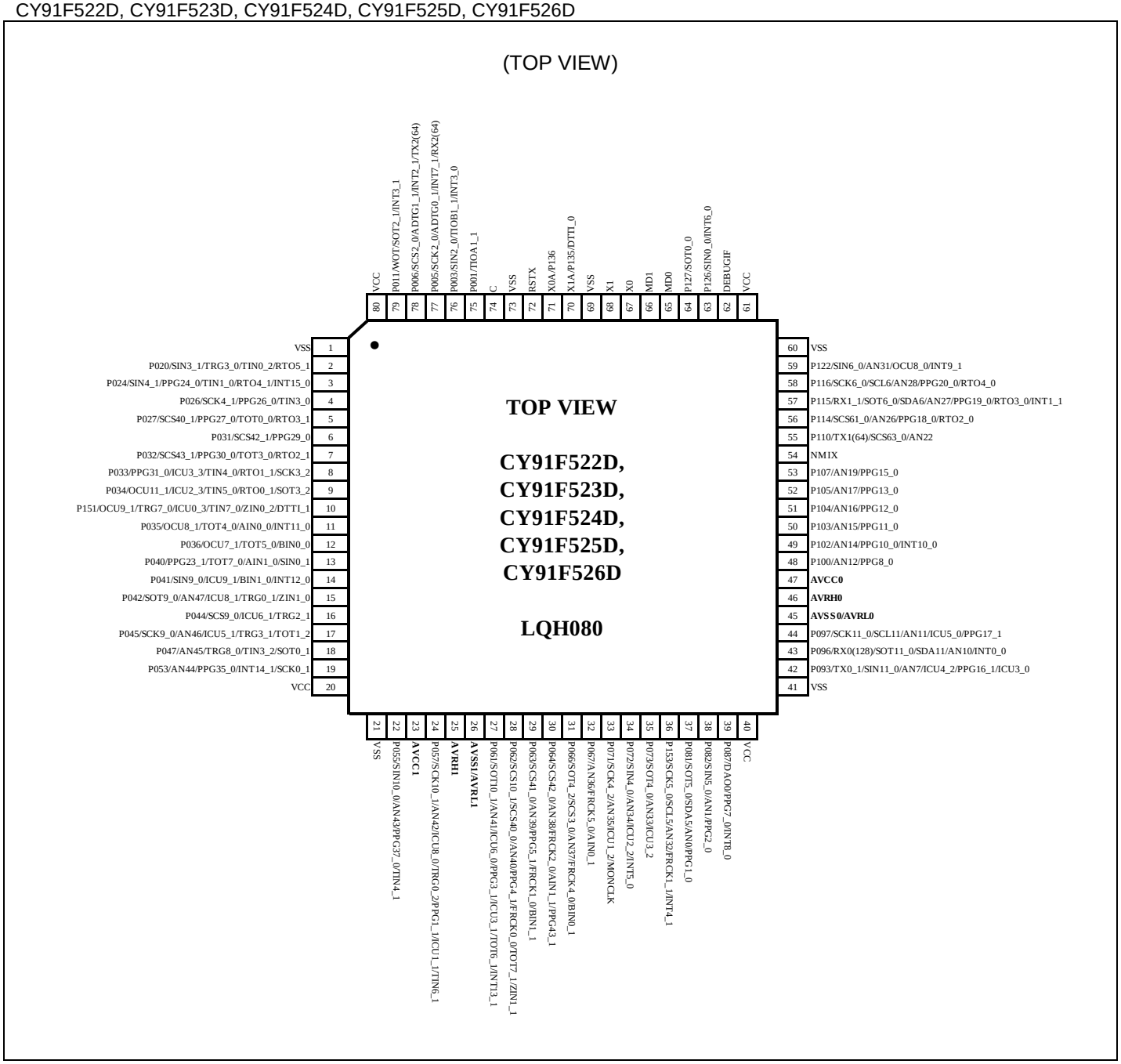
CY91F522B, CY91F523B, CY91F524B, CY91F525B, CY91F526B




* In a single clock product, pin 56 and pin 57 are the general-purpose ports.

**CY91F52xD**

CY91F522D, CY91F523D, CY91F524D, CY91F525D, CY91F526D

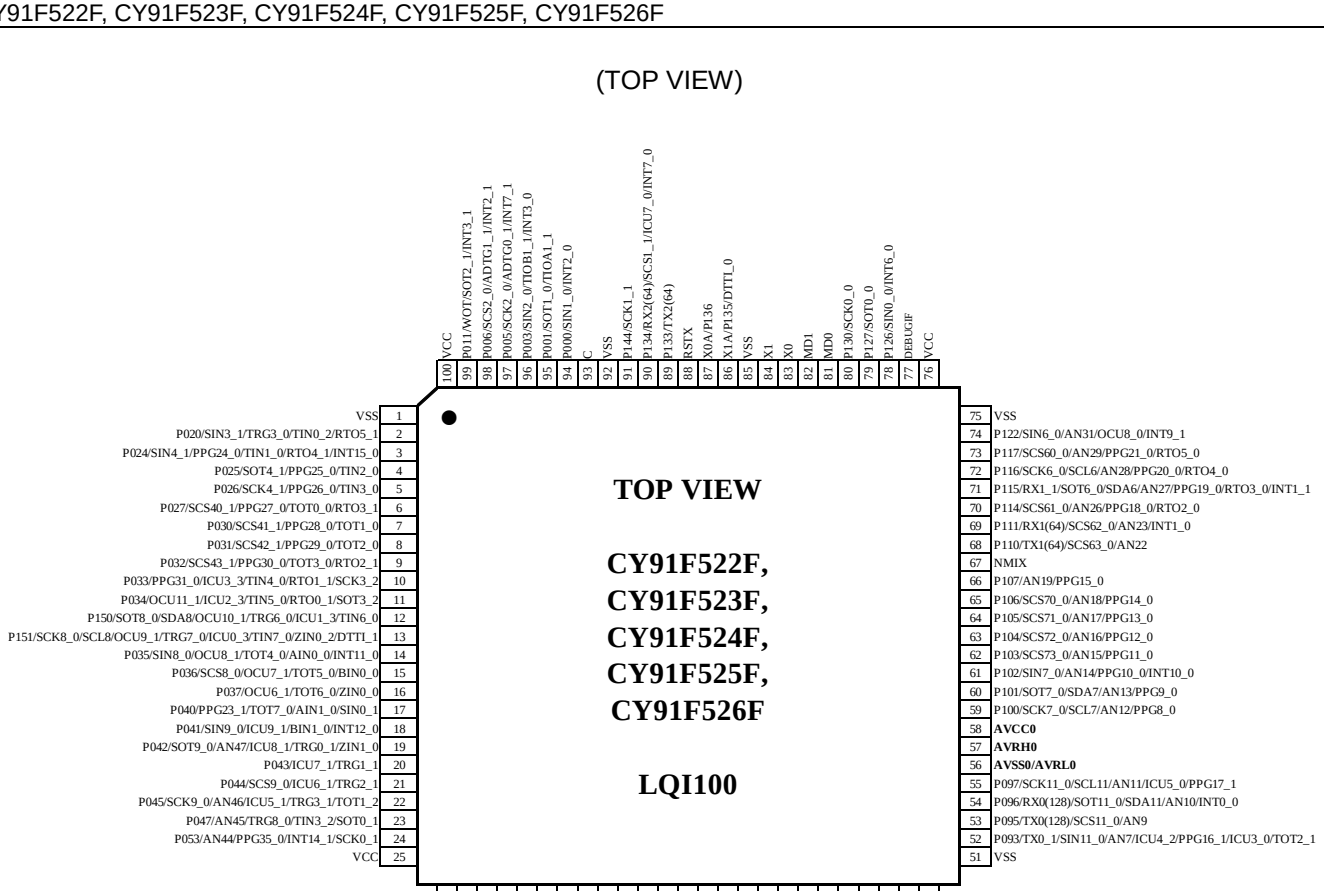



* In a single clock product, pin 70 and pin 71 are the general-purpose ports.

**CY91F52xF**

CY91F522F, CY91F523F, CY91F524F, CY91F525F, CY91F526F

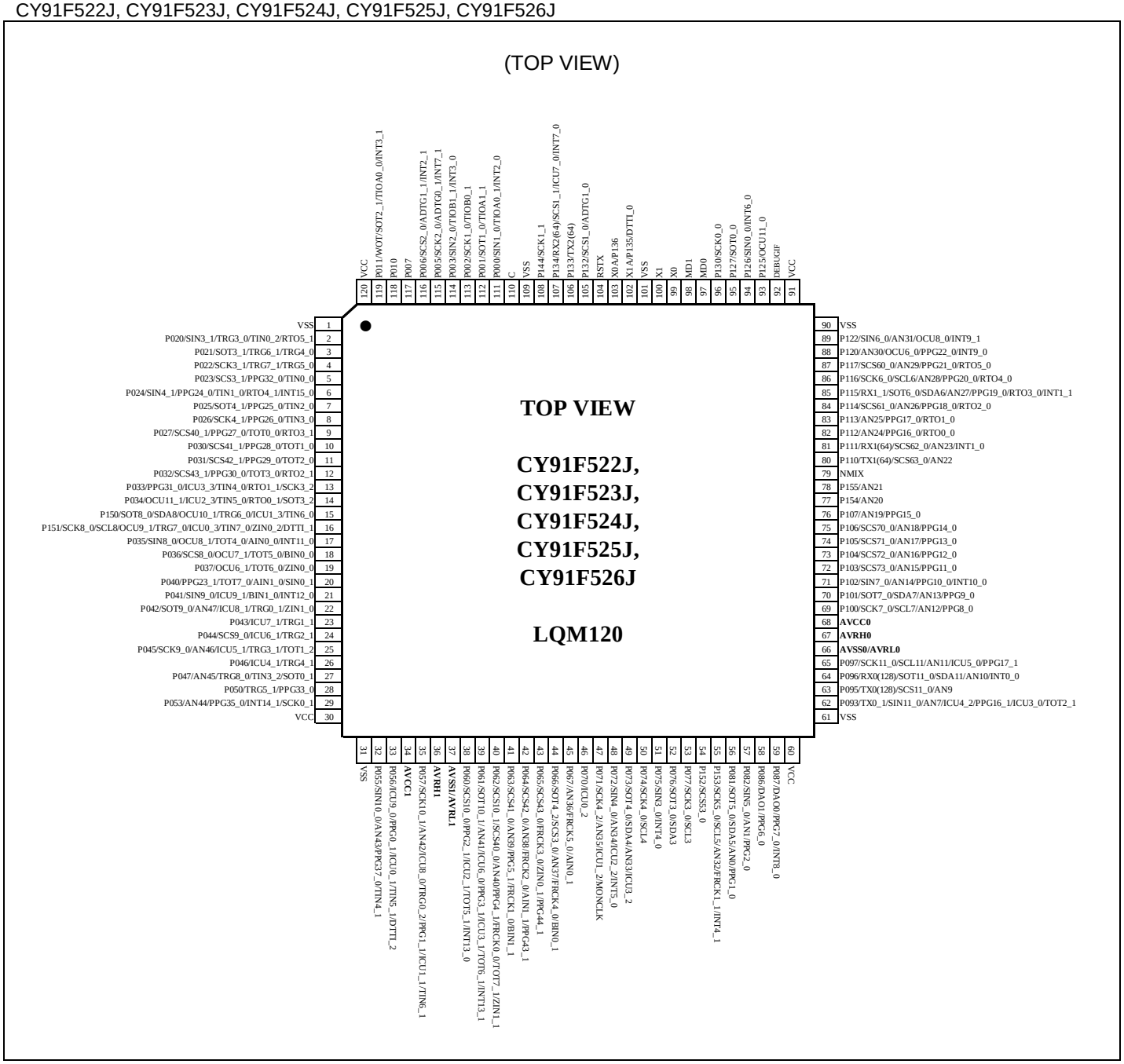
(TOP VIEW)




* In a single clock product, pin 86 and pin 87 are the general-purpose ports.

**CY91F52xJ**

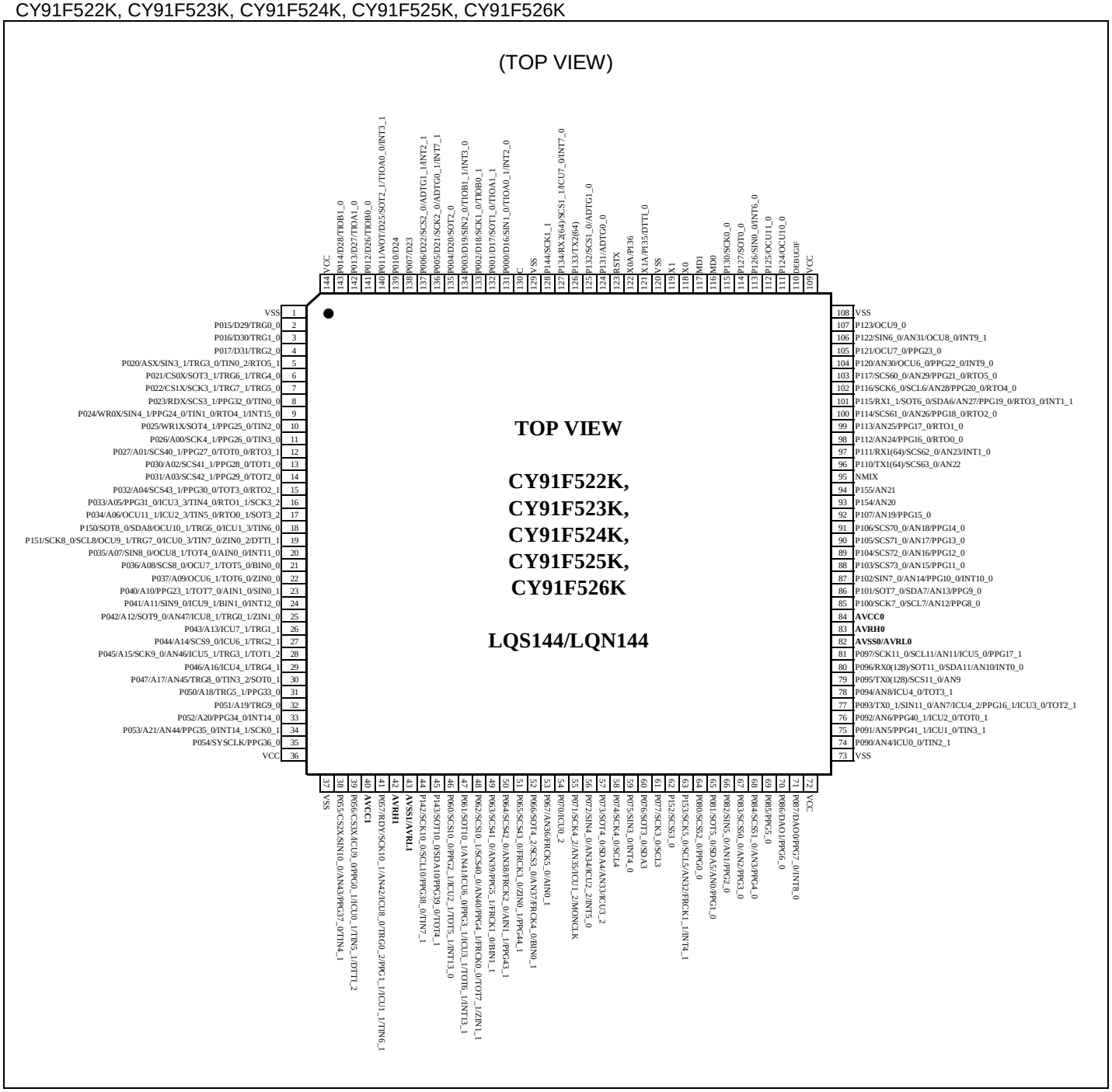
CY91F522J, CY91F523J, CY91F524J, CY91F525J, CY91F526J




* In a single clock product, pin 102 and pin 103 are the general-purpose ports.

**CY91F52xK**

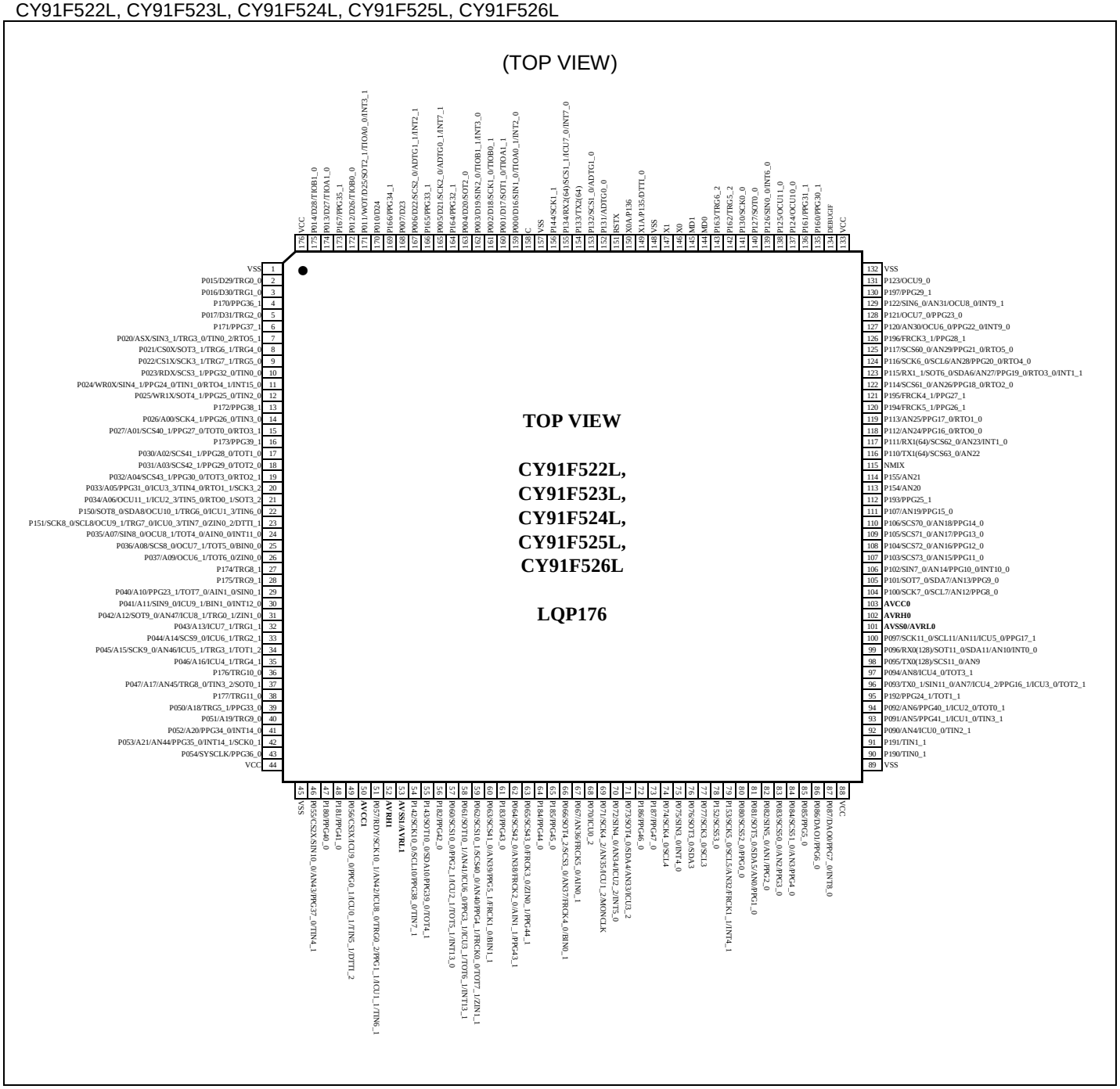
CY91F522K, CY91F523K, CY91F524K, CY91F525K, CY91F526K




* In a single clock product, pin 121 and pin 122 are the general-purpose ports.

**CY91F52xL**

CY91F522L, CY91F523L, CY91F524L, CY91F525L, CY91F526L




* In a single clock product, pin 149 and pin 150 are the general-purpose ports.

## 3. Pin Description

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 2 | 2 | P015 | - | A | General-purpose I/O port |
| | | | | | | D29 | - | | External bus data bit29 I/O (0) |
| | | | | | | TRG0_0 | - | | PPG trigger 0 input (0) |
| - | - | - | - | 3 | 3 | P016 | - | A | General-purpose I/O port |
| | | | | | | D30 | - | | External bus data bit30 I/O (0) |
| | | | | | | TRG1_0 | - | | PPG trigger 1 input (0) |
| - | - | - | - | - | 4 | P170 | - | A | General-purpose I/O port |
| | | | | | | PPG36_1 | - | | PPG ch.36 output (1) |
| - | - | - | - | 4 | 5 | P017 | - | A | General-purpose I/O port |
| | | | | | | D31 | - | | External bus data bit31 I/O (0) |
| | | | | | | TRG2_0 | - | | PPG trigger 2 input (0) |
| - | - | - | - | - | 6 | P171 | - | A | General-purpose I/O port |
| | | | | | | PPG37_1 | - | | PPG ch.37 output (1) |
| 2 *1 | 2 *1 | 2 *1 | 2 *1 | 5 | 7 | P020 | - | F | General-purpose I/O port |
| | | | | | | ASX *2, *3, *4, *5 | - | | External bus/Address strobe output |
| | | | | | | SIN3_1 | - | | Multi-function serial ch.3 serial data input (1) |
| | | | | | | TRG3_0 | - | | PPG trigger 3 input (0) |
| | | | | | | TIN0_2 | - | | Reload timer ch.0 event input (2) |
| | | | | | | RTO5_1 | - | | Waveform generator ch.5 output pin (1) |
| - | - | - | 3 *1 | 6 | 8 | P021 | - | A | General-purpose I/O port |
| | | | | | | CS0X *5 | - | | External bus chip select 0 output |
| | | | | | | SOT3_1 | - | | Multi-function serial ch.3 serial data output (1) |
| | | | | | | TRG6_1 | - | | PPG trigger 6 input (1) |
| | | | | | | TRG4_0 | - | | PPG trigger 4 input (0) |
| - | - | - | 4 *1 | 7 | 9 | P022 | - | F | General-purpose I/O port |
| | | | | | | CS1X *5 | - | | External bus chip select 1 output |
| | | | | | | SCK3_1 | - | | Multi-function serial ch.3 clock I/O (1) |
| | | | | | | TRG7_1 | - | | PPG trigger 7 input (1) |
| | | | | | | TRG5_0 | - | | PPG trigger 5 input (0) |
| - | - | - | 5 *1 | 8 | 10 | P023 | - | A | General-purpose I/O port |
| | | | | | | RDX *5 | - | | External bus/Read strobe output |
| | | | | | | SCS3_1 | - | | Serial chip select 3 output (1) |
| | | | | | | PPG32_0 | - | | PPG ch.32 output (0) |
| | | | | | | TIN0_0 | - | | Reload timer ch.0 event input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 3 *1 | 3 *1 | 3 *1 | 6 *1 | 9 | 11 | P024 | - | F | General-purpose I/O port |
| | | | | | | WR0X *2, *3, *4, *5 | - | | External bus/Write strobe 0 output |
| | | | | | | SIN4_1 | - | | Multi-function serial ch.4 serial data input (1) |
| | | | | | | PPG24_0 | - | | PPG ch.24 output (0) |
| | | | | | | TIN1_0 | - | | Reload timer ch.1 event input (0) |
| | | | | | | RTO4_1 | - | | Waveform generator ch.4 output pin (1) |
| | | | | | | INT15_0 | - | | INT15 External interrupt input (0) |
| - | - | 4 *1 | 7 *1 | 10 | 12 | P025 | - | A | General-purpose I/O port |
| | | | | | | WR1X *4, *5 | - | | External bus/Write strobe 1 output |
| | | | | | | SOT4_1 | - | | Multi-function serial ch.4 serial data output (1) |
| | | | | | | PPG25_0 | - | | PPG ch.25 output (0) |
| | | | | | | TIN2_0 | - | | Reload timer ch.2 event input (0) |
| - | - | - | - | - | 13 | P172 | - | A | General-purpose I/O port |
| | | | | | | PPG38_1 | - | | PPG ch.38 output (1) |
| - | 4 *1 | 5 *1 | 8 *1 | 11 | 14 | P026 | - | F | General-purpose I/O port |
| | | | | | | A00 *3, *4, *5 | - | | External bus/Address bit0 output (0) |
| | | | | | | SCK4_1 | - | | Multi-function serial ch.4 clock I/O (1) |
| | | | | | | PPG26_0 | - | | PPG ch.26 output (0) |
| | | | | | | TIN3_0 | - | | Reload timer ch.3 event input (0) |
| 4 *1 | 5 *1 | 6 *1 | 9 *1 | 12 | 15 | P027 | - | A | General-purpose I/O port |
| | | | | | | A01 *2, *3, *4, *5 | - | | External bus/Address bit1 output (0) |
| | | | | | | SCS40_1 | - | | Serial chip select 40 I/O (1) |
| | | | | | | PPG27_0 | - | | PPG ch.27 output (0) |
| | | | | | | TOT0_0 | - | | Reload timer ch.0 output (0) |
| | | | | | | RTO3_1 | - | | Waveform generator ch.3 output pin (1) |
| - | - | - | - | - | 16 | P173 | - | A | General-purpose I/O port |
| | | | | | | PPG39_1 | - | | PPG ch.39 output (1) |
| - | - | 7 *1 | 10 *1 | 13 | 17 | P030 | - | A | General-purpose I/O port |
| | | | | | | A02 *4, *5 | - | | External bus/Address bit2 output (0) |
| | | | | | | SCS41_1 | - | | Serial chip select 41 output (1) |
| | | | | | | PPG28_0 | - | | PPG ch.28 output (0) |
| | | | | | | TOT1_0 | - | | Reload timer ch.1 output (0) |
| - | 6 *1 | 8 *1 | 11 *1 | 14 | 18 | P031 | - | A | General-purpose I/O port |
| | | | | | | A03 *3, *4, *5 | - | | External bus/Address bit3 output (0) |
| | | | | | | SCS42_1 | - | | Serial chip select 42 output (1) |
| | | | | | | PPG29_0 | - | | PPG ch.29 output (0) |
| | | | | | | TOT2_0 *3 | - | | Reload timer ch.2 output (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 5 *1 | 7 *1 | 9 *1 | 12 *1 | 15 | 19 | P032 | - | A | General-purpose I/O port |
| | | | | | | A04 *2, *3, *4, *5 | - | | External bus/Address bit4 output (0) |
| | | | | | | SCS43_1 | - | | Serial chip select 43 output (1) |
| | | | | | | PPG30_0 | - | | PPG ch.30 output (0) |
| | | | | | | TOT3_0 | - | | Reload timer ch.3 output (0) |
| | | | | | | RTO2_1 | - | | Waveform generator ch.2 output pin (1) |
| 6 *1 | 8 *1 | 10 *1 | 13 *1 | 16 | 20 | P033 | - | A | General-purpose I/O port |
| | | | | | | A05 *2, *3, *4, *5 | - | | External bus/Address bit5 output (0) |
| | | | | | | PPG31_0 | - | | PPG ch.31 output (0) |
| | | | | | | ICU3_3 | - | | Input capture ch.3 input (3) |
| | | | | | | TIN4_0 | - | | Reload timer ch.4 event input (0) |
| | | | | | | RTO1_1 | - | | Waveform generator ch.1 output pin (1) |
| | | | | | | SCK3_2 | - | | Multi-function serial ch.3 clock I/O (2) |
| 7 *1 | 9 *1 | 11 *1 | 14 *1 | 17 | 21 | P034 | - | A | General-purpose I/O port |
| | | | | | | A06 *2, *3, *4, *5 | - | | External bus/Address bit6 output (0) |
| | | | | | | OCU11_1 | - | | Output compare ch.11 output (1) |
| | | | | | | ICU2_3 | - | | Input capture ch.2 input (3) |
| | | | | | | TIN5_0 | - | | Reload timer ch.5 event input (0) |
| | | | | | | RTO0_1 | - | | Waveform generator ch.0 output pin (1) |
| | | | | | | SOT3_2 | - | | Multi-function serial ch.3 serial data output (2) |
| - | - | 12 | 15 | 18 | 22 | P150 | - | F | General-purpose I/O port |
| | | | | | | SOT8_0/ SDA8 | - | | Multi-function serial ch.8 serial data output (0)/ $I^2C$ bus serial data I/O |
| | | | | | | OCU10_1 | - | | Output compare ch.10 output (1) |
| | | | | | | TRG6_0 | - | | PPG trigger 6 input (0) |
| | | | | | | ICU1_3 | - | | Input capture ch.1 input (3) |
| | | | | | | TIN6_0 | - | | Reload timer ch.6 event input (0) |
| 8 *1 | 10 *1 | 13 | 16 | 19 | 23 | P151 | - | F | General-purpose I/O port |
| | | | | | | SCK8_0/ SCL8 *2, *3 | - | | Multi-function serial ch.8 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | OCU9_1 | - | | Output compare ch.9 output (1) |
| | | | | | | TRG7_0 | - | | PPG trigger 7 input (0) |
| | | | | | | ICU0_3 | - | | Input capture ch.0 input (3) |
| | | | | | | TIN7_0 | - | | Reload timer ch.7 event input (0) |
| | | | | | | ZIN0_2 | - | | U/D counter ch.0 ZIN input (2) |
| | | | | | | DTTI_1 | - | | Waveform generator ch.1 input pin (1) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 9 *1 | 11 *1 | 14 *1 | 17 *1 | 20 | 24 | P035 | - | I | General-purpose I/O port |
| | | | | | | A07 *2, *3, *4, *5 | - | | External bus/Address bit7 output |
| | | | | | | SIN8_0 *2, *3 | - | | Multi-function serial ch.8 serial data input (0) |
| | | | | | | OCU8_1 | - | | Output compare ch.8 output (1) |
| | | | | | | TOT4_0 | - | | Reload timer ch.4 output (0) |
| | | | | | | AIN0_0 | - | | U/D counter ch.0 AIN input (0) |
| | | | | | | INT11_0 | - | | INT11 External interrupt input (0) |
| 10 *1 | 12 *1 | 15 *1 | 18 *1 | 21 | 25 | P036 | - | A | General-purpose I/O port |
| | | | | | | A08 *2, *3, *4, *5 | - | | External bus/Address bit8 output (0) |
| | | | | | | SCS8_0 *2, *3 | - | | Serial chip select 8 I/O (0) |
| | | | | | | OCU7_1 | - | | Output compare ch.7 output (1) |
| | | | | | | TOT5_0 | - | | Reload timer ch.5 output (0) |
| | | | | | | BIN0_0 | - | | U/D counter ch.0 BIN input (0) |
| - | - | 16 *1 | 19 *1 | 22 | 26 | P037 | - | A | General-purpose I/O port |
| | | | | | | A09 *4, *5 | - | | External bus/Address bit9 output (0) |
| | | | | | | OCU6_1 | - | | Output compare ch.6 output (1) |
| | | | | | | TOT6_0 | - | | Reload timer ch.6 output (0) |
| | | | | | | ZIN0_0 | - | | U/D counter ch.0 ZIN input (0) |
| - | - | - | - | - | 27 | P174 | - | A | General-purpose I/O port |
| | | | | | | TRG8_1 | - | | PPG trigger 8 input (1) |
| - | - | - | - | - | 28 | P175 | - | A | General-purpose I/O port |
| | | | | | | TRG9_1 | - | | PPG trigger 9 input (1) |
| 11 *1 | 13 *1 | 17 *1 | 20 *1 | 23 | 29 | P040 | - | A | General-purpose I/O port |
| | | | | | | A10 *2, *3, *4, *5 | - | | External bus/Address bit10 output (0) |
| | | | | | | PPG23_1 | - | | PPG ch.23 output (1) |
| | | | | | | TOT7_0 | - | | Reload timer ch.7 output (0) |
| | | | | | | AIN1_0 | - | | U/D counter ch.1 AIN input (0) |
| | | | | | | SIN0_1 | - | | Multi-function serial ch.0 serial data input (1) |
| 12 *1 | 14 *1 | 18 *1 | 21 *1 | 24 | 30 | P041 | - | I | General-purpose I/O port |
| | | | | | | A11 *2, *3, *4, *5 | - | | External bus/Address bit11 output (0) |
| | | | | | | SIN9_0 | - | | Multi-function serial ch.9 serial data input (0) |
| | | | | | | ICU9_1 | - | | Input capture ch.9 input (1) |
| | | | | | | BIN1_0 | - | | U/D counter ch.1 BIN input (0) |
| | | | | | | INT12_0 | - | | INT12 External interrupt input (0) |
| 13 *1 | 15 *1 | 19 *1 | 22 *1 | 25 | 31 | P042 | - | B | General-purpose I/O port |
| | | | | | | A12 *2, *3, *4, *5 | - | | External bus/Address bit12 output |
| | | | | | | SOT9_0 | - | | Multi-function serial ch.9 serial data output (0) |
| | | | | | | AN47 | - | | ADC analog 47 input |
| | | | | | | ICU8_1 | - | | Input capture ch.8 input (1) |
| | | | | | | TRG0_1 | - | | PPG trigger 0 input (1) |
| | | | | | | ZIN1_0 | - | | U/D counter ch.1 ZIN input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | 20 *1 | 23 *1 | 26 | 32 | P043 | - | A | General-purpose I/O port |
| | | | | | | A13 *4, *5 | - | | External bus/Address bit13 output (0) |
| | | | | | | ICU7_1 | - | | Input capture ch.7 input (1) |
| | | | | | | TRG1_1 | - | | PPG trigger 1 input (1) |
| - | 16 *1 | 21 *1 | 24 *1 | 27 | 33 | P044 | - | A | General-purpose I/O port |
| | | | | | | A14 *3, *4, *5 | - | | External bus/Address bit14 output (0) |
| | | | | | | SCS9_0 | - | | Serial chip select 9 I/O (0) |
| | | | | | | ICU6_1 | - | | Input capture ch.6 input (1) |
| | | | | | | TRG2_1 | - | | PPG trigger 2 input (1) |
| 14 *1 | 17 *1 | 22 *1 | 25 *1 | 28 | 34 | P045 | - | G | General-purpose I/O port |
| | | | | | | A15 *2, *3, *4, *5 | - | | External bus/Address bit15 output (0) |
| | | | | | | SCK9_0 | - | | Multi-function serial ch.9 clock I/O (0) |
| | | | | | | AN46 | - | | ADC analog 46 input |
| | | | | | | ICU5_1 | - | | Input capture ch.5 input (1) |
| | | | | | | TRG3_1 | - | | PPG trigger 3 input (1) |
| | | | | | | TOT1_2 | - | | Reload timer ch.1 output (2) |
| - | - | - | 26 *1 | 29 | 35 | P046 | - | A | General-purpose I/O port |
| | | | | | | A16 *5 | - | | External bus/Address bit16 output (0) |
| | | | | | | ICU4_1 | - | | Input capture ch.4 input (1) |
| | | | | | | TRG4_1 | - | | PPG trigger 4 input (1) |
| - | - | - | - | - | 36 | P176 | - | A | General-purpose I/O port |
| | | | | | | TRG10_0 | - | | PPG trigger 10 input (0) |
| 15 *1 | 18 *1 | 23 *1 | 27 *1 | 30 | 37 | P047 | - | B | General-purpose I/O port |
| | | | | | | A17 *2, *3, *4, *5 | - | | External bus/Address bit17 output (0) |
| | | | | | | AN45 | - | | ADC analog 45 input |
| | | | | | | TRG8_0 | - | | PPG trigger 8 input (0) |
| | | | | | | TIN3_2 | - | | Reload timer ch.3 event input (2) |
| | | | | | | SOT0_1 | - | | Multi-function serial ch.0 serial data output (1) |
| - | - | - | - | - | 38 | P177 | - | A | General-purpose I/O port |
| | | | | | | TRG11_0 | - | | PPG trigger 11 input (0) |
| - | - | - | 28 *1 | 31 | 39 | P050 | - | A | General-purpose I/O port |
| | | | | | | A18 *5 | - | | External bus/Address bit18 output |
| | | | | | | TRG5_1 | - | | PPG trigger 5 input (1) |
| | | | | | | PPG33_0 | - | | PPG ch.33 output (0) |
| - | - | - | - | 32 | 40 | P051 | - | A | General-purpose I/O port |
| | | | | | | A19 | - | | External bus/Address bit19 output |
| | | | | | | TRG9_0 | - | | PPG trigger 9 input (0) |
| - | - | - | - | 33 | 41 | P052 | - | A | General-purpose I/O port |
| | | | | | | A20 | - | | External bus/Address bit20 output |
| | | | | | | PPG34_0 | - | | PPG ch.34 output (0) |
| | | | | | | INT14_0 | - | | INT14 External interrupt input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 16 *1 | 19 *1 | 24 *1 | 29 *1 | 34 | 42 | P053 | - | B | General-purpose I/O port |
| | | | | | | A21 *2, *3, *4, *5 | - | | External bus/Address bit21 output |
| | | | | | | AN44 | - | | ADC analog 44 input |
| | | | | | | PPG35_0 | - | | PPG ch.35 output (0) |
| | | | | | | INT14_1 | - | | INT14 External interrupt input (1) |
| | | | | | | SCK0_1 | - | | Multi-function serial ch.0 clock I/O (1) |
| - | - | - | - | 35 | 43 | P054 | - | A | General-purpose I/O port |
| | | | | | | SYSCLK | - | | External bus/System clock output |
| | | | | | | PPG36_0 | - | | PPG ch.36 output (0) |
| 17 *1 | 22 *1 | 27 *1 | 32 *1 | 38 | 46 | P055 | - | G | General-purpose I/O port |
| | | | | | | CS2X *2, *3, *4, *5 | - | | External bus chip select 2 output |
| | | | | | | SIN10_0 | - | | Multi-function serial ch.10 serial data input (0) |
| | | | | | | AN43 | - | | ADC analog 43 input |
| | | | | | | PPG37_0 | - | | PPG ch.37 output (0) |
| | | | | | | TIN4_1 | - | | Reload timer ch.4 event input (1) |
| - | - | - | - | - | 47 | P180 | - | A | General-purpose I/O port |
| | | | | | | PPG40_0 | - | | PPG ch.40 output (0) |
| - | - | - | - | - | 48 | P181 | - | A | General-purpose I/O port |
| | | | | | | PPG41_0 | - | | PPG ch.41 output (0) |
| - | - | - | 33 *1 | 39 | 49 | P056 | - | A | General-purpose I/O port |
| | | | | | | CS3X *5 | - | | External bus chip select 3 output |
| | | | | | | ICU9_0 | - | | Input capture ch.9 input (0) |
| | | | | | | PPG0_1 | - | | PPG ch.0 output (1) |
| | | | | | | ICU0_1 | - | | Input capture ch.0 input (1) |
| | | | | | | TIN5_1 | - | | Reload timer ch.5 event input (1) |
| | | | | | | DTTI_2 | - | | Waveform generator ch.0-ch.5 input pin (2) |
| 19 *1 | 24 *1 | 29 *1 | 35 *1 | 41 | 51 | P057 | - | G | General-purpose I/O port |
| | | | | | | RDY *2, *3, *4, *5 | - | | External bus/Ready input (0) |
| | | | | | | SCK10_1 | - | | Multi-function serial ch.10 clock I/O (1) |
| | | | | | | AN42 | - | | ADC analog 42 input |
| | | | | | | ICU8_0 | - | | Input capture ch.8 input (0) |
| | | | | | | TRG0_2 | - | | PPG trigger 0 input (2) |
| | | | | | | PPG1_1 | - | | PPG ch.1 output (1) |
| | | | | | | ICU1_1 | - | | Input capture ch.1 input (1) |
| | | | | | | TIN6_1 | - | | Reload timer ch.6 event input (1) |
| - | - | - | - | 44 | 54 | P142 | - | F | General-purpose I/O port |
| | | | | | | SCK10_0/ SCL10 | - | | Multi-function serial ch.10 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | PPG38_0 | - | | PPG ch.38 output (0) |
| | | | | | | TIN7_1 | - | | Reload timer ch.7 event input (1) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 45 | 55 | P143 | - | F | General-purpose I/O port |
| | | | | | | SOT10_0/SDA10 | - | | Multi-function serial ch.10 serial data output (0)/ I2C bus serial data I/O |
| | | | | | | PPG39_0 | - | | PPG ch.39 output (0) |
| | | | | | | TOT4_1 | - | | Reload timer ch.4 output (1) |
| - | - | - | - | - | 56 | P182 | - | A | General-purpose I/O port |
| | | | | | | PPG42_0 | - | | PPG ch.42 output (0) |
| - | - | 32 | 38 | 46 | 57 | P060 | - | A | General-purpose I/O port |
| | | | | | | SCS10_0 | - | | Serial chip select 10 I/O (0) |
| | | | | | | PPG2_1 | - | | PPG ch.2 output (1) |
| | | | | | | ICU2_1 | - | | Input capture ch.2 input (1) |
| | | | | | | TOT5_1 | - | | Reload timer ch.5 output (1) |
| | | | | | | INT13_0 | - | | INT13 External interrupt input (0) |
| 22 | 27 | 33 | 39 | 47 | 58 | P061 | - | B | General-purpose I/O port |
| | | | | | | SOT10_1 | - | | Multi-function serial ch.10 serial data output (1) |
| | | | | | | AN41 | - | | ADC analog 41 input |
| | | | | | | ICU6_0 | - | | Input capture ch.6 input (0) |
| | | | | | | PPG3_1 | - | | PPG ch.3 output (1) |
| | | | | | | ICU3_1 | - | | Input capture ch.3 input (1) |
| | | | | | | TOT6_1 | - | | Reload timer ch.6 output (1) |
| | | | | | | INT13_1 | - | | INT13 External interrupt input (1) |
| 23 | 28 | 34 | 40 | 48 | 59 | P062 | - | B | General-purpose I/O port |
| | | | | | | SCS10_1 | - | | Serial chip select 10 I/O (1) |
| | | | | | | SCS40_0 | - | | Serial chip select 40 I/O (0) |
| | | | | | | AN40 | - | | ADC analog 40 input |
| | | | | | | PPG4_1 | - | | PPG ch.4 output (1) |
| | | | | | | FRCK0_0 | - | | Free-run timer 0 clock input (0) |
| | | | | | | TOT7_1 | - | | Reload timer ch.7 output (1) |
| | | | | | | ZIN1_1 | - | | U/D counter ch.1 ZIN input (1) |
| - | 29 | 35 | 41 | 49 | 60 | P063 | - | B | General-purpose I/O port |
| | | | | | | SCS41_0 | - | | Serial chip select 41 output (0) |
| | | | | | | AN39 | - | | ADC analog 39 input |
| | | | | | | PPG5_1 | - | | PPG ch.5 output (1) |
| | | | | | | FRCK1_0 | - | | Free-run timer 1 clock input (0) |
| | | | | | | BIN1_1 | - | | U/D counter ch.1 BIN input (1) |
| - | - | - | - | - | 61 | P183 | - | A | General-purpose I/O port |
| | | | | | | PPG43_0 | - | | PPG ch.43 output (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 24 | 30 | 36 | 42 | 50 | 62 | P064 | - | B | General-purpose I/O port |
| | | | | | | SCS42_0 | - | | Serial chip select 42 output (0) |
| | | | | | | AN38 | - | | ADC analog 38 input |
| | | | | | | FRCK2_0 | - | | Free-run timer 2 clock input (0) |
| | | | | | | AIN1_1 | - | | U/D counter ch.1 AIN input (1) |
| | | | | | | PPG43_1 | - | | PPG ch.43 output (1) |
| - | - | 37 | 43 | 51 | 63 | P065 | - | A | General-purpose I/O port |
| | | | | | | SCS43_0 | - | | Serial chip select 43 output (0) |
| | | | | | | FRCK3_0 | - | | Free-run timer 3 clock input (0) |
| | | | | | | ZIN0_1 | - | | U/D counter ch.0 ZIN input (1) |
| | | | | | | PPG44_1 | - | | PPG ch.44 output (1) |
| - | - | - | - | - | 64 | P184 | - | A | General-purpose I/O port |
| | | | | | | PPG44_0 | - | | PPG ch.44 output (0) |
| - | - | - | - | - | 65 | P185 | - | A | General-purpose I/O port |
| | | | | | | PPG45_0 | - | | PPG ch.45 output (0) |
| 25 | 31 | 38 | 44 | 52 | 66 | P066 | - | B | General-purpose I/O port |
| | | | | | | SOT4_2 | - | | Multi-function serial ch.4 serial data output (2) |
| | | | | | | SCS3_0 | - | | Serial chip select 3 I/O (0) |
| | | | | | | AN37 | - | | ADC analog 37 input |
| | | | | | | FRCK4_0 | - | | Free-run timer 4 clock input (0) |
| | | | | | | BIN0_1 | - | | U/D counter ch.0 BIN input (1) |
| - | 32 | 39 | 45 | 53 | 67 | P067 | - | B | General-purpose I/O port |
| | | | | | | AN36 | - | | ADC analog 36 input |
| | | | | | | FRCK5_0 | - | | Free-run timer 5 clock input (0) |
| | | | | | | AIN0_1 | - | | U/D counter ch.0 AIN input (1) |
| - | - | 40 | 46 | 54 | 68 | P070 | - | A | General-purpose I/O port |
| | | | | | | ICU0_2 | - | | Input capture ch.0 input (2) |
| 26 | 33 | 41 | 47 | 55 | 69 | P071 | - | G | General-purpose I/O port |
| | | | | | | SCK4_2 | - | | Multi-function serial ch.4 clock I/O (2) |
| | | | | | | AN35 | - | | ADC analog 35 input |
| | | | | | | ICU1_2 | - | | Input capture ch.1 input (2) |
| | | | | | | MONCLK | - | | Clock monitor output pin |
| 27 | 34 | 42 | 48 | 56 | 70 | P072 | - | G | General-purpose I/O port |
| | | | | | | SIN4_0 | - | | Multi-function serial ch.4 serial data input (0) |
| | | | | | | AN34 | - | | ADC analog 34 input |
| | | | | | | ICU2_2 | - | | Input capture ch.2 input (2) |
| | | | | | | INT5_0 | - | | INT5 External interrupt input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | 35 *3 | 43 *4 | 49 | 57 | 71 | P073 | - | D | General-purpose I/O port |
| | | | | | | SOT4_0/ SDA4 *3, *4 | - | | Multi-function serial ch.4 serial data output (0)/I²C bus serial data I/O |
| | | | | | | AN33 | - | | ADC analog 33 input |
| | | | | | | ICU3_2 | - | | Input capture ch.3 input (2) |
| - | - | - | - | - | 72 | P186 | - | A | General-purpose I/O port |
| | | | | | | PPG46_0 | - | | PPG ch.46 output (0) |
| - | - | - | - | - | 73 | P187 | - | A | General-purpose I/O port |
| | | | | | | PPG47_0 | - | | PPG ch.47 output (0) |
| - | - | - | 50 | 58 | 74 | P074 | - | E | General-purpose I/O port |
| | | | | | | SCK4_0/ SCL4 | - | | Multi-function serial ch.4 clock I/O (0)/ I²C bus serial clock I/O |
| - | - | - | 51 | 59 | 75 | P075 | - | F | General-purpose I/O port |
| | | | | | | SIN3_0 | - | | Multi-function serial ch.3 serial data input (0) |
| | | | | | | INT4_0 | - | | INT4 External interrupt input (0) |
| - | - | - | 52 | 60 | 76 | P076 | - | E | General-purpose I/O port |
| | | | | | | SOT3_0/ SDA3 | - | | Multi-function serial ch.3 serial data output (0)/I²C bus serial data I/O |
| - | - | - | 53 | 61 | 77 | P077 | - | E | General-purpose I/O port |
| | | | | | | SCK3_0/ SCL3 | - | | Multi-function serial ch.3 clock I/O (0)/ I²C bus serial clock I/O |
| - | - | 44 | 54 | 62 | 78 | P152 | - | A | General-purpose I/O port |
| | | | | | | SCS53_0 | - | | Serial chip select 53 output (0) |
| 28 | 36 | 45 | 55 | 63 | 79 | P153 | - | G | General-purpose I/O port |
| | | | | | | SCK5_0/ SCL5 | - | | Multi-function serial ch.5 clock I/O (0)/ I²C bus serial clock I/O |
| | | | | | | AN32 | - | | ADC analog 32 input |
| | | | | | | FRCK1_1 | - | | Free-run timer 1 clock input (1) |
| | | | | | | INT4_1 | - | | INT4 External interrupt input (1) |
| - | - | - | - | 64 | 80 | P080 | - | A | General-purpose I/O port |
| | | | | | | SCS52_0 | - | | Serial chip select 52 output (0) |
| | | | | | | PPG0_0 | - | | PPG ch.0 output (0) |
| 29 | 37 | 46 | 56 | 65 | 81 | P081 | - | G | General-purpose I/O port |
| | | | | | | SOT5_0/ SDA5 | - | | Multi-function serial ch.5 serial data output (0)/I²C bus serial data I/O |
| | | | | | | AN0 | - | | ADC analog 0 input |
| | | | | | | PPG1_0 | - | | PPG ch.1 output (0) |
| 30 | 38 | 47 | 57 | 66 | 82 | P082 | - | G | General-purpose I/O port |
| | | | | | | SIN5_0 | - | | Multi-function serial ch.5 serial data input (0) |
| | | | | | | AN1 | - | | ADC analog 1 input |
| | | | | | | PPG2_0 | - | | PPG ch.2 output (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 67 | 83 | P083 | - | B | General-purpose I/O port |
| | | | | | | SCS50_0 | - | | Serial chip select 50 I/O (0) |
| | | | | | | AN2 | - | | ADC analog 2 input |
| | | | | | | PPG3_0 | - | | PPG ch.3 output (0) |
| - | - | - | - | 68 | 84 | P084 | - | B | General-purpose I/O port |
| | | | | | | SCS51_0 | - | | Serial chip select 51 output (0) |
| | | | | | | AN3 | - | | ADC analog 3 input |
| | | | | | | PPG4_0 | - | | PPG ch.4 output (0) |
| - | - | - | - | 69 | 85 | P085 | - | A | General-purpose I/O port |
| | | | | | | PPG5_0 | - | | PPG ch.5 output (0) |
| - | - | 48 | 58 | 70 | 86 | P086 | - | C | General-purpose I/O port |
| | | | | | | DAO1 | - | | DAC analog 1 output |
| | | | | | | PPG6_0 | - | | PPG ch.6 output (0) |
| 31 | 39 | 49 | 59 | 71 | 87 | P087 | - | C | General-purpose I/O port |
| | | | | | | DAO0 | - | | DAC analog 0 output |
| | | | | | | PPG7_0 | - | | PPG ch.7 output (0) |
| | | | | | | INT8_0 | - | | INT8 External interrupt input (0) |
| - | - | - | - | - | 90 | P190 | - | A | General-purpose I/O port |
| | | | | | | TIN0_1 | - | | Reload timer ch.0 event input (1) |
| - | - | - | - | - | 91 | P191 | - | A | General-purpose I/O port |
| | | | | | | TIN1_1 | - | | Reload timer ch.1 event input (1) |
| - | - | - | - | 74 | 92 | P090 | - | B | General-purpose I/O port |
| | | | | | | AN4 | - | | ADC analog 4 input |
| | | | | | | ICU0_0 | - | | Input capture ch.0 input (0) |
| | | | | | | TIN2_1 | - | | Reload timer ch.2 event input (1) |
| - | - | - | - | 75 | 93 | P091 | - | B | General-purpose I/O port |
| | | | | | | AN5 | - | | ADC analog 5 input |
| | | | | | | PPG41_1 | - | | PPG ch.41 output (1) |
| | | | | | | ICU1_0 | - | | Input capture ch.1 input (0) |
| | | | | | | TIN3_1 | - | | Reload timer ch.3 event input (1) |
| - | - | - | - | 76 | 94 | P092 | - | B | General-purpose I/O port |
| | | | | | | AN6 | - | | ADC analog 6 input |
| | | | | | | PPG40_1 | - | | PPG ch.40 output (1) |
| | | | | | | ICU2_0 | - | | Input capture ch.2 input (0) |
| | | | | | | TOT0_1 | - | | Reload timer ch.0 output (1) |
| - | - | - | - | - | 95 | P192 | - | A | General-purpose I/O port |
| | | | | | | PPG24_1 | - | | PPG ch.24 output (1) |
| | | | | | | TOT1_1 | - | | Reload timer ch.1 output (1) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 34 *1 | 42 *1 | 52 | 62 | 77 | 96 | P093 | - | J | General-purpose I/O port |
| | | | | | | TX0_1 | - | | CAN transmission data 0 output (1) |
| | | | | | | SIN11_0 | - | | Multi-function serial ch.11 serial data input (0) |
| | | | | | | AN7 | - | | ADC analog 7 input |
| | | | | | | ICU4_2 | - | | Input capture ch.4 input (2) |
| | | | | | | PPG16_1 | - | | PPG ch.16 output (1) |
| | | | | | | ICU3_0 | - | | Input capture ch.3 input (0) |
| | | | | | | TOT2_1 *2, *3 | - | | Reload timer ch.2 output (1) |
| - | - | - | - | 78 | 97 | P094 | - | B | General-purpose I/O port |
| | | | | | | AN8 | - | | ADC analog 8 input |
| | | | | | | ICU4_0 | - | | Input capture ch.4 input (0) |
| | | | | | | TOT3_1 | - | | Reload timer ch.3 output (1) |
| - | - | 53 | 63 | 79 | 98 | P095 | - | B | General-purpose I/O port |
| | | | | | | TX0(128) | - | | CAN transmission data 0 output |
| | | | | | | SCS11_0 | - | | Serial chip select 11 I/O (0) |
| | | | | | | AN9 | - | | ADC analog 9 input |
| 35 | 43 | 54 | 64 | 80 | 99 | P096 | - | G | General-purpose I/O port |
| | | | | | | RX0(128) | - | | CAN reception data 0 input |
| | | | | | | SOT11_0/ SDA11 | - | | Multi-function serial ch.11 serial data output (0)/$I^2C$ bus serial data I/O |
| | | | | | | AN10 | - | | ADC analog 10 input |
| | | | | | | INT0_0 | - | | INT0 External interrupt input (0) |
| 36 | 44 | 55 | 65 | 81 | 100 | P097 | - | G | General-purpose I/O port |
| | | | | | | SCK11_0/ SCL11 | - | | Multi-function serial ch.11 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | AN11 | - | | ADC analog 11 input |
| | | | | | | ICU5_0 | - | | Input capture ch.5 input (0) |
| | | | | | | PPG17_1 | - | | PPG ch.17 output (1) |
| - | 48 *1 | 59 | 69 | 85 | 104 | P100 | - | G | General-purpose I/O port |
| | | | | | | SCK7_0/ SCL7 *3 | - | | Multi-function serial ch.7 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | AN12 | - | | ADC analog 12 input |
| | | | | | | PPG8_0 | - | | PPG ch.8 output (0) |
| - | - | 60 | 70 | 86 | 105 | P101 | - | G | General-purpose I/O port |
| | | | | | | SOT7_0/ SDA7 | - | | Multi-function serial ch.7 serial data output (0)/$I^2C$ bus serial data I/O |
| | | | | | | AN13 | - | | ADC analog 13 input |
| | | | | | | PPG9_0 | - | | PPG ch.9 output (0) |
| 40 *1 | 49 *1 | 61 | 71 | 87 | 106 | P102 | - | G | General-purpose I/O port |
| | | | | | | SIN7_0 *2, *3 | - | | Multi-function serial ch.7 serial data input (0) |
| | | | | | | AN14 | - | | ADC analog 14 input |
| | | | | | | PPG10_0 | - | | PPG ch.10 output (0) |
| | | | | | | INT10_0 | - | | INT10 External interrupt input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 41 *1 | 50 *1 | 62 | 72 | 88 | 107 | P103 | - | H | General-purpose I/O port |
| | | | | | | SCS73_0 *2, *3 | - | | Serial chip select 73 output (0) |
| | | | | | | AN15 | - | | ADC analog 15 input |
| | | | | | | PPG11_0 | - | | PPG ch.11 output (0) |
| 42 *1 | 51 *1 | 63 | 73 | 89 | 108 | P104 | - | H | General-purpose I/O port |
| | | | | | | SCS72_0 *2, *3 | - | | Serial chip select 72 output (0) |
| | | | | | | AN16 | - | | ADC analog 16 input |
| | | | | | | PPG12_0 | - | | PPG ch.12 output (0) |
| 43 *1 | 52 *1 | 64 | 74 | 90 | 109 | P105 | - | H | General-purpose I/O port |
| | | | | | | SCS71_0 *2, *3 | - | | Serial chip select 71 output (0) |
| | | | | | | AN17 | - | | ADC analog 17 input |
| | | | | | | PPG13_0 | - | | PPG ch.13 output (0) |
| - | - | 65 | 75 | 91 | 110 | P106 | - | H | General-purpose I/O port |
| | | | | | | SCS70_0 | - | | Serial chip select 70 I/O (0) |
| | | | | | | AN18 | - | | ADC analog 18 input |
| | | | | | | PPG14_0 | - | | PPG ch.14 output (0) |
| - | 53 | 66 | 76 | 92 | 111 | P107 | - | B | General-purpose I/O port |
| | | | | | | AN19 | - | | ADC analog 19 input |
| | | | | | | PPG15_0 | - | | PPG ch.15 output (0) |
| - | - | - | - | - | 112 | P193 | - | A | General-purpose I/O port |
| | | | | | | PPG25_1 | - | | PPG ch.25 output (1) |
| - | - | - | 77 | 93 | 113 | P154 | - | B | General-purpose I/O port |
| | | | | | | AN20 | - | | ADC analog 20 input |
| - | - | - | 78 | 94 | 114 | P155 | - | B | General-purpose I/O port |
| | | | | | | AN21 | - | | ADC analog 21 input |
| 44 | 54 | 67 | 79 | 95 | 115 | NMIX | N | M | Non-masking interrupt input |
| 45 | 55 | 68 | 80 | 96 | 116 | P110 | - | B | General-purpose I/O port |
| | | | | | | TX1(64) | - | | CAN transmission data 1 output |
| | | | | | | SCS63_0 | - | | Serial chip select 63 output (0) |
| | | | | | | AN22 | - | | ADC analog 22 input |
| - | - | 69 | 81 | 97 | 117 | P111 | - | G | General-purpose I/O port |
| | | | | | | RX1(64) | - | | CAN reception data 1 input |
| | | | | | | SCS62_0 | - | | Serial chip select 62 output (0) |
| | | | | | | AN23 | - | | ADC analog 23 input |
| | | | | | | INT1_0 | - | | INT1 External interrupt input (0) |
| - | - | - | 82 | 98 | 118 | P112 | - | B | General-purpose I/O port |
| | | | | | | AN24 | - | | ADC analog 24 input |
| | | | | | | PPG16_0 | - | | PPG ch.16 output (0) |
| | | | | | | RTO0_0 | - | | Waveform generator ch. 0 output pin (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | 83 | 99 | 119 | P113 | - | B | General-purpose I/O port |
| | | | | | | AN25 | - | | ADC analog 25 input |
| | | | | | | PPG17_0 | - | | PPG ch.17 output (0) |
| | | | | | | RTO1_0 | - | | Waveform generator ch. 1 output pin (0) |
| - | - | - | - | - | 120 | P194 | - | A | General-purpose I/O port |
| | | | | | | FRCK5_1 | - | | Free-run timer 5 clock input (1) |
| | | | | | | PPG26_1 | - | | PPG ch.26 output (1) |
| - | - | - | - | - | 121 | P195 | - | A | General-purpose I/O port |
| | | | | | | FRCK4_1 | - | | Free-run timer 4 clock input (1) |
| | | | | | | PPG27_1 | - | | PPG ch.27 output (1) |
| - | 56 | 70 | 84 | 100 | 122 | P114 | - | B | General-purpose I/O port |
| | | | | | | SCS61_0 | - | | Serial chip select 61 output (0) |
| | | | | | | AN26 | - | | ADC analog 26 input |
| | | | | | | PPG18_0 | - | | PPG ch.18 output (0) |
| | | | | | | RTO2_0 | - | | Waveform generator ch.2 output pin (0) |
| 46 | 57 | 71 | 85 | 101 | 123 | P115 | - | G | General-purpose I/O port |
| | | | | | | RX1_1 | - | | CAN reception data 1 input (1) |
| | | | | | | SOT6_0/ SDA6 | - | | Multi-function serial ch.6 serial data output (0)/$I^2C$ bus serial data I/O |
| | | | | | | AN27 | - | | ADC analog 27 input |
| | | | | | | PPG19_0 | - | | PPG ch.19 output (0) |
| | | | | | | RTO3_0 | - | | Waveform generator ch.3 output pin (0) |
| | | | | | | INT1_1 | - | | INT1 External interrupt input (1) |
| 47 | 58 | 72 | 86 | 102 | 124 | P116 | - | G | General-purpose I/O port |
| | | | | | | SCK6_0/ SCL6 | - | | Multi-function serial ch.6 clock I/O (0)/ $I^2C$ bus serial clock I/O |
| | | | | | | AN28 | - | | ADC analog 28 input |
| | | | | | | PPG20_0 | - | | PPG ch.20 output (0) |
| | | | | | | RTO4_0 | - | | Waveform generator ch.4 output pin (0) |
| - | - | 73 | 87 | 103 | 125 | P117 | - | B | General-purpose I/O port |
| | | | | | | SCS60_0 | - | | Serial chip select 60 I/O (0) |
| | | | | | | AN29 | - | | ADC analog 29 input |
| | | | | | | PPG21_0 | - | | PPG ch.21 output (0) |
| | | | | | | RTO5_0 | - | | Waveform generator ch.5 output pin (0) |
| - | - | - | - | - | 126 | P196 | - | A | General-purpose I/O port |
| | | | | | | FRCK3_1 | - | | Free-run timer 3 clock input (1) |
| | | | | | | PPG28_1 | - | | PPG ch.28 output (1) |
| - | - | - | 88 | 104 | 127 | P120 | - | B | General-purpose I/O port |
| | | | | | | AN30 | - | | ADC analog 30 input |
| | | | | | | OCU6_0 | - | | Output compare ch.6 output (0) |
| | | | | | | PPG22_0 | - | | PPG ch.22 output (0) |
| | | | | | | INT9_0 | - | | INT9 External interrupt input (0) |

| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| - | - | - | - | 105 | 128 | P121 | - | A | General-purpose I/O port |
| | | | | | | OCU7_0 | - | | Output compare ch.7 output (0) |
| | | | | | | PPG23_0 | - | | PPG ch.23 output (0) |
| 48 | 59 | 74 | 89 | 106 | 129 | P122 | - | J | General-purpose I/O port |
| | | | | | | SIN6_0 | - | | Multi-function serial ch.6 serial data input (0) |
| | | | | | | AN31 | - | | ADC analog 31 input |
| | | | | | | OCU8_0 | - | | Output compare ch.8 output (0) |
| | | | | | | INT9_1 | - | | INT9 External interrupt input (1) |
| - | - | - | - | - | 130 | P197 | - | A | General-purpose I/O port |
| | | | | | | PPG29_1 | - | | PPG ch.29 output (1) |
| - | - | - | - | 107 | 131 | P123 | - | A | General-purpose I/O port |
| | | | | | | OCU9_0 | - | | Output compare ch.9 output (0) |
| 49 | 62 | 77 | 92 | 110 | 134 | DEBUGIF | - | L | MDI I/O for debugger (OCD) |
| - | - | - | - | - | 135 | P160 | - | A | General-purpose I/O port |
| | | | | | | PPG30_1 | - | | PPG ch.30 output (1) |
| - | - | - | - | - | 136 | P161 | - | A | General-purpose I/O port |
| | | | | | | PPG31_1 | - | | PPG ch.31 output (1) |
| - | - | - | - | 111 | 137 | P124 | - | A | General-purpose I/O port |
| | | | | | | OCU10_0 | - | | Output compare ch.10 output (0) |
| - | - | - | 93 | 112 | 138 | P125 | - | A | General-purpose I/O port |
| | | | | | | OCU11_0 | - | | Output compare ch.11 output (0) |
| 50 | 63 | 78 | 94 | 113 | 139 | P126 | - | F | General-purpose I/O port |
| | | | | | | SIN0_0 | - | | Multi-function serial ch.0 serial data input (0) |
| | | | | | | INT6_0 | - | | INT6 External interrupt input (0) |
| - | 64 | 79 | 95 | 114 | 140 | P127 | - | A | General-purpose I/O port |
| | | | | | | SOT0_0 | - | | Multi-function serial ch.0 serial data output (0) |
| - | - | 80 | 96 | 115 | 141 | P130 | - | F | General-purpose I/O port |
| | | | | | | SCK0_0 | - | | Multi-function serial ch.0 clock I/O (0) |
| - | - | - | - | - | 142 | P162 | - | A | General-purpose I/O port |
| | | | | | | TRG5_2 | - | | PPG trigger 5 input (2) |
| - | - | - | - | - | 143 | P163 | - | A | General-purpose I/O port |
| | | | | | | TRG6_2 | - | | PPG trigger 6 input (2) |
| 51 | 65 | 81 | 97 | 116 | 144 | MD0 | - | K | Mode pin 0 |
| 52 | 66 | 82 | 98 | 117 | 145 | MD1 | - | K | Mode pin 1 |
| 53 | 67 | 83 | 99 | 118 | 146 | X0 | - | N | Main clock oscillation input |
| 54 | 68 | 84 | 100 | 119 | 147 | X1 | - | N | Main clock oscillation output |
| 56 | 70 | 86 | 102 | 121 | 149 | P135 | - | A | General-purpose I/O port |
| | | | | | | DTTI_0 | - | | Waveform generator ch.0-ch.5 input pin (0) |
| | | | | | | X1A | - | O | Sub clock oscillation output |
| 57 | 71 | 87 | 103 | 122 | 150 | P136 | - | A | General-purpose I/O port |
| | | | | | | X0A | - | O | Sub clock oscillation input |

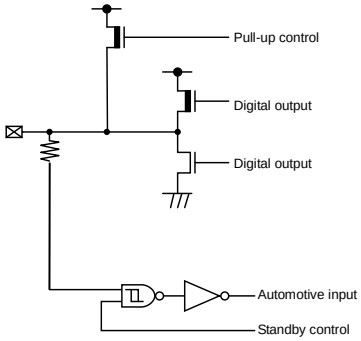
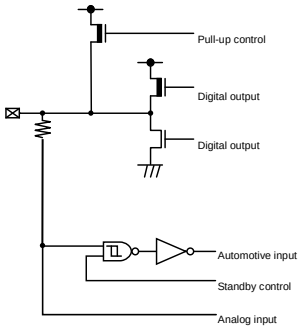
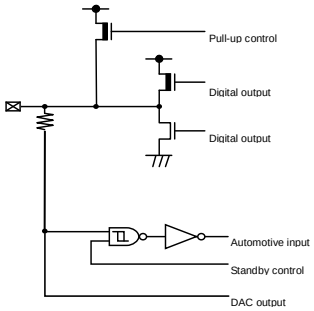
| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 58 | 72 | 88 | 104 | 123 | 151 | RSTX | N | M | External reset input |
| - | - | - | - | 124 | 152 | P131 | - | A | General-purpose I/O port |
| | | | | | | ADTG0_0 | - | | A/D converter external trigger input 0 (0) |
| - | - | - | 105 | 125 | 153 | P132 | - | A | General-purpose I/O port |
| | | | | | | SCS1_0 | - | | Serial chip select 1 I/O (0) |
| | | | | | | ADTG1_0 | - | | A/D converter external trigger input 1 (0) |
| - | - | 89 | 106 | 126 | 154 | P133 | - | A | General-purpose I/O port |
| | | | | | | TX2(64) | - | | CAN transmission data 2 output |
| - | - | 90 | 107 | 127 | 155 | P134 | - | F | General-purpose I/O port |
| | | | | | | RX2(64) | - | | CAN reception data 2 input |
| | | | | | | SCS1_1 | - | | Serial chip select 1 I/O (1) |
| | | | | | | ICU7_0 | - | | Input capture ch.7 input (0) |
| | | | | | | INT7_0 | - | | INT7 External interrupt input (0) |
| - | - | 91 | 108 | 128 | 156 | P144 | - | F | General-purpose I/O port |
| | | | | | | SCK1_1 | - | | Multi-function serial ch.1 clock I/O (1) |
| - | - | 94 *1 | 111 *1 | 131 | 159 | P000 | - | F | General-purpose I/O port |
| | | | | | | D16 *4, *5 | - | | External bus data bit16 I/O (0) |
| | | | | | | SIN1_0 | - | | Multi-function serial ch.1 serial data input (0) |
| | | | | | | TIOA0_1 *4 | - | | TIOA output of Base timer ch.0 (1) |
| | | | | | | INT2_0 | - | | INT2 External interrupt input (0) |
| - | 75 *1 | 95 *1 | 112 *1 | 132 | 160 | P001 | - | A | General-purpose I/O port |
| | | | | | | D17 *3, *4, *5 | - | | External bus data bit17 I/O |
| | | | | | | SOT1_0 *3 | - | | Multi-function serial ch.1 serial data output (0) |
| | | | | | | TIOA1_1 | - | | TIOA I/O of Base timer ch.1 (1) |
| - | - | - | 113 *1 | 133 | 161 | P002 | - | F | General-purpose I/O port |
| | | | | | | D18 *5 | - | | External bus data bit18 I/O |
| | | | | | | SCK1_0 | - | | Multi-function serial ch.1 clock I/O (0) |
| | | | | | | TIOB0_1 | - | | TIOB input of Base timer ch.0 (1) |
| - | 76 *1 | 96 *1 | 114 *1 | 134 | 162 | P003 | - | F | General-purpose I/O port |
| | | | | | | D19 *3, *4, *5 | - | | External bus data bit19 I/O |
| | | | | | | SIN2_0 | - | | Multi-function serial ch.2 serial data input (0) |
| | | | | | | TIOB1_1 | - | | TIOB input of Base timer ch.1 (1) |
| | | | | | | INT3_0 | - | | INT3 External interrupt input (0) |
| - | - | - | - | 135 | 163 | P004 | - | A | General-purpose I/O port |
| | | | | | | D20 | - | | External bus data bit20 I/O (0) |
| | | | | | | SOT2_0 | - | | Multi-function serial ch.2 serial data output (0) |
| - | - | - | - | - | 164 | P164 | - | A | General-purpose I/O port |
| | | | | | | PPG32_1 | - | | PPG ch.32 output (1) |

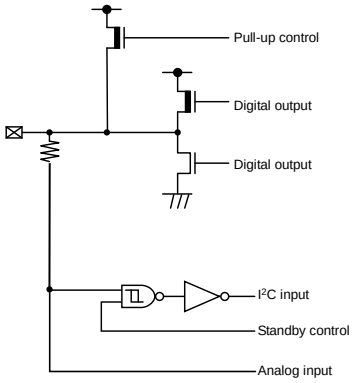
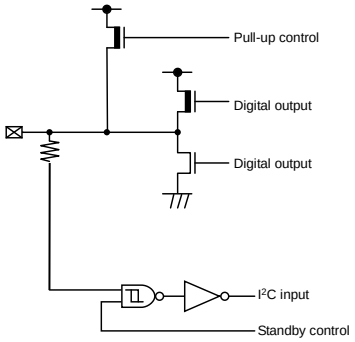
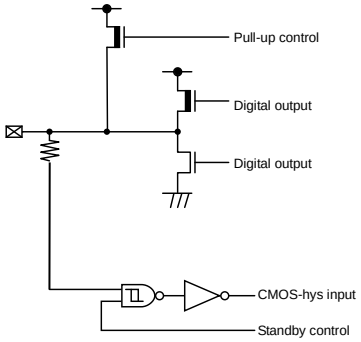
| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 61 *1 | 77 *1 | 97 *1 | 115 *1 | 136 *1 | 165 *1 | P005 | - | F | General-purpose I/O port |
| | | | | | | D21 *2, *3, *4, *5 | - | | External bus data bit21 I/O (0) |
| | | | | | | SCK2_0 *2 | - | | Multi-function serial ch.2 clock I/O (0) |
| | | | | | | ADTG0_1 | - | | A/D converter external trigger input 0 (1) |
| | | | | | | INT7_1 | - | | INT7 External interrupt input (1) |
| | | | | | | RX2(64) *4, *5, *6, *7 | - | | CAN reception data 2 input |
| - | - | - | - | - | 166 | P165 | - | A | General-purpose I/O port |
| | | | | | | PPG33_1 | - | | PPG ch.33 output (1) |
| 62 *1 | 78 *1 | 98 *1 | 116 *1 | 137 *1 | 167 *1 | P006 | - | A | General-purpose I/O port |
| | | | | | | D22 *2, *3, *4, *5 | - | | External bus data bit22 I/O (0) |
| | | | | | | SCS2_0 *2 | - | | Serial chip select 2 I/O (0) |
| | | | | | | ADTG1_1 | - | | A/D converter external trigger input 1 (1) |
| | | | | | | INT2_1 | - | | INT2 External interrupt input (1) |
| | | | | | | TX2(64) *4, *5, *6, *7 | - | | CAN transmission data 2 output |
| - | - | - | 117 *1 | 138 | 168 | P007 | - | A | General-purpose I/O port |
| | | | | | | D23 *5 | - | | External bus data bit23 I/O |
| - | - | - | - | - | 169 | P166 | - | A | General-purpose I/O port |
| | | | | | | PPG34_1 | - | | PPG ch.34 output (1) |
| - | - | - | 118 *1 | 139 | 170 | P010 | - | A | General-purpose I/O port |
| | | | | | | D24 *5 | - | | External bus data bit24 I/O |
| 63 *1 | 79 *1 | 99 *1 | 119 *1 | 140 | 171 | P011 | - | A | General-purpose I/O port |
| | | | | | | WOT | - | | RTC output signal |
| | | | | | | D25 *2, *3, *4, *5 | - | | External bus data bit25 I/O |
| | | | | | | SOT2_1 *2 | - | | Multi-function serial ch.2 serial data output (1) |
| | | | | | | TIOA0_0 *2, *3, *4 | - | | TIOA output of Base timer ch.0 (0) |
| | | | | | | INT3_1 | - | | INT3 External interrupt input (1) |
| - | - | - | - | 141 | 172 | P012 | - | A | General-purpose I/O port |
| | | | | | | D26 | - | | External bus data bit26 I/O |
| | | | | | | TIOB0_0 | - | | TIOB input of Base timer ch.0 (0) |
| - | - | - | - | - | 173 | P167 | - | A | General-purpose I/O port |
| | | | | | | PPG35_1 | - | | PPG ch.35 output (1) |
| - | - | - | - | 142 | 174 | P013 | - | A | General-purpose I/O port |
| | | | | | | D27 | - | | External bus data bit27 I/O |
| | | | | | | TIOA1_0 | - | | TIOA I/O of Base timer ch.1 (0) |
| - | - | - | - | 143 | 175 | P014 | - | A | General-purpose I/O port |
| | | | | | | D28 | - | | External bus data bit28 I/O |
| | | | | | | TIOB1_0 | - | | TIOB input of Base timer ch.1 (0) |
| 18 | 23 | 28 | 34 | 40 | 50 | AVCC1 | - | - | Analog power supply for AD/DA convertor unit1 |
| 39 | 47 | 58 | 68 | 84 | 103 | AVCC0 | - | - | Analog power supply for AD/DA convertor unit0 |

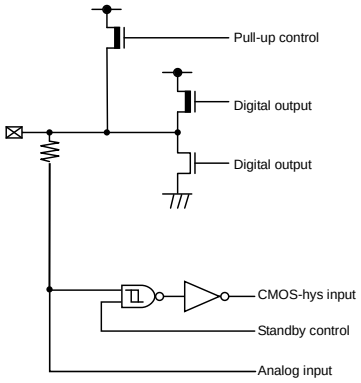
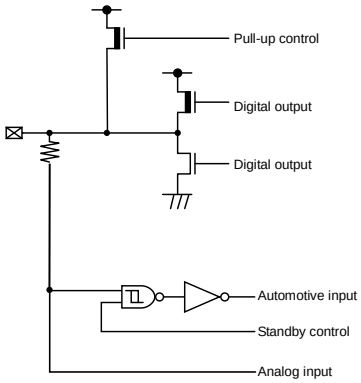
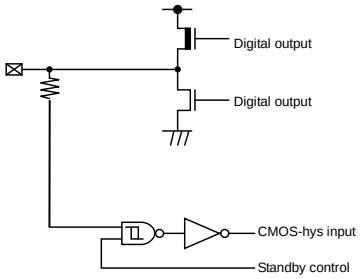
| Pin No. | | | | | | Pin Name | Polarity | I/O Circuit types*8 | Function*9 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 20 | 25 | 30 | 36 | 42 | 52 | AVRH1 | - | - | Upper limit reference voltage for AD convertor unit1 |
| 38 | 46 | 57 | 67 | 83 | 102 | AVRH0 | - | - | Upper limit reference voltage for AD convertor unit0 |
| 21 | 26 | 31 | 37 | 43 | 53 | AVSS1/ AVRL1 | - | - | GND for AD/DA convertor unit1 Lower limit reference voltage for AD convertor unit1 |
| 37 | 45 | 56 | 66 | 82 | 101 | AVSS0/ AVRL0 | - | - | GND for AD/DA convertor unit0 Lower limit reference voltage for AD convertor unit0 |
| 60 | 74 | 93 | 110 | 130 | 158 | C | - | - | External capacity connection output |
| - | 20 | 25 | 30 | 36 | 44 | VCC | - | - | +5.0V power supply |
| 32 | 40 | 50 | 60 | 72 | 88 | | | | |
| - | 61 | 76 | 91 | 109 | 133 | | | | |
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | VSS | - | - | GND |
| - | 21 | 26 | 31 | 37 | 45 | | | | |
| 33 | 41 | 51 | 61 | 73 | 89 | | | | |
| - | 60 | 75 | 90 | 108 | 132 | | | | |
| 55 | 69 | 85 | 101 | 120 | 148 | | | | |
| 59 | 73 | 92 | 109 | 129 | 157 | | | | |

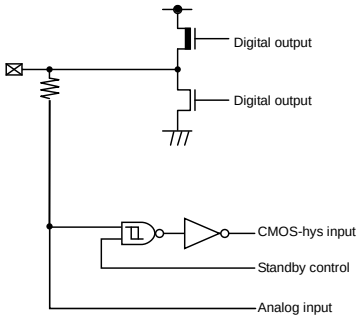
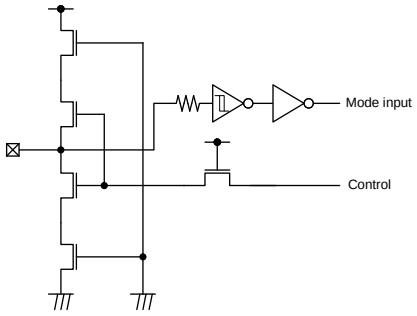
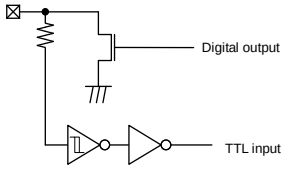
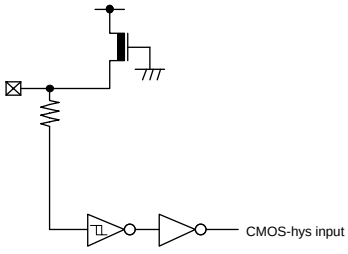
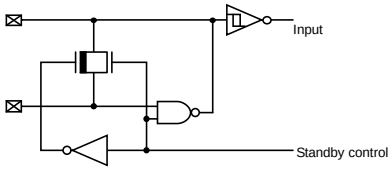
*1: There is a restriction of pin functions. See "Pin Name" of this table.
*2: not supported in 64 pin
*3: not supported in 80 pin
*4: not supported in 100 pin
*5: not supported in 120 pin
*6: not supported in 144 pin
*7: not supported in 176 pin
*8: For the I/O circuit types, see I/O Circuit Type.
*9: For switching, see "I/O Port" in HARDWARE MANUAL.

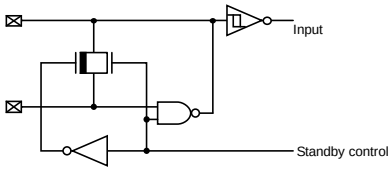
## 4. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | •General-purpose I/O port<br>•Output 4 mA<br>•Pull-up resistor control 50 kΩ<br>•Automotive input |
| B |  | •Analog input, General-purpose I/O port<br>•Output 4 mA<br>•Pull-up resistor control 50 kΩ<br>•Automotive input |
| C |  | •DAC output, General-purpose I/O port<br>•Output 4 mA<br>•Pull-up resistor control 50 kΩ<br>•Automotive input |

| Type | Circuit | Remarks |
|---|---|---|
| D |  | •I²C Analog input, General-purpose I/O port<br>•Output 3 mA<br>•Pull-up resistor control 50 kΩ<br>•I²C hysteresis input |
| E |  | •I²C,General-purpose I/O port<br>•Output 3 mA<br>•Pull-up resistor control 50 kΩ<br>•I²C hysteresis input |
| F |  | •General-purpose I/O port<br>•Output 4 mA<br>•Pull-up resistor control 50 kΩ<br>•CMOS hysteresis input |

| Type | Circuit | Remarks |
|---|---|---|
| G |  | •Analog input, General-purpose I/O port<br>•Output 4 mA<br>•Pull-up resistor control 50 kΩ<br>• CMOS hysteresis input |
| H |  | •Analog input, General-purpose I/O port<br>•Output 12 mA<br>•Pull-up resistor control 50 kΩ<br>•Automotive input |
| I |  | • General-purpose I/O port (5 V tolerant)<br>• Output 4 mA<br>• CMOS hysteresis input |

| Type | Circuit | Remarks |
|---|---|---|
| J |  | • Analog input, General-purpose I/O port (5 V tolerant)<br>• Output 4 mA<br>• CMOS hysteresis input |
| K |  | •Mode I/O<br>• CMOS hysteresis input |
| L |  | •Open-drain I/O<br>•Output 25 mA (Nch open-drain)<br>•TTL input |
| M |  | • CMOS hysteresis input<br>•Pull-up resistor 50 kΩ |
| N |  | •Main oscillation I/O |

| Type | Circuit | Remarks |
|---|---|---|
| O |  | •Sub oscillation I/O |

## 5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

**CAUTION:** The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

**CAUTION:** Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

**CAUTION:** When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause

absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40 % to 70 % relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40 % and 70 %. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 6. Handling Devices

This section explains the latch-up prevention and pin processing.

- For latch-up prevention
  If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

  Also, the analog power supply (AVCC, AVRH) and analog input must not be exceed the digital power supply (VCC) when the power supply to the analog system is turned on or off.

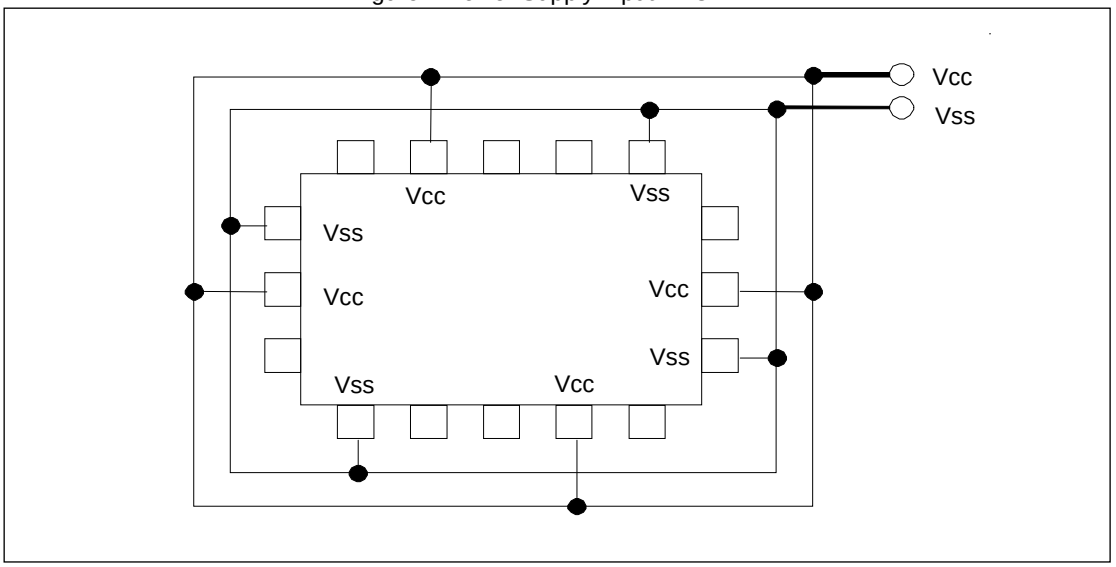
  In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC) and analog power supplies (AVCC, AVRH) simultaneously. Or, turn on the digital power supply (VCC), and then turn on analog power supplies (AVCC, AVRH).

- Treatment of unused pins
  If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2 kΩ resistor to each of the unused pins for pull-up or pull-down processing.

  Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

- Power supply pins
  The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins




The power supply pins should be connected to VCC and VSS pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

- Crystal oscillation circuit
  An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

  The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

- Mode pins (MD1, MD0)
  Connect the MD1 and MD0 mode pins to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

- During power-on
  To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

- Notes during PLL clock operation
  When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

- Treatment of A/D converter power supply pins
  Connect the pins to have AVCC = AVRH = VCC and AVSS/AVRL = VSS even if the A/D converter is not used.

- Notes on using external clock
  An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

- Power-on sequence of A/D converter analog inputs
  Be sure to turn on the digital power supply (Vcc) first, and then turn on the A/D converter power supplies (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN47). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc). When the AVRH pin voltage is turned on or off, it must not exceed AVCC. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

- Treatment of C pin
  This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

  **Note:** Please see the latest data sheet for a detailed specification of the operation voltage.

- Function switching of a multiplexed port
  To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see " I/O PORTS" in the hardware manual.

- Low-power consumption mode
  To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL" in the hardware manual.

  Take the following notes when using a monitor debugger.

  - Do not set a break point for the low-power consumption transition program.
  - Do not execute an operation step for the low-power consumption transition program.

- Notes When Writing Data in a Register Having the Status Flag
  When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

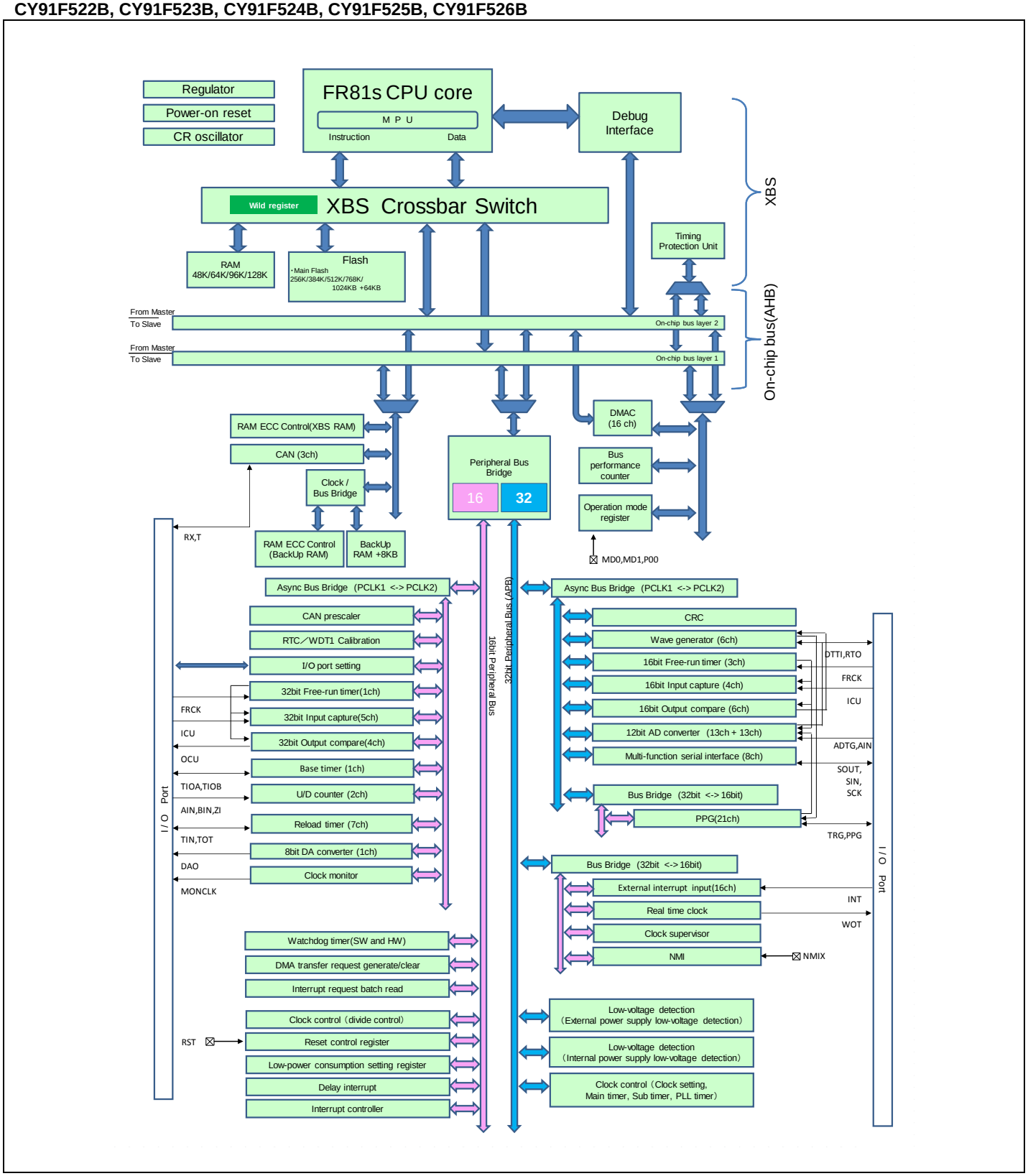
  The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

  Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

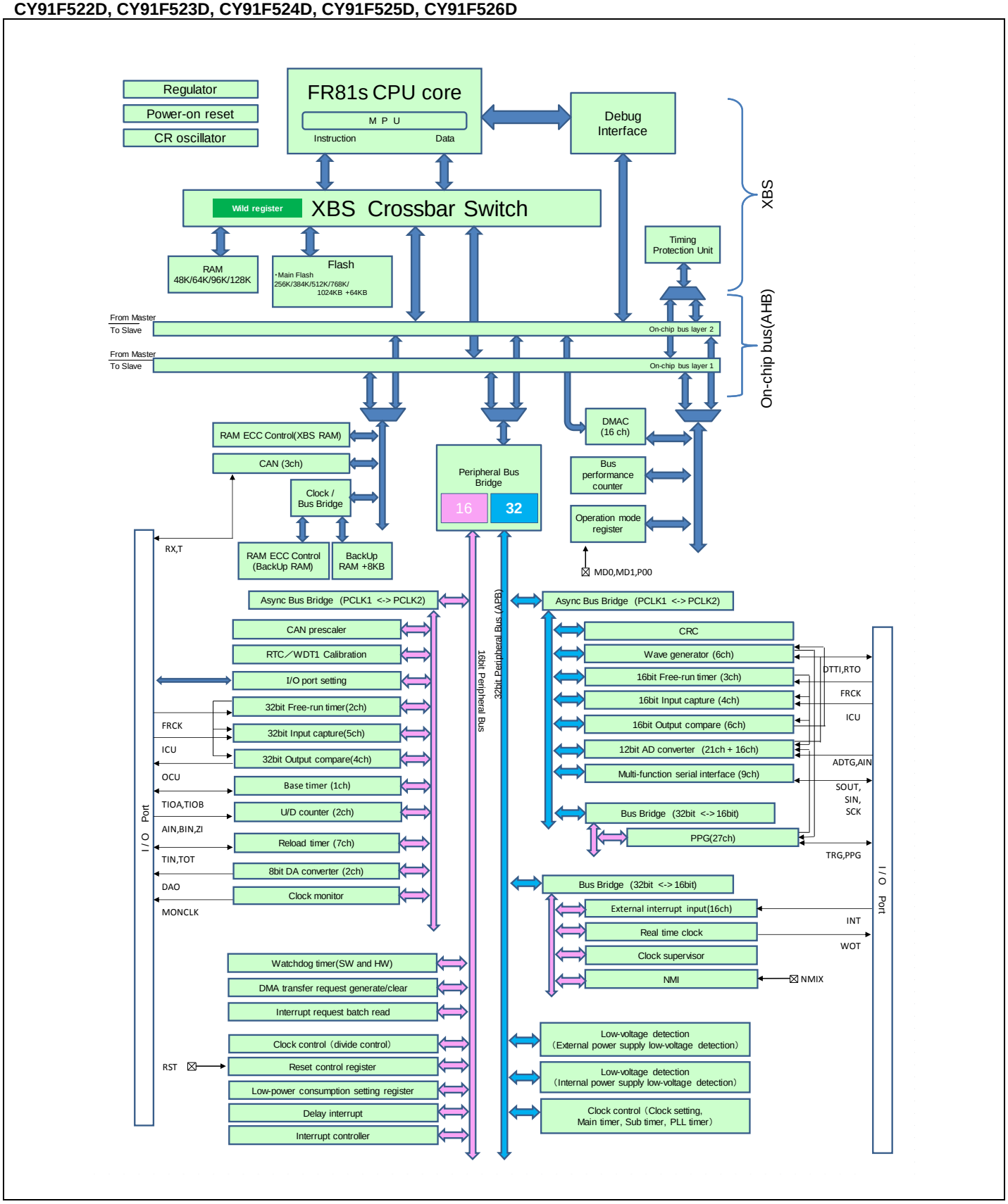
  **Note:** These points can be ignored because the bit instructions are already taken the points into consideration.

# 7. Block Diagram

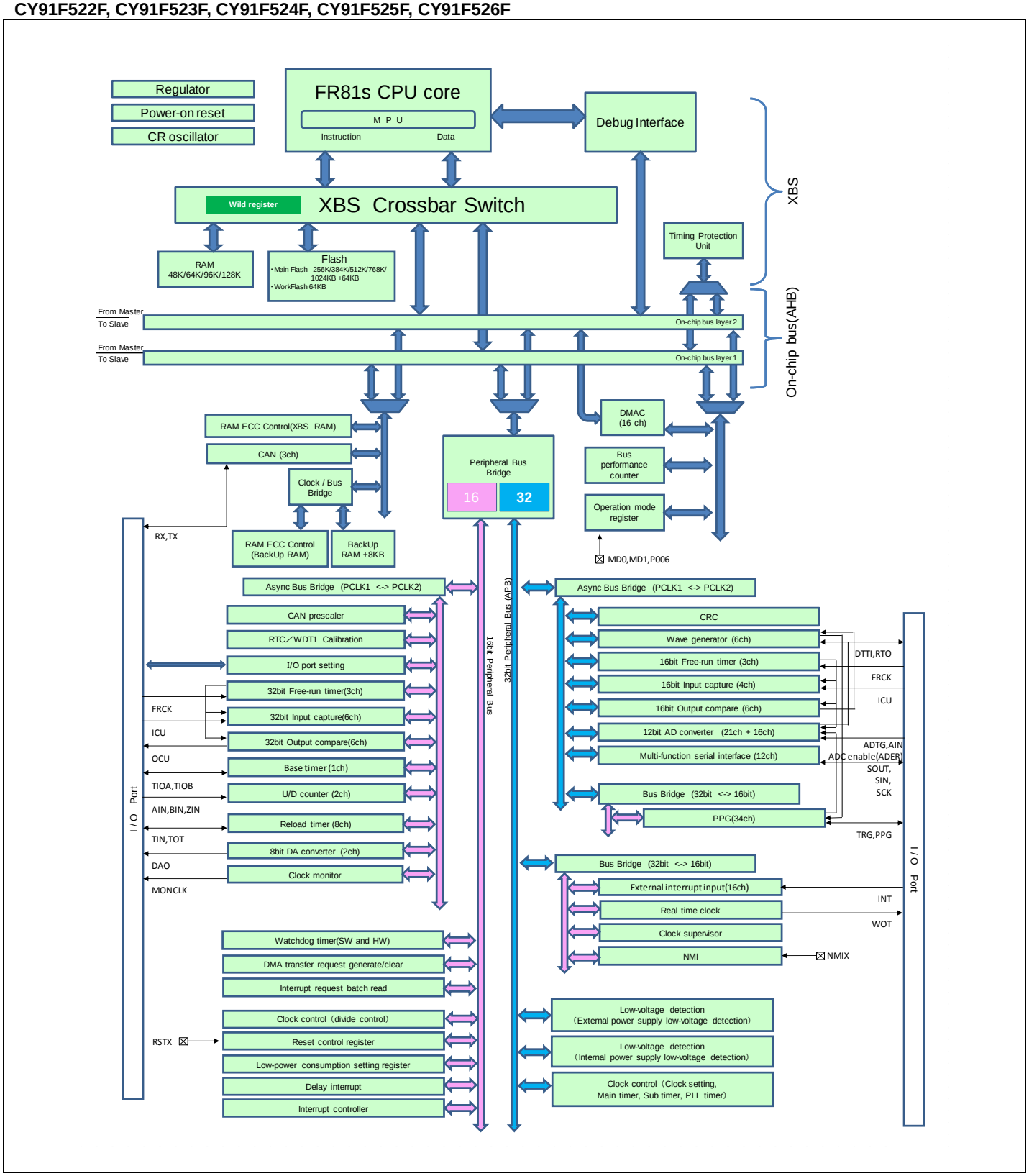
### CY91F522B, CY91F523B, CY91F524B, CY91F525B, CY91F526B



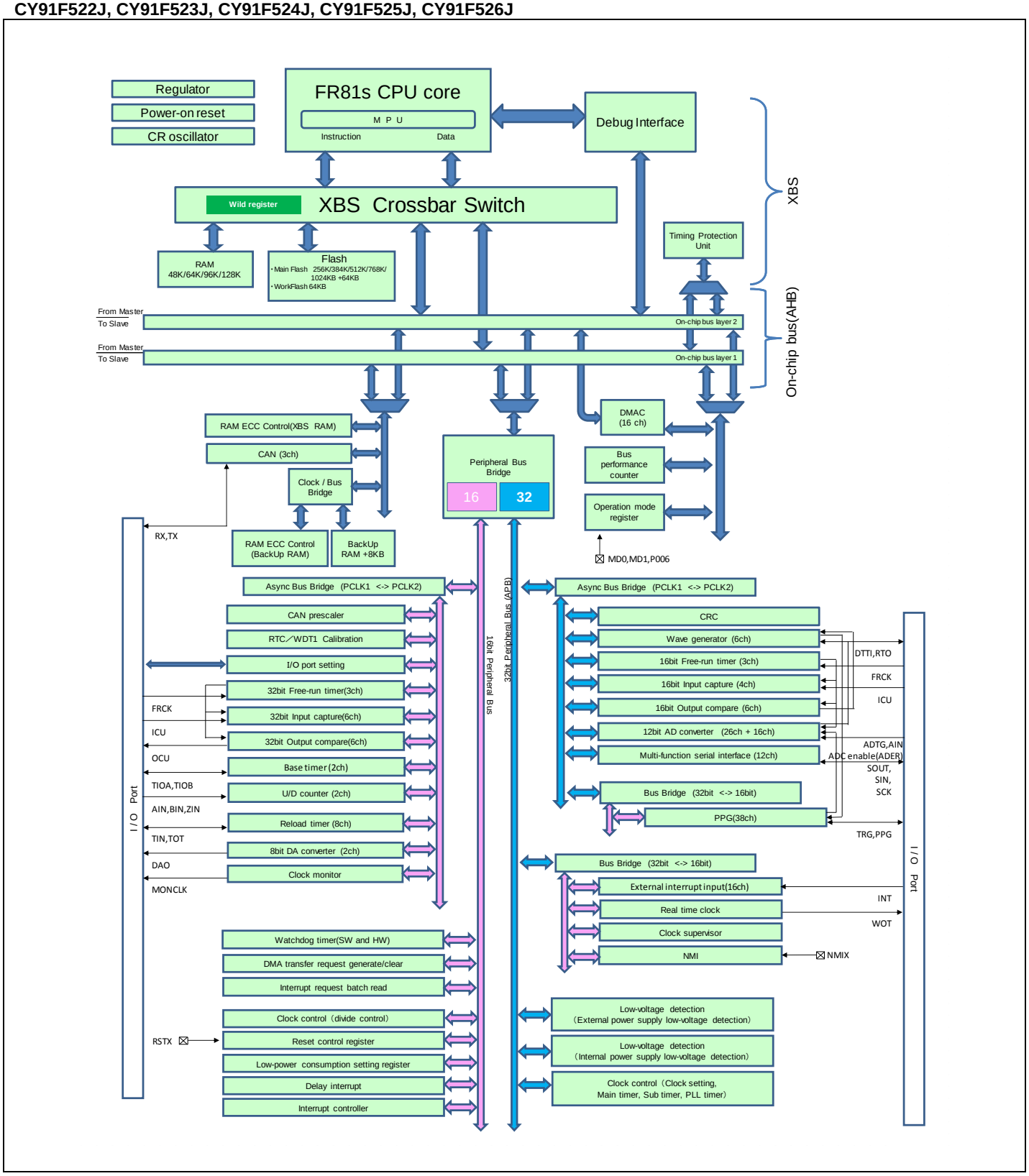
**CY91F522D, CY91F523D, CY91F524D, CY91F525D, CY91F526D**



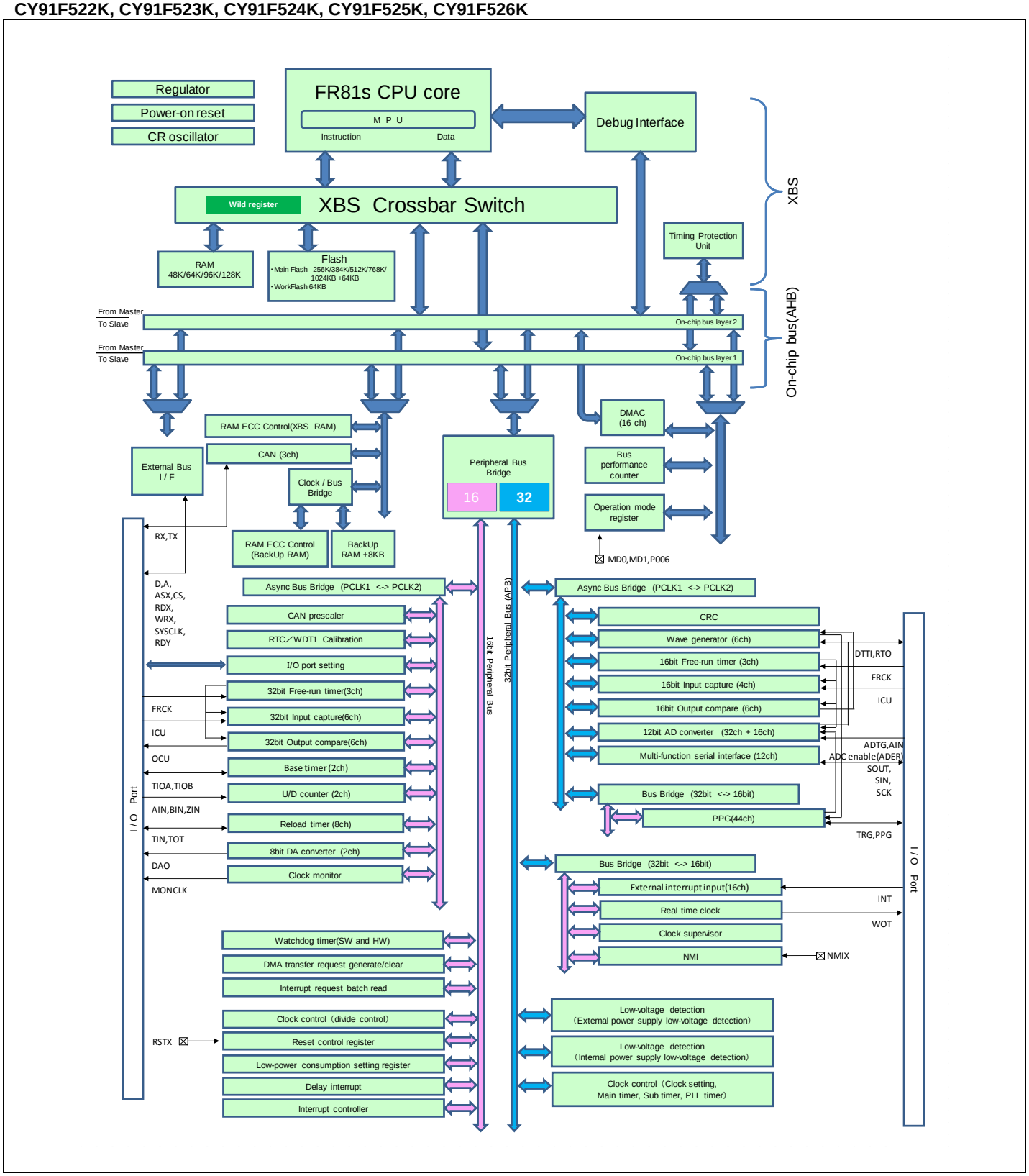
**CY91F522F, CY91F523F, CY91F524F, CY91F525F, CY91F526F**



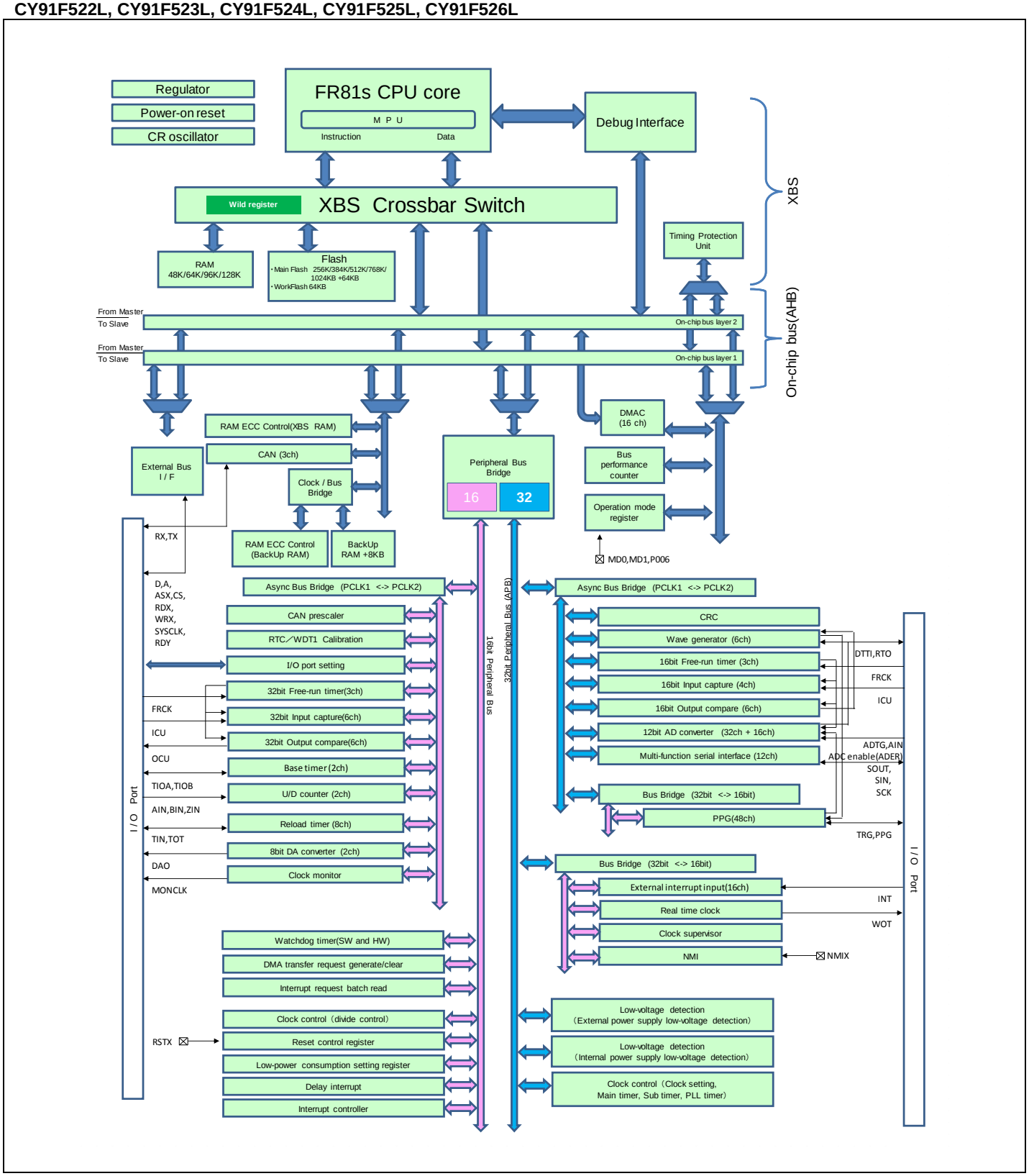
**CY91F522J, CY91F523J, CY91F524J, CY91F525J, CY91F526J**



**CY91F522K, CY91F523K, CY91F524K, CY91F525K, CY91F526K**

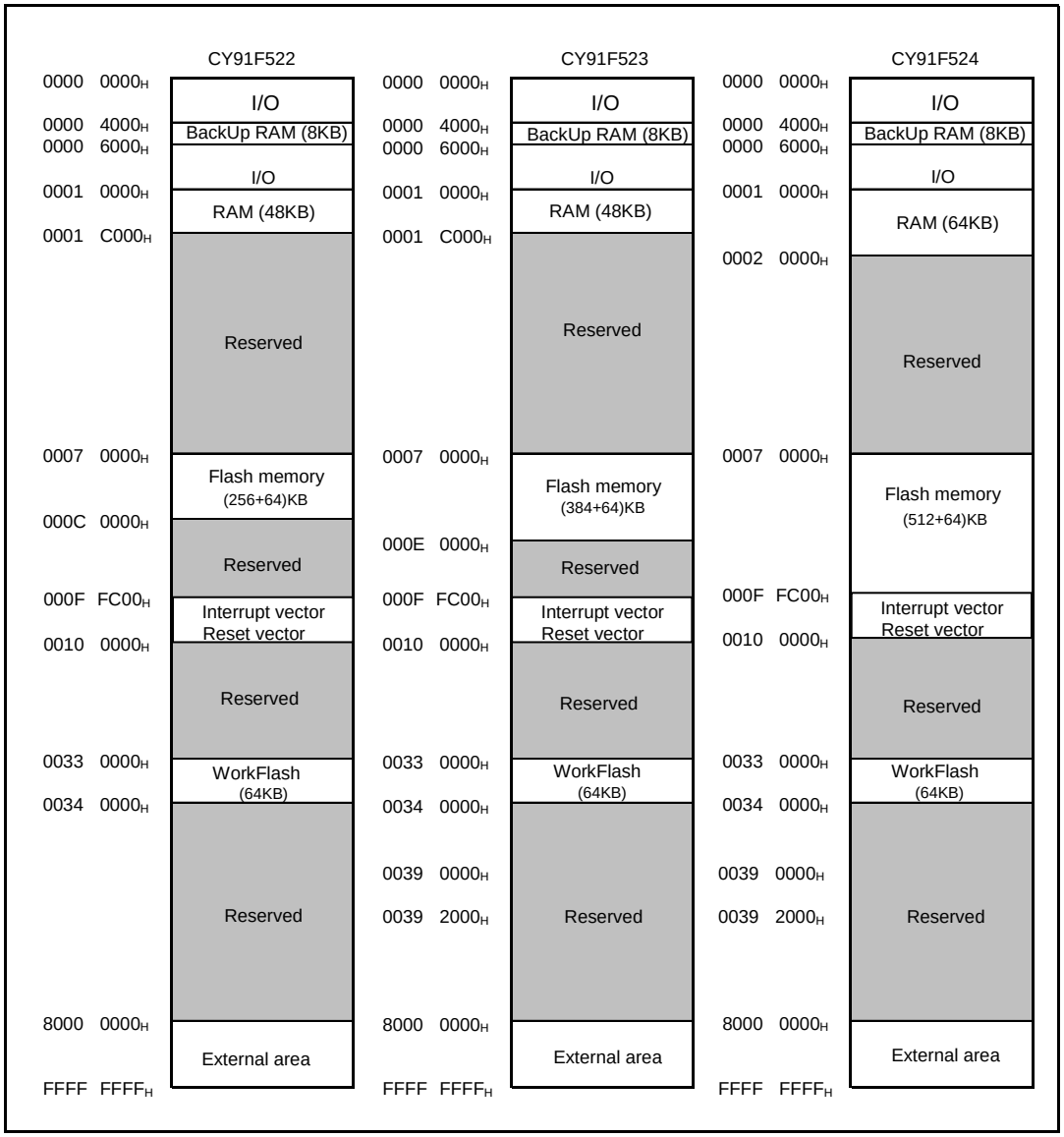


**CY91F522L, CY91F523L, CY91F524L, CY91F525L, CY91F526L**

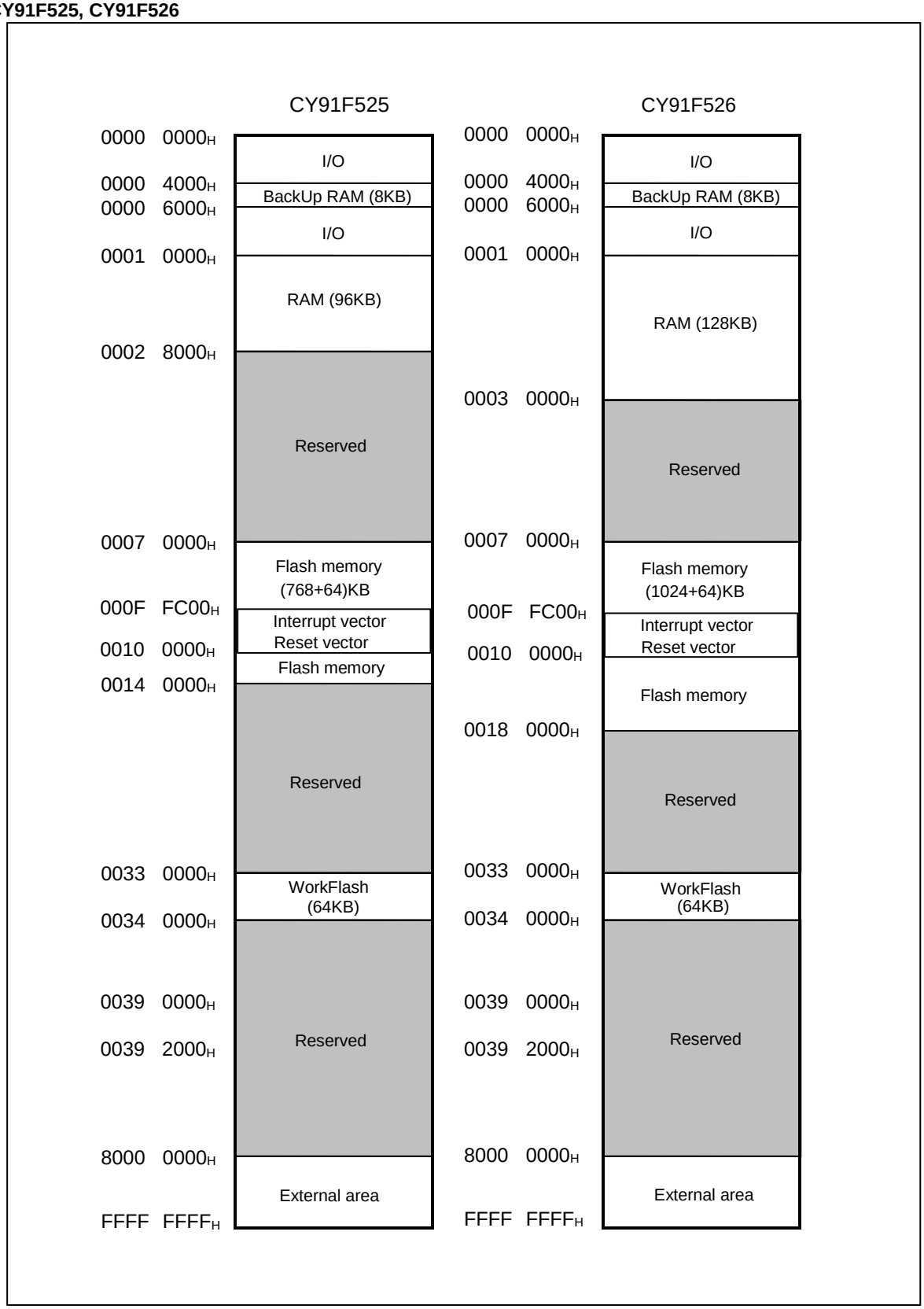


# 8. Memory Map

### CY91F522, CY91F523, CY91F524



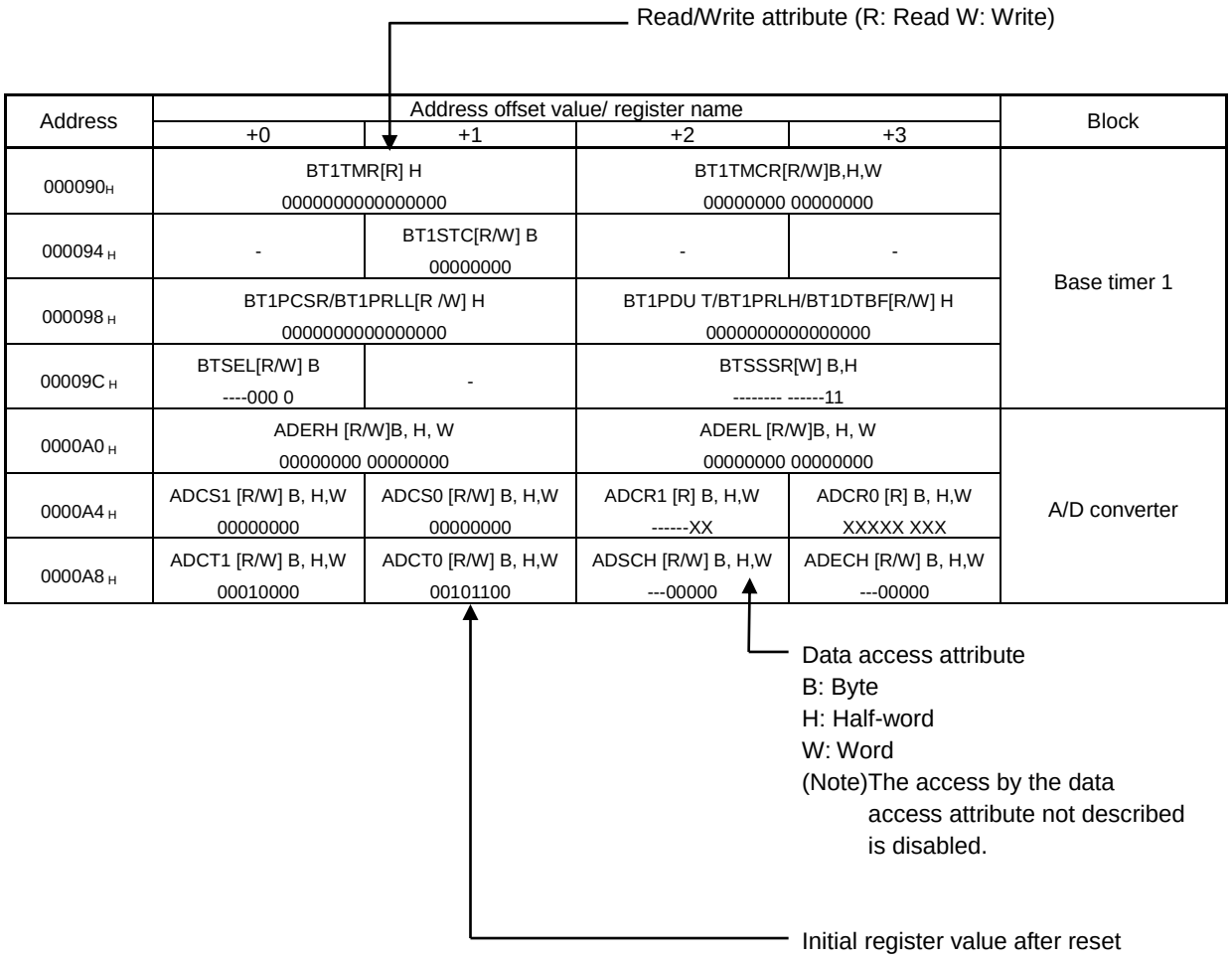
**CY91F525, CY91F526**



## 9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map




| Address | Address offset value/ register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000090H | BT1TMR[R] H<br>0000000000000000 | | BT1TMCR[R/W]B,H,W<br>00000000 00000000 | | Base timer 1 |
| 000094 H | - | BT1STC[R/W] B<br>00000000 | - | - | |
| 000098 H | BT1PCSR/BT1PRLL[R /W] H<br>0000000000000000 | | BT1PDU T/BT1PRLH/BT1DTBF[R/W] H<br>0000000000000000 | | |
| 00009C H | BTSEL[R/W] B<br>----000 0 | - | BTSSSR[W] B,H<br>-------- ------11 | | |
| 0000A0 H | ADERH [R/W]B, H, W<br>00000000 00000000 | | ADERL [R/W]B, H, W<br>00000000 00000000 | | A/D converter |
| 0000A4 H | ADCS1 [R/W] B, H,W<br>00000000 | ADCS0 [R/W] B, H,W<br>00000000 | ADCR1 [R] B, H,W<br>------XX | ADCR0 [R] B, H,W<br>XXXXX XXX | |
| 0000A8 H | ADCT1 [R/W] B, H,W<br>00010000 | ADCT0 [R/W] B, H,W<br>00101100 | ADSCH [R/W] B, H,W<br>---00000 | ADECH [R/W] B, H,W<br>---00000 | |

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

**Note:** The access to addresses not described is disabled.

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| $000000_H$ | PDR00 [R/W] B,H,W<br>XXXXXXXX | PDR01 [R/W] B,H,W<br>XXXXXXXX | PDR02 [R/W] B,H,W<br>XXXXXXXX | PDR03 [R/W] B,H,W<br>XXXXXXXX | Port Data Register |
| $000004_H$ | PDR04 [R/W] B,H,W<br>XXXXXXXX | PDR05 [R/W] B,H,W<br>XXXXXXXX | PDR06 [R/W] B,H,W<br>XXXXXXXX | PDR07 [R/W] B,H,W<br>XXXXXXXX | |
| $000008_H$ | PDR08 [R/W] B,H,W<br>XXXXXXXX | PDR09 [R/W] B,H,W<br>XXXXXXXX | PDR10 [R/W] B,H,W<br>XXXXXXXX | PDR11 [R/W] B,H,W<br>XXXXXXXX | |
| $00000C_H$ | PDR12 [R/W] B,H,W<br>XXXXXXXX | PDR13 [R/W] B,H,W<br>-XXXXXXX | PDR14 [R/W] B,H,W<br>---XXX-- | PDR15 [R/W] B,H,W<br>--XXXXXX | |
| $000010_H$ | — | — | — | — | |
| $000014_H$ | — | — | — | — | |
| $000018_H$ | PDR16 [R/W] B,H,W<br>XXXXXXXX | PDR17 [R/W] B,H,W<br>XXXXXXXX | PDR18 [R/W] B,H,W<br>XXXXXXXX | PDR19 [R/W] B,H,W<br>XXXXXXXX | |
| $00001C_H$ to $000034_H$ | — | — | — | — | Reserved |
| $000038_H$ | WDTECR0 [R/W] B,H,W<br>---00000 | — | — | — | Watchdog Timer [S] |
| $00003C_H$ | WDTCR0 [R/W] B,H,W<br>-0--0000 | WDTCPR0 [W] B,H,W<br>00000000 | WDTCR1 [R] B,H,W<br>----0110 | WDTCPR1 [W] B,H,W<br>00000000 | |
| $000040_H$ | — | — | — | — | Reserved |
| $000044_H$ | DICR [R/W] B,H,W<br>-------0 | — | — | — | Delayed Interrupt |
| $000048_H$ to $00005C_H$ | — | — | — | — | Reserved |
| $000060_H$ | TMRLRA0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR0 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 0 |
| $000064_H$ | TMRLRB0 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR0 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000068_H$ | TMRLRA7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR7 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 7 |
| $00006C_H$ | TMRLRB7 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR7 [R/W] B,H,W<br>00000000 0-000000 | | |
| $000070_H$ | — | FRS8 [R/W] B,H,W<br>--00--00 --00--00 --00--00 | | | Free-run timer selection register 8 |
| $000074_H$ | — | FRS9 [R/W] B,H,W<br>--00--00 --00--00 --00--00 | | | Free-run timer selection register 9 |
| $000078_H$ | — | — | — | OCLS67 [R/W] B,H,W<br>----0000 | OCU67 Output level control register |
| $00007C_H$ | — | — | — | OCLS89 [R/W] B,H,W<br>----0000 | OCU89 Output level control register |
| $000080_H$ | BT0TMR [R] H<br>00000000 00000000 | | BT0TMCR [R/W] H<br>-000--00 -000-000 | | Base Timer 0 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000084H | BT0TMCR2 [R/W] B<br>-------0 | BT0STC [R/W] B<br>-0-0-0-0 | — | — | |
| 000088H | BT0PCSR/BT0PRLL [R/W] H<br>00000000 00000000 | | BT0PDUT/BT0PRLH/BT0DTBF [R/W] H<br>00000000 00000000 | | |
| 00008CH | — | — | — | — | Reserved |
| 000090H | BT1TMR [R] H<br>00000000 00000000 | | BT1TMCR [R/W] H<br>-000--00 -000-000 | | Base Timer 1 |
| 000094H | BT1TMCR2 [R/W] B<br>-------0 | BT1STC [R/W] B<br>-0-0-0-0 | — | — | |
| 000098H | BT1PCSR/BT1PRLL [R/W] H<br>00000000 00000000 | | BT1PDUT/BT1PRLH/BT1DTBF [R/W] H<br>00000000 00000000 | | |
| 00009CH | BTSEL01 [R/W] B<br>----0000 | — | BTSSSR [W] B,H<br>-------- ------11 | | Base Timer 0,1 |
| 0000A0H to 0000FCH | — | — | — | — | Reserved |
| 000100H | TMRLRA1 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR1 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 1 |
| 000104H | TMRLRB1 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR1 [R/W] B, H,W<br>00000000 0-000000 | | |
| 000108H | TMRLRA2 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR2 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 2 |
| 00010CH | TMRLRB2 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR2 [R/W] B,H,W<br>00000000 0-000000 | | |
| 000110H | TMRLRA3 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR3 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 3 |
| 000114H | TMRLRB3 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR3 [R/W] B,H,W<br>00000000 0-000000 | | |
| 000118H | MSCY4 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 4,5<br>Cycle measurement data register 45 |
| 00011CH | MSCY5 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000120H | OCCP6 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | Output Compare 6,7 32-bit OCU |
| 000124H | OCCP7 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000128H | — | — | OCSH67 [R/W] B,H,W<br>---0--00 | OCSL67 [R/W] B,H,W<br>0000--00 | |
| 00012CH | OCCP8 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | Output Compare 8,9 32-bit OCU |
| 000130H | OCCP9 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000134H | — | — | OCSH89 [R/W] B,H,W<br>---0--00 | OCSL89 [R/W] B,H,W<br>0000--00 | |
| 000138H to 0001B4H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0001B8H | EPFR64 [R/W]<br>B,H,W<br>-----00- | EPFR65 [R/W]<br>B,H,W<br>0000-000 | EPFR66 [R/W]<br>B,H,W<br>--000000 | EPFR67 [R/W]<br>B,H,W<br>----0000 | Extended port function register |
| 0001BCH | EPFR68 [R/W]<br>B,H,W<br>----0000 | EPFR69 [R/W]<br>B,H,W<br>----0000 | EPFR70 [R/W]<br>B,H,W<br>---00000 | EPFR71 [R/W]<br>B,H,W<br>-0-0-0-0 | |
| 0001C0H | EPFR72 [R/W]<br>B,H,W<br>000000-0 | EPFR73 [R/W]<br>B,H,W<br>00000000 | EPFR74 [R/W]<br>B,H,W<br>00000000 | EPFR75 [R/W]<br>B,H,W<br>00000000 | |
| 0001C4H | EPFR76 [R/W]<br>B,H,W<br>00000000 | EPFR77 [R/W]<br>B,H,W<br>--000000 | EPFR78 [R/W]<br>B,H,W<br>------00 | EPFR79 [R/W]<br>B,H,W<br>00000000 | |
| 0001C8H | EPFR80 [R/W]<br>B,H,W<br>---00000 | EPFR81 [R/W]<br>B,H,W<br>00000000 | EPFR82 [R/W]<br>B,H,W<br>00000000 | EPFR83 [R/W]<br>B,H,W<br>-0000000 | |
| 0001CCH | EPFR84 [R/W]<br>B,H,W<br>00000000 | EPFR85 [R/W]<br>B,H,W<br>--000000 | EPFR86 [R/W]<br>B,H,W<br>---00000 | EPFR87 [R/W]<br>B,H,W<br>------00 | |
| 0001D0H | EPFR88 [R/W]<br>B,H,W<br>-------0 | — | — | — | |
| 0001D4H | — | — | — | — | Reserved |
| 0001D8H | TMRLRA4 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR4 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 4 |
| 0001DCH | TMRLRB4 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR4 [R/W] B, H,W<br>00000000 0-000000 | | |
| 0001E0H to 0001ECH | — | — | — | — | Reserved |
| 0001F0H | TMRLRA5 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR5 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 5 |
| 0001F4H | TMRLRB5 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR5 [R/W] B, H,W<br>00000000 0-000000 | | |
| 0001F8H | TMRLRA6 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMR6 [R] H<br>XXXXXXXX XXXXXXXX | | Reload Timer 6 |
| 0001FCH | TMRLRB6 [R/W] H<br>XXXXXXXX XXXXXXXX | | TMCSR6 [R/W] B, H,W<br>00000000 0-000000 | | |
| 000200H to 000238H | — | — | — | — | Reserved |
| 00023CH | DACR0 [R/W] B,H,W<br>-------0 | DADR0 [R/W] B,H,W<br>XXXXXXXX | DACR1 [R/W] B,H,W<br>-------0 | DADR1 [R/W] B,H,W<br>XXXXXXXX | DA Converter |
| 000240H | CPCLR3 [R/W] W<br>11111111 11111111 11111111 11111111 | | | | Free-run Timer 3 32-bit FRT |
| 000244H | TCDT3 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000248H | TCCSH3 [R/W]<br>B,H,W<br>0-----00 | TCCSL3 [R/W]<br>B,H,W<br>-1-00000 | — | — | |
| 00024CH | CPCLR4 [R/W] W<br>11111111 11111111 11111111 11111111 | | | | Free-run Timer 4 32-bit FRT |
| 000250H | TCDT4 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000254H | TCCSH4 [R/W]<br>B,H,W<br>0-----00 | TCCSL4 [R/W]<br>B,H,W<br>-1-00000 | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000258$_H$ to 0002C0$_H$ | — | — | — | — | Reserved |
| 0002C4$_H$ to 0002FC$_H$ | — | — | — | — | Reserved |
| 000300$_H$ to 00030C$_H$ | — | — | — | — | Reserved |
| 000310$_H$ | — | — | MPUCR [R/W] H<br>000000-0 ----0100 | | MPU [S]<br>(Only CPU core can access this area) |
| 000314$_H$ | — | — | — | — | |
| 000318$_H$ | — | | | | |
| 00031C$_H$ | — | — | — | | |
| 000320$_H$ | DPVAR [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000324$_H$ | — | — | DPVSR [R/W] H<br>-------- 00000--0 | | |
| 000328$_H$ | DEAR [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 00032C$_H$ | — | — | DESR [R/W] H<br>-------- 00000--0 | | |
| 000330$_H$ | PABR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 000334$_H$ | — | — | PACR0 [R/W] H<br>000000-0 00000--0 | | |
| 000338$_H$ | PABR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 00033C$_H$ | — | — | PACR1 [R/W] H<br>000000-0 00000--0 | | |
| 000340$_H$ | PABR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 000344$_H$ | — | — | PACR2 [R/W] H<br>000000-0 00000--0 | | |
| 000348$_H$ | PABR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 00034C$_H$ | — | — | PACR3 [R/W] H<br>000000-0 00000--0 | | |
| 000350$_H$ | PABR4 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 000354$_H$ | — | — | PACR4 [R/W] H<br>000000-0 00000--0 | | |
| 000358$_H$ | PABR5 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 00035C$_H$ | — | — | PACR5 [R/W] H<br>000000-0 00000--0 | | |
| 000360$_H$ | PABR6 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | |
| 000364$_H$ | — | — | PACR6 [R/W] H<br>000000-0 00000--0 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000368H | PABR7 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000 | | | | MPU [S]<br>(Only CPU core can access this area) |
| 00036CH | — | — | PACR7 [R/W] H<br>000000-0 00000--0 | | |
| 000370H to 0003ACH | — | | | | Reserved [S] |
| 0003B0H to 0003FCH | — | — | — | — | Reserved [S] |
| 000400H | ICSEL0 [R/W] B,H,W<br>-----000 | ICSEL1 [R/W] B,H,W<br>-----000 | ICSEL2 [R/W] B,H,W<br>-------0 | ICSEL3 [R/W] B,H,W<br>-------0 | DMA request generation and clear |
| 000404H | — | ICSEL5 [R/W] B,H,W<br>-----000 | ICSEL6 [R/W] B,H,W<br>----0000 | ICSEL7 [R/W] B,H,W<br>----0000 | |
| 000408H | ICSEL8 [R/W] B,H,W<br>------00 | ICSEL9 [R/W] B,H,W<br>------00 | ICSEL10 [R/W] B,H,W<br>------00 | ICSEL11 [R/W] B,H,W<br>-----000 | |
| 00040CH | — | ICSEL13 [R/W] B,H,W<br>------00 | ICSEL14 [R/W] B,H,W<br>------00 | ICSEL15 [R/W] B,H,W<br>------00 | |
| 000410H | ICSEL16 [R/W] B,H,W<br>----0000 | ICSEL17 [R/W] B,H,W<br>------00 | ICSEL18 [R/W] B,H,W<br>---00000 | ICSEL19 [R/W] B,H,W<br>-----000 | |
| 000414H | ICSEL20 [R/W] B,H,W<br>-----000 | ICSEL21 [R/W] B,H,W<br>------00 | ICSEL22 [R/W] B,H,W<br>------00 | ICSEL23 [R/W] B,H,W<br>------00 | |
| 000418H | IRPR0H [R] B,H,W<br>00------ | IRPR0L [R] B,H,W<br>00------ | IRPR1H [R] B,H,W<br>00------ | IRPR1L [R] B,H,W<br>00------ | Interrupt Request Batch Reading Register |
| 00041CH | — | — | IRPR3H [R] B,H,W<br>000000-- | IRPR3L [R] B,H,W<br>000000-- | |
| 000420H | IRPR4H [R] B,H,W<br>0000---- | IRPR4L [R] B,H,W<br>0000---- | IRPR5H [R] B,H,W<br>0000---- | IRPR5L [R] B,H,W<br>000----- | |
| 000424H | IRPR6H [R] B,H,W<br>--00---- | IRPR6L [R] B,H,W<br>0000---- | IRPR7H [R] B,H,W<br>-0-00--- | IRPR7L [R] B,H,W<br>------00 | |
| 000428H | IRPR8H [R] B,H,W<br>--0----- | IRPR8L [R] B,H,W<br>-00----- | IRPR9H [R] B,H,W<br>-0------ | IRPR9L [R] B,H,W<br>-0------ | |
| 00042CH | IRPR10H [R] B,H,W<br>-0------ | IRPR10L [R] B,H,W<br>-0------ | IRPR11H [R] B,H,W<br>0------- | IRPR11L [R] B,H,W<br>0------- | |
| 000430H | IRPR12H [R] B,H,W<br>--0000-- | IRPR12L [R] B,H,W<br>----00-- | IRPR13H [R] B,H,W<br>00------ | IRPR13L [R] B,H,W<br>00------ | |
| 000434H | IRPR14H [R] B,H,W<br>00000000 | IRPR14L [R] B,H,W<br>00000000 | IRPR15H [R] B,H,W<br>000----- | IRPR15L [R] B,H,W<br>0000000- | |
| 000438H | ICSEL24 [R/W] B,H,W<br>------00 | ICSEL25 [R/W] B,H,W<br>---00000 | ICSEL26 [R/W] B,H,W<br>-------0 | ICSEL27 [R/W] B,H,W<br>-------0 | DMA request generation and clear |
| 00043CH | — | — | — | — | Reserved [S] |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000440H | ICR00 [R/W] B,H,W<br>---11111 | ICR01 [R/W] B,H,W<br>---11111 | ICR02 [R/W] B,H,W<br>---11111 | ICR03 [R/W] B,H,W<br>---11111 | Interrupt Controller [S] |
| 000444H | ICR04 [R/W] B,H,W<br>---11111 | ICR05 [R/W] B,H,W<br>---11111 | ICR06 [R/W] B,H,W<br>---11111 | ICR07 [R/W] B,H,W<br>---11111 | |
| 000448H | ICR08 [R/W] B,H,W<br>---11111 | ICR09 [R/W] B,H,W<br>---11111 | ICR10 [R/W] B,H,W<br>---11111 | ICR11 [R/W] B,H,W<br>---11111 | |
| 00044CH | ICR12 [R/W] B,H,W<br>---11111 | ICR13 [R/W] B,H,W<br>---11111 | ICR14 [R/W] B,H,W<br>---11111 | ICR15 [R/W] B,H,W<br>---11111 | |
| 000450H | ICR16 [R/W] B,H,W<br>---11111 | ICR17 [R/W] B,H,W<br>---11111 | ICR18 [R/W] B,H,W<br>---11111 | ICR19 [R/W] B,H,W<br>---11111 | |
| 000454H | ICR20 [R/W] B,H,W<br>---11111 | ICR21 [R/W] B,H,W<br>---11111 | ICR22 [R/W] B,H,W<br>---11111 | ICR23 [R/W] B,H,W<br>---11111 | |
| 000458H | ICR24 [R/W] B,H,W<br>---11111 | ICR25 [R/W] B,H,W<br>---11111 | ICR26 [R/W] B,H,W<br>---11111 | ICR27 [R/W] B,H,W<br>---11111 | |
| 00045CH | ICR28 [R/W] B,H,W<br>---11111 | ICR29 [R/W] B,H,W<br>---11111 | ICR30 [R/W] B,H,W<br>---11111 | ICR31 [R/W] B,H,W<br>---11111 | |
| 000460H | ICR32 [R/W] B,H,W<br>---11111 | ICR33 [R/W] B,H,W<br>---11111 | ICR34 [R/W] B,H,W<br>---11111 | ICR35 [R/W] B,H,W<br>---11111 | |
| 000464H | ICR36 [R/W] B,H,W<br>---11111 | ICR37 [R/W] B,H,W<br>---11111 | ICR38 [R/W] B,H,W<br>---11111 | ICR39 [R/W] B,H,W<br>---11111 | |
| 000468H | ICR40 [R/W] B,H,W<br>---11111 | ICR41 [R/W] B,H,W<br>---11111 | ICR42 [R/W] B,H,W<br>---11111 | ICR43 [R/W] B,H,W<br>---11111 | |
| 00046CH | ICR44 [R/W] B,H,W<br>---11111 | ICR45 [R/W] B,H,W<br>---11111 | ICR46 [R/W] B,H,W<br>---11111 | ICR47 [R/W] B,H,W<br>---11111 | |
| 000470H to 00047CH | — | — | — | — | Reserved [S] |
| 000480H | RSTRR [R]<br>B,H,W<br>XXXX--XX | RSTCR [R/W]<br>B,H,W<br>111----0 | STBCR [R/W]<br>B,H,W *<br>000---11 | — | Reset Control [S]<br>Power Control [S]<br>*: Writing STBCR by DMA is forbidden |
| 000484H | — | — | — | — | Reserved [S] |
| 000488H | DIVR0 [R/W] B,H,W<br>000----- | DIVR1 [R/W] B,H,W<br>0001---- | DIVR2 [R/W] B,H,W<br>0011---- | — | Clock Control [S] |
| 00048CH | — | — | — | — | Reserved [S] |
| 000490H | IORR0 [R/W] B,H,W<br>-0000000 | IORR1 [R/W] B,H,W<br>-0000000 | IORR2 [R/W] B,H,W<br>-0000000 | IORR3 [R/W] B,H,W<br>-0000000 | DMA request by peripheral [S] |
| 000494H | IORR4 [R/W] B,H,W<br>-0000000 | IORR5 [R/W] B,H,W<br>-0000000 | IORR6 [R/W] B,H,W<br>-0000000 | IORR7 [R/W] B,H,W<br>-0000000 | |
| 000498H | IORR8 [R/W] B,H,W<br>-0000000 | IORR9 [R/W] B,H,W<br>-0000000 | IORR10 [R/W] B,H,W<br>-0000000 | IORR11 [R/W] B,H,W<br>-0000000 | |
| 00049CH | IORR12 [R/W] B,H,W<br>-0000000 | IORR13 [R/W] B,H,W<br>-0000000 | IORR14 [R/W] B,H,W<br>-0000000 | IORR15 [R/W] B,H,W<br>-0000000 | DMA request by peripheral [S] |
| 0004A0H | — | — | — | — | Reserved |
| 0004A4H | CANPRE [R/W]<br>B,H,W<br>---00000 | — | — | — | CAN prescaler |
| 0004A8H | — | — | CSCFG[R/W]B,H,W<br>---0---- | CMCFG[R/W]B,H,W<br>00000000 | Clock monitor control register |
| 0004ACH | ADERH0[R/W] B,H<br>11111111 11111111 | | ADERL0[R/W] B,H<br>11111111 11111111 | | Analog input control register 0 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0004B0H | — | | ADERL1[R/W] B,H<br>11111111 11111111 | | Analog input control register 1 |
| 0004B4H | — | — | — | — | Reserved |
| 0004B8H | CUCR0 [R/W] B,H,W<br>-------- ---0--00 | | CUTD0 [R/W] B,H,W<br>10000000 00000000 | | RTC/WDT1 calibration |
| 0004BCH | CUTR0 [R] B,H,W<br>-------- 00000000 00000000 00000000 | | | | |
| 0004C0H | — | — | — | — | |
| 0004C4H | CUCR1 [R/W] B,H,W<br>-------- ---0--00 | | CUTD1 [R/W] B,H,W<br>11000011 01010000 | | |
| 0004C8H | CUTR1 [R] B,H,W<br>-------- 00000000 00000000 00000000 | | | | |
| 0004CCH to 00050CH | — | — | — | — | Reserved |
| 000510H | CSELR [R/W] B,H,W<br>001---00 | CMONR [R] B,H,W<br>001---00 | MTMCR [R/W] B,H,W<br>00001111 | STMCR [R/W] B,H,W<br>0000-111 | Clock Control [S] |
| 000514H | PLLCR [R/W] B,H,W<br>-------- 11110000 | | CSTBR [R/W] B,H,W<br>-0000000 | PTMCR [R/W] B,H,W<br>00------ | |
| 000518H | — | — | CPUAR [R/W] B,H,W<br>0----XXX | — | Reset Control [S] |
| 00051CH | — | — | — | — | Reserved [S] |
| 000520H | CCPSSELR [R/W] B,H,W<br>-------0 | — | — | CCPSDIVR [R/W] B,H,W<br>-000-000 | Clock Control 2 [S] |
| 000524H | — | CCPLLFBR [R/W] B,H,W<br>-0000000 | CCSSFBR0 [R/W] B,H,W<br>--000000 | CCSSFBR1 [R/W] B,H,W<br>---00000 | |
| 000528H | — | CCSSCCR0 [R/W] B,H,W<br>----0000 | CCSSCCR1 [R/W] H,W<br>000----- -------- | | |
| 00052CH | — | CCCGRCR0 [R/W] B,H,W<br>00----00 | CCCGRCR1 [R/W] B,H,W<br>00000000 | CCCGRCR2 [R/W] B,H,W<br>00000000 | Clock Control 2 [S] |
| 000530H | CCRTSELR [R/W] B,H,W<br>0------0 | — | CCPMUCR0 [R/W] B,H,W<br>0-----00 | CCPMUCR1 [R/W] B,H,W<br>0--00000 | |
| 000534H to 00054CH | — | — | — | — | Reserved |
| 000550H | EIRR0 [R/W] B,H,W<br>XXXXXXXX | ENIR0 [R/W] B,H,W<br>00000000 | ELVR0 [R/W] B,H,W<br>00000000 00000000 | | External Interrupt (INT0 to 7) |
| 000554H | EIRR1 [R/W] B,H,W<br>XXXXXXXX | ENIR1 [R/W] B,H,W<br>00000000 | ELVR1 [R/W] B,H,W<br>00000000 00000000 | | External Interrupt (INT8 to 15) |
| 000558H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 00055C$_H$ | — | — | WTDR [R/W] H<br>00000000 00000000 | | Real Time Clock (RTC) |
| 000560$_H$ | — | WTCRH [R/W] B<br>------00 | WTCRM [R/W] B,H<br>00000000 | WTCRL [R/W] B,H<br>----00-0 | |
| 000564$_H$ | — | WTBRH [R/W] B<br>--XXXXXX | WTBRM [R/W] B<br>XXXXXXXX | WTBRL [R/W] B<br>XXXXXXXX | |
| 000568$_H$ | WTHR [R/W] B,H<br>---00000 | WTMR [R/W] B,H<br>--000000 | WTSR [R/W] B<br>--000000 | — | |
| 00056C$_H$ | — | CSVCR [R/W] B<br>000111-- | — | — | Clock Supervisor |
| 000570$_H$<br>to<br>00057C$_H$ | — | — | — | — | Reserved |
| 000580$_H$ | REGSEL [R/W]<br>B,H,W<br>0110011- | — | — | — | Regulator Control / Low Voltage Detection |
| 000584$_H$ | LVD5R [R/W]<br>B,H,W<br>-------1 | LVD5F [R/W]<br>B,H,W<br>00000001 | LVD [R/W]<br>B,H,W<br>01000--0 | — | |
| 000588$_H$<br>to<br>00058C$_H$ | — | — | — | — | Reserved |
| 000590$_H$ | PMUSTR [R/W]<br>B,H,W<br>0-----1X | PMUCTLR [R/W]<br>B,H,W<br>0-00---- | PWRTMCTL [R/W]<br>B,H,W<br>-----011 | — | PMU |
| 000594$_H$ | PMUINTF0 [R/W]<br>B,H,W<br>00000000 | PMUINTF1 [R/W]<br>B,H,W<br>00000000 | PMUINTF2 [R/W]<br>B,H,W<br>0000---- | — | |
| 000598$_H$ | — | — | — | — | |
| 00059C$_H$<br>to<br>0005BC$_H$ | — | — | — | — | Reserved |
| 0005C0$_H$<br>to<br>0005FC$_H$ | — | — | — | — | Reserved |
| 000600$_H$ | ASR0 [R/W] W<br>00000000 00000000 -------- 1111-001 | | | | External Bus Interface [S] |
| 000604$_H$ | ASR1 [R/W] W<br>XXXXXXXX XXXXXXXX -------- XXXX-XX0 | | | | |
| 000608$_H$ | ASR2 [R/W] W<br>XXXXXXXX XXXXXXXX -------- XXXX-XX0 | | | | |
| 00060C$_H$ | ASR3 [R/W] W<br>XXXXXXXX XXXXXXXX -------- XXXX-XX0 | | | | |
| 000610$_H$<br>to<br>00063C$_H$ | — | — | — | — | Reserved [S] |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000640H | ACR0 [R/W] W<br>-------- -------- -------- 01--00-- | | | | External Bus Interface [S] |
| 000644H | ACR1 [R/W] W<br>-------- -------- -------- XX--XX-- | | | | |
| 000648H | ACR2 [R/W] W<br>-------- -------- -------- XX--XX-- | | | | |
| 00064CH | ACR3 [R/W] W<br>-------- -------- -------- XX--XX-- | | | | |
| 000650H to 00067CH | — | — | — | — | Reserved [S] |
| 000680H | AWR0 [R/W] W<br>----1111 00000000 11110000 00000-0- | | | | External Bus Interface [S] |
| 000684H | AWR1 [R/W] W<br>----XXXX XXXXXXXX XXXXXXXX XXXXX-X- | | | | |
| 000688H | AWR2 [R/W] W<br>----XXXX XXXXXXXX XXXXXXXX XXXXX-X- | | | | External Bus Interface [S] |
| 00068CH | AWR3 [R/W] W<br>----XXXX XXXXXXXX XXXXXXXX XXXXX-X- | | | | |
| 000690H to 0006FCH | — | — | — | — | Reserved [S] |
| 000700H to 00070CH | — | — | — | — | Reserved |
| 000710H | BPCCRA [R/W] B<br>00000000 | BPCCRB [R/W] B<br>00000000 | BPCCRC [R/W] B<br>00000000 | — | Bus Performance Counter |
| 000714H | BPCTRA [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000718H | BPCTRB [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 00071CH | BPCTRC [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000720H to 0007F8H | — | — | — | — | Reserved |
| 0007FCH | BMODR [R] B, H, W<br>XXXXXXXX | — | — | — | Mode Register |
| 000800H to 00083CH | — | — | — | — | Reserved [S] |
| 000840H | FCTLR [R/W] H<br>-0--1000 0--0---- | | — | FSTR [R/W] B<br>-----001 | Flash Memory Register [S] |
| 000844H to 000854H | — | — | — | — | Reserved [S] |
| 000858H | — | — | WREN [R/W] H<br>00000000 00000000 | | Wild Register [S] |
| 00085CH to 00087CH | — | — | — | — | Reserved [S] |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000880H | WRAR00 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | Wild Register [S] |
| 000884H | WRDR00 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000888H | WRAR01 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 00088CH | WRDR01 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000890H | WRAR02 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | Wild Register [S] |
| 000894H | WRDR02 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000898H | WRAR03 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 00089CH | WRDR03 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008A0H | WRAR04 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008A4H | WRDR04 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008A8H | WRAR05 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008ACH | WRDR05 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008B0H | WRAR06 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008B4H | WRDR06 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008B8H | WRAR07 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008BCH | WRDR07 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008C0H | WRAR08 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008C4H | WRDR08 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008C8H | WRAR09 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008CCH | WRDR09 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008D0H | WRAR10 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008D4H | WRDR10 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008D8H | WRAR11 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008DCH | WRDR11 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008E0H | WRAR12 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0008E4H | WRDR12 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Wild Register [S] |
| 0008E8H | WRAR13 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008ECH | WRDR13 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0008F0H | WRAR14 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008F4H | WRDR14 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Wild Register [S] |
| 0008F8H | WRAR15 [R/W] W<br>-------- --XXXXXX XXXXXXXX XXXXXX-- | | | | |
| 0008FCH | WRDR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000900H | TPUUNLOCK [R/W] W<br>00000000 00000000 00000000 00000000 | | | | Time Protection Unit [S] |
| 000904H | TPULST [R] B,H,W<br>-------0 | — | TPUVST [R/W] B,H,W<br>-----000 | — | |
| 000908H | TPUCFG [R/W] B,H,W<br>-------0 0-000000 -------- -------0 | | | | |
| 00090CH | TPUTIR [R] B,H,W<br>00000000 | — | — | — | |
| 000910H | TPUTST [R] B,H,W<br>00000000 | — | — | — | |
| 000914H | TPUTIE [R/W] B,H,W<br>00000000 | — | — | — | |
| 000918H | TPUTMID [R] B,H,W<br>00000000 00000000 00000000 00000000 | | | | |
| 00091CH to 00092CH | — | — | — | — | |
| 000930H | TPUTCN00 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000934H | TPUTCN01 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000938H | TPUTCN02 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 00093CH | TPUTCN03 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000940H | TPUTCN04 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000944H | TPUTCN05 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000948H | TPUTCN06 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 00094CH | TPUTCN07 [R/W] B,H,W<br>000000-- 00000000 00000000 00000000 | | | | |
| 000950H | TPUTCN10 [R/W] B,H,W<br>---00000 | — | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000954H | TPUTCN11 [R/W] B,H,W ---00000 | — | — | — | Time Protection Unit [S] |
| 000958H | TPUTCN12 [R/W] B,H,W ---00000 | — | — | — | |
| 00095CH | TPUTCN13 [R/W] B,H,W ---00000 | — | — | — | |
| 000960H | TPUTCN14 [R/W] B,H,W ---00000 | — | — | — | |
| 000964H | TPUTCN15 [R/W] B,H,W ---00000 | — | — | — | |
| 000968H | TPUTCN16 [R/W] B,H,W ---00000 | — | — | — | |
| 00096CH | TPUTCN17 [R/W] B,H,W ---00000 | — | — | — | |
| 000970H | TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000974H | TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000978H | TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 00097CH | TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000980H | TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000984H | TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000988H | TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 00098CH | TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000 | | | | |
| 000990H to 0009FCH | — | — | — | — | |
| 000A00H to 000BECH | — | — | — | — | Reserved |
| 000BF0H | HSCFR [R/W] B,H,W -------- ------00 00000000 00000000 | | | | OCDU |
| 000BF4H | — | — | — | — | |
| 000BF8H | — | — | MBR [R/W] B,H,W 00------ XXXXXXXX | | OCDU |
| 000BFCH | — | — | UER [W] B,H,W -------- -------X | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000C00H | DCCR0 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | DMA Controller [S] |
| 000C04H | DCSR0 [R/W] H<br>0------- -----000 | | DTCR0 [R/W] H<br>00000000 00000000 | | |
| 000C08H | DSAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C0CH | DDAR0 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C10H | DCCR1 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C14H | DCSR1 [R/W] H<br>0------- -----000 | | DTCR1 [R/W] H<br>00000000 00000000 | | |
| 000C18H | DSAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C1CH | DDAR1 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C20H | DCCR2 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C24H | DCSR2 [R/W] H<br>0------- -----000 | | DTCR2 [R/W] H<br>00000000 00000000 | | |
| 000C28H | DSAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C2CH | DDAR2 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C30H | DCCR3 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C34H | DCSR3 [R/W] H<br>0------- -----000 | | DTCR3 [R/W] H<br>00000000 00000000 | | |
| 000C38H | DSAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C3CH | DDAR3 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C40H | DCCR4 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C44H | DCSR4 [R/W] H<br>0------- -----000 | | DTCR4 [R/W] H<br>00000000 00000000 | | |
| 000C48H | DSAR4 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C4CH | DDAR4 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C50H | DCCR5 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C54H | DCSR5 [R/W] H<br>0------- -----000 | | DTCR5 [R/W] H<br>00000000 00000000 | | |
| 000C58H | DSAR5 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C5CH | DDAR5 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C60H | DCCR6 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000C64H | DCSR6 [R/W] H<br>0------- -----000 | | DTCR6 [R/W] H<br>00000000 00000000 | | DMA Controller [S] |
| 000C68H | DSAR6 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C6CH | DDAR6 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C70H | DCCR7 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C74H | DCSR7 [R/W] H<br>0------- -----000 | | DTCR7 [R/W] H<br>00000000 00000000 | | |
| 000C78H | DSAR7 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C7CH | DDAR7 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C80H | DCCR8 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C84H | DCSR8 [R/W] H<br>0------- -----000 | | DTCR8 [R/W] H<br>00000000 00000000 | | |
| 000C88H | DSAR8 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C8CH | DDAR8 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C90H | DCCR9 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000C94H | DCSR9 [R/W] H<br>0------- -----000 | | DTCR9 [R/W] H<br>00000000 00000000 | | |
| 000C98H | DSAR9 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000C9CH | DDAR9 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CA0H | DCCR10 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CA4H | DCSR10 [R/W] H<br>0------- -----000 | | DTCR10 [R/W] H<br>00000000 00000000 | | |
| 000CA8H | DSAR10 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CACH | DDAR10 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CB0H | DCCR11 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CB4H | DCSR11 [R/W] H<br>0------- -----000 | | DTCR11 [R/W] H<br>00000000 00000000 | | |
| 000CB8H | DSAR11 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CBCH | DDAR11 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CC0H | DCCR12 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CC4H | DCSR12 [R/W] H<br>0------- -----000 | | DTCR12 [R/W] H<br>00000000 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000CC8H | DSAR12 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | DMA Controller [S] |
| 000CCCH | DDAR12 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CD0H | DCCR13 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CD4H | DCSR13 [R/W] H<br>0------- -----000 | | DTCR13 [R/W] H<br>00000000 00000000 | | |
| 000CD8H | DSAR13 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CDCH | DDAR13 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CE0H | DCCR14 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CE4H | DCSR14 [R/W] H<br>0------- -----000 | | DTCR14 [R/W] H<br>00000000 00000000 | | |
| 000CE8H | DSAR14 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CECH | DDAR14 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CF0H | DCCR15 [R/W] W<br>0----000 --00--00 00000000 0-000000 | | | | |
| 000CF4H | DCSR15 [R/W] H<br>0------- -----000 | | DTCR15 [R/W] H<br>00000000 00000000 | | |
| 000CF8H | DSAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000CFCH | DDAR15 [R/W] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000D00H to 000DF0H | — | — | — | — | Reserved [S] |
| 000DF4H | — | — | DNMIR [R/W] B<br>0------0 | DILVR [R/W] B<br>---11111 | DMA Controller [S] |
| 000DF8H | DMACR[R/W] W<br>0------- -------- 0------- -------- | | | | |
| 000DFCH | — | — | — | — | Reserved [S] |
| 000E00H | DDR00 [R/W] B,H,W<br>00000000 | DDR01 [R/W] B,H,W<br>00000000 | DDR02 [R/W] B,H,W<br>00000000 | DDR03 [R/W] B,H,W<br>00000000 | Data Direction Register |
| 000E04H | DDR04 [R/W] B,H,W<br>00000000 | DDR05 [R/W] B,H,W<br>00000000 | DDR06 [R/W] B,H,W<br>00000000 | DDR07 [R/W] B,H,W<br>00000000 | |
| 000E08H | DDR08 [R/W] B,H,W<br>00000000 | DDR09 [R/W] B,H,W<br>00000000 | DDR10 [R/W] B,H,W<br>00000000 | DDR11 [R/W] B,H,W<br>00000000 | Data Direction Register |
| 000E0CH | DDR12 [R/W] B,H,W<br>00000000 | DDR13 [R/W] B,H,W<br>-0000000 | DDR14 [R/W] B,H,W<br>---000-- | DDR15 [R/W] B,H,W<br>--000000 | |
| 000E10H | — | — | — | — | |
| 000E14H | — | — | — | — | |
| 000E18H | DDR16 [R/W] B,H,W<br>00000000 | DDR17 [R/W] B,H,W<br>00000000 | DDR18 [R/W] B,H,W<br>00000000 | DDR19 [R/W] B,H,W<br>00000000 | |
| 000E1CH | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000E20H | PFR00 [R/W] B,H,W<br>00000000 | PFR01 [R/W] B,H,W<br>00000000 | PFR02 [R/W] B,H,W<br>00000000 | PFR03 [R/W] B,H,W<br>00000000 | Port Function Register |
| 000E24H | PFR04 [R/W] B,H,W<br>00000000 | PFR05 [R/W] B,H,W<br>00000000 | PFR06 [R/W] B,H,W<br>00000000 | PFR07 [R/W] B,H,W<br>00000000 | |
| 000E28H | PFR08 [R/W] B,H,W<br>00000000 | PFR09 [R/W] B,H,W<br>00000000 | PFR10 [R/W] B,H,W<br>00000000 | PFR11 [R/W] B,H,W<br>00000000 | |
| 000E2CH | PFR12 [R/W] B,H,W<br>00000000 | PFR13 [R/W] B,H,W<br>-0000000 | PFR14 [R/W] B,H,W<br>---000-- | PFR15 [R/W] B,H,W<br>--000000 | |
| 000E30H | — | — | — | — | |
| 000E34H | — | — | — | — | |
| 000E38H | PFR16 [R/W] B,H,W<br>00000000 | PFR17 [R/W] B,H,W<br>00000000 | PFR18 [R/W] B,H,W<br>00000000 | PFR19 [R/W] B,H,W<br>00000000 | |
| 000E3CH | — | — | — | — | Reserved |
| 000E40H | PDDR00 [R] B,H,W<br>XXXXXXXX | PDDR01 [R] B,H,W<br>XXXXXXXX | PDDR02 [R] B,H,W<br>XXXXXXXX | PDDR03 [R] B,H,W<br>XXXXXXXX | Port Direct Read Register |
| 000E44H | PDDR04 [R] B,H,W<br>XXXXXXXX | PDDR05 [R] B,H,W<br>XXXXXXXX | PDDR06 [R] B,H,W<br>XXXXXXXX | PDDR07 [R] B,H,W<br>XXXXXXXX | |
| 000E48H | PDDR08 [R] B,H,W<br>XXXXXXXX | PDDR09 [R] B,H,W<br>XXXXXXXX | PDDR10 [R] B,H,W<br>XXXXXXXX | PDDR11 [R] B,H,W<br>XXXXXXXX | |
| 000E4CH | PDDR12 [R] B,H,W<br>XXXXXXXX | PDDR13 [R] B,H,W<br>-XXXXXXX | PDDR14 [R] B,H,W<br>---XXX-- | PDDR15 [R] B,H,W<br>--XXXXXX | |
| 000E50H | — | — | — | — | |
| 000E54H | — | — | — | — | |
| 000E58H | PDDR16 [R] B,H,W<br>XXXXXXXX | PDDR17 [R] B,H,W<br>XXXXXXXX | PDDR18 [R] B,H,W<br>XXXXXXXX | PDDR19 [R] B,H,W<br>XXXXXXXX | |
| 000E5CH | — | — | — | — | Reserved |
| 000E60H | EPFR00 [R/W]<br>B,H,W<br>00000000 | EPFR01 [R/W]<br>B,H,W<br>-0-0-000 | EPFR02 [R/W]<br>B,H,W<br>----0000 | EPFR03 [R/W]<br>B,H,W<br>---000-0 | Extended Port Function Register |
| 000E64H | EPFR04 [R/W]<br>B,H,W<br>----00-0 | EPFR05 [R/W]<br>B,H,W<br>----0000 | EPFR06 [R/W]<br>B,H,W<br>----000- | EPFR07 [R/W]<br>B,H,W<br>---00000 | |
| 000E68H | EPFR08 [R/W]<br>B,H,W<br>---00000 | EPFR09 [R/W]<br>B,H,W<br>-----00- | EPFR10 [R/W]<br>B,H,W<br>----0000 | EPFR11 [R/W]<br>B,H,W<br>----0000 | |
| 000E6CH | EPFR12 [R/W]<br>B,H,W<br>----0000 | EPFR13 [R/W]<br>B,H,W<br>------00 | EPFR14 [R/W]<br>B,H,W<br>------00 | EPFR15 [R/W]<br>B,H,W<br>-----000 | |
| 000E70H | — | — | — | — | |
| 000E74H | — | — | — | — | |
| 000E78H | — | — | EPFR26 [R/W]<br>B,H,W<br>00000000 | EPFR27 [R/W]<br>B,H,W<br>---0---- | |
| 000E7CH | EPFR28 [R/W]<br>B,H,W<br>--000-0- | EPFR29 [R/W]<br>B,H,W<br>00000000 | — | — | |
| 000E80H | — | EPFR33 [R/W]<br>B,H,W<br>-----00- | EPFR34 [R/W]<br>B,H,W<br>-----00- | EPFR35 [R/W]<br>B,H,W<br>---00000 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000E84H | EPFR36 [R/W]<br>B,H,W<br>----000- | — | — | — | Extended Port Function Register |
| 000E88H | — | — | EPFR42 [R/W]<br>B,H,W<br>------00 | EPFR43 [R/W]<br>B,H,W<br>0--0000- | |
| 000E8CH | EPFR44 [R/W]<br>B,H,W<br>-00---0- | EPFR45 [R/W]<br>B,H,W<br>-0000000 | — | — | |
| 000E90H | — | — | — | — | |
| 000E94H | — | — | — | — | |
| 000E98H | EPFR56 [R/W]<br>B,H,W<br>-----0-0 | EPFR57 [R/W]<br>B,H,W<br>----00-0 | EPFR58 [R/W]<br>B,H,W<br>----00-0 | EPFR59 [R/W]<br>B,H,W<br>----00-0 | |
| 000E9CH | EPFR60 [R/W]<br>B,H,W<br>----00-0 | EPFR61 [R/W]<br>B,H,W<br>-----00- | EPFR62 [R/W]<br>B,H,W<br>-----00- | EPFR63 [R/W]<br>B,H,W<br>---0000- | |
| 000EA0H to 000EBCH | — | — | — | — | Reserved |
| 000EC0H | PPER00 [R/W]<br>B,H,W<br>00000000 | PPER01 [R/W]<br>B,H,W<br>00000000 | PPER02 [R/W]<br>B,H,W<br>00000000 | PPER03 [R/W]<br>B,H,W<br>00000000 | Port Pull-up/down Enable Register |
| 000EC4H | PPER04 [R/W]<br>B,H,W<br>00000000 | PPER05 [R/W]<br>B,H,W<br>00000000 | PPER06 [R/W]<br>B,H,W<br>00000000 | PPER07 [R/W]<br>B,H,W<br>00000000 | |
| 000EC8H | PPER08 [R/W]<br>B,H,W<br>00000000 | PPER09 [R/W]<br>B,H,W<br>00000000 | PPER10 [R/W]<br>B,H,W<br>00000000 | PPER11 [R/W]<br>B,H,W<br>00000000 | |
| 000ECCH | PPER12 [R/W]<br>B,H,W<br>00000000 | PPER13 [R/W]<br>B,H,W<br>-0000000 | PPER14 [R/W]<br>B,H,W<br>---000-- | PPER15 [R/W]<br>B,H,W<br>--000000 | |
| 000ED0H | — | — | — | — | |
| 000ED4H | — | — | — | — | |
| 000ED8H | PPER16 [R/W]<br>B,H,W<br>00000000 | PPER17 [R/W]<br>B,H,W<br>00000000 | PPER18 [R/W]<br>B,H,W<br>00000000 | PPER19 [R/W]<br>B,H,W<br>00000000 | |
| 000EDCH to 000F3CH | — | — | — | — | Reserved |
| 000F40H | PORTEN [R/W]<br>B,H,W<br>-------0 | — | — | — | Port Enable Register |
| 000F44H | KEYCDR [R/W] H<br>00000000 00000000 | | — | — | KeyCodeRegister |
| 000F48H to 000F64H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000F68H | MSCY6 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 6,7 Cycle measurement data register 67 |
| 000F6CH | MSCY7 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000F70H | RCRH0 [W] H,W<br>XXXXXXXX | RCRL0 [W] B,H,W<br>XXXXXXXX | UDCRH0 [R] H,W<br>00000000 | UDCRL0 [R] B,H,W<br>00000000 | Up/Down Counter 0 |
| 000F74H | CCR0 [R/W] B,H<br>00000000 -0001000 | | — | CSR0 [R/W] B<br>00000000 | |
| 000F78H to 000F7CH | — | — | — | — | Reserved |
| 000F80H | RCRH1 [W] H,W<br>XXXXXXXX | RCRL1 [W] B,H,W<br>XXXXXXXX | UDCRH1 [R] H,W<br>00000000 | UDCRL1 [R] B,H,W<br>00000000 | Up/Down Counter 1 |
| 000F84H | CCR1 [R/W] B,H<br>00000000 -0001000 | | — | CSR1 [R/W] B<br>00000000 | |
| 000F88H | — | — | MSCH45 [R] B,H,W<br>00000000 | MSCL45 [R/W] B,H,W<br>------00 | Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45 |
| 000F8CH | — | — | MSCH67 [R] B,H,W<br>00000000 | MSCL67 [R/W] B,H,W<br>------00 | Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67 |
| 000F90H | OCCP10 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | Output Compare 10,11 32-bit OCU |
| 000F94H | OCCP11 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000F98H | — | — | OCSH1011 [R/W] B,H,W<br>---0--00 | OCSL1011 [R/W] B,H,W<br>0000--00 | Output Compare 10,11 32-bit OCU |
| 000F9CH | — | — | — | OCLS1011 [R/W] B,H,W<br>----0000 | OCU1011 Output level control register |
| 000FA0H | CPCLR5 [R/W] W<br>11111111 11111111 11111111 11111111 | | | | Free-run Timer 5 32-bit FRT |
| 000FA4H | TCDT5 [R/W] W<br>00000000 00000000 00000000 00000000 | | | | |
| 000FA8H | TCCSH5 [R/W]B,H,W<br>0-----00 | TCCSL5 [R/W]B,H,W<br>-1-00000 | — | — | |
| 000FACH to 000FCCH | — | — | — | — | Reserved |
| 000FD0H | IPCP4 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 4,5 32-bit ICU |
| 000FD4H | IPCP5 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000FD8H | — | — | LSYNS1 [R/W] B,H,W<br>00000000 | ICS45 [R/W] B,H,W<br>00000000 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 000FDC$_H$ | IPCP6 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 6,7 32-bit ICU |
| 000FE0$_H$ | IPCP7 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000FE4$_H$ | — | — | — | ICS67 [R/W] B,H,W<br>00000000 | |
| 000FE8$_H$ | IPCP8 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 8,9 32-bit ICU |
| 000FEC$_H$ | IPCP9 [R] W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000FF0$_H$ | — | — | — | ICS89 [R/W] B,H,W<br>00000000 | |
| 000FF4$_H$ | MSCY8 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Input Capture 8,9 32-bit ICU Cycle measurement data register 89 |
| 000FF8$_H$ | MSCY9 [R] H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000FFC$_H$ | — | — | MSCH89 [R] B,H,W<br>00000000 | MSCL89 [R/W] B,H,W<br>------00 | Cycle and pulse width measurement control 89 |
| 001000$_H$ | SACR [R/W] B,H,W<br>-------0 | PICD [R/W] B,H,W<br>----0011 | — | — | Clock Control |
| 001004$_H$ to 00112C$_H$ | — | — | — | — | Reserved |
| 001130$_H$ | — | — | — | CRCCR [R/W] B,H,W<br>-0000000 | CRC calculation unit |
| 001134$_H$ | CRCINIT [R/W] B,H,W<br>11111111 11111111 11111111 11111111 | | | | |
| 001138$_H$ | CRCIN [R/W] B,H,W<br>00000000 00000000 00000000 00000000 | | | | |
| 00113C$_H$ | CRCR [R] B,H,W<br>11111111 11111111 11111111 11111111 | | | | |
| 001140$_H$ to 0011FC$_H$ | — | — | — | — | Reserved |
| 001200$_H$ | TCGS [R/W] B,H,W<br>------00 | — | — | TCGSE [R/W] B,H,W<br>-----000 | 16-bit Free-run timer synchronous activation |
| 001204$_H$ | CPCLRB0/CPCLR0 [W] H,W<br>11111111 11111111 | | TCDT0 [R/W] H,W<br>00000000 00000000 | | 16-bit Free-run Timer 0 |
| 001208$_H$ | TCCS0 [R/W] B,H,W<br>00000000 01000000 ----0000 -------- | | | | |
| 00120C$_H$ | CPCLRB1/CPCLR1 [W] H,W<br>11111111 11111111 | | TCDT1 [R/W] H,W<br>00000000 00000000 | | 16-bit Free-run Timer 1 |
| 001210$_H$ | TCCS1 [R/W] B,H,W<br>00000000 01000000 ----0000 -------- | | | | |
| 001214$_H$ | CPCLRB2/CPCLR2 [W] H,W<br>11111111 11111111 | | TCDT2 [R/W] H,W<br>00000000 00000000 | | 16-bit Free-run Timer 2 |
| 001218$_H$ | TCCS2 [R/W] B,H,W<br>00000000 01000000 ----0000 -------- | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 00121C$_H$ to 001230$_H$ | — | — | — | — | Reserved |
| 001234$_H$ | FRS0 [R/W] B,H,W<br>-------- --00--00 --00--00 --00--00 | | | | 16-bit Free-run timer selection |
| 001238$_H$ | — | | FRS1 [R/W] B,H,W<br>--00--00 --00--00 | | |
| 00123C$_H$ | FRS2 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | |
| 001240$_H$ | FRS3 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | |
| 001244$_H$ | FRS4 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | |
| 001248$_H$ | — | — | — | — | Reserved |
| 00124C$_H$ | OCCPB0/OCCP0 [R/W] H,W<br>00000000 00000000 | | OCCPB1/OCCP1 [R/W] H,W<br>00000000 00000000 | | 16-bit Output compare 0/1 |
| 001250$_H$ | OCS01 [R/W] B,H,W<br>-110--00 00001100 | | — | OCMOD01 [R/W] B,H,W<br>------00 | |
| 001254$_H$ | OCCPB2/OCCP2 [R/W] H,W<br>00000000 00000000 | | OCCPB3/OCCP3 [R/W] H,W<br>00000000 00000000 | | 16-bit Output compare 2/3 |
| 001258$_H$ | OCS23 [R/W] B,H,W<br>-110--00 00001100 | | — | OCMOD23 [R/W] B,H,W<br>------00 | |
| 00125C$_H$ | OCCPB4/OCCP4 [R/W] H,W<br>00000000 00000000 | | OCCPB5/OCCP5 [R/W] H,W<br>00000000 00000000 | | 16-bit Output compare 4/5 |
| 001260$_H$ | OCS45 [R/W] B,H,W<br>-110--00 00001100 | | — | OCMOD45 [R/W] B,H,W<br>------00 | |
| 001264$_H$ to 001278$_H$ | — | — | — | — | Reserved |
| 00127C$_H$ | IPCP0 [R] H,W<br>00000000 00000000 | | IPCP1 [R] H,W<br>00000000 00000000 | | 16-bit Input capture 0/1 |
| 001280$_H$ | ICS01 [R/W] B,H,W<br>------00 00000000 | | — | LSYNS [R/W] B,H,W<br>----0000 | |
| 001284$_H$ | IPCP2 [R] H,W<br>00000000 00000000 | | IPCP3 [R] H,W<br>00000000 00000000 | | 16-bit Input capture 2/3 |
| 001288$_H$ | ICS23 [R/W] B,H,W<br>------00 00000000 | | — | — | |
| 00128C$_H$ to 001298$_H$ | — | — | — | — | Reserved |
| 00129C$_H$ | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0012A0H | TMRR0 [R/W] H,W<br>00000000 00000001 | | TMRR1 [R/W] H,W<br>00000000 00000001 | | Waveform generator 0/1/2 |
| 0012A4H | TMRR2 [R/W] H,W<br>00000000 00000001 | | — | — | |
| 0012A8H | DTSCR0 [R/W]<br>B,H,W<br>00000000 | DTSCR1 [R/W]<br>B,H,W<br>00000000 | DTSCR2 [R/W]<br>B,H,W<br>00000000 | — | |
| 0012ACH | — | DTIR0 [R/W] B,H,W<br>000000-- | — | DTMNS0 [R/W]<br>B,H,W<br>00---000 | |
| 0012B0H | — | SIGCR10 [R/W]<br>B,H,W<br>00000000 | — | SIGCR20 [R/W]<br>B,H,W<br>000000-1 | |
| 0012B4H | PICS0 [R/W] B,H,W<br>000000-- -------- -------- -------- | | | | |
| 0012B8H<br>to<br>0012CCH | — | — | — | — | Reserved |
| 0012D0H | FRS5 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | 16-bit Free-run timer selection<br>A/D activation compare |
| 0012D4H | FRS6 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | 16-bit Free-run timer selection<br>A/D activation compare |
| 0012D8H | FRS7 [R/W] B,H,W<br>--00--00 --00--00 --00--00 --00--00 | | | | |
| 0012DCH<br>to<br>0012FCH | — | — | — | — | Reserved |
| 001300H | — | | | | Reserved |
| 001304H | ADTSS0[R/W]<br>B,H,W<br>-------0 | — | — | — | 12-bit A/D converter 1/2 unit |
| 001308H | ADTSE0[R/W] B,H,W<br>00000000 00000000 00000000 00000000 | | | | |
| 00130CH | ADCOMP0/ADCOMPB0[R/W] H,W<br>00000000 00000000 | | ADCOMP1/ADCOMPB1[R/W] H,W<br>00000000 00000000 | | |
| 001310H | ADCOMP2/ADCOMPB2[R/W] H,W<br>00000000 00000000 | | ADCOMP3/ADCOMPB3[R/W] H,W<br>00000000 00000000 | | |
| 001314H | ADCOMP4/ADCOMPB4[R/W] H,W<br>00000000 00000000 | | ADCOMP5/ADCOMPB5[R/W] H,W<br>00000000 00000000 | | |
| 001318H | ADCOMP6/ADCOMPB6[R/W] H,W<br>00000000 00000000 | | ADCOMP7/ADCOMPB7[R/W] H,W<br>00000000 00000000 | | |
| 00131CH | ADCOMP8/ADCOMPB8[R/W] H,W<br>00000000 00000000 | | ADCOMP9/ADCOMPB9[R/W] H,W<br>00000000 00000000 | | |
| 001320H | ADCOMP10/ADCOMPB10[R/W] H,W<br>00000000 00000000 | | ADCOMP11/ADCOMPB11[R/W] H,W<br>00000000 00000000 | | |
| 001324H | ADCOMP12/ADCOMPB12[R/W] H,W<br>00000000 00000000 | | ADCOMP13/ADCOMPB13[R/W] H,W<br>00000000 00000000 | | |
| 001328H | ADCOMP14/ADCOMPB14[R/W] H,W<br>00000000 00000000 | | ADCOMP15/ADCOMPB15[R/W] H,W<br>00000000 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 00132C$_H$ | ADCOMP16/ADCOMPB16[R/W] H,W<br>00000000 00000000 | | ADCOMP17/ADCOMPB17[R/W] H,W<br>00000000 00000000 | | 12-bit A/D converter 1/2 unit |
| 001330$_H$ | ADCOMP18/ADCOMPB18[R/W] H,W<br>00000000 00000000 | | ADCOMP19/ADCOMPB19[R/W] H,W<br>00000000 00000000 | | |
| 001334$_H$ | ADCOMP20/ADCOMPB20[R/W] H,W<br>00000000 00000000 | | ADCOMP21/ADCOMPB21[R/W] H,W<br>00000000 00000000 | | |
| 001338$_H$ | ADCOMP22/ADCOMPB22[R/W] H,W<br>00000000 00000000 | | ADCOMP23/ADCOMPB23[R/W] H,W<br>00000000 00000000 | | |
| 00133C$_H$ | ADCOMP24/ADCOMPB24[R/W] H,W<br>00000000 00000000 | | ADCOMP25/ADCOMPB25[R/W] H,W<br>00000000 00000000 | | |
| 001340$_H$ | ADCOMP26/ADCOMPB26[R/W] H,W<br>00000000 00000000 | | ADCOMP27/ADCOMPB27[R/W] H,W<br>00000000 00000000 | | |
| 001344$_H$ | ADCOMP28/ADCOMPB28[R/W] H,W<br>00000000 00000000 | | ADCOMP29/ADCOMPB29[R/W] H,W<br>00000000 00000000 | | |
| 001348$_H$ | ADCOMP30/ADCOMPB30[R/W] H,W<br>00000000 00000000 | | ADCOMP31/ADCOMPB31[R/W] H,W<br>00000000 00000000 | | |
| 00134C$_H$ | ADTCS0[R/W] B,H,W<br>00000000 0010---- | | ADTCS1[R/W] B,H,W<br>00000000 0010---- | | |
| 001350$_H$ | ADTCS2[R/W] B,H,W<br>00000000 0010---- | | ADTCS3[R/W] B,H,W<br>00000000 0010---- | | |
| 001354$_H$ | ADTCS4[R/W] B,H,W<br>00000000 0010---- | | ADTCS5[R/W] B,H,W<br>00000000 0010---- | | |
| 001358$_H$ | ADTCS6[R/W] B,H,W<br>00000000 0010---- | | ADTCS7[R/W] B,H,W<br>00000000 0010---- | | |
| 00135C$_H$ | ADTCS8[R/W] B,H,W<br>00000000 0010---- | | ADTCS9[R/W] B,H,W<br>00000000 0010---- | | |
| 001360$_H$ | ADTCS10[R/W] B,H,W<br>00000000 0010---- | | ADTCS11[R/W] B,H,W<br>00000000 0010---- | | |
| 001364$_H$ | ADTCS12[R/W] B,H,W<br>00000000 0010---- | | ADTCS13[R/W] B,H,W<br>00000000 0010---- | | |
| 001368$_H$ | ADTCS14[R/W] B,H,W<br>00000000 0010---- | | ADTCS15[R/W] B,H,W<br>00000000 0010---- | | |
| 00136C$_H$ | ADTCS16[R/W] B,H,W<br>00000000 0010---- | | ADTCS17[R/W] B,H,W<br>00000000 0010---- | | |
| 001370$_H$ | ADTCS18[R/W] B,H,W<br>00000000 0010---- | | ADTCS19[R/W] B,H,W<br>00000000 0010---- | | |
| 001374$_H$ | ADTCS20[R/W] B,H,W<br>00000000 0010---- | | ADTCS21[R/W] B,H,W<br>00000000 0010---- | | |
| 001378$_H$ | ADTCS22[R/W] B,H,W<br>00000000 0010---- | | ADTCS23[R/W] B,H,W<br>00000000 0010---- | | |
| 00137C$_H$ | ADTCS24[R/W] B,H,W<br>00000000 0010---- | | ADTCS25[R/W] B,H,W<br>00000000 0010---- | | |
| 001380$_H$ | ADTCS26[R/W] B,H,W<br>00000000 0010---- | | ADTCS27[R/W] B,H,W<br>00000000 0010---- | | |
| 001384$_H$ | ADTCS28[R/W] B,H,W<br>00000000 0010---- | | ADTCS29[R/W] B,H,W<br>00000000 0010---- | | |
| 001388$_H$ | ADTCS30[R/W] B,H,W<br>00000000 0010---- | | ADTCS31[R/W] B,H,W<br>00000000 0010---- | | |
| 00138C$_H$ | ADTCD0[R] B,H,W<br>10--0000 00000000 | | ADTCD1[R] B,H,W<br>10--0000 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001390H | ADTCD2[R] B,H,W<br>10--0000 00000000 | | ADTCD3[R] B,H,W<br>10--0000 00000000 | | 12-bit A/D converter 1/2 unit |
| 001394H | ADTCD4[R] B,H,W<br>10--0000 00000000 | | ADTCD5[R] B,H,W<br>10--0000 00000000 | | |
| 001398H | ADTCD6[R] B,H,W<br>10--0000 00000000 | | ADTCD7[R] B,H,W<br>10--0000 00000000 | | |
| 00139CH | ADTCD8[R] B,H,W<br>10--0000 00000000 | | ADTCD9[R] B,H,W<br>10--0000 00000000 | | |
| 0013A0H | ADTCD10[R] B,H,W<br>10--0000 00000000 | | ADTCD11[R] B,H,W<br>10--0000 00000000 | | |
| 0013A4H | ADTCD12[R] B,H,W<br>10--0000 00000000 | | ADTCD13[R] B,H,W<br>10--0000 00000000 | | |
| 0013A8H | ADTCD14[R] B,H,W<br>10--0000 00000000 | | ADTCD15[R] B,H,W<br>10--0000 00000000 | | |
| 0013ACH | ADTCD16[R] B,H,W<br>10--0000 00000000 | | ADTCD17[R] B,H,W<br>10--0000 00000000 | | |
| 0013B0H | ADTCD18[R] B,H,W<br>10--0000 00000000 | | ADTCD19[R] B,H,W<br>10--0000 00000000 | | |
| 0013B4H | ADTCD20[R] B,H,W<br>10--0000 00000000 | | ADTCD21[R] B,H,W<br>10--0000 00000000 | | |
| 0013B8H | ADTCD22[R] B,H,W<br>10--0000 00000000 | | ADTCD23[R] B,H,W<br>10--0000 00000000 | | |
| 0013BCH | ADTCD24[R] B,H,W<br>10--0000 00000000 | | ADTCD25[R] B,H,W<br>10--0000 00000000 | | |
| 0013C0H | ADTCD26[R] B,H,W<br>10--0000 00000000 | | ADTCD27[R] B,H,W<br>10--0000 00000000 | | |
| 0013C4H | ADTCD28[R] B,H,W<br>10--0000 00000000 | | ADTCD29[R] B,H,W<br>10--0000 00000000 | | |
| 0013C8H | ADTCD30[R] B,H,W<br>10--0000 00000000 | | ADTCD31[R] B,H,W<br>10--0000 00000000 | | |
| 0013CCH | ADTECS0[R/W] B,H,W<br>-------0 ---00000 | | ADTECS1[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013D0H | ADTECS2[R/W] B,H,W<br>-------0 ---00000 | | ADTECS3[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013D4H | ADTECS4[R/W] B,H,W<br>-------0 ---00000 | | ADTECS5[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013D8H | ADTECS6[R/W] B,H,W<br>-------0 ---00000 | | ADTECS7[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013DCH | ADTECS8[R/W] B,H,W<br>-------0 ---00000 | | ADTECS9[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013E0H | ADTECS10[R/W] B,H,W<br>-------0 ---00000 | | ADTECS11[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013E4H | ADTECS12[R/W] B,H,W<br>-------0 ---00000 | | ADTECS13[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013E8H | ADTECS14[R/W] B,H,W<br>-------0 ---00000 | | ADTECS15[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013ECH | ADTECS16[R/W] B,H,W<br>-------0 ---00000 | | ADTECS17[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013F0H | ADTECS18[R/W] B,H,W<br>-------0 ---00000 | | ADTECS19[R/W] B,H,W<br>-------0 ---00000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0013F4H | ADTECS20[R/W] B,H,W<br>-------0 ---00000 | | ADTECS21[R/W] B,H,W<br>-------0 ---00000 | | 12-bit A/D converter 1/2 unit |
| 0013F8H | ADTECS22[R/W] B,H,W<br>-------0 ---00000 | | ADTECS23[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013FCH | ADTECS24[R/W] B,H,W<br>-------0 ---00000 | | ADTECS25[R/W] B,H,W<br>-------0 ---00000 | | |
| 001400H | ADTECS26[R/W] B,H,W<br>-------0 ---00000 | | ADTECS27[R/W] B,H,W<br>-------0 ---00000 | | |
| 001404H | ADTECS28[R/W] B,H,W<br>-------0 ---00000 | | ADTECS29[R/W] B,H,W<br>-------0 ---00000 | | |
| 001408H | ADTECS30[R/W] B,H,W<br>-------0 ---00000 | | ADTECS31[R/W] B,H,W<br>-------0 ---00000 | | |
| 00140CH | ADRCUT0[R/W] B,H,W<br>----0000 00000000 | | ADRCLT0[R/W] B,H,W<br>----0000 00000000 | | |
| 001410H | ADRCUT1[R/W] B,H,W<br>----0000 00000000 | | ADRCLT1[R/W] B,H,W<br>----0000 00000000 | | |
| 001414H | ADRCUT2[R/W] B,H,W<br>----0000 00000000 | | ADRCLT2[R/W] B,H,W<br>----0000 00000000 | | |
| 001418H | ADRCUT3[R/W] B,H,W<br>----0000 00000000 | | ADRCLT3[R/W] B,H,W<br>----0000 00000000 | | |
| 00141CH | ADRCCS0[R/W]<br>B,H,W<br>00000000 | ADRCCS1[R/W]<br>B,H,W<br>00000000 | ADRCCS2[R/W]<br>B,H,W<br>00000000 | ADRCCS3[R/W]<br>B,H,W<br>00000000 | |
| 001420H | ADRCCS4[R/W]<br>B,H,W<br>00000000 | ADRCCS5[R/W]<br>B,H,W<br>00000000 | ADRCCS6[R/W]<br>B,H,W<br>00000000 | ADRCCS7[R/W]<br>B,H,W<br>00000000 | |
| 001424H | ADRCCS8[R/W]<br>B,H,W<br>00000000 | ADRCCS9[R/W]<br>B,H,W<br>00000000 | ADRCCS10[R/W]<br>B,H,W<br>00000000 | ADRCCS11[R/W]<br>B,H,W<br>00000000 | |
| 001428H | ADRCCS12[R/W]<br>B,H,W<br>00000000 | ADRCCS13[R/W]<br>B,H,W<br>00000000 | ADRCCS14[R/W]<br>B,H,W<br>00000000 | ADRCCS15[R/W]<br>B,H,W<br>00000000 | |
| 00142CH | ADRCCS16[R/W]<br>B,H,W<br>00000000 | ADRCCS17[R/W]<br>B,H,W<br>00000000 | ADRCCS18[R/W]<br>B,H,W<br>00000000 | ADRCCS19[R/W]<br>B,H,W<br>00000000 | |
| 001430H | ADRCCS20[R/W]<br>B,H,W<br>00000000 | ADRCCS21[R/W]<br>B,H,W<br>00000000 | ADRCCS22[R/W]<br>B,H,W<br>00000000 | ADRCCS23[R/W]<br>B,H,W<br>00000000 | |
| 001434H | ADRCCS24[R/W]<br>B,H,W<br>00000000 | ADRCCS25[R/W]<br>B,H,W<br>00000000 | ADRCCS26[R/W]<br>B,H,W<br>00000000 | ADRCCS27[R/W]<br>B,H,W<br>00000000 | |
| 001438H | ADRCCS28[R/W]<br>B,H,W<br>00000000 | ADRCCS29[R/W]<br>B,H,W<br>00000000 | ADRCCS30[R/W]<br>B,H,W<br>00000000 | ADRCCS31[R/W]<br>B,H,W<br>00000000 | |
| 00143CH | ADRCOT0[R] B,H,W<br>00000000 00000000 00000000 00000000 | | | | |
| 001440H | ADRCIF0[R,W] B,H,W<br>00000000 00000000 00000000 00000000 | | | | |
| 001444H | ADSCANS0[R/W]<br>B,H,W<br>000----- | — | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001448H | ADNCS0[R/W] B,H,W 0-000-00 | ADNCS1[R/W] B,H,W 0-000-00 | ADNCS2[R/W] B,H,W 0-000-00 | ADNCS3[R/W] B,H,W 0-000-00 | 12-bit A/D converter 1/2 unit |
| 00144CH | ADNCS4[R/W] B,H,W 0-000-00 | ADNCS5[R/W] B,H,W 0-000-00 | ADNCS6[R/W] B,H,W 0-000-00 | ADNCS7[R/W] B,H,W 0-000-00 | |
| 001450H | ADNCS8[R/W] B,H,W 0-000-00 | ADNCS9[R/W] B,H,W 0-000-00 | ADNCS10[R/W] B,H,W 0-000-00 | ADNCS11[R/W] B,H,W 0-000-00 | |
| 001454H | ADNCS12[R/W] B,H,W 0-000-00 | ADNCS13[R/W] B,H,W 0-000-00 | ADNCS14[R/W] B,H,W 0-000-00 | ADNCS15[R/W] B,H,W 0-000-00 | |
| 001458H | ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000 | | | | |
| 00145CH | ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111 | | | | |
| 001460H | ADCS0[R] B,H,W 0------- -------- | | ADCH0[R] B,H,W ---00000 | ADMD0[R/W] B,H,W 0---0000 | |
| 001464H | ADSTPCS0[R/W] B,H,W 00000000 | ADSTPCS1[R/W] B,H,W 00000000 | ADSTPCS2[R/W] B,H,W 00000000 | ADSTPCS3[R/W] B,H,W 00000000 | |
| 001468H | ADSTPCS4[R/W] B,H,W 00000000 | ADSTPCS5[R/W] B,H,W 00000000 | ADSTPCS6[R/W] B,H,W 00000000 | ADSTPCS7[R/W] B,H,W 00000000 | |
| 00146CH | — | | | | 12-bit A/D converter 2/2 unit |
| 001470H | ADTSS1[R/W] B,H,W -------0 | — | — | — | |
| 001474H | ADTSE1[R/W] B,H,W -------- -------- 00000000 00000000 | | | | |
| 001478H | ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000 | | ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000 | | |
| 00147CH | ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000 | | ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000 | | 12-bit A/D converter 2/2 unit |
| 001480H | ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000 | | ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000 | | |
| 001484H | ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000 | | ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000 | | |
| 001488H | ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000 | | ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000 | | |
| 00148CH | ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000 | | ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000 | | |
| 001490H | ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000 | | ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000 | | |
| 001494H | ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000 | | ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000 | | |
| 001498H to 0014B4H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0014B8H | ADTCS32[R/W] B,H,W<br>00000000 0010---- | | ADTCS33[R/W] B,H,W<br>00000000 0010---- | | 12-bit A/D converter 2/2 unit |
| 0014BCH | ADTCS34[R/W] B,H,W<br>00000000 0010---- | | ADTCS35[R/W] B,H,W<br>00000000 0010---- | | |
| 0014C0H | ADTCS36[R/W] B,H,W<br>00000000 0010---- | | ADTCS37[R/W] B,H,W<br>00000000 0010---- | | |
| 0014C4H | ADTCS38[R/W] B,H,W<br>00000000 0010---- | | ADTCS39[R/W] B,H,W<br>00000000 0010---- | | |
| 0014C8H | ADTCS40[R/W] B,H,W<br>00000000 0010---- | | ADTCS41[R/W] B,H,W<br>00000000 0010---- | | |
| 0014CCH | ADTCS42[R/W] B,H,W<br>00000000 0010---- | | ADTCS43[R/W] B,H,W<br>00000000 0010---- | | |
| 0014D0H | ADTCS44[R/W] B,H,W<br>00000000 0010---- | | ADTCS45[R/W] B,H,W<br>00000000 0010---- | | |
| 0014D4H | ADTCS46[R/W] B,H,W<br>00000000 0010---- | | ADTCS47[R/W] B,H,W<br>00000000 0010---- | | |
| 0014D8H<br>to<br>0014F4H | — | — | — | — | Reserved |
| 0014F8H | ADTCD32[R] B,H,W<br>10--0000 00000000 | | ADTCD33[R] B,H,W<br>10--0000 00000000 | | 12-bit A/D converter 2/2 unit |
| 0014FCH | ADTCD34[R] B,H,W<br>10--0000 00000000 | | ADTCD35[R] B,H,W<br>10--0000 00000000 | | |
| 001500H | ADTCD36[R] B,H,W<br>10--0000 00000000 | | ADTCD37[R] B,H,W<br>10--0000 00000000 | | 12-bit A/D converter 2/2 unit |
| 001504H | ADTCD38[R] B,H,W<br>10--0000 00000000 | | ADTCD39[R] B,H,W<br>10--0000 00000000 | | |
| 001508H | ADTCD40[R] B,H,W<br>10--0000 00000000 | | ADTCD41[R] B,H,W<br>10--0000 00000000 | | |
| 00150CH | ADTCD42[R] B,H,W<br>10--0000 00000000 | | ADTCD43[R] B,H,W<br>10--0000 00000000 | | |
| 001510H | ADTCD44[R] B,H,W<br>10--0000 00000000 | | ADTCD45[R] B,H,W<br>10--0000 00000000 | | |
| 001514H | ADTCD46[R] B,H,W<br>10--0000 00000000 | | ADTCD47[R] B,H,W<br>10--0000 00000000 | | |
| 001518H<br>to<br>001534H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001538H | ADTECS32[R/W] B,H,W<br>-------0 ----0000 | | ADTECS33[R/W] B,H,W<br>-------0 ----0000 | | 12-bit A/D converter 2/2 unit |
| 00153CH | ADTECS34[R/W] B,H,W<br>-------0 ----0000 | | ADTECS35[R/W] B,H,W<br>-------0 ----0000 | | |
| 001540H | ADTECS36[R/W] B,H,W<br>-------0 ----0000 | | ADTECS37[R/W] B,H,W<br>-------0 ----0000 | | |
| 001544H | ADTECS38[R/W] B,H,W<br>-------0 ----0000 | | ADTECS39[R/W] B,H,W<br>-------0 ----0000 | | |
| 001548H | ADTECS40[R/W] B,H,W<br>-------0 ----0000 | | ADTECS41[R/W] B,H,W<br>-------0 ----0000 | | |
| 00154CH | ADTECS42[R/W] B,H,W<br>-------0 ----0000 | | ADTECS43[R/W] B,H,W<br>-------0 ----0000 | | |
| 001550H | ADTECS44[R/W] B,H,W<br>-------0 ----0000 | | ADTECS45[R/W] B,H,W<br>-------0 ----0000 | | |
| 001554H | ADTECS46[R/W] B,H,W<br>-------0 ----0000 | | ADTECS47[R/W] B,H,W<br>-------0 ----0000 | | |
| 001558H<br>to<br>001574H | — | — | — | — | Reserved |
| 001578H | ADRCUT4[R/W] B,H,W<br>----0000 00000000 | | ADRCLT4[R/W] B,H,W<br>----0000 00000000 | | 12-bit A/D converter 2/2 unit |
| 00157CH | ADRCUT5[R/W] B,H,W<br>----0000 00000000 | | ADRCLT5[R/W] B,H,W<br>----0000 00000000 | | |
| 001580H | ADRCUT6[R/W] B,H,W<br>----0000 00000000 | | ADRCLT6[R/W] B,H,W<br>----0000 00000000 | | |
| 001584H | ADRCUT7[R/W] B,H,W<br>----0000 00000000 | | ADRCLT7[R/W] B,H,W<br>----0000 00000000 | | |
| 001588H | ADRCCS32[R/W] B,H,W<br>00000000 | ADRCCS33[R/W] B,H,W<br>00000000 | ADRCCS34[R/W] B,H,W<br>00000000 | ADRCCS35[R/W] B,H,W<br>00000000 | 12-bit A/D converter 2/2 unit |
| 00158CH | ADRCCS36[R/W] B,H,W<br>00000000 | ADRCCS37[R/W] B,H,W<br>00000000 | ADRCCS38[R/W] B,H,W<br>00000000 | ADRCCS39[R/W] B,H,W<br>00000000 | |
| 001590H | ADRCCS40[R/W] B,H,W<br>00000000 | ADRCCS41[R/W] B,H,W<br>00000000 | ADRCCS42[R/W] B,H,W<br>00000000 | ADRCCS43[R/W] B,H,W<br>00000000 | |
| 001594H | ADRCCS44[R/W] B,H,W<br>00000000 | ADRCCS45[R/W] B,H,W<br>00000000 | ADRCCS46[R/W] B,H,W<br>00000000 | ADRCCS47[R/W] B,H,W<br>00000000 | |
| 001598H<br>to<br>0015A4H | — | — | — | — | Reserved |
| 0015A8H | ADRCOT1 [R] B,H,W<br>-------- -------- 00000000 00000000 | | | | 12-bit A/D converter 2/2 unit |
| 0015ACH | ADRCIF1 [R,W] B,H,W<br>-------- -------- 00000000 00000000 | | | | |
| 0015B0H | ADSCANS1 [R/W] B,H,W<br>000----- | — | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0015B4H | ADNCS16 [R/W] B,H,W 0-000-00 | ADNCS17 [R/W] B,H,W 0-000-00 | ADNCS18 [R/W] B,H,W 0-000-00 | ADNCS19 [R/W] B,H,W 0-000-00 | 12-bit A/D converter 2/2 unit |
| 0015B8H | ADNCS20 [R/W] B,H,W 0-000-00 | ADNCS21 [R/W] B,H,W 0-000-00 | ADNCS22 [R/W] B,H,W 0-000-00 | ADNCS23 [R/W] B,H,W 0-000-00 | |
| 0015BCH | — | — | — | — | |
| 0015C0H | — | — | — | — | |
| 0015C4H | ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000 | | | | |
| 0015C8H | ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111 | | | | |
| 0015CCH | ADCS1 [R] B,H,W 0------- -------- | | ADCH1 [R] B,H,W ---00000 | ADMD1 [R/W] B,H,W 0---0000 | |
| 0015D0H | ADSTPCS8 [R/W] B,H,W 00000000 | ADSTPCS9 [R/W] B,H,W 00000000 | ADSTPCS10 [R/W] B,H,W 00000000 | ADSTPCS11 [R/W] B,H,W 00000000 | |
| 0015D4H to 00174CH | — | — | — | — | Reserved |
| 001750H | SCR0/(IBCR0)[R/W] B,H,W 0--00000 | SMR0[R/W] B,H,W 000-00-0 | SSR0[R/W] B,H,W 0-000011 | ESCR0/(IBSR0)[R/W] B,H,W 00000000 | Multi-UART0<br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 001754H | — /(RDR10/(TDR10))[R/W] B,H,W -------- -------- *3 | | RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1 | | |
| 001758H | SACSR0[R/W] B,H,W 0----000 00000000 | | STMR0[R] B,H,W 00000000 00000000 | | |
| 00175CH | STMCR0[R/W] B,H,W 00000000 00000000 | | — /(SCSCR0/SFUR0)[R/W] B,H,W -------- -------- *3 *4 | | |
| 001760H | — /(SCSTR30)/ (LAMSR0) [R/W] B,H,W -------- *3 | — /(SCSTR20)/ (LAMCR0) [R/W] B,H,W -------- *3 | — /(SCSTR10) /(SFLR10) [R/W] B,H,W -------- *3 | — /(SCSTR00)/ (SFLR00) [R/W] B,H,W -------- *3 | |
| 001764H | — | — /(SCSFR20) [R/W] B,H,W -------- *3 | — /(SCSFR10) [R/W] B,H,W -------- *3 | — /(SCSFR00) [R/W] B,H,W -------- *3 | |
| 001768H | —/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -------- *3 | —/(TBYTE20) /(LAMERT0) [R/W] B,H,W -------- *3 | —/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -------- *3 | TBYTE00/(LAMRID0) / (LAMTID0) [R/W] B,H,W 00000000 | |
| 00176CH | BGR0[R/W] H, W 00000000 00000000 | | — /(ISMK0) [R/W] B,H,W -------- *2 | — /(ISBA0) [R/W] B,H,W -------- *2 | |
| 001770H | FCR10[R/W] B,H,W ---00100 | FCR00[R/W] B,H,W -0000000 | FBYTE0[R/W] B,H,W 00000000 00000000 | | |
| 001774H | FTICR0[R/W] B,H,W 00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001778H | SCR1/(IBCR1) [R/W] B,H,W 0--00000 | SMR1[R/W] B,H,W 000-00-0 | SSR1[R/W] B,H,W 0-000011 | ESCR1/(IBSR1)[R/W] B,H,W 00000000 | Multi-UART1 |
| 00177CH | — /(RDR11/(TDR11))[R/W] B,H,W -------- -------- *3 | | RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1 | | |
| 001780H | SACSR1[R/W] B,H,W 0----000 00000000 | | STMR1[R] B,H,W 00000000 00000000 | | Multi-UART1<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset. |
| 001784H | STMCR1[R/W] B,H,W 00000000 00000000 | | — /(SCSCR1/SFUR1)[R/W] B,H,W -------- -------- *3 *4 | | |
| 001788H | — /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -------- *3 | — /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -------- *3 | — /(SCSTR11)/ (SFLR11) [R/W] B,H,W -------- *3 | — /(SCSTR01)/ (SFLR01) [R/W] B,H,W -------- *3 | |
| 00178CH | — | — /(SCSFR21)[R/W] B,H,W -------- *3 | — /(SCSFR11) [R/W] B,H,W -------- *3 | — /(SCSFR01) [R/W] B,H,W -------- *3 | |
| 001790H | —/(TBYTE31)/ (LAMESR1) [R/W] B,H,W -------- *3 | —/(TBYTE21)/ (LAMERT1) [R/W] B,H,W -------- *3 | —/(TBYTE11)/ (LAMIER1) [R/W] B,H,W -------- *3 | TBYTE01/(LAMRID1) / (LAMTID1) [R/W] B,H,W 00000000 | Multi-UART1<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 001794H | BGR1[R/W] H,W 00000000 00000000 | | — /(ISMK1)[R/W] B,H,W -------- *2 | — /(ISBA1)[R/W] B,H,W -------- *2 | |
| 001798H | FCR11[R/W] B,H,W ---00100 | FCR01[R/W] B,H,W -0000000 | FBYTE1[R/W] B,H,W 00000000 00000000 | | |
| 00179CH | FTICR1[R/W] B,H,W 00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0017A0H | SCR2/(IBCR2)[R/W] B,H,W 0--00000 | SMR2[R/W] B,H,W 000-00-0 | SSR2[R/W] B,H,W 0-000011 | ESCR2/(IBSR2)[R/W] B,H,W 00000000 | Multi-UART2<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I²C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 0017A4H | — /(RDR12/(TDR12))[R/W] B,H,W -------- -------- *3 | | RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1 | | |
| 0017A8H | SACSR2[R/W] B,H,W 0----000 00000000 | | STMR2[R] B,H,W 00000000 00000000 | | |
| 0017ACH | STMCR2[R/W] B,H,W 00000000 00000000 | | — /(SCSCR2/SFUR2)[R/W] B,H,W -------- -------- *3 *4 | | |
| 0017B0H | — /(SCSTR32)/ (LAMSR2) [R/W] B,H,W -------- *3 | — /(SCSTR22)/ (LAMCR2) [R/W] B,H,W -------- *3 | — /(SCSTR12)/ (SFLR12) [R/W] B,H,W -------- *3 | — /(SCSTR02)/ (SFLR02) [R/W] B,H,W -------- *3 | |
| 0017B4H | — | — /(SCSFR22) [R/W] B,H,W -------- *3 | — /(SCSFR12) [R/W] B,H,W -------- *3 | — /(SCSFR02) [R/W] B,H,W -------- *3 | |
| 0017B8H | —/(TBYTE32)/ (LAMESR2) [R/W] B,H,W -------- *3 | —/(TBYTE22)/ (LAMERT2) [R/W] B,H,W -------- *3 | —/(TBYTE12)/ (LAMIER2) [R/W] B,H,W -------- *3 | TBYTE02/(LAMRID2) / (LAMTID2) [R/W] B,H,W 00000000 | |
| 0017BCH | BGR2[R/W] H, W 00000000 00000000 | | — /(ISMK2)[R/W] B,H,W -------- *2 | — /(ISBA2)[R/W] B,H,W -------- *2 | |
| 0017C0H | FCR12[R/W] B,H,W ---00100 | FCR02[R/W] B,H,W -0000000 | FBYTE2[R/W] B,H,W 00000000 00000000 | | Multi-UART2 |
| 0017C4H | FTICR2[R/W] B,H,W 00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0017C8H | SCR3/(IBCR3) [R/W] B,H,W 0--00000 | SMR3[R/W] B,H,W 000-00-0 | SSR3[R/W] B,H,W 0-000011 | ESCR3/(IBSR3)[R/W] B,H,W 00000000 | Multi-UART3<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I²C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 0017CCH | — /(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3 | | RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1 | | |
| 0017D0H | SACSR3[R/W] B,H,W 0----000 00000000 | | STMR3[R] B,H,W 00000000 00000000 | | |
| 0017D4H | STMCR3[R/W] B,H,W 00000000 00000000 | | — /(SCSCR3/SFUR3)[R/W] B,H,W -------- -------- *3 *4 | | |
| 0017D8H | — /(SCSTR33)/ (LAMSR3) [R/W] B,H,W -------- *3 | — /(SCSTR23)/ (LAMCR3) [R/W] B,H,W -------- *3 | — /(SCSTR13)/ (SFLR13) [R/W] B,H,W -------- *3 | — /(SCSTR03)/ (SFLR03) [R/W] B,H,W -------- *3 | |
| 0017DCH | — | — /(SCSFR23) [R/W] B,H,W -------- *3 | — /(SCSFR13) [R/W] B,H,W -------- *3 | — /(SCSFR03) [R/W] B,H,W -------- *3 | |
| 0017E0H | —/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -------- *3 | —/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -------- *3 | —/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -------- *3 | TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000 | |
| 0017E4H | BGR3[R/W] H, W 00000000 00000000 | | — /(ISMK3)[R/W] B,H,W -------- *2 | — /(ISBA3)[R/W] B,H,W -------- *2 | |
| 0017E8H | FCR13[R/W] B,H,W ---00100 | FCR03[R/W] B,H,W -0000000 | FBYTE3[R/W] B,H,W 00000000 00000000 | | |
| 0017ECH | FTICR3[R/W] B,H,W 00000000 00000000 | | — | — | |
| 0017F0H | SCR4/(IBCR4) [R/W] B,H,W 0--00000 | SMR4[R/W] B,H,W 000-00-0 | SSR4[R/W] B,H,W 0-000011 | ESCR4/(IBSR4)[R/W] B,H,W 00000000 | Multi-UART4<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I²C mode is not set immediately after reset. |
| 0017F4H | — /(RDR14/(TDR14))[R/W] B,H,W -------- -------- *3 | | RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1 | | |
| 0017F8H | SACSR4[R/W] B,H,W 0----000 00000000 | | STMR4[R] B,H,W 00000000 00000000 | | |
| 0017FCH | STMCR4[R/W] B,H,W 00000000 00000000 | | — /(SCSCR4/SFUR4)[R/W] B,H,W -------- -------- *3 *4 | | |
| 001800H | — /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -------- *3 | — /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -------- *3 | — /(SCSTR14)/ (SFLR14) [R/W] B,H,W -------- *3 | — /(SCSTR04)/ (SFLR04) [R/W] B,H,W -------- *3 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001804H | — | — /(SCSFR24)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR14)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR04)<br>[R/W] B,H,W<br>-------- *3 | Multi-UART4<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 001808H | —/(TBYTE34)/<br>(LAMESR4)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE24)/<br>(LAMERT4)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE14)/<br>(LAMIER4)<br>[R/W] B,H,W<br>-------- *3 | TBYTE04/(LAMRID4)<br>/<br>(LAMTID4)<br>[R/W] B,H,W<br>00000000 | |
| 00180CH | BGR4[R/W] H, W<br>00000000 00000000 | | — /(ISMK4)[R/W]<br>B,H,W<br>-------- *2 | — /(ISBA4)[R/W]<br>B,H,W<br>-------- *2 | |
| 001810H | FCR14[R/W]<br>B,H,W<br>---00100 | FCR04[R/W]<br>B,H,W<br>-0000000 | FBYTE4[R/W] B,H,W<br>00000000 00000000 | | |
| 001814H | FTICR4[R/W] B,H,W<br>00000000 00000000 | | — | — | |
| 001818H | SCR5/(IBCR5) [R/W]<br>B,H,W<br>0--00000 | SMR5[R/W] B,H,W<br>000-00-0 | SSR5[R/W] B,H,W<br>0-000011 | ESCR5/(IBSR5)[R/W<br>] B,H,W<br>00000000 | Multi-UART5<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 00181CH | — /(RDR15/(TDR15))[R/W] B,H,W<br>-------- -------- *3 | | RDR05/(TDR05)[R/W] B,H,W<br>-------0 00000000 *1 | | |
| 001820H | SACSR5[R/W] B,H,W<br>0----000 00000000 | | STMR5[R] B,H,W<br>00000000 00000000 | | |
| 001824H | STMCR5[R/W] B,H,W<br>00000000 00000000 | | — /(SCSCR5/SFUR5)[R/W] B,H,W<br>-------- -------- *3 *4 | | |
| 001828H | — /(SCSTR35)/<br>(LAMSR5)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR25)/<br>(LAMCR5)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR15)/<br>(SFLR15)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR05)/<br>(SFLR05)<br>[R/W] B,H,W<br>-------- *3 | |
| 00182CH | — | — /(SCSFR25)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR15)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR05)<br>[R/W] B,H,W<br>-------- *3 | |
| 001830H | —/(TBYTE35)/<br>(LAMESR5)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE25)/<br>(LAMERT5)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE15)/<br>(LAMIER5)<br>[R/W] B,H,W<br>-------- *3 | TBYTE05/(LAMRID5)<br>/<br>(LAMTID5)<br>[R/W] B,H,W<br>00000000 | |
| 001834H | BGR5[R/W] H, W<br>00000000 00000000 | | — /(ISMK5)[R/W]<br>B,H,W<br>-------- *2 | — /(ISBA5)[R/W]<br>B,H,W<br>-------- *2 | |
| 001838H | FCR15[R/W]<br>B,H,W<br>---00100 | FCR05[R/W]<br>B,H,W<br>-0000000 | FBYTE5[R/W] B,H,W<br>00000000 00000000 | | |
| 00183CH | FTICR5[R/W] B,H,W<br>00000000 00000000 | | — | — | |
| 001840H | SCR6/(IBCR6) [R/W]<br>B,H,W<br>0--00000 | SMR6[R/W] B,H,W<br>000-00-0 | SSR6[R/W] B,H,W<br>0-000011 | ESCR6/(IBSR6)[R/W<br>] B,H,W<br>00000000 | Multi-UART6 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001844H | — /(RDR16/(TDR16))[R/W] B,H,W<br>-------- -------- *3 | | RDR06/(TDR06)[R/W] B,H,W<br>-------0 00000000 *1 | | Multi-UART6<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 001848H | SACSR6[R/W] B,H,W<br>0----000 00000000 | | STMR6[R] B,H,W<br>00000000 00000000 | | |
| 00184CH | STMCR6[R/W] B,H,W<br>00000000 00000000 | | — /(SCSCR6/SFUR6)[R/W] B,H,W<br>-------- -------- *3 *4 | | |
| 001850H | — /(SCSTR36)/<br>(LAMSR6)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR26)/<br>(LAMCR6)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR16)/<br>(SFLR16)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR06)/<br>(SFLR06)<br>[R/W] B,H,W<br>-------- *3 | |
| 001854H | — | — /(SCSFR26)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR16)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR06)<br>[R/W] B,H,W<br>-------- *3 | |
| 001858H | —/(TBYTE36)/<br>(LAMESR6)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE26)/<br>(LAMERT6)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE16)/<br>(LAMIER6)<br>[R/W] B,H,W<br>-------- *3 | TBYTE06/(LAMRID6)<br>/<br>(LAMTID6)<br>[R/W] B,H,W<br>00000000 | |
| 00185CH | BGR6[R/W] H, W<br>00000000 00000000 | | — /(ISMK6)[R/W]<br>B,H,W<br>-------- *2 | — /(ISBA6)[R/W]<br>B,H,W<br>-------- *2 | |
| 001860H | FCR16[R/W]<br>B,H,W<br>---00100 | FCR06[R/W]<br>B,H,W<br>-0000000 | FBYTE6[R/W] B,H,W<br>00000000 00000000 | | |
| 001864H | FTICR6[R/W] B,H,W<br>00000000 00000000 | | — | — | |
| 001868H | SCR7/(IBCR7) [R/W]<br>B,H,W<br>0--00000 | SMR7[R/W] B,H,W<br>000-00-0 | SSR7[R/W] B,H,W<br>0-000011 | ESCR7/(IBSR7)[R/W<br>] B,H,W<br>00000000 | Multi-UART7<br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset. |
| 00186CH | — /(RDR17/(TDR17))[R/W] B,H,W<br>-------- -------- *3 | | RDR07/(TDR07)[R/W] B,H,W<br>-------0 00000000 *1 | | |
| 001870H | SACSR7[R/W] B,H,W<br>0----000 00000000 | | STMR7[R] B,H,W<br>00000000 00000000 | | |
| 001874H | STMCR7[R/W] B,H,W<br>00000000 00000000 | | — /(SCSCR7/SFUR7)[R/W] B,H,W<br>-------- -------- *3 *4 | | |
| 001878H | — /(SCSTR37)/<br>(LAMSR7)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR27)/<br>(LAMCR7)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR17)/<br>(SFLR17)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR07)/<br>(SFLR07)<br>[R/W] B,H,W<br>-------- *3 | Multi-UART7<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 00187CH | — | — /(SCSFR27)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR17)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR07)<br>[R/W] B,H,W<br>-------- *3 | |
| 001880H | —/(TBYTE37)/<br>(LAMESR7)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE27)/<br>(LAMERT7)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE17)/<br>(LAMIER7)<br>[R/W] B,H,W<br>-------- *3 | TBYTE07/(LAMRID7)<br>/<br>(LAMTID7)<br>[R/W] B,H,W<br>00000000 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001884H | BGR7[R/W] H, W<br>00000000 00000000 | | — /(ISMK7)[R/W]<br>B,H,W<br>-------- *2 | — /(ISBA7)[R/W]<br>B,H,W<br>-------- *2 | Multi-UART7 |
| 001888H | FCR17[R/W]<br>B,H,W<br>---00100 | FCR07[R/W]<br>B,H,W<br>-0000000 | FBYTE7[R/W] B,H,W<br>00000000 00000000 | | |
| 00188CH | FTICR7[R/W] B,H,W<br>00000000 00000000 | | — | — | |
| 001890H | SCR8/(IBCR8) [R/W]<br>B,H,W<br>0--00000 | SMR8[R/W] B,H,W<br>000-00-0 | SSR8[R/W] B,H,W<br>0-000011 | ESCR8/(IBSR8)[R/W<br>] B,H,W<br>00000000 | Multi-UART8<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 001894H | — /(RDR18/(TDR18))[R/W] B,H,W<br>-------- -------- *3 | | RDR08/(TDR08)[R/W] B,H,W<br>-------0 00000000 *1 | | |
| 001898H | SACSR8[R/W] B,H,W<br>0----000 00000000 | | STMR8[R] B,H,W<br>00000000 00000000 | | |
| 00189CH | STMCR8[R/W] B,H,W<br>00000000 00000000 | | — /(SCSCR8/SFUR8)[R/W] B,H,W<br>-------- -------- *3 *4 | | |
| 0018A0H | — /(SCSTR38)/<br>(LAMSR8)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR28)/<br>(LAMCR8)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR18)/<br>(SFLR18)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSTR08)/<br>(SFLR08)<br>[R/W] B,H,W<br>-------- *3 | |
| 0018A4H | — | — /(SCSFR28)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR18)<br>[R/W] B,H,W<br>-------- *3 | — /(SCSFR08)<br>[R/W] B,H,W<br>-------- *3 | |
| 0018A8H | —/(TBYTE38)/<br>(LAMESR8)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE28)/<br>(LAMERT8)<br>[R/W] B,H,W<br>-------- *3 | —/(TBYTE18)/<br>(LAMIER8)<br>[R/W] B,H,W<br>-------- *3 | TBYTE08/(LAMRID8)<br>/<br>(LAMTID8)<br>[R/W] B,H,W<br>00000000 | |
| 0018ACH | BGR8[R/W] H,W<br>00000000 00000000 | | — /(ISMK8)[R/W]<br>B,H,W<br>-------- *2 | — /(ISBA8)[R/W]<br>B,H,W<br>-------- *2 | |
| 0018B0H | FCR18[R/W]<br>B,H,W<br>---00100 | FCR08[R/W]<br>B,H,W<br>-0000000 | FBYTE8[R/W] B,H,W<br>00000000 00000000 | | Multi-UART8 |
| 0018B4H | FTICR8[R/W] B,H,W<br>00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0018B8H | SCR9/(IBCR9) [R/W] B,H,W 0--00000 | SMR9[R/W] B,H,W 000-00-0 | SSR9[R/W] B,H,W 0-000011 | ESCR9/(IBSR9)[R/W] B,H,W 00000000 | Multi-UART9<br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 0018BCH | — /(RDR19/(TDR19))[R/W] B,H,W -------- -------- *3 | | RDR09/(TDR09)[R/W] B,H,W -------0 00000000 *1 | | |
| 0018C0H | SACSR9[R/W] B,H,W 0----000 00000000 | | STMR9[R] B,H,W 00000000 00000000 | | |
| 0018C4H | STMCR9[R/W] B,H,W 00000000 00000000 | | — /(SCSCR9/SFUR9)[R/W] B,H,W -------- -------- *3 *4 | | |
| 0018C8H | — /(SCSTR39)/ (LAMSR9) [R/W] B,H,W -------- *3 | — /(SCSTR29)/ (LAMCR9) [R/W] B,H,W -------- *3 | — /(SCSTR19)/ (SFLR19) [R/W] B,H,W -------- *3 | — /(SCSTR09)/ (SFLR09) [R/W] B,H,W -------- *3 | |
| 0018CCH | — | — /(SCSFR29) [R/W] B,H,W -------- *3 | — /(SCSFR19) [R/W] B,H,W -------- *3 | — /(SCSFR09) [R/W] B,H,W -------- *3 | |
| 0018D0H | —/(TBYTE39)/ (LAMESR9) [R/W] B,H,W -------- *3 | —/(TBYTE29)/ (LAMERT9) [R/W] B,H,W -------- *3 | —/(TBYTE19)/ (LAMIER9) [R/W] B,H,W -------- *3 | TBYTE09/(LAMRID9) / (LAMTID9) [R/W] B,H,W 00000000 | |
| 0018D4H | BGR9[R/W] H, W 00000000 00000000 | | — /(ISMK9)[R/W] B,H,W -------- *2 | — /(ISBA9)[R/W] B,H,W -------- *2 | |
| 0018D8H | FCR19[R/W] B,H,W ---00100 | FCR09[R/W] B,H,W -0000000 | FBYTE9[R/W] B,H,W 00000000 00000000 | | |
| 0018DCH | FTICR9[R/W] B,H,W 00000000 00000000 | | — | — | |
| 0018E0H | SCR10/(IBCR10) [R/W] B,H,W 0--00000 | SMR10[R/W] B,H,W 000-00-0 | SSR10[R/W] B,H,W 0-000011 | ESCR10/(IBSR10) [R/W] B,H,W 00000000 | Multi-UART10<br><br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I2C mode is not set immediately after reset. |
| 0018E4H | — /(RDR110/(TDR110))[R/W] B,H,W -------- -------- *3 | | RDR010/(TDR010)[R/W] B,H,W -------0 00000000 *1 | | |
| 0018E8H | SACSR10[R/W] B,H,W 0----000 00000000 | | STMR10[R] B,H,W 00000000 00000000 | | |
| 0018ECH | STMCR10[R/W] B,H,W 00000000 00000000 | | — /(SCSCR10/SFUR10)[R/W] B,H,W -------- -------- *3 *4 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0018F0H | — /(SCSTR310)/ (LAMSR10) [R/W] B,H,W -------- *3 | — /(SCSTR210)/ (LAMCR10) [R/W] B,H,W -------- *3 | — /(SCSTR110)/ (SFLR110)[R/W] B,H,W -------- *3 | — /(SCSTR010)/ (SFLR010)[R/W] B,H,W -------- *3 | Multi-UART10<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 0018F4H | — | — /(SCSFR210) [R/W] B,H,W -------- *3 | — /(SCSFR110) [R/W] B,H,W -------- *3 | — /(SCSFR010) [R/W] B,H,W -------- *3 | |
| 0018F8H | —/(TBYTE310)/ (LAMESR10) [R/W] B,H,W -------- *3 | —/(TBYTE210)/ (LAMERT10) [R/W] B,H,W -------- *3 | —/(TBYTE110)/ (LAMIER10) [R/W] B,H,W -------- *3 | TBYTE010/(LAMRID10)/(LAMTID10) [R/W] B,H,W 00000000 | |
| 0018FCH | BGR10[R/W] H, W 00000000 00000000 | | — /(ISMK10)[R/W] B,H,W -------- *2 | — /(ISBA10)[R/W] B,H,W -------- *2 | |
| 001900H | FCR110[R/W] B,H,W ---00100 | FCR010[R/W] B,H,W -0000000 | FBYTE10[R/W] B,H,W 00000000 00000000 | | |
| 001904H | FTICR10[R/W] B,H,W 00000000 00000000 | | — | — | |
| 001908H | SCR11/(IBCR11) [R/W] B,H,W 0--00000 | SMR11[R/W] B,H,W 000-00-0 | SSR11[R/W] B,H,W 0-000011 | ESCR11/(IBSR11) [R/W] B,H,W 00000000 | Multi-UART11<br>*1: Byte access is possible only for access to lower 8 bits.<br><br>*2: Reserved because I²C mode is not set immediately after reset.<br><br>*3: Reserved because CSIO mode is not set immediately after reset.<br><br>*4: Reserved because LIN2.1 mode is not set immediately after reset. |
| 00190CH | — /(RDR111/(TDR111))[R/W] B,H,W -------- -------- *3 | | RDR011/(TDR011)[R/W] B,H,W -------0 00000000 *1 | | |
| 001910H | SACSR11[R/W] B,H,W 0----000 00000000 | | STMR11[R] B,H,W 00000000 00000000 | | |
| 001914H | STMCR11[R/W] B,H,W 00000000 00000000 | | — /(SCSCR11/SFUR11)[R/W] B,H,W -------- -------- *3 *4 | | |
| 001918H | — /(SCSTR311)/ (LAMSR11) [R/W] B,H,W -------- *3 | — /(SCSTR211)/ (LAMCR11) [R/W] B,H,W -------- *3 | — /(SCSTR111)/ (SFLR111)[R/W] B,H,W -------- *3 | — /(SCSTR011)/ (SFLR011)[R/W] B,H,W -------- *3 | |
| 00191CH | — | — /(SCSFR211) [R/W] B,H,W -------- *3 | — /(SCSFR111) [R/W] B,H,W -------- *3 | — /(SCSFR011) [R/W] B,H,W -------- *3 | |
| 001920H | —/(TBYTE311)/ (LAMESR11) [R/W] B,H,W -------- *3 | —/(TBYTE211)/ (LAMERT11) [R/W] B,H,W -------- *3 | —/(TBYTE111)/ (LAMIER11) [R/W] B,H,W -------- *3 | TBYTE011/(LAMRID11)/(LAMTID11) [R/W] B,H,W 00000000 | |
| 001924H | BGR11[R/W] H, W 00000000 00000000 | | — /(ISMK11)[R/W] B,H,W -------- *2 | — /(ISBA11)[R/W] B,H,W -------- *2 | |
| 001928H | FCR111[R/W] B,H,W ---00100 | FCR011[R/W] B,H,W -0000000 | FBYTE11[R/W] B,H,W 00000000 00000000 | | Multi-UART11 |
| 00192CH | FTICR11[R/W] B,H,W 00000000 00000000 | | — | — | |
| 001930H to 0019D8H | — | — | — | — | Reserved |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 0019DC$_H$ | — | GATEC0 [R/W]<br>B,H,W<br>------00 | — | GATEC2 [R/W]<br>B,H,W<br>------00 | PPG GATE control |
| 0019E0$_H$ | — | GATEC4 [R/W]<br>B,H,W<br>------00 | — | — | |
| 0019E4$_H$ | — | — | — | — | Reserved |
| 0019E8$_H$ | GTRS0 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS1 [R/W] B,H,W<br>-0000000 -0000000 | | PPG controller |
| 0019EC$_H$ | GTRS2 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS3 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 0019F0$_H$ | GTRS4 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS5 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 0019F4$_H$ | GTRS6 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS7 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 0019F8$_H$ | GTRS8 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS9 [R/W] B,H,W<br>-0000000 -0000000 | | PPG controller |
| 0019FC$_H$ | GTRS10 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS11 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A00$_H$ | GTRS12 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS13 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A04$_H$ | GTRS14 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS15 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A08$_H$ | GTRS16 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS17 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A0C$_H$ | GTRS18 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS19 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A10$_H$ | GTRS20 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS21 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A14$_H$ | GTRS22 [R/W] B,H,W<br>-0000000 -0000000 | | GTRS23 [R/W] B,H,W<br>-0000000 -0000000 | | |
| 001A18$_H$<br>to<br>001A2C$_H$ | — | — | — | — | Reserved |
| 001A30$_H$ | — | — | — | — | Reserved |
| 001A34$_H$ | — | — | — | — | |
| 001A38$_H$ | GTREN0 [R/W] H,W<br>00000000 00000000 | | GTREN1 [R/W] H,W<br>00000000 00000000 | | PPG controller |
| 001A3C$_H$ | GTREN2 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001A40$_H$ | PCN0 [R/W] B,H,W<br>00000000 000000-0 | | PCSR0 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG0<br>* for communication |
| 001A44$_H$ | PDUT0 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR0 [R] H,W<br>11111111 11111111 | | |
| 001A48$_H$ | PCN200 [R/W] B,H,W<br>--000000 -----110 | | PSDR0 [R/W] H,W<br>00000000 00000000 | | |
| 001A4C$_H$ | PTPC0 [R/W] H,W<br>00000000 00000000 | | PCMDWD0 [R/W] B,H,W<br>-------- ----0000 | | |
| 001A50$_H$ | PHCSR0 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLCSR0 [W] H,W<br>XXXXXXXX XXXXXXXX | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001A54H | PHDUT0 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLDUT0 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG0<br>* for communication |
| 001A58H | PCMDDT0 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001A5CH | PCN1 [R/W] B,H,W<br>00000000 000000-0 | | PCSR1 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG1<br>* for communication |
| 001A60H | PDUT1 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR1 [R] H,W<br>11111111 11111111 | | |
| 001A64H | PCN201 [R/W] B,H,W<br>--000000 -----110 | | PSDR1 [R/W] H,W<br>00000000 00000000 | | PPG1<br>* for communication |
| 001A68H | PTPC1 [R/W] H,W<br>00000000 00000000 | | PCMDWD1 [R/W] B,H,W<br>-------- ----0000 | | |
| 001A6CH | PHCSR1 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLCSR1 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001A70H | PHDUT1 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLDUT1 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001A74H | PCMDDT1 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001A78H | PCN2 [R/W] B,H,W<br>00000000 000000-0 | | PCSR2 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG2<br>* for communication |
| 001A7CH | PDUT2 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR2 [R] H,W<br>11111111 11111111 | | |
| 001A80H | PCN202 [R/W] B,H,W<br>--000000 -----110 | | PSDR2 [R/W] H,W<br>00000000 00000000 | | PPG2<br>* for communication |
| 001A84H | PTPC2 [R/W] H,W<br>00000000 00000000 | | PCMDWD2 [R/W] B,H,W<br>-------- ----0000 | | |
| 001A88H | PHCSR2 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLCSR2 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001A8CH | PHDUT2 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLDUT2 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001A90H | PCMDDT2 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001A94H | PCN3 [R/W] B,H,W<br>00000000 000000-0 | | PCSR3 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG3<br>* for communication |
| 001A98H | PDUT3 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR3 [R] H,W<br>11111111 11111111 | | |
| 001A9CH | PCN203 [R/W] B,H,W<br>--000000 -----110 | | PSDR3 [R/W] H,W<br>00000000 00000000 | | |
| 001AA0H | PTPC3 [R/W] H,W<br>00000000 00000000 | | PCMDWD3 [R/W] B,H,W<br>-------- ----0000 | | |
| 001AA4H | PHCSR3 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLCSR3 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001AA8H | PHDUT3 [W] H,W<br>XXXXXXXX XXXXXXXX | | PLDUT3 [W] H,W<br>XXXXXXXX XXXXXXXX | | |
| 001AACH | PCMDDT3 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001AB0H | PCN4 [R/W] B,H,W<br>00000000 000000-0 | | PCSR4 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG4 |
| 001AB4H | PDUT4 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR4 [R] H,W<br>11111111 11111111 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001AB8H | PCN204 [R/W] B,H,W<br>--000000 -----110 | | PSDR4 [R/W] H,W<br>00000000 00000000 | | PPG4 |
| 001ABCH | PTPC4 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001AC0H | PCN5 [R/W] B,H,W<br>00000000 000000-0 | | PCSR5 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG5 |
| 001AC4H | PDUT5 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR5 [R] H,W<br>11111111 11111111 | | |
| 001AC8H | PCN205 [R/W] B,H,W<br>--000000 -----110 | | PSDR5 [R/W] H,W<br>00000000 00000000 | | |
| 001ACCH | PTPC5 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001AD0H | PCN6 [R/W] B,H,W<br>00000000 000000-0 | | PCSR6 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG6 |
| 001AD4H | PDUT6 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR6 [R] H,W<br>11111111 11111111 | | |
| 001AD8H | PCN206 [R/W] B,H,W<br>--000000 -----110 | | PSDR6 [R/W] H,W<br>00000000 00000000 | | |
| 001ADCH | PTPC6 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001AE0H | PCN7 [R/W] B,H,W<br>00000000 000000-0 | | PCSR7 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG7 |
| 001AE4H | PDUT7 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR7 [R] H,W<br>11111111 11111111 | | |
| 001AE8H | PCN207 [R/W] B,H,W<br>--000000 -----110 | | PSDR7 [R/W] H,W<br>00000000 00000000 | | |
| 001AECH | PTPC7 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001AF0H | PCN8 [R/W] B,H,W<br>00000000 000000-0 | | PCSR8 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG8 |
| 001AF4H | PDUT8 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR8 [R] H,W<br>11111111 11111111 | | |
| 001AF8H | PCN208 [R/W] B,H,W<br>--000000 -----110 | | PSDR8 [R/W] H,W<br>00000000 00000000 | | |
| 001AFCH | PTPC8 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B00H | PCN9 [R/W] B,H,W<br>00000000 000000-0 | | PCSR9 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG9 |
| 001B04H | PDUT9 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR9 [R] H,W<br>11111111 11111111 | | |
| 001B08H | PCN209 [R/W] B,H,W<br>--000000 -----110 | | PSDR9 [R/W] H,W<br>00000000 00000000 | | |
| 001B0CH | PTPC9 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B10H | PCN10 [R/W] B,H,W<br>00000000 000000-0 | | PCSR10 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG10 |
| 001B14H | PDUT10 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR10 [R] H,W<br>11111111 11111111 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001B18H | PCN210 [R/W] B,H,W<br>--000000 -----110 | | PSDR10 [R/W] H,W<br>00000000 00000000 | | PPG10 |
| 001B1CH | PTPC10 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B20H | PCN11 [R/W] B,H,W<br>00000000 000000-0 | | PCSR11 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG11 |
| 001B24H | PDUT11 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR11 [R] H,W<br>11111111 11111111 | | PPG11 |
| 001B28H | PCN211 [R/W] B,H,W<br>--000000 -----110 | | PSDR11 [R/W] H,W<br>00000000 00000000 | | |
| 001B2CH | PTPC11 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B30H | PCN12 [R/W] B,H,W<br>00000000 000000-0 | | PCSR12 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG12 |
| 001B34H | PDUT12 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR12 [R] H,W<br>11111111 11111111 | | |
| 001B38H | PCN212 [R/W] B,H,W<br>--000000 -----110 | | PSDR12 [R/W] H,W<br>00000000 00000000 | | |
| 001B3CH | PTPC12 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B40H | PCN13 [R/W] B,H,W<br>00000000 000000-0 | | PCSR13 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG13 |
| 001B44H | PDUT13 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR13 [R] H,W<br>11111111 11111111 | | |
| 001B48H | PCN213 [R/W] B,H,W<br>--000000 -----110 | | PSDR13 [R/W] H,W<br>00000000 00000000 | | |
| 001B4CH | PTPC13 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B50H | PCN14 [R/W] B,H,W<br>00000000 000000-0 | | PCSR14 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG14 |
| 001B54H | PDUT14 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR14 [R] H,W<br>11111111 11111111 | | |
| 001B58H | PCN214 [R/W] B,H,W<br>--000000 -----110 | | PSDR14 [R/W] H,W<br>00000000 00000000 | | |
| 001B5CH | PTPC14 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B60H | PCN15 [R/W] B,H,W<br>00000000 000000-0 | | PCSR15 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG15 |
| 001B64H | PDUT15 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR15 [R] H,W<br>11111111 11111111 | | |
| 001B68H | PCN215 [R/W] B,H,W<br>--000000 -----110 | | PSDR15 [R/W] H,W<br>00000000 00000000 | | |
| 001B6CH | PTPC15 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B70H | PCN16 [R/W] B,H,W<br>00000000 000000-0 | | PCSR16 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG16 |
| 001B74H | PDUT16 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR16 [R] H,W<br>11111111 11111111 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001B78H | PCN216 [R/W] B,H,W<br>--000000 -----110 | | PSDR16 [R/W] H,W<br>00000000 00000000 | | PPG16 |
| 001B7CH | PTPC16 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B80H | PCN17 [R/W] B,H,W<br>00000000 000000-0 | | PCSR17 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG17 |
| 001B84H | PDUT17 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR17 [R] H,W<br>11111111 11111111 | | |
| 001B88H | PCN217 [R/W] B,H,W<br>--000000 -----110 | | PSDR17 [R/W] H,W<br>00000000 00000000 | | |
| 001B8CH | PTPC17 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001B90H | PCN18 [R/W] B,H,W<br>00000000 000000-0 | | PCSR18 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG18 |
| 001B94H | PDUT18 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR18 [R] H,W<br>11111111 11111111 | | |
| 001B98H | PCN218 [R/W] B,H,W<br>--000000 -----110 | | PSDR18 [R/W] H,W<br>00000000 00000000 | | |
| 001B9CH | PTPC18 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001BA0H | PCN19 [R/W] B,H,W<br>00000000 000000-0 | | PCSR19 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG19 |
| 001BA4H | PDUT19 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR19 [R] H,W<br>11111111 11111111 | | |
| 001BA8H | PCN219 [R/W] B,H,W<br>--000000 -----110 | | PSDR19 [R/W] H,W<br>00000000 00000000 | | |
| 001BACH | PTPC19 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001BB0H | PCN20 [R/W] B,H,W<br>00000000 000000-0 | | PCSR20 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG20 |
| 001BB4H | PDUT20 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR20 [R] H,W<br>11111111 11111111 | | |
| 001BB8H | PCN220 [R/W] B,H,W<br>--000000 -----110 | | PSDR20 [R/W] H,W<br>00000000 00000000 | | |
| 001BBCH | PTPC20 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001BC0H | PCN21 [R/W] B,H,W<br>00000000 000000-0 | | PCSR21 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG21 |
| 001BC4H | PDUT21 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR21 [R] H,W<br>11111111 11111111 | | |
| 001BC8H | PCN221 [R/W] B,H,W<br>--000000 -----110 | | PSDR21 [R/W] H,W<br>00000000 00000000 | | |
| 001BCCH | PTPC21 [R/W] H,W<br>00000000 00000000 | | — | — | PPG21 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001BD0H | PCN22 [R/W] B,H,W<br>00000000 000000-0 | | PCSR22 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG22 |
| 001BD4H | PDUT22 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR22 [R] H,W<br>11111111 11111111 | | |
| 001BD8H | PCN222 [R/W] B,H,W<br>--000000 -----110 | | PSDR22 [R/W] H,W<br>00000000 00000000 | | |
| 001BDCH | PTPC22 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001BE0H | PCN23 [R/W] B,H,W<br>00000000 000000-0 | | PCSR23 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG23 |
| 001BE4H | PDUT23 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR23 [R] H,W<br>11111111 11111111 | | |
| 001BE8H | PCN223 [R/W] B,H,W<br>--000000 -----110 | | PSDR23 [R/W] H,W<br>00000000 00000000 | | |
| 001BECH | PTPC23 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001BF0H | PCN24 [R/W] B,H,W<br>00000000 000000-0 | | PCSR24 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG24 |
| 001BF4H | PDUT24 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR24 [R] H,W<br>11111111 11111111 | | |
| 001BF8H | PCN224 [R/W] B,H,W<br>--000000 -----110 | | PSDR24 [R/W] H,W<br>00000000 00000000 | | |
| 001BFCH | PTPC24 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C00H | PCN25 [R/W] B,H,W<br>00000000 000000-0 | | PCSR25 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG25 |
| 001C04H | PDUT25 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR25 [R] H,W<br>11111111 11111111 | | |
| 001C08H | PCN225 [R/W] B,H,W<br>--000000 -----110 | | PSDR25 [R/W] H,W<br>00000000 00000000 | | |
| 001C0CH | PTPC25 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C10H | PCN26 [R/W] B,H,W<br>00000000 000000-0 | | PCSR26 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG26 |
| 001C14H | PDUT26 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR26 [R] H,W<br>11111111 11111111 | | |
| 001C18H | PCN226 [R/W] B,H,W<br>--000000 -----110 | | PSDR26 [R/W] H,W<br>00000000 00000000 | | |
| 001C1CH | PTPC26 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C20H | PCN27 [R/W] B,H,W<br>00000000 000000-0 | | PCSR27 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG27 |
| 001C24H | PDUT27 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR27 [R] H,W<br>11111111 11111111 | | PPG27 |
| 001C28H | PCN227 [R/W] B,H,W<br>--000000 -----110 | | PSDR27 [R/W] H,W<br>00000000 00000000 | | |
| 001C2CH | PTPC27 [R/W] H,W<br>00000000 00000000 | | — | — | PPG27 |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001C30H | PCN28 [R/W] B,H,W<br>00000000 000000-0 | | PCSR28 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG28 |
| 001C34H | PDUT28 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR28 [R] H,W<br>11111111 11111111 | | |
| 001C38H | PCN228 [R/W] B,H,W<br>--000000 -----110 | | PSDR28 [R/W] H,W<br>00000000 00000000 | | |
| 001C3CH | PTPC28 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C40H | PCN29 [R/W] B,H,W<br>00000000 000000-0 | | PCSR29 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG29 |
| 001C44H | PDUT29 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR29 [R] H,W<br>11111111 11111111 | | |
| 001C48H | PCN229 [R/W] B,H,W<br>--000000 -----110 | | PSDR29 [R/W] H,W<br>00000000 00000000 | | |
| 001C4CH | PTPC29 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C50H | PCN30 [R/W] B,H,W<br>00000000 000000-0 | | PCSR30 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG30 |
| 001C54H | PDUT30 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR30 [R] H,W<br>11111111 11111111 | | |
| 001C58H | PCN230 [R/W] B,H,W<br>--000000 -----110 | | PSDR30 [R/W] H,W<br>00000000 00000000 | | |
| 001C5CH | PTPC30 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C60H | PCN31 [R/W] B,H,W<br>00000000 000000-0 | | PCSR31 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG31 |
| 001C64H | PDUT31 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR31 [R] H,W<br>11111111 11111111 | | |
| 001C68H | PCN231 [R/W] B,H,W<br>--000000 -----110 | | PSDR31 [R/W] H,W<br>00000000 00000000 | | |
| 001C6CH | PTPC31 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C70H | PCN32 [R/W] B,H,W<br>00000000 000000-0 | | PCSR32 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG32 |
| 001C74H | PDUT32 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR32 [R] H,W<br>11111111 11111111 | | |
| 001C78H | PCN232 [R/W] B,H,W<br>--000000 -----110 | | PSDR32 [R/W] H,W<br>00000000 00000000 | | PPG32 |
| 001C7CH | PTPC32 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001C80H | PCN33 [R/W] B,H,W<br>00000000 000000-0 | | PCSR33 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG33 |
| 001C84H | PDUT33 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR33 [R] H,W<br>11111111 11111111 | | |
| 001C88H | PCN233 [R/W] B,H,W<br>--000000 -----110 | | PSDR33 [R/W] H,W<br>00000000 00000000 | | PPG33 |
| 001C8CH | PTPC33 [R/W] H,W<br>00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001C90H | PCN34 [R/W] B,H,W<br>00000000 000000-0 | | PCSR34 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG34 |
| 001C94H | PDUT34 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR34 [R] H,W<br>11111111 11111111 | | |
| 001C98H | PCN234 [R/W] B,H,W<br>--000000 -----110 | | PSDR34 [R/W] H,W<br>00000000 00000000 | | |
| 001C9CH | PTPC34 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001CA0H | PCN35 [R/W] B,H,W<br>00000000 000000-0 | | PCSR35 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG35 |
| 001CA4H | PDUT35 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR35 [R] H,W<br>11111111 11111111 | | |
| 001CA8H | PCN235 [R/W] B,H,W<br>--000000 -----110 | | PSDR35 [R/W] H,W<br>00000000 00000000 | | |
| 001CACH | PTPC35 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001CB0H | PCN36 [R/W] B,H,W<br>00000000 000000-0 | | PCSR36 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG36 |
| 001CB4H | PDUT36 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR36 [R] H,W<br>11111111 11111111 | | |
| 001CB8H | PCN236 [R/W] B,H,W<br>--000000 -----110 | | PSDR36 [R/W] H,W<br>00000000 00000000 | | |
| 001CBCH | PTPC36 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001CC0H | PCN37 [R/W] B,H,W<br>00000000 000000-0 | | PCSR37 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG37 |
| 001CC4H | PDUT37 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR37 [R] H,W<br>11111111 11111111 | | |
| 001CC8H | PCN237 [R/W] B,H,W<br>--000000 -----110 | | PSDR37 [R/W] H,W<br>00000000 00000000 | | |
| 001CCCH | PTPC37 [R/W] H,W<br>00000000 00000000 | | — | — | PPG37 |
| 001CD0H | PCN38 [R/W] B,H,W<br>00000000 000000-0 | | PCSR38 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG38 |
| 001CD4H | PDUT38 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR38 [R] H,W<br>11111111 11111111 | | |
| 001CD8H | PCN238 [R/W] B,H,W<br>--000000 -----110 | | PSDR38 [R/W] H,W<br>00000000 00000000 | | |
| 001CDCH | PTPC38 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001CE0H | PCN39 [R/W] B,H,W<br>00000000 000000-0 | | PCSR39 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG39 |
| 001CE4H | PDUT39 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR39 [R] H,W<br>11111111 11111111 | | PPG39 |
| 001CE8H | PCN239 [R/W] B,H,W<br>--000000 -----110 | | PSDR39 [R/W] H,W<br>00000000 00000000 | | |
| 001CECH | PTPC39 [R/W] H,W<br>00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001CF0H | PCN40 [R/W] B,H,W<br>00000000 000000-0 | | PCSR40 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG40 |
| 001CF4H | PDUT40 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR40 [R] H,W<br>11111111 11111111 | | |
| 001CF8H | PCN240 [R/W] B,H,W<br>--000000 -----110 | | PSDR40 [R/W] H,W<br>00000000 00000000 | | |
| 001CFCH | PTPC40 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D00H | PCN41 [R/W] B,H,W<br>00000000 000000-0 | | PCSR41 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG41 |
| 001D04H | PDUT41 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR41 [R] H,W<br>11111111 11111111 | | |
| 001D08H | PCN241 [R/W] B,H,W<br>--000000 -----110 | | PSDR41 [R/W] H,W<br>00000000 00000000 | | |
| 001D0CH | PTPC41 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D10H | PCN42 [R/W] B,H,W<br>00000000 000000-0 | | PCSR42 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG42 |
| 001D14H | PDUT42 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR42 [R] H,W<br>11111111 11111111 | | |
| 001D18H | PCN242 [R/W] B,H,W<br>--000000 -----110 | | PSDR42 [R/W] H,W<br>00000000 00000000 | | |
| 001D1CH | PTPC42 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D20H | PCN43 [R/W] B,H,W<br>00000000 000000-0 | | PCSR43 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG43 |
| 001D24H | PDUT43 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR43 [R] H,W<br>11111111 11111111 | | |
| 001D28H | PCN243 [R/W] B,H,W<br>--000000 -----110 | | PSDR43 [R/W] H,W<br>00000000 00000000 | | |
| 001D2CH | PTPC43 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D30H | PCN44 [R/W] B,H,W<br>00000000 000000-0 | | PCSR44 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG44 |
| 001D34H | PDUT44 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR44 [R] H,W<br>11111111 11111111 | | |
| 001D38H | PCN244 [R/W] B,H,W<br>--000000 -----110 | | PSDR44 [R/W] H,W<br>00000000 00000000 | | |
| 001D3CH | PTPC44 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D40H | PCN45 [R/W] B,H,W<br>00000000 000000-0 | | PCSR45 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG45 |
| 001D44H | PDUT45 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR45 [R] H,W<br>11111111 11111111 | | |
| 001D48H | PCN245 [R/W] B,H,W<br>--000000 -----110 | | PSDR45 [R/W] H,W<br>00000000 00000000 | | |
| 001D4CH | PTPC45 [R/W] H,W<br>00000000 00000000 | | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 001D50H | PCN46 [R/W] B,H,W<br>00000000 000000-0 | | PCSR46 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG46 |
| 001D54H | PDUT46 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR46 [R] H,W<br>11111111 11111111 | | |
| 001D58H | PCN246 [R/W] B,H,W<br>--000000 -----110 | | PSDR46 [R/W] H,W<br>00000000 00000000 | | |
| 001D5CH | PTPC46 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D60H | PCN47 [R/W] B,H,W<br>00000000 000000-0 | | PCSR47 [W] H,W<br>XXXXXXXX XXXXXXXX | | PPG47 |
| 001D64H | PDUT47 [W] H,W<br>XXXXXXXX XXXXXXXX | | PTMR47 [R] H,W<br>11111111 11111111 | | |
| 001D68H | PCN247 [R/W] B,H,W<br>--000000 -----110 | | PSDR47 [R/W] H,W<br>00000000 00000000 | | |
| 001D6CH | PTPC47 [R/W] H,W<br>00000000 00000000 | | — | — | |
| 001D70H<br>to<br>001FFCH | — | — | — | — | Reserved |
| 002000H | CTRLR0 [R/W] B,H,W<br>-------- 000-0001 | | STATR0 [R/W] B,H,W<br>-------- 00000000 | | CAN0<br>(128msb) |
| 002004H | ERRCNT0 [R] B,H,W<br>00000000 00000000 | | BTR0 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002008H | INTR0 [R] B,H,W<br>00000000 00000000 | | TESTR0 [R/W] B,H,W<br>-------- X00000-- | | |
| 00200CH | BRPER0 [R/W] B,H,W<br>-------- ----0000 | | — | — | |
| 002010H | IF1CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002014H | IF1MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002018H | IF1ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB10 [R/W] B,H,W<br>00000000 00000000 | | |
| 00201CH | IF1MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002020H | IF1DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002024H | IF1DTB10 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002028H | — | — | — | — | |
| 00202CH | — | — | — | — | |
| 002030H,<br>002034H | Reserved(IF1 data mirror) | | | | |
| 002038H | — | — | — | — | |
| 00203CH | — | — | — | — | |
| 002040H | IF2CREQ0 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK0 [R/W] B,H,W<br>-------- 00000000 | | |
| 002044H | IF2MSK20 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK10 [R/W] B,H,W<br>11111111 11111111 | | |
| 002048H | IF2ARB20 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB10 [R/W] B,H,W<br>00000000 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 00204C$_H$ | IF2MCTR0 [R/W] B,H,W<br>00000000 0---0000 | | — | — | CAN0<br>(128msb) |
| 002050$_H$ | IF2DTA10 [R/W] B,H,W<br>00000000 00000000 | | IF2DTA20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002054$_H$ | IF2DTB10 [R/W] B,H,W<br>00000000 00000000 | | IF2DTB20 [R/W] B,H,W<br>00000000 00000000 | | |
| 002058$_H$ | — | — | — | — | |
| 00205C$_H$ | — | — | — | — | |
| 002060$_H$,<br>002064$_H$ | Reserved(IF2 data mirror) | | | | |
| 002068$_H$<br>to<br>00207C$_H$ | — | | | | |
| 002080$_H$ | TREQR20 [R] B,H,W<br>00000000 00000000 | | TREQR10 [R] B,H,W<br>00000000 00000000 | | |
| 002084$_H$ | TREQR40 [R] B,H,W<br>00000000 00000000 | | TREQR30 [R] B,H,W<br>00000000 00000000 | | |
| 002088$_H$ | TREQR60 [R] B,H,W<br>00000000 00000000 | | TREQR50 [R] B,H,W<br>00000000 00000000 | | |
| 00208C$_H$ | TREQR80 [R] B,H,W<br>00000000 00000000 | | TREQR70 [R] B,H,W<br>00000000 00000000 | | |
| 002090$_H$ | NEWDT20 [R] B,H,W<br>00000000 00000000 | | NEWDT10 [R] B,H,W<br>00000000 00000000 | | |
| 002094$_H$ | NEWDT40 [R] B,H,W<br>00000000 00000000 | | NEWDT30 [R] B,H,W<br>00000000 00000000 | | |
| 002098$_H$ | NEWDT60 [R] B,H,W<br>00000000 00000000 | | NEWDT50 [R] B,H,W<br>00000000 00000000 | | |
| 00209C$_H$ | NEWDT80 [R] B,H,W<br>00000000 00000000 | | NEWDT70 [R] B,H,W<br>00000000 00000000 | | |
| 0020A0$_H$ | INTPND20 [R] B,H,W<br>00000000 00000000 | | INTPND10 [R] B,H,W<br>00000000 00000000 | | |
| 0020A4$_H$ | INTPND40 [R] B,H,W<br>00000000 00000000 | | INTPND30 [R] B,H,W<br>00000000 00000000 | | |
| 0020A8$_H$ | INTPND60 [R] B,H,W<br>00000000 00000000 | | INTPND50 [R] B,H,W<br>00000000 00000000 | | |
| 0020AC$_H$ | INTPND80 [R] B,H,W<br>00000000 00000000 | | INTPND70 [R] B,H,W<br>00000000 00000000 | | |
| 0020B0$_H$ | MSGVAL20 [R] B,H,W<br>00000000 00000000 | | MSGVAL10 [R] B,H,W<br>00000000 00000000 | | |
| 0020B4$_H$ | MSGVAL40 [R] B,H,W<br>00000000 00000000 | | MSGVAL30 [R] B,H,W<br>00000000 00000000 | | |
| 0020B8$_H$ | MSGVAL60 [R] B,H,W<br>00000000 00000000 | | MSGVAL50 [R] B,H,W<br>00000000 00000000 | | |
| 0020BC$_H$ | MSGVAL80 [R] B,H,W<br>00000000 00000000 | | MSGVAL70 [R] B,H,W<br>00000000 00000000 | | CAN0<br>(128msb) |
| 0020C0$_H$<br>to<br>0020FC$_H$ | — | | | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 002100H | CTRLR1 [R/W] B,H,W<br>-------- 000-0001 | | STATR1 [R/W] B,H,W<br>-------- 00000000 | | CAN1<br>(64msb) |
| 002104H | ERRCNT1 [R] B,H,W<br>00000000 00000000 | | BTR1 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002108H | INTR1 [R] B,H,W<br>00000000 00000000 | | TESTR1 [R/W] B,H,W<br>-------- X00000-- | | |
| 00210CH | BRPER1 [R/W] B,H,W<br>-------- ----0000 | | — | — | |
| 002110H | IF1CREQ1 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK1 [R/W] B,H,W<br>-------- 00000000 | | |
| 002114H | IF1MSK21 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK11 [R/W] B,H,W<br>11111111 11111111 | | |
| 002118H | IF1ARB21 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB11 [R/W] B,H,W<br>00000000 00000000 | | |
| 00211CH | IF1MCTR1 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002120H | IF1DTA11 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002124H | IF1DTB11 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002128H | — | — | — | — | |
| 00212CH | — | — | — | — | |
| 002130H,<br>002134H | Reserved (IF1 data mirror) | | | | CAN1<br>(64msb) |
| 002138H | — | — | — | — | |
| 00213CH | — | — | — | — | |
| 002140H | IF2CREQ1 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK1 [R/W] B,H,W<br>-------- 00000000 | | |
| 002144H | IF2MSK21 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK11 [R/W] B,H,W<br>11111111 11111111 | | |
| 002148H | IF2ARB21 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB11 [R/W] B,H,W<br>00000000 00000000 | | |
| 00214CH | IF2MCTR1 [R/W] B,H,W<br>00000000 0---0000 | | — | — | |
| 002150H | IF2DTA11 [R/W] B,H,W<br>00000000 00000000 | | IF2DTA21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002154H | IF2DTB11 [R/W] B,H,W<br>00000000 00000000 | | IF2DTB21 [R/W] B,H,W<br>00000000 00000000 | | |
| 002158H | — | — | — | — | |
| 00215CH | — | — | — | — | |
| 002160H,<br>002164H | Reserved (IF2 data mirror) | | | | |
| 002168H<br>to<br>00217CH | — | | | | |
| 002180H | TREQR21 [R] B,H,W<br>00000000 00000000 | | TREQR11 [R] B,H,W<br>00000000 00000000 | | |
| 002184H | TREQR41 [R] B,H,W<br>00000000 00000000 | | TREQR31 [R] B,H,W<br>00000000 00000000 | | |
| 002188H | — | — | — | — | |
| 00218CH | — | — | — | — | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 002190H | NEWDT21 [R] B,H,W<br>00000000 00000000 | | NEWDT11 [R] B,H,W<br>00000000 00000000 | | CAN1<br>(64msb) |
| 002194H | NEWDT41 [R] B,H,W<br>00000000 00000000 | | NEWDT31 [R] B,H,W<br>00000000 00000000 | | |
| 002198H | — | — | — | — | |
| 00219CH | — | — | — | — | |
| 0021A0H | INTPND21 [R] B,H,W<br>00000000 00000000 | | INTPND11 [R] B,H,W<br>00000000 00000000 | | |
| 0021A4H | INTPND41 [R] B,H,W<br>00000000 00000000 | | INTPND31 [R] B,H,W<br>00000000 00000000 | | |
| 0021A8H | — | — | — | — | |
| 0021ACH | — | — | — | — | |
| 0021B0H | MSGVAL21 [R] B,H,W<br>00000000 00000000 | | MSGVAL11 [R] B,H,W<br>00000000 00000000 | | |
| 0021B4H | MSGVAL41 [R] B,H,W<br>00000000 00000000 | | MSGVAL31 [R] B,H,W<br>00000000 00000000 | | |
| 0021B8H | — | — | — | — | |
| 0021BCH | — | — | — | — | |
| 0021C0H<br>to<br>0021FCH | — | | | | |
| 002200H | CTRLR2 [R/W] B,H,W<br>-------- 000-0001 | | STATR2 [R/W] B,H,W<br>-------- 00000000 | | CAN2<br>(64msb) |
| 002204H | ERRCNT2 [R] B,H,W<br>00000000 00000000 | | BTR2 [R/W] B,H,W<br>-0100011 00000001 | | |
| 002208H | INTR2 [R] B,H,W<br>00000000 00000000 | | TESTR2 [R/W] B,H,W<br>-------- X00000-- | | |
| 00220CH | BRPER2 [R/W] B,H,W<br>-------- ----0000 | | — | | |
| 002210H | IF1CREQ2 [R/W] B,H,W<br>0------- 00000001 | | IF1CMSK2 [R/W] B,H,W<br>-------- 00000000 | | |
| 002214H | IF1MSK22 [R/W] B,H,W<br>11-11111 11111111 | | IF1MSK12 [R/W] B,H,W<br>11111111 11111111 | | |
| 002218H | IF1ARB22 [R/W] B,H,W<br>00000000 00000000 | | IF1ARB12 [R/W] B,H,W<br>00000000 00000000 | | |
| 00221CH | IF1MCTR2 [R/W] B,H,W<br>00000000 0---0000 | | — | | |
| 002220H | IF1DTA12 [R/W] B,H,W<br>00000000 00000000 | | IF1DTA22 [R/W] B,H,W<br>00000000 00000000 | | |
| 002224H | IF1DTB12 [R/W] B,H,W<br>00000000 00000000 | | IF1DTB22 [R/W] B,H,W<br>00000000 00000000 | | |
| 002228H | — | — | — | — | |
| 00222CH | — | — | — | — | |
| 002230H,<br>002234H | Reserved (IF1 data mirror) | | | | |
| 002238H | — | — | — | — | |
| 00223CH | — | — | — | — | |
| 002240H | IF2CREQ2 [R/W] B,H,W<br>0------- 00000001 | | IF2CMSK2 [R/W] B,H,W<br>-------- 00000000 | | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 002244H | IF2MSK22 [R/W] B,H,W<br>11-11111 11111111 | | IF2MSK12 [R/W] B,H,W<br>11111111 11111111 | | CAN2 (64msb) |
| 002248H | IF2ARB22 [R/W] B,H,W<br>00000000 00000000 | | IF2ARB12 [R/W] B,H,W<br>00000000 00000000 | | |
| 00224CH | IF2MCTR2 [R/W] B,H,W<br>00000000 0---0000 | | — | | |
| 002250H | IF2DTA12 [R/W] B,H,W<br>00000000 00000000 | | IF2DTA22 [R/W] B,H,W<br>00000000 00000000 | | |
| 002254H | IF2DTB12 [R/W] B,H,W<br>00000000 00000000 | | IF2DTB22 [R/W] B,H,W<br>00000000 00000000 | | |
| 002258H | — | — | — | — | |
| 00225CH | — | — | — | — | |
| 002260H, 002264H | Reserved (IF2 data mirror) | | | | |
| 002268H to 00227CH | — | | | | |
| 002280H | TREQR22 [R] B,H,W<br>00000000 00000000 | | TREQR12 [R] B,H,W<br>00000000 00000000 | | |
| 002284H | TREQR42 [R] B,H,W<br>00000000 00000000 | | TREQR32 [R] B,H,W<br>00000000 00000000 | | |
| 002288H | — | — | — | — | |
| 00228CH | — | — | — | — | |
| 002290H | NEWDT22 [R] B,H,W<br>00000000 00000000 | | NEWDT12 [R] B,H,W<br>00000000 00000000 | | |
| 002294H | NEWDT42 [R] B,H,W<br>00000000 00000000 | | NEWDT32 [R] B,H,W<br>00000000 00000000 | | |
| 002298H | — | — | — | — | |
| 00229CH | — | — | — | — | |
| 0022A0H | INTPND22 [R] B,H,W<br>00000000 00000000 | | INTPND12 [R] B,H,W<br>00000000 00000000 | | |
| 0022A4H | INTPND42 [R] B,H,W<br>00000000 00000000 | | INTPND32 [R] B,H,W<br>00000000 00000000 | | |
| 0022A8H | — | — | — | — | |
| 0022ACH | — | — | — | — | |
| 0022B0H | MSGVAL22 [R] B,H,W<br>00000000 00000000 | | MSGVAL12 [R] B,H,W<br>00000000 00000000 | | |
| 0022B4H | MSGVAL42 [R] B,H,W<br>00000000 00000000 | | MSGVAL32 [R] B,H,W<br>00000000 00000000 | | |
| 0022B8H | — | — | — | — | |
| 0022BCH | — | — | — | — | |
| 0022C0H to 0022FCH | — | | | | |
| 002300H | DFCTLR [R/W] B,H,W<br>-0------ -------- | | — | DFSTR [R/W] B,H,W<br>-----001 | WorkFlash |
| 002304H | — | — | — | — | |
| 002308H | FLIFCTLR [R/W] B,H,W<br>---0--00 | — | FLIFFER1 [R/W] B,H,W<br>-------- | FLIFFER2 [R/W] B,H,W<br>-------- | Flash / WorkFlash |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 00230C$_H$ to 0023FC$_H$ | — | | | | Reserved |
| 002400$_H$ | SEEARX [R] B,H,W<br>-0000000 00000000 | | DEEARX [R] B,H,W<br>-0000000 00000000 | | XBS RAM ECC control |
| 002404$_H$ | EECSRX [R/W] B,H,W<br>----00-- | — | EFEARX [R/W] B,H,W<br>-0000000 00000000 | | |
| 002408$_H$ | — | EFECRX [R/W] B,H,W<br>-------0 00000000 00000000 | | | |
| 00240C$_H$ to 002FFC$_H$ | — | | | | Reserved |
| 003000$_H$ | SEEARA [R] B,H,W<br>-----000 00000000 | | DEEARA [R] B,H,W<br>-----000 00000000 | | Backup RAM ECC control |
| 003004$_H$ | EECSRA [R/W] B,H,W<br>----00-- | — | EFEARA [R/W] B,H,W<br>-----000 00000000 | | |
| 003008$_H$ | — | EFECRA [R/W] B,H,W<br>-------0 00000000 00000000 | | | |
| 00300C$_H$ | TEAR0X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | RAM/ diagnosis XBS RAM |
| 003010$_H$ | TEAR1X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | |
| 003014$_H$ | TEAR2X[R] B,H,W<br>000----- -------- -0000000 00000000 | | | | |
| 003018$_H$ | TAEARX [R/W] B,H,W<br>-1111111 11111111 | | TASARX [R/W] B,H,W<br>-0000000 00000000 | | |
| 00301C$_H$ | TFECRX [R/W] B,H,W<br>----0000 | TICRX [R/W] B,H,W<br>----0000 | TTCRX [R/W] B,H,W<br>------00 00001100 | | |
| 003020$_H$ | TSRCRX [W] B,H,W<br>0------- | — | — | TKCCRX [R/W] B,H,W<br>00----00 | |
| 003024$_H$ to 00302C$_H$ | — | | | | Reserved |
| 003030$_H$ | TEAR0A[R] B,H,W<br>000----- -------- -----000 00000000 | | | | RAM/ diagnosis Backup RAM |
| 003034$_H$ | TEAR1A[R] B,H,W<br>000----- -------- -----000 00000000 | | | | |
| 003038$_H$ | TEAR2A[R] B,H,W<br>000----- -------- -----000 00000000 | | | | |
| 00303C$_H$ | TAEARA[R/W] B,H,W<br>-----111 11111111 | | TASARA[R/W] B,H,W<br>-----000 00000000 | | |
| 003040$_H$ | TFECRA [R/W] B,H,W<br>----0000 | TICRA [R/W] B,H,W<br>----0000 | TTCRA [R/W] B,H,W<br>------00 00001100 | | RAM/ diagnosis Backup RAM |
| 003044$_H$ | TSRCRA [R/W] B,H,W<br>0------- | — | — | TKCCRA [R/W] B,H,W<br>00----00 | |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | +0 | +1 | +2 | +3 | |
| 003048H to 0030FCH | — | | | | Reserved |
| 003100H | BUSDIGSR0[R/W] H,W<br>00000000 0-----00 | | BUSDIGSR1[R/W] H,W<br>00000000 0-----00 | | BUS diagnosis |
| 003104H | BUSDIGSR2[R/W] H,W<br>00000000 0-----00 | | BUSTSTR0[R/W] H,W<br>00--0000 00000000 | | |
| 003108H | BUSADR0 [R] W<br>00000000 00000000 00000000 00000000 | | | | |
| 00310CH | BUSADR1 [R] W<br>00000000 00000000 00000000 00000000 | | | | |
| 003110H | BUSADR2 [R] W<br>00000000 00000000 00000000 00000000 | | | | |
| 003114H | — | — | BUSDIGSR3[R/W] H,W<br>00000000 0-----00 | | |
| 003118H | BUSDIGSR4[R/W] H,W<br>00000000 0-----00 | | BUSTSTR1[R/W] H,W<br>00--000- 00000000 | | |
| 00311CH | — | — | — | — | |
| 003120H | BUSADR3 [R] W<br>00000000 00000000 00000000 00000000 | | | | |
| 003124H | BUSADR4 [R] W<br>00000000 00000000 00000000 00000000 | | | | |
| 003128H to 003FFCH | — | | | | Reserved |
| 004000H to 005FFCH | Backup-RAM | | | | Backup RAM area |
| 006000H to 00EFFCH | — | — | — | — | Reserved |
| 00F000H to 00FEFCH | — | — | — | — | Reserved [S] |
| 00FF00H | DSUCR [R/W] B,H,W<br>-------- -------0 | | — | — | OCDU [S] |
| 00FF04H to 00FF0CH | — | | | | Reserved [S] |
| 00FF10H | PCSR [R/W] B,H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | OCDU [S] |
| 00FF14H | PSSR [R/W] B,H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | OCDU [S] |
| 00FF18H to 00FFF4H | — | | | | Reserved [S] |
| 00FFF8H | EDIR1 [R] B,H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | OCDU [S] |
| 00FFFCH | EDIR0 [R] B,H,W<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

## 10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

**Interrupt Vector**
**64 Pins**

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| - | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | -*6 |
| - | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | -*6 |
| - | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | -*6 |
| - | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | -*6 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | 38C$_H$ | 000FFF8C$_H$ | 12*1 |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | 388$_H$ | 000FFF88$_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | 384$_H$ | 000FFF84$_H$ | 14*1 |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | 380$_H$ | 000FFF80$_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | 37C$_H$ | 000FFF7C$_H$ | 16*1 |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | 378$_H$ | 000FFF78$_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | 374$_H$ | 000FFF74$_H$ | - |
| CAN1 | 35 | 23 | ICR19 | 370$_H$ | 000FFF70$_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | 36C$_H$ | 000FFF6C$_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | 368$_H$ | 000FFF68$_H$ | - |
| - | 38 | 26 | ICR22 | 364$_H$ | 000FFF64$_H$ | -*6 |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | 360$_H$ | 000FFF60$_H$ | 23 |
| PPG 1/10/11/20/30/31 | 40 | 28 | ICR24 | 35C$_H$ | 000FFF5C$_H$ | 24*3 |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/23/43 | 41 | 29 | ICR25 | 358$_H$ | 000FFF58$_H$ | 25*3 |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/24/35 | 42 | 2A | ICR26 | 354$_H$ | 000FFF54$_H$ | 26*3 |
| PPG 7/16/17/27/37 | 43 | 2B | ICR27 | 350$_H$ | 000FFF50$_H$ | 27*3 |
| PPG 19 | 44 | 2C | ICR28 | 34C$_H$ | 000FFF4C$_H$ | 28*3 |
| 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | 348$_H$ | 000FFF48$_H$ | 29 |
| Main timer | 46 | 2E | ICR30 | 344$_H$ | 000FFF44$_H$ | 30 |
| Sub timer | | | | | | |
| PLL timer | | | | | | |
| 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | | | | | | |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1,*4 |
| A/D converter 0/1/7/10/11/14/15/16/17/22/27/28/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit (CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0 / 1/ 2<br>WG dead timer reload 0 / 1/ 2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter 32/34/35/37/38/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU7/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| - | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | -*6 |
| -<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | - |
| DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved (Used for REALOS™*8) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved (Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Used with the INT instruction | 66 \| 255 | 42 \| FF | - | $2F4_H$ \| $000_H$ | $000FFEF4_H$ \| $000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

*8: REALOS is a trademark of Cypress.

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| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| - | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | -*6 |
| - | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | -*6 |
| Multi-function serial interface ch.2 (reception completed)<br>Multi-function serial interface ch.2 (status) | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | 8*1 |
| Multi-function serial interface ch.2 (transmission completed) | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | 9*1 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | $38C_H$ | $000FFF8C_H$ | 12*1 |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | $388_H$ | $000FFF88_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | $384_H$ | $000FFF84_H$ | 14*1 |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | $380_H$ | $000FFF80_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | $37C_H$ | $000FFF7C_H$ | 16*1 |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | $378_H$ | $000FFF78_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | $374_H$ | $000FFF74_H$ | - |
| CAN1 | 35 | 23 | ICR19 | $370_H$ | $000FFF70_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | $36C_H$ | $000FFF6C_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | $368_H$ | $000FFF68_H$ | - |
| - | 38 | 26 | ICR22 | $364_H$ | $000FFF64_H$ | -*6 |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | $360_H$ | $000FFF60_H$ | 23 |
| PPG 1/10/11/20/30/31 | 40 | 28 | ICR24 | $35C_H$ | $000FFF5C_H$ | 24*3 |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/23/43 | 41 | 29 | ICR25 | $358_H$ | $000FFF58_H$ | 25*3 |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/5/15/24/35 | 42 | 2A | ICR26 | $354_H$ | $000FFF54_H$ | 26*3 |
| PPG 7/16/17/26/27/37 | 43 | 2B | ICR27 | $350_H$ | $000FFF50_H$ | 27*3 |
| PPG 8/18/19/29 | 44 | 2C | ICR28 | $34C_H$ | $000FFF4C_H$ | 28*3 |
| 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29 |
| Main timer | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Sub timer | | | | | | |
| PLL timer | | | | | | |
| 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | | | | | | |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1,*4 |
| A/D converter 0/1/7/10/11/12/14/15/16/17/19/22/26/27/28/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit (CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0 / 1/ 2<br>WG dead timer reload 0 / 1/ 2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter 32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU7/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| - | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | -*6 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| System reserved (Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved (Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66 \| 255 | 42 \| FF | - | $2F4_H$ \| $000_H$ | $000FFEF4_H$ \| $000FFC00_H$ | - |

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

**100 Pins**

| Interrupt Factor | Interrupt number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 2/3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| Multi-function serial interface ch.1 (reception completed)<br>Multi-function serial interface ch.1 (status) | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | 6*1 |
| Multi-function serial interface ch.1 (transmission completed) | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | 7*1 |
| Multi-function serial interface ch.2 (reception completed)<br>Multi-function serial interface ch.2 (status) | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | 8*1 |
| Multi-function serial interface ch.2 (transmission completed) | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | 9*1 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |

| Interrupt Factor | Interrupt number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | $38C_H$ | $000FFF8C_H$ | 12*1 |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | $388_H$ | $000FFF88_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | $384_H$ | $000FFF84_H$ | 14*1 |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | $380_H$ | $000FFF80_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | $37C_H$ | $000FFF7C_H$ | 16*1 |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | $378_H$ | $000FFF78_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | $374_H$ | $000FFF74_H$ | - |
| CAN1 | 35 | 23 | ICR19 | $370_H$ | $000FFF70_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | $36C_H$ | $000FFF6C_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | $368_H$ | $000FFF68_H$ | - |
| Multi-function serial interface ch.7 (reception completed) | 38 | 26 | ICR22 | $364_H$ | $000FFF64_H$ | 22*1 |
| Multi-function serial interface ch.7 (status) | | | | | | |
| 16-bit Free-running timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | $360_H$ | $000FFF60_H$ | 23 |
| Multi-function serial interface ch.7 (transmission completed) | | | | | | |
| PPG 1/10/11/20/21/30/31 | 40 | 28 | ICR24 | $35C_H$ | $000FFF5C_H$ | 24*3 |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/23/32/43 | 41 | 29 | ICR25 | $358_H$ | $000FFF58_H$ | 25*3 |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/5/14/15/24/25/35/44 | 42 | 2A | ICR26 | $354_H$ | $000FFF54_H$ | 26*3 |
| PPG 6/7/16/17/26/27/37 | 43 | 2B | ICR27 | $350_H$ | $000FFF50_H$ | 27*3 |
| PPG 8/9/18/19/28/29 | 44 | 2C | ICR28 | $34C_H$ | $000FFF4C_H$ | 28*3 |

| Interrupt Factor | Interrupt number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.8 (reception completed)<br>Multi-function serial interface ch.8 (status)<br>16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Main timer<br>Sub timer<br>PLL timer<br>Multi-function serial interface ch.8 (transmission completed)<br>16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| A/D converter 0/1/7/9/10/11/12/13/14/15/16 17/18/19/22/23/26/27/28/29/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit (CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 3/5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| 32-bit ICU7 (fetching/measurement)<br>Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0/1/2<br>WG dead timer reload 0/1/2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |

| Interrupt Factor | Interrupt number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU 8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| -<br>- | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

Note: It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

**120 Pins**

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 2/3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| Multi-function serial interface ch.1 (reception completed)<br>Multi-function serial interface ch.1 (status) | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | 6*1 |
| Multi-function serial interface ch.1 (transmission completed) | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | 7*1 |
| Multi-function serial interface ch.2 (reception completed)<br>Multi-function serial interface ch.2 (status) | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | 8*1 |
| Multi-function serial interface ch.2 (transmission completed) | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | 9*1 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | $38C_H$ | $000FFF8C_H$ | 12*1 |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | $388_H$ | $000FFF88_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | $384_H$ | $000FFF84_H$ | 14*1 |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | $380_H$ | $000FFF80_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | $37C_H$ | $000FFF7C_H$ | 16*1 |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | $378_H$ | $000FFF78_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | $374_H$ | $000FFF74_H$ | - |
| CAN1 | 35 | 23 | ICR19 | $370_H$ | $000FFF70_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | $36C_H$ | $000FFF6C_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | $368_H$ | $000FFF68_H$ | - |
| Multi-function serial interface ch.7 (reception completed) | 38 | 26 | ICR22 | $364_H$ | $000FFF64_H$ | 22*1 |
| Multi-function serial interface ch.7 (status) | | | | | | |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | $360_H$ | $000FFF60_H$ | 23 |
| Multi-function serial interface ch.7 (transmission completed) | | | | | | |
| PPG 0/1/10/11/20/21/30/31 | 40 | 28 | ICR24 | $35C_H$ | $000FFF5C_H$ | 24*3 |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/22/23/32/33/43 | 41 | 29 | ICR25 | $358_H$ | $000FFF58_H$ | 25*3 |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/5/14/15/24/25/35/44 | 42 | 2A | ICR26 | $354_H$ | $000FFF54_H$ | 26*3 |
| PPG 6/7/16/17/26/27/37 | 43 | 2B | ICR27 | $350_H$ | $000FFF50_H$ | 27*3 |
| PPG 8/9/18/19/28/29 | 44 | 2C | ICR28 | $34C_H$ | $000FFF4C_H$ | 28*3 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.8 (reception completed)<br>Multi-function serial interface ch.8 (status)<br>16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Main timer<br>Sub timer<br>PLL timer<br>Multi-function serial interface ch.8 (transmission completed)<br>16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| A/D converter 0/1/7/9/10/11/12/13/14/15/16/ 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit ( CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 3/5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| 32-bit ICU7 (fetching/measurement)<br>Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0/1/2<br>WG dead timer reload 0/1/2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU 8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| -<br>- | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

**144 Pins**

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 2/3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| Multi-function serial interface ch.1 (reception completed)<br>Multi-function serial interface ch.1 (status) | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | 6*1 |
| Multi-function serial interface ch.1 (transmission completed) | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | 7*1 |
| Multi-function serial interface ch.2 (reception completed)<br>Multi-function serial interface ch.2 (status) | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | 8*1 |
| Multi-function serial interface ch.2 (transmission completed) | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | 9*1 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | $38C_H$ | $000FFF8C_H$ | 12*1 |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | $388_H$ | $000FFF88_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | $384_H$ | $000FFF84_H$ | 14*1 |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | $380_H$ | $000FFF80_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | $37C_H$ | $000FFF7C_H$ | 16*1 |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | $378_H$ | $000FFF78_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | $374_H$ | $000FFF74_H$ | - |
| CAN1 | 35 | 23 | ICR19 | $370_H$ | $000FFF70_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | $36C_H$ | $000FFF6C_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | $368_H$ | $000FFF68_H$ | - |
| Multi-function serial interface ch.7 (reception completed) | 38 | 26 | ICR22 | $364_H$ | $000FFF64_H$ | 22*1 |
| Multi-function serial interface ch.7 (status) | | | | | | |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | $360_H$ | $000FFF60_H$ | 23 |
| Multi-function serial interface ch.7 (transmission completed) | | | | | | |
| PPG 0/1/10/11/20/21/30/31/40/41 | 40 | 28 | ICR24 | $35C_H$ | $000FFF5C_H$ | 24*3 |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/22/23/32/33/43 | 41 | 29 | ICR25 | $358_H$ | $000FFF58_H$ | 25*3 |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/5/14/15/24/25/34/35/44 | 42 | 2A | ICR26 | $354_H$ | $000FFF54_H$ | 26*3 |
| PPG 6/7/16/17/26/27/36/37 | 43 | 2B | ICR27 | $350_H$ | $000FFF50_H$ | 27*3 |
| PPG 8/9/18/19/28/29/38/39 | 44 | 2C | ICR28 | $34C_H$ | $000FFF4C_H$ | 28*3 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.8 (reception completed) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Multi-function serial interface ch.8 (status) | | | | | | |
| 16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | | | | | | |
| Main timer | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Sub timer | | | | | | |
| PLL timer | | | | | | |
| Multi-function serial interface ch.8 (transmission completed) | | | | | | |
| 16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | | | | | | |
| Clock calibration unit (sub oscillation) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| Multi-function serial interface ch.9 (reception completed) | | | | | | |
| Multi-function serial interface ch.9 (status) | | | | | | |
| A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit ( CR oscillation) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| Multi-function serial interface ch.9 (transmission completed) | | | | | | |
| 16-bit OCU 0 (match) / 16-bit OCU 1 (match) | | | | | | |
| 32-bit Free-run timer 4 | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 16-bit OCU 2 (match) / 16-bit OCU 3 (match) | | | | | | |
| 32-bit Free-run timer 3/5 | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 16-bit OCU 4 (match) / 16-bit OCU 5 (match) | | | | | | |
| 32-bit ICU 6 (fetching/measurement) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| Multi-function serial interface ch.10 (reception completed) | | | | | | |
| Multi-function serial interface ch.10 (status) | | | | | | |
| 32-bit ICU7 (fetching/measurement) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| Multi-function serial interface ch.10 (transmission completed) | | | | | | |
| 32-bit ICU8 (fetching/measurement) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| Multi-function serial interface ch.11 (reception completed) | | | | | | |
| Multi-function serial interface ch.11 (status) | | | | | | |
| 32-bit ICU9 (fetching/measurement) | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| WG dead timer underflow 0 / 1/ 2 | | | | | | |
| WG dead timer reload 0 / 1/ 2 | | | | | | |
| WG DTTI 0 | | | | | | |
| 32-bit ICU4 (fetching/measurement) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |
| Multi-function serial interface ch.11 (transmission completed) | | | | | | |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| Base timer 0 IRQ0<br>Base timer 0 IRQ1 | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

**176 Pins**

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Reset | 0 | 0 | - | $3FC_H$ | $000FFFFC_H$ | - |
| System reserved | 1 | 1 | - | $3F8_H$ | $000FFFF8_H$ | - |
| System reserved | 2 | 2 | - | $3F4_H$ | $000FFFF4_H$ | - |
| System reserved | 3 | 3 | - | $3F0_H$ | $000FFFF0_H$ | - |
| System reserved | 4 | 4 | - | $3EC_H$ | $000FFFEC_H$ | - |
| FPU exception | 5 | 5 | - | $3E8_H$ | $000FFFE8_H$ | - |
| Exception of instruction access protection violation | 6 | 6 | - | $3E4_H$ | $000FFFE4_H$ | - |
| Exception of data access protection violation | 7 | 7 | - | $3E0_H$ | $000FFFE0_H$ | - |
| Data access error interrupt | 8 | 8 | - | $3DC_H$ | $000FFFDC_H$ | - |
| INTE instruction | 9 | 9 | - | $3D8_H$ | $000FFFD8_H$ | - |
| Instruction break | 10 | 0A | - | $3D4_H$ | $000FFFD4_H$ | - |
| System reserved | 11 | 0B | - | $3D0_H$ | $000FFFD0_H$ | - |
| System reserved | 12 | 0C | - | $3CC_H$ | $000FFFCC_H$ | - |
| System reserved | 13 | 0D | - | $3C8_H$ | $000FFFC8_H$ | - |
| Exception of invalid instruction | 14 | 0E | - | $3C4_H$ | $000FFFC4_H$ | - |
| NMI request<br>Error generation during internal bus diagnosis<br>XBS RAM double-bit error generation<br>Backup RAM double-bit error generation<br>TPU violation | 15 | 0F | 15 ($F_H$) Fixed | $3C0_H$ | $000FFFC0_H$ | - |
| External interrupt 0-7 | 16 | 10 | ICR00 | $3BC_H$ | $000FFFBC_H$ | 0 |
| External interrupt 8-15<br>External low-voltage detection interrupt | 17 | 11 | ICR01 | $3B8_H$ | $000FFFB8_H$ | 1*7 |
| Reload timer 0/1/4/5 | 18 | 12 | ICR02 | $3B4_H$ | $000FFFB4_H$ | 2*2 |
| Reload timer 2/3/6/7 | 19 | 13 | ICR03 | $3B0_H$ | $000FFFB0_H$ | 3*2 |
| Multi-function serial interface ch.0 (reception completed)<br>Multi-function serial interface ch.0 (status) | 20 | 14 | ICR04 | $3AC_H$ | $000FFFAC_H$ | 4*1 |
| Multi-function serial interface ch.0 (transmission completed) | 21 | 15 | ICR05 | $3A8_H$ | $000FFFA8_H$ | 5*1 |
| Multi-function serial interface ch.1 (reception completed)<br>Multi-function serial interface ch.1 (status) | 22 | 16 | ICR06 | $3A4_H$ | $000FFFA4_H$ | 6*1 |
| Multi-function serial interface ch.1 (transmission completed) | 23 | 17 | ICR07 | $3A0_H$ | $000FFFA0_H$ | 7*1 |
| Multi-function serial interface ch.2 (reception completed)<br>Multi-function serial interface ch.2 (status) | 24 | 18 | ICR08 | $39C_H$ | $000FFF9C_H$ | 8*1 |
| Multi-function serial interface ch.2 (transmission completed) | 25 | 19 | ICR09 | $398_H$ | $000FFF98_H$ | 9*1 |
| Multi-function serial interface ch.3 (reception completed)<br>Multi-function serial interface ch.3 (status) | 26 | 1A | ICR10 | $394_H$ | $000FFF94_H$ | 10*1 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | $390_H$ | $000FFF90_H$ | 11 |
| Multi-function serial interface ch.4 (reception completed) / Multi-function serial interface ch.4 (status) | 28 | 1C | ICR12 | $38C_H$ | $000FFF8C_H$ | 12*1 |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | $388_H$ | $000FFF88_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) / Multi-function serial interface ch.5 (status) | 30 | 1E | ICR14 | $384_H$ | $000FFF84_H$ | 14*1 |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | $380_H$ | $000FFF80_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) / Multi-function serial interface ch.6 (status) | 32 | 20 | ICR16 | $37C_H$ | $000FFF7C_H$ | 16*1 |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | $378_H$ | $000FFF78_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | $374_H$ | $000FFF74_H$ | - |
| CAN1 / RAM diagnosis end / RAM initialization completion / Error generation during RAM diagnosis / Backup RAM diagnosis end / Backup RAM initialization completion / Error generation during Backup RAM diagnosis | 35 | 23 | ICR19 | $370_H$ | $000FFF70_H$ | - |
| CAN2 / Up/down counter 0 / Up/down counter 1 | 36 | 24 | ICR20 | $36C_H$ | $000FFF6C_H$ | - |
| Real time clock | 37 | 25 | ICR21 | $368_H$ | $000FFF68_H$ | - |
| Multi-function serial interface ch.7 (reception completed) / Multi-function serial interface ch.7 (status) | 38 | 26 | ICR22 | $364_H$ | $000FFF64_H$ | 22*1 |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) / Multi-function serial interface ch.7 (transmission completed) | 39 | 27 | ICR23 | $360_H$ | $000FFF60_H$ | 23 |
| PPG 0/1/10/11/20/21/30/31/40/41 / 16-bit Free-run timer 1 (0 detection) / (compare clear) | 40 | 28 | ICR24 | $35C_H$ | $000FFF5C_H$ | 24*3 |
| PPG 2/3/12/13/22/23/32/33/43 / 16-bit Free-run timer 2 (0 detection) / (compare clear) | 41 | 29 | ICR25 | $358_H$ | $000FFF58_H$ | 25*3 |
| PPG 4/5/14/15/24/25/34/35/44/45 | 42 | 2A | ICR26 | $354_H$ | $000FFF54_H$ | 26*3 |
| PPG 6/7/16/17/26/27/36/37/46/47 | 43 | 2B | ICR27 | $350_H$ | $000FFF50_H$ | 27*3 |
| PPG 8/9/18/19/28/29/38/39 | 44 | 2C | ICR28 | $34C_H$ | $000FFF4C_H$ | 28*3 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| Multi-function serial interface ch.8 (reception completed)<br>Multi-function serial interface ch.8 (status)<br>16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching) | 45 | 2D | ICR29 | $348_H$ | $000FFF48_H$ | 29*1 |
| Main timer<br>Sub timer<br>PLL timer<br>Multi-function serial interface ch.8 (transmission completed)<br>16-bit ICU 2 (fetching) /16-bit ICU 3 (fetching) | 46 | 2E | ICR30 | $344_H$ | $000FFF44_H$ | 30 |
| Clock calibration unit (sub oscillation)<br>Multi-function serial interface ch.9 (reception completed)<br>Multi-function serial interface ch.9 (status) | 47 | 2F | ICR31 | $340_H$ | $000FFF40_H$ | 31*1, *4 |
| A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31 | 48 | 30 | ICR32 | $33C_H$ | $000FFF3C_H$ | 32 |
| Clock calibration unit (CR oscillation)<br>Multi-function serial interface ch.9 (transmission completed)<br>16-bit OCU 0 (match) / 16-bit OCU 1 (match) | 49 | 31 | ICR33 | $338_H$ | $000FFF38_H$ | 33 |
| 32-bit Free-run timer 4<br>16-bit OCU 2 (match) / 16-bit OCU 3 (match) | 50 | 32 | ICR34 | $334_H$ | $000FFF34_H$ | 34*5 |
| 32-bit Free-run timer 3/5<br>16-bit OCU 4 (match) / 16-bit OCU 5 (match) | 51 | 33 | ICR35 | $330_H$ | $000FFF30_H$ | 35*5 |
| 32-bit ICU6 (fetching/measurement)<br>Multi-function serial interface ch.10 (reception completed)<br>Multi-function serial interface ch.10 (status) | 52 | 34 | ICR36 | $32C_H$ | $000FFF2C_H$ | 36*1 |
| 32-bit ICU7 (fetching/measurement)<br>Multi-function serial interface ch.10 (transmission completed) | 53 | 35 | ICR37 | $328_H$ | $000FFF28_H$ | 37 |
| 32-bit ICU8 (fetching/measurement)<br>Multi-function serial interface ch.11 (reception completed)<br>Multi-function serial interface ch.11 (status) | 54 | 36 | ICR38 | $324_H$ | $000FFF24_H$ | 38*1 |
| 32-bit ICU9 (fetching/measurement)<br>WG dead timer underflow 0/1/2<br>WG dead timer reload 0/1/2<br>WG DTTI 0 | 55 | 37 | ICR39 | $320_H$ | $000FFF20_H$ | 39 |
| 32-bit ICU4 (fetching/measurement)<br>Multi-function serial interface ch.11 (transmission completed) | 56 | 38 | ICR40 | $31C_H$ | $000FFF1C_H$ | 40 |

| Interrupt Factor | Interrupt Number | | Interrupt Level | Offset | Default Address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexa Decimal | | | | |
| 32-bit ICU5 (fetching/measurement)<br>A/D converter<br>32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47 | 57 | 39 | ICR41 | $318_H$ | $000FFF18_H$ | 41 |
| 32-bit OCU 6/7/10/11 (match) | 58 | 3A | ICR42 | $314_H$ | $000FFF14_H$ | 42 |
| 32-bit OCU 8/9 (match) | 59 | 3B | ICR43 | $310_H$ | $000FFF10_H$ | 43 |
| Base timer 0 IRQ0<br>Base timer 0 IRQ1 | 60 | 3C | ICR44 | $30C_H$ | $000FFF0C_H$ | 44 |
| Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>-<br>- | 61 | 3D | ICR45 | $308_H$ | $000FFF08_H$ | 45 |
| DMAC 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15 | 62 | 3E | ICR46 | $304_H$ | $000FFF04_H$ | - |
| Delay interrupt | 63 | 3F | ICR47 | $300_H$ | $000FFF00_H$ | - |
| System reserved<br>(Used for REALOS) | 64 | 40 | - | $2FC_H$ | $000FFEFC_H$ | - |
| System reserved<br>(Used for REALOS) | 65 | 41 | - | $2F8_H$ | $000FFEF8_H$ | - |
| Used with the INT instruction | 66<br>\|<br>255 | 42<br>\|<br>FF | - | $2F4_H$<br>\|<br>$000_H$ | $000FFEF4_H$<br>\|<br>$000FFC00_H$ | - |

**Note:** It does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: It does not support a DMA transfer by the status of the multi-function serial interface and $I^2C$ reception.

*2: Reload timer ch.4 to ch.7 do not support a DMA transfer by the interrupt.

*3: PPG ch.24 to ch.47 do not support a DMA transfer by the interrupt.

*4: The clock calibration unit does not support a DMA transfer by the interrupt.

*5: 32-bit Free-run timer ch.3, ch.4 and ch.5 do not support a DMA transfer by the interrupt.

*6: There is no resource corresponding to the interrupt level.

*7: It does not support a DMA transfer by the external low-voltage detection interrupt.

## 11. Electrical Characteristics

**Absolute Maximum Ratings**

| Parameter | | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply voltage *1,*2 | | $V_{CC}$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | |
| Analog power supply voltage *1,*2 | | $AV_{CC}$ | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | AVRH ≤ $AV_{CC}$ ≤ $V_{CC}$ |
| Analog reference voltage *1 | | AVRH | $V_{SS}$-0.3 | $V_{SS}$+6.0 | V | AVRH ≤ $AV_{CC}$ |
| Input voltage *1 | | $V_I$ | $V_{SS}$-0.3 | $V_{CC}$+0.3 | V | |
| Analog pin input voltage *1 | | $V_{IA5}$ | $V_{SS}$-0.3 | $V_{CC}$+0.3 | V | |
| Output voltage *1 | | $V_o$ | $V_{SS}$-0.3 | $V_{CC}$+0.3 | V | |
| Maximum clamp current | | $I_{CLAMP}$ | - | 4.0 | mA | *6 |
| Total maximum clamp current | | $\Sigma\|I_{CLAMP}\|$ | - | 20 | mA | *6 |
| "L" level maximum output current *3 | | $I_{OL1}$ | - | 15 | mA | |
| | | $I_{OL2}$ | - | 30 | mA | |
| "L" level average output current *4 | | $I_{OLAV1}$ | - | 4 | mA | *9 |
| | | $I_{OLAV2}$ | - | 12 | mA | *10 |
| "L" level total output current *5 | | $\Sigma I_{OL1}$ | - | 100 | mA | |
| | | $\Sigma I_{OL2}$ | - | 120 | mA | |
| "H" level maximum output current*3 | | $I_{OH1}$ | - | -15 | mA | |
| | | $I_{OH2}$ | - | -30 | mA | |
| "H" level average output current*4 | | $I_{OHAV1}$ | - | -4 | mA | *9 |
| | | $I_{OHAV2}$ | - | -12 | mA | *10 |
| "H" level total output current *5 | | $\Sigma I_{OH1}$ | - | -100 | mA | |
| | | $\Sigma I_{OH2}$ | - | -120 | mA | |
| Power consumption | $T_A$: -40 °C to +105 °C | $P_D$ | - | 882 | mW | *8 |
| | $T_A$: -40 °C to +125 °C | | - | 675 | mW | *8 |
| Operating temperature | | $T_A$ | -40 | +105 | °C | |
| | | | -40 | +125 | °C | *7 |
| Storage temperature | | Tstg | -55 | +150 | °C | |

*1: These parameters are based on the condition that $V_{SS}$ = $AV_{SS}$ = 0.0 V

*2: Caution must be taken that $AV_{CC}$, AVRH do not exceed $V_{CC}$ upon power-on and under other circumstances.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

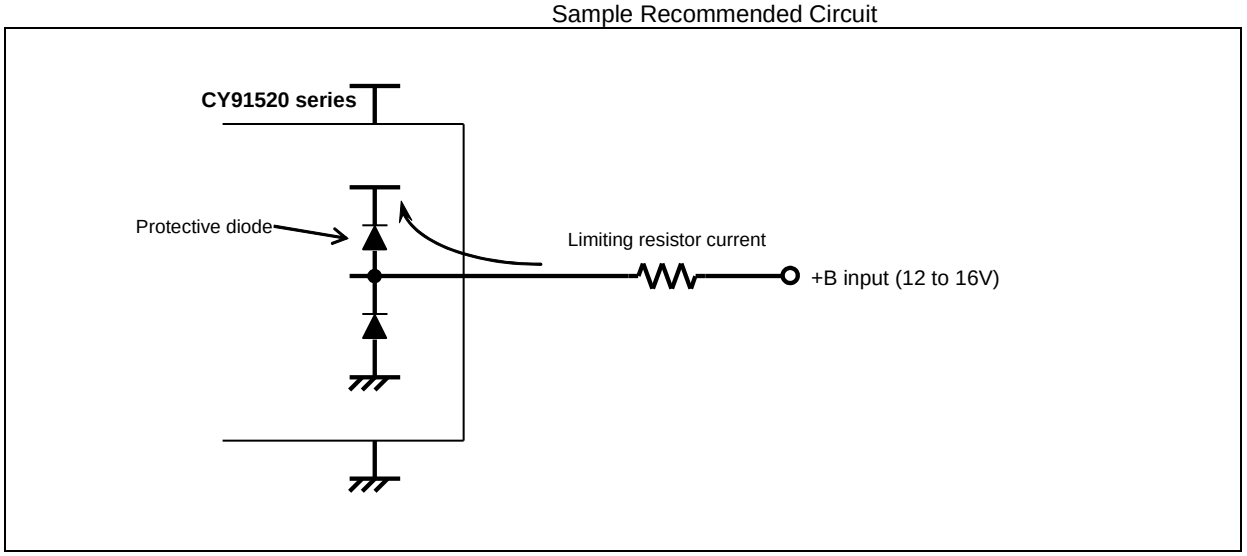
*6:
- Corresponding pins: all general-purpose ports except P035, 041, 093, 122.
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the $V_{CC}$ pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*7: When it is used under this condition, contact your sales representative.

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit




**<WARNING>**

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

**Recommended Operating Conditions**

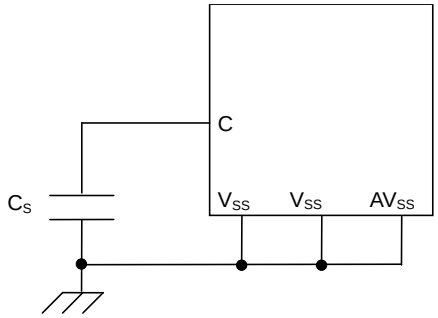
($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.5 | 5.5 | V | Recommended operation guarantee range (When 5.0 V is used) |
| | | 3.0 | 3.6 | V | Recommended operation guarantee range (When 3.3 V is used) |
| | | 2.7 | 5.5 | V | Operation guarantee range*1 |
| Smoothing capacitor *2 | $C_S$ | 4.7 (tolerance within ±50 %) | | µF | Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than $C_S$ as the smoothing capacitor on the VCC pin. |
| Operating temperature | $T_A$ | -40 | +105 | °C | |
| | | -40 | +125 | °C | *3 |

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
*2: See the following diagram for details on the connection of smoothing capacitor $C_S$.
*3: When it is used under this condition, contact your sales representative.

· C Pin Connection Diagram




**<WARNING>**

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

**DC Characteristics**

($T_A$: -40 °C to +105 °C, $V_{CC}$ = AVcc = 5.0 V ± 10 %/3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC}5$ | VCC | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at normal operation | | - | 60 | 80 | mA | |
| | | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at Flash write | | - | 70 | 90 | mA | |
| | | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at Flash erase | | - | 70 | 90 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at normal operation | | - | 54 | 71 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at Flash write | | - | 64 | 81 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at Flash erase | | - | 64 | 81 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at normal operation | | - | 46 | 62 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at Flash write | | - | 56 | 72 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at Flash erase | | - | 56 | 72 | mA | |
| | $I_{CCS}5$ | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at CPU sleep mode | | - | 45 | 61 | mA | |
| | $I_{CCBS}5$ | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at bus sleep mode | | - | 23 | 51 | mA | |
| | $I_{CCT}5$ | | Watch mode | When using crystal 4 MHz $T_A$ = +25 °C* | - | 1500 | 2610 | µA | |
| | | | | When using built-in CR clock 50 kHz $T_A$ = +25 °C* | - | 450 | 2000 | | |
| | | | | When using sub clock 32 kHz $T_A$ = +25 °C* | - | 460 | 2000 | | |
| | $I_{CCH}5$ | | Stop mode | $T_A$ = +25 °C* | - | 450 | 2000 | µA | |
| | $I_{CCT}52$ | | Watch mode (power off) | When using crystal 4 MHz $T_A$ = +25 °C* | - | 1100 | 1300 | µA | LVD/ RTC operation, Backup RAM 8 KB retention |
| | | | | When using built-in CR clock 50 kHz , $T_A$ = +25 °C* | - | 77 | 267 | | |
| | | | | When using sub clock 32 kHz $T_A$ = +25 °C* | - | 100 | 285 | | |
| | $I_{CCH}52$ | | Stop mode (power off) | $T_A$ = +25 °C* | - | 74 | 265 | µA | Backup RAM 8 KB retention |

($T_A$: -40 °C to +125 °C, $V_{CC}$ = AVcc = 5.0 V ± 10 %/3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC}5$ | VCC | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at normal operation | | - | 60 | 102 | mA | |
| | | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at Flash write | | - | 70 | 115 | mA | |
| | | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at Flash erase | | - | 70 | 115 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at normal operation | | - | 54 | 92 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at Flash write | | - | 64 | 105 | mA | |
| | | | Operating frequency $F_{CP}$ = 64 MHz, Fcpp = 32 MHz, at Flash erase | | - | 64 | 105 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at normal operation | | - | 46 | 82 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at Flash write | | - | 56 | 95 | mA | |
| | | | Operating frequency $F_{CP}$ = 48 MHz, Fcpp = 24 MHz, at Flash erase | | - | 56 | 95 | mA | |
| | $I_{CCS}5$ | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at CPU sleep mode | | - | 45 | 82 | mA | |
| | $I_{CCBS}5$ | | Operating frequency $F_{CP}$ = 80 MHz, Fcpp = 40 MHz, at bus sleep mode | | - | 23 | 72 | mA | |
| | $I_{CCT}5$ | | Watch mode | When using crystal 4 MHz $T_A$ = +25 °C* | - | 1500 | 2610 | µA | |
| | | | | When using built-in CR clock 50 kHz $T_A$ = +25 °C* | - | 450 | 2000 | | |
| | | | | When using sub clock 32 kHz $T_A$ = +25 °C* | - | 460 | 2000 | | |
| | $I_{CCH}5$ | | Stop mode | $T_A$ = +25 °C* | - | 450 | 2000 | µA | |
| | $I_{CCT}52$ | | Watch mode (power off) | When using crystal 4 MHz $T_A$ = +25 °C* | - | 1100 | 1300 | µA | LVD/ RTC operation, Backup RAM 8 KB retention |
| | | | | When using built-in CR clock 50 kHz , $T_A$ = +25 °C* | - | 77 | 267 | | |
| | | | | When using sub clock 32 kHz $T_A$ = +25 °C* | - | 100 | 285 | | |
| | $I_{CCH}52$ | | Stop mode (power off) | $T_A$ = +25 °C* | - | 74 | 265 | µA | Backup RAM 8 KB retention |

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/Vcc = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leak current | $I_{IL}$ | All input pins | $V_{CC}$ = $AV_{CC}$ = 5.5 V<br>$V_{SS}$<$V_I$<$V_{CC}$ | -5 | - | 5 | µA | |
| Input capacitance 1 | $C_{IN1}$ | Other than VCC,VSS, AVCC, AVSS, C | - | - | 5 | 15 | pF | |
| Pull-up resistance | $R_{UP1}$ | RSTX, NMIX | $V_{CC}$ = 5.0 V ± 10 % | 25 | - | 100 | kΩ | |
| | | | Vcc = 3.3 V ± 0.3 V | 45 | - | 140 | | |
| | $R_{UP2}$ | P073,074 076,077 | $V_{CC}$ = 5.0 V ± 10 % | 25 | - | 60 | | |
| | | | Vcc = 3.3 V ± 0.3 V | 33 | - | 90 | | |
| | $R_{UP3}$ | Port pin other than P035, 041,073,074, 076,077,093, 122 | $V_{CC}$ = 5.0 V ± 10 % | 25 | - | 100 | kΩ | |
| | | | Vcc = 3.3 V ± 0.3 V | 45 | - | 140 | | |
| “H” level output voltage | $V_{OH1}$ | Normal output pin | Vcc = 4.5 V<br>$I_{OH}$ = -4.0 mA | $V_{CC}$ -0.5 | - | $V_{CC}$ | V | |
| | | | Vcc = 3.0 V<br>$I_{OH}$ = -2.0 mA | | | | | |
| | $V_{OH2}$ | P073,074,076, 077 | Vcc = 4.5 V<br>$I_{OH}$ = -3.0 mA | $V_{CC}$ -0.5 | - | $V_{CC}$ | V | $I^2C$ pin output |
| | $V_{OH3}$ | P103 to 106 | Vcc = 4.5 V<br>$I_{OH}$ = -12.0 mA | $V_{CC}$ -0.5 | - | $V_{CC}$ | V | |
| | | | Vcc = 3.0 V<br>$I_{OH}$ = -8.0 mA | | | | | |
| “L” level output voltage | $V_{OL1}$ | Normal output pin | Vcc = 4.5 V<br>$I_{OL}$ = 4.0 mA | 0 | - | 0.4 | V | |
| | | | Vcc = 3.0 V<br>$I_{OL}$ = 2.0 mA | | | | | |
| | $V_{OL2}$ | P073,074,076, 077 | Vcc = 4.5 V<br>$I_{OL}$ = 3.0 mA | 0 | - | 0.4 | V | $I^2C$ pin output |
| | $V_{OL3}$ | P103 to 106 | Vcc = 4.5 V<br>$I_{OL}$ = 12.0 mA | 0 | - | 0.4 | V | |
| | | | Vcc = 3.0 V<br>$I_{OL}$ = 8.0 mA | | | | | |

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH1}$ | P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153 | CMOS hysteresis input level | 0.7× $V_{CC}$ | - | $V_{CC}$ | V | |
| | $V_{IH3}$ | Port other than $V_{IH1}$ | Automotive input level | 0.8× $V_{CC}$ | - | $V_{CC}$ | V | |
| | $V_{IH5}$ | RSTX,NMIX,MD 0,MD1 | CMOS hysteresis input level | 0.8× $V_{CC}$ | - | $V_{CC}$ | V | |
| | $V_{IHT}$ | DEBUGIF | TTL input level | 2 | - | $V_{CC}$ | V | |
| "L" level input voltage | $V_{IL1}$ | P000,002,003, 005,020,022, 024,026,150, 151,035,041, 045,055,057, 071-077,081, 082,093,096, 097,100-102, 111,115,116, 122,126,130, 134,142,143, 144,153 | CMOS hysteresis input level | Vss | - | 0.3× $V_{CC}$ | V | |
| | $V_{IL3}$ | Port other than $V_{IH1}$ | Automotive input level | Vss | - | 0.5× $V_{CC}$ | V | |
| | $V_{IL5}$ | RSTX,NMIX,MD 0,MD1 | CMOS hysteresis input level | Vss | - | 0.2× $V_{CC}$ | V | |
| | $V_{ILT}$ | DEBUGIF | TTL input level | Vss | - | 0.8 | V | |

*: It is a standard in BRAMSC (Backup RAM sleep control bit) = 1 (Enter the state of the sleep at the standby mode) condition.

**AC Characteristics**

(1) Main Clock Timing

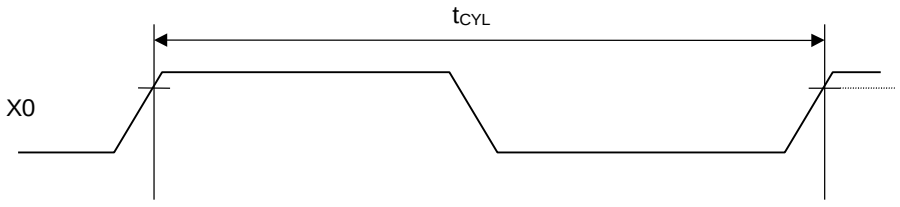
($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | $F_C$ | X0, X1 | | - | 4 | 16 | MHz | |
| Source oscillation clock cycle time | $t_{CYL}$ | X0, X1 | | 62.5 | 250 | - | ns | |
| Internal operating clock frequency*1 | $F_{CP}$ | - | | 2 | - | 80 | MHz | CPU clock |
| | $F_{CPP}$ | | | 1 | | 40 | | Peripheral bus clock |
| | $F_{CPT}$ | | | 1 | | 40 | | External bus clock (When $V_{CC}$ = 5.0 V is used) *2 |
| | | | | 1 | | 32 | | External bus clock (When $V_{CC}$ = 3.3 V is used) |
| Internal operating clock cycle time*1 | $t_{CP}$ | - | - | 12.5 | - | 500 | ns | CPU clock |
| | $t_{CPP}$ | | | 25 | | 1000 | | Peripheral bus clock |
| | $t_{CPT}$ | | | 25 | | 1000 | | External bus clock (When $V_{CC}$ = 5.0 V is used) |
| | | | | 31.25 | | 1000 | | External bus clock (When $V_{CC}$ = 3.3 V is used) |
| CAN PLL jitter (during lock) | $t_{PJ}$ | - | | -10 | - | 10 | ns | $F_{CP}$ = 80 MHz (4 MHz Multiplied by 20) |
| Built-in CR oscillation frequency | $F_{CCR}$ | - | | 50 | 100 | 150 | kHz | |

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

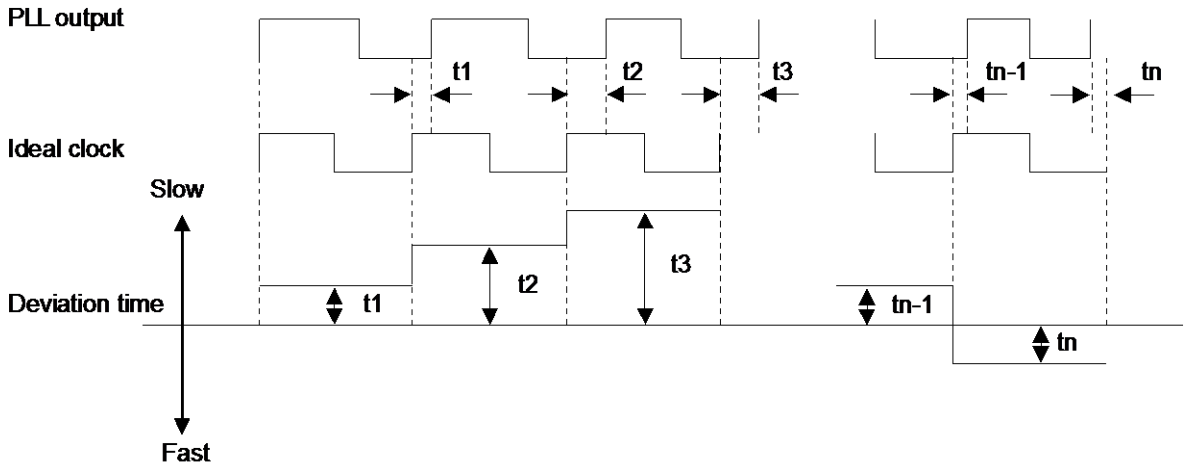
*2: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).

• X0,X1 clock timing



• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

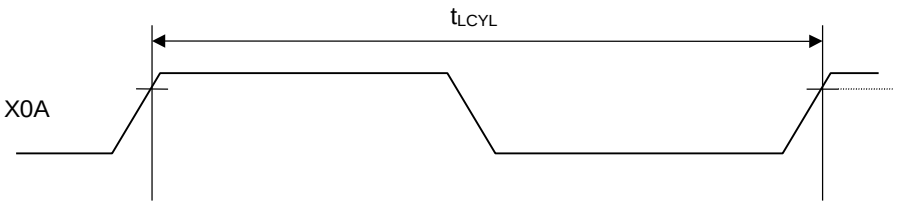


(1-2) Sub clock timing

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

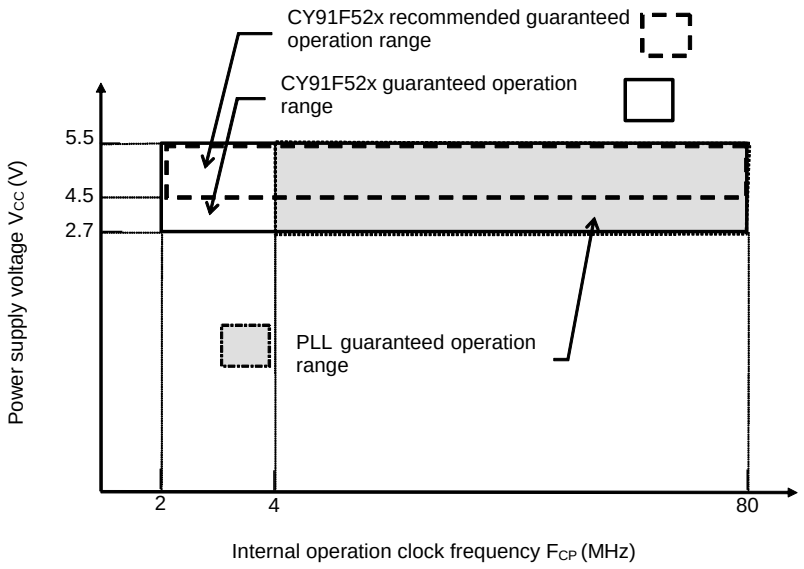
| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | $F_{CL}$ | X0A, X1A | - | - | 32.768 | - | kHz | |
| Source oscillation clock cycle time | $t_{LCYL}$ | X0A, X1A | | - | 30.52 | - | µs | |

・X0A,X1A clock timing



- Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

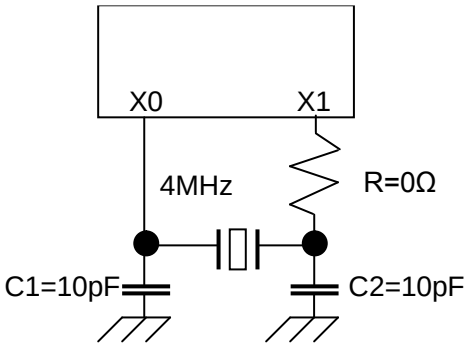



**Note:** The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Oscillation clock frequency vs. Internal operation clock frequency

| | | Internal operation clock frequency | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Main Clock | PLL clock | | | | | | |
| | | | Multiplied by 1 | Multiplied by 2 | Multiplied by 3 | Multiplied by 4 | ... | Multiplied by 19 | Multiplied by 20 |
| Oscillation clock frequency | 4 MHz | 2 MHz | 4 MHz | 8 MHz | 12 MHz | 16 MHz | ... | 76 MHz | 80 MHz |

・Example of oscillation circuit

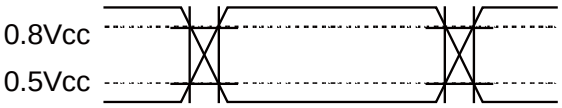



**Note:** As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20 ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20 ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

AC characteristics are specified by the following measurement reference voltage values.

● Input Signal Waveform

Hysteresis Input Pin (Automotive)




Hysteresis Input Pin (CMOS schmitt)

● Output Signal Waveform

Output Pin

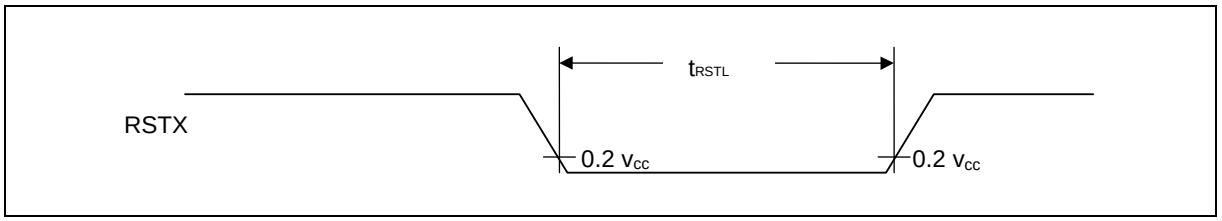
(2) Reset Input

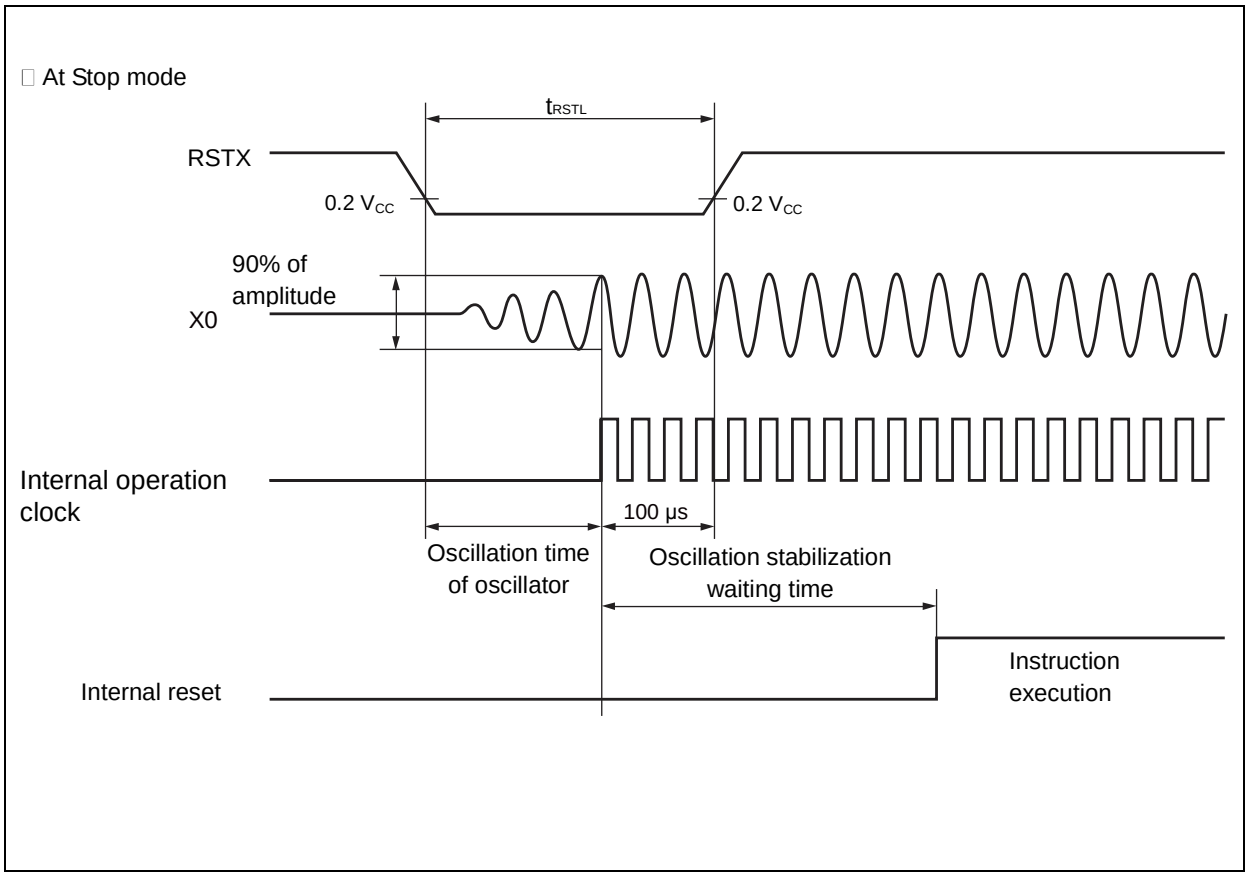
($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | RSTX | – | 10 | – | µs | When normal operation |
| | | | | Oscillation time of oscillator* +100 | – | µs | At Stop mode<br>At Power-on*2 |
| | | | | 100 | – | µs | At Watch mode |
| Width for reset input removal | | | | 1 | – | µs | |

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90 %. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using CY91F52xxxD or CY91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.



(3) Power-on Conditions

(3-1) [CY9152xxxB/CY9152xxxC/CY9152xxxD]

($T_A$: -40 °C to +125 °C, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Level detection voltage | – | $V_{CC}$ | – | 2.024 | 2.2 | 2.376 | V | |
| Level detection hysteresis width | – | $V_{CC}$ | – | – | 100 | – | mV | |
| Level detection time | – | – | – | – | – | 30 | µs | *1 |
| Power off time | $t_{OFF}$ | $V_{CC}$ | – | 50 | – | – | ms | *2 |
| Power ramp rate | dV/dt | $V_{CC}$ | VCC: 0.2 V to 2.376 V | – | – | 4 | mV/µs | *3 |
| C pin voltage at Power-on | – | C | – | – | – | 60 | mV | *4 |

*1: This spec is at 4 mV/µs of power ramp rate. If the power ramp rate is faster than 4mV/µs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Vcc must be held below 0.2 V for a minimum period of $t_{OFF}$.

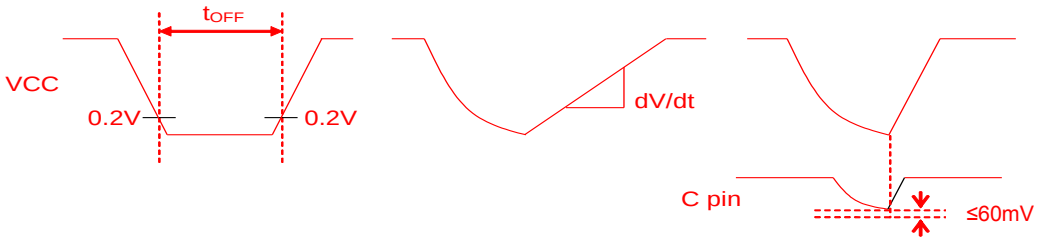
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when VCC is turned on again.

Note:

When using CY91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use CY91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on



(3-2) [CY9152xxxE]

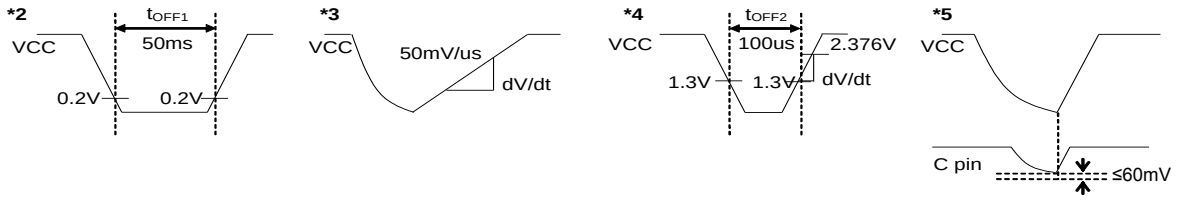
($T_A$: -40 °C to +125 °C, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Level detection voltage | – | $V_{CC}$ | – | 2.024 | 2.2 | 2.376 | V | |
| Level detection hysteresis width | – | $V_{CC}$ | – | – | 100 | – | mV | |
| Level detection time | – | – | – | – | – | 30 | µs | *1 |
| Power off time | $t_{OFF1}$ | $V_{CC}$ | Vcc ≤ 0.2 V | 50 | – | – | ms | *2 |
| | $t_{OFF2}$ | $V_{CC}$ | Vcc ≤ 1.3 V | 100 | – | – | µs | *4 |
| Power ramp rate | dV/dt | $V_{CC}$ | VCC: 0.2 V to 2.376 V ($t_{OFF1}$ < 50 ms ) | – | – | 50 | mV/µs | *3 |
| | dV/dt | $V_{CC}$ | VCC: 1.3 V to 2.376 V ($t_{OFF2}$ ≥ 100 µs) | – | – | 1000 | mV/µs | *4 |
| C pin voltage at Power-on | – | C | – | – | – | 60 | mV | *5 |
| Maximum ramp rate guaranteed to not generate power-on reset | \|dV/dt\| | Vcc | VCC: Between 2.4 V and 4.5 V | – | – | 50 | mV/µs | *6 |

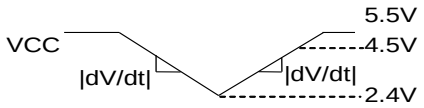
*1: The specified level detection time applies only for power ramp rate of 1000 mV/µs or less.
*2: Vcc must be held below 0.2 V for a minimum period of $t_{OFF1}$.
*3: Power-on can detect by satisfying power ramp rate when $t_{OFF1}$ is not satisfied.
*4: Vcc must be held below 1.3 V for a minimum period of $t_{OFF2}$.
Power ramp rate must be 1000 mV/µs or less from 1.3 V to 2.376 V.
Power-on can detect by satisfying power ramp rate and power off time.
*5: C-pin voltage is below 60 mV when VCC is turned on again.
*6: This specification is specified the power supply fluctuation after power on detection. When VCC voltage is between 2.4 V and 4.5 V, the power supply fluctuation is below 50 mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5 V and 5.5 V.

Note: When using CY91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

・Power off time, Power ramp rate, C pin voltage at Power-on



・Maximum ramp rate guaranteed to not generate power-on reset



(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR : MD0 = 0, SMR: SCINV = 0, SCR:SPI = 0

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V±0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**

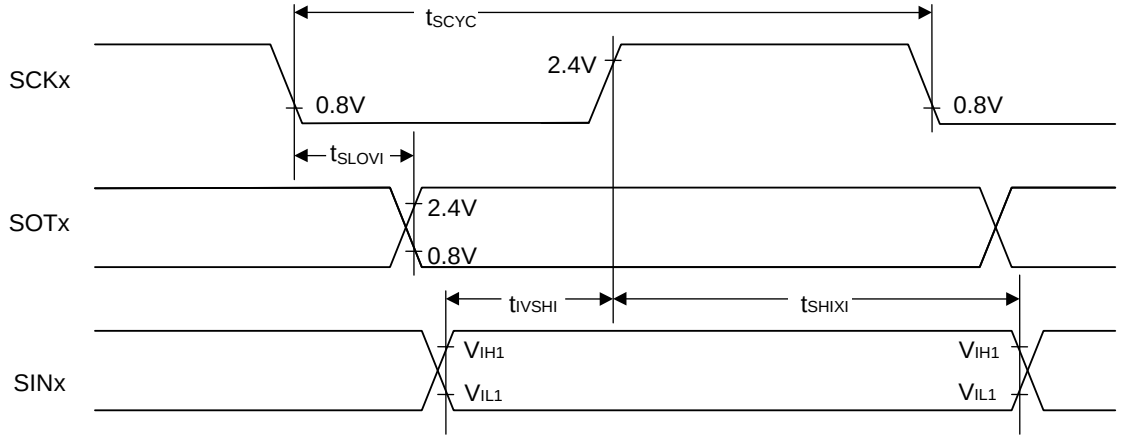
AC characteristic in CLK synchronized mode.

$C_L$ is the load capacitance applied to pins during testing.

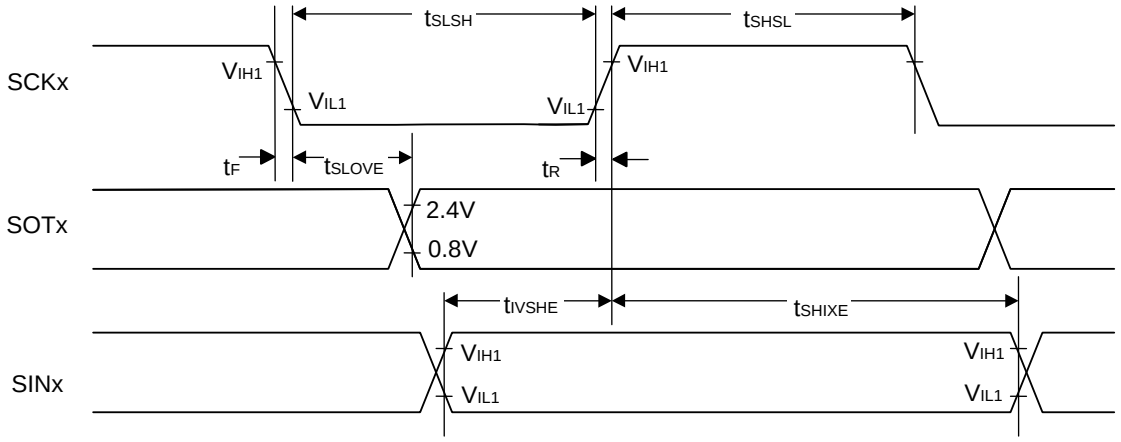
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

- Internal shift clock mode




- External shift clock mode



(4-1-2) Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR : MD0 = 0, SMR: SCINV = 1, SCR:SPI = 0

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3, SIN4 | | 300 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**

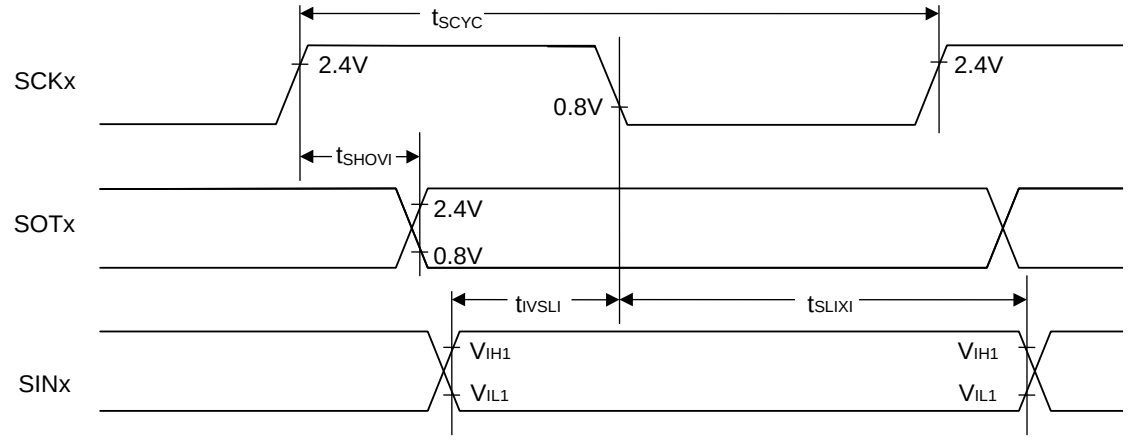
AC characteristic in CLK synchronized mode.

$C_L$ is the load capacitance applied to pins during testing.

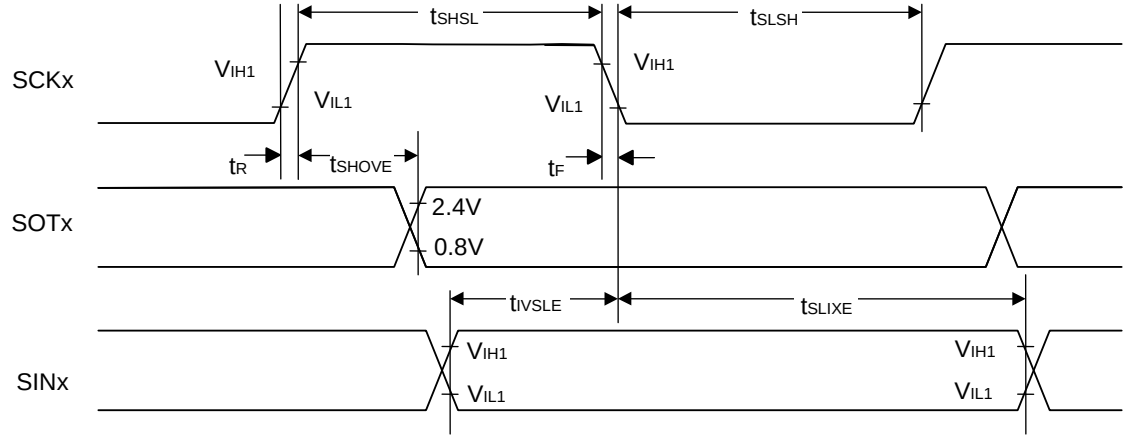
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.

See Hardware Manual for details.

- Internal shift clock mode




- External shift clock mode

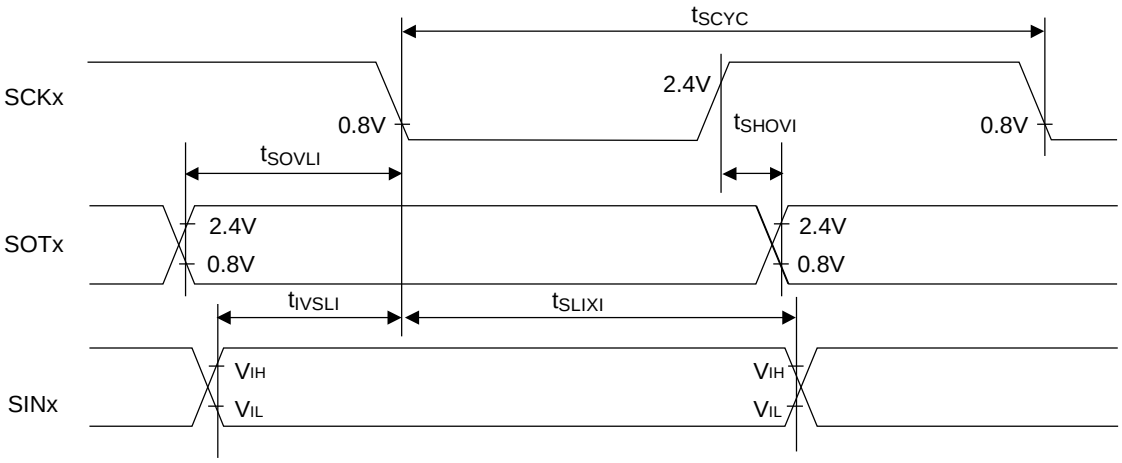


(4-1-3) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 0, SCR:SPI = 1
($T_A$:-40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

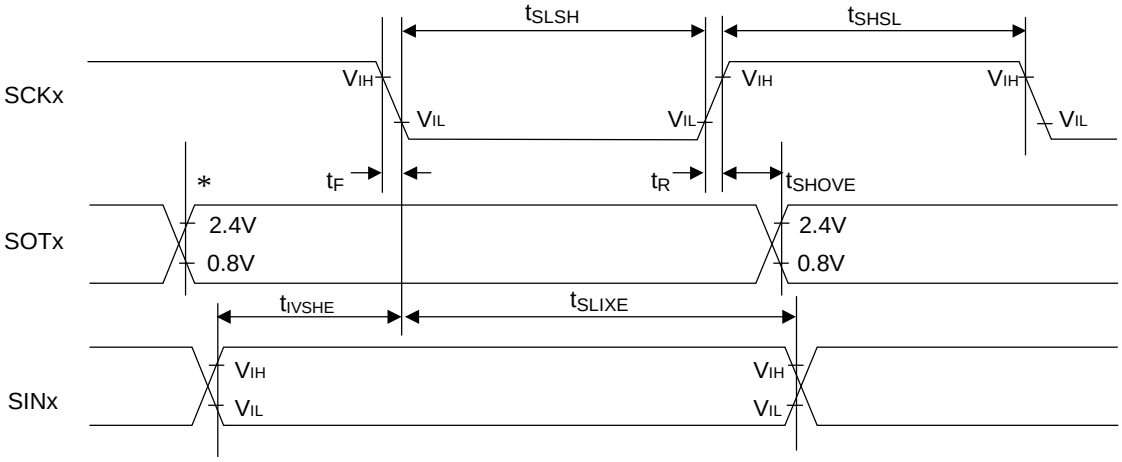
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSLI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| SOT→SCK↓ delay time | $t_{SOVLI}$ | SCK0 to SCK11 SOT0 to SOT11 | | $2t_{CPP}$ -30 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+ 10 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$ -10 | - | ns | |
| SCK ↑ → SOT delay time | $t_{SHOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK ↓ setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | $t_{SLIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**
AC characteristic in CLK synchronized mode.
$C_L$ is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.
See Hardware Manual for details.

□ Internal shift clock mode




・ External shift clock mode



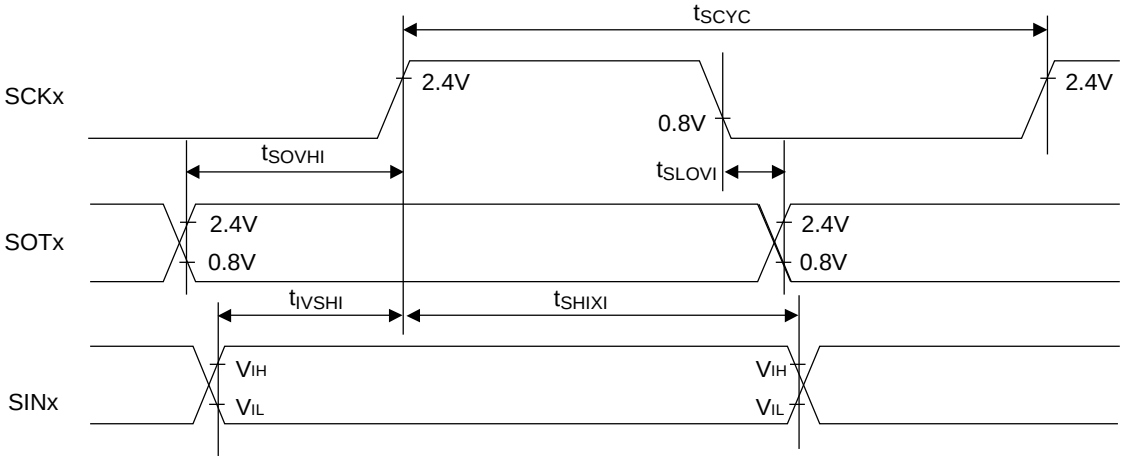

*: It writes in the TDR register and, then, it changes.

(4-1-4) Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 0, SMR:SCINV = 1, SCR:SPI = 1
($T_A$:-40 °C to +125 °C, $V_{CC}$ = A $V_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ±0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

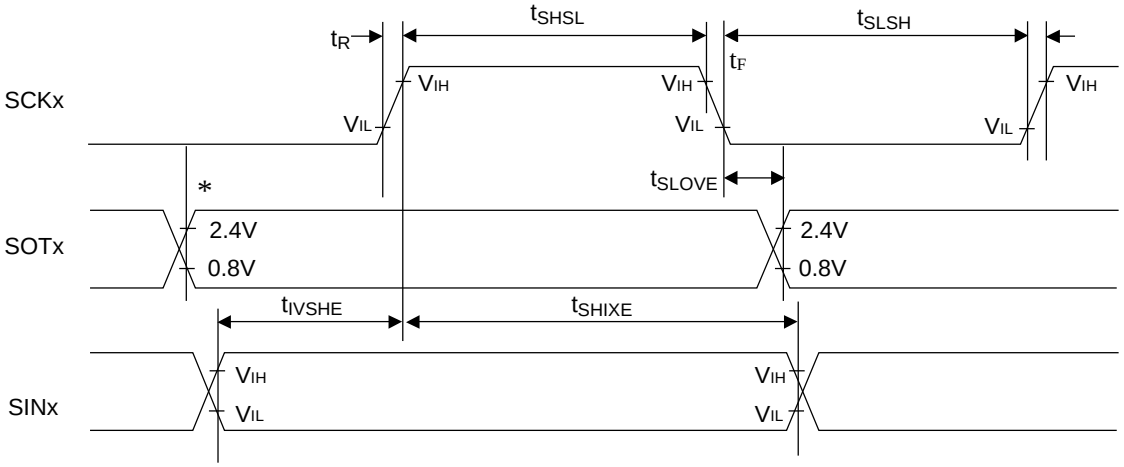
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| SCK↓→ SOT delay time | $t_{SLOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK↑setup time | $t_{IVSHI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK↑→ Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCK0 to SCK11 SOT0 to SOT11 | | $2t_{CPP}$-30 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK↓→ SOT delay time | $t_{SLOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK↑setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK↑→ Valid SIN hold time | $t_{SHIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**
AC characteristic in CLK synchronized mode.
$C_L$ is the load capacitance applied to pins during testing.
The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400 kbps or less.
See Hardware Manual for details.

• Internal shift clock mode




• External shift clock mode




*: It writes in the TDR register and, then, it changes.

(4-1-5) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used : SCSCR:CSEN = 1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1
($T_A$:-40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V±0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↓→SCK↓ setup time | $t_{CSSI}$ | SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $t_{CSSU}$-50 *1 | $t_{CSSU}$+0 *1 | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSSU}$-50 *1 | $t_{CSSU}$+300 *1 | ns | |
| SCK↑→SCS↑ hold time | $t_{CSHI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSHD}$-10 *2 | $t_{CSHD}$+50 *2 | ns | |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSHD}$-300 *2 | $t_{CSHD}$+50 *2 | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSDS}$-50 *3 | $t_{CSDS}$+50 *3 | ns | |

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↓→SCK↓ setup time | $t_{CSSE}$ | SCK1 to SCK11<br>SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$+30 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↑→SCS↑ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | | $3t_{CPP}$+30 | - | ns | |
| SCS↓→SOT delay time | $t_{DSE}$ | SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 , SOT2 ,<br>SOT5 to SOT11 | | - | 40 | ns | |
| | | SCS3,<br>SCS40 to SCS43<br>SOT3 , SOT4 | | - | 300 | ns | |
| SCS↑→SOT delay time | $t_{DEE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↓→SCS↓ clock switch time | $t_{SCC}$ | SCK1 , SCK2,<br>SCK5 to SCK11<br>SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$-10 | $3t_{CPP}$+50 | ns | Internal shift clock mode Round operation output pin: $C_L$ = 50 pF |
| | | SCK3 , SCK4<br>SCS3 ,<br>SCS40 to SCS43 | | $3t_{CPP}$-300 | $3t_{CPP}$+50 | ns | |

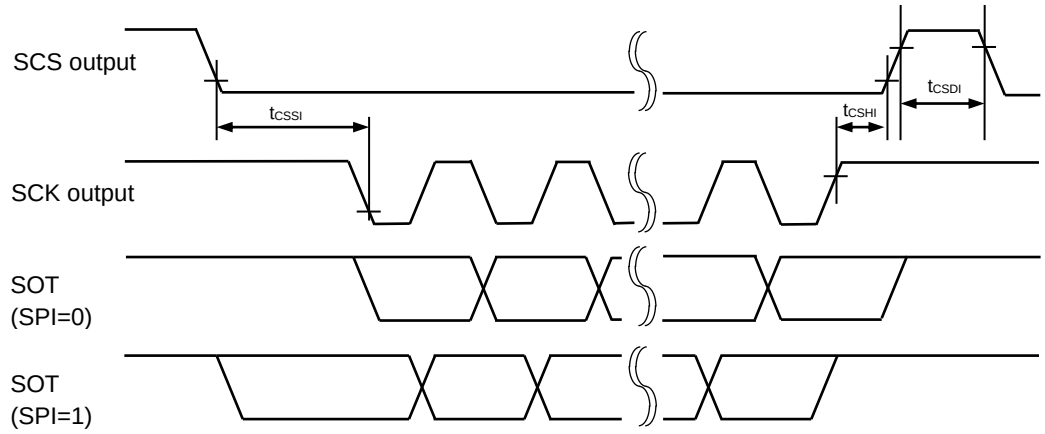
*1: $t_{CSSU}$ = SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: $t_{CSHD}$ = SCSTR:CSHD7-0×Serial chip select timing operating clock

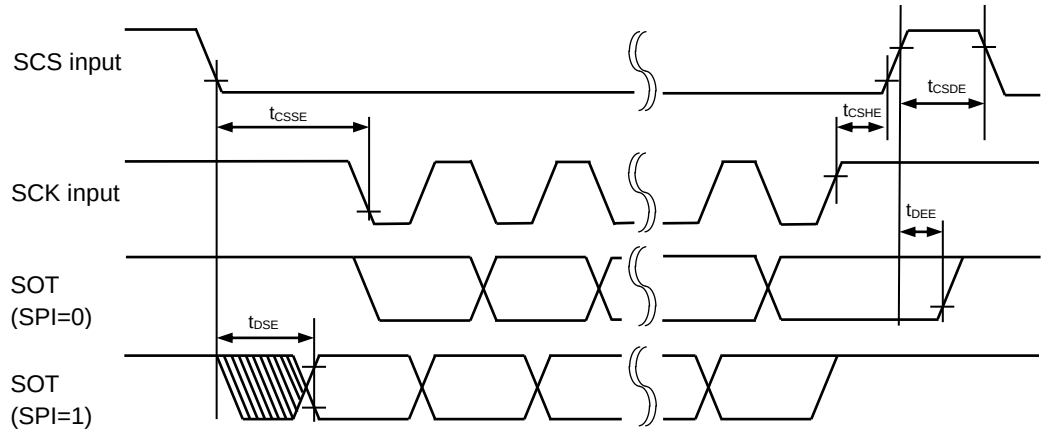
*3: $t_{CSDS}$ = SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

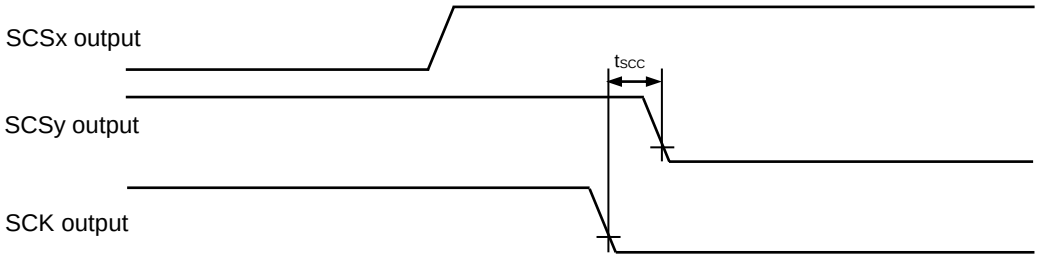
Please see the hardware manual for details of above-mentioned *1,*2, and *3.




When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode




When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
External shift clock mode




When Serial chip select is used , Serial clock output mark level "H"
,Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

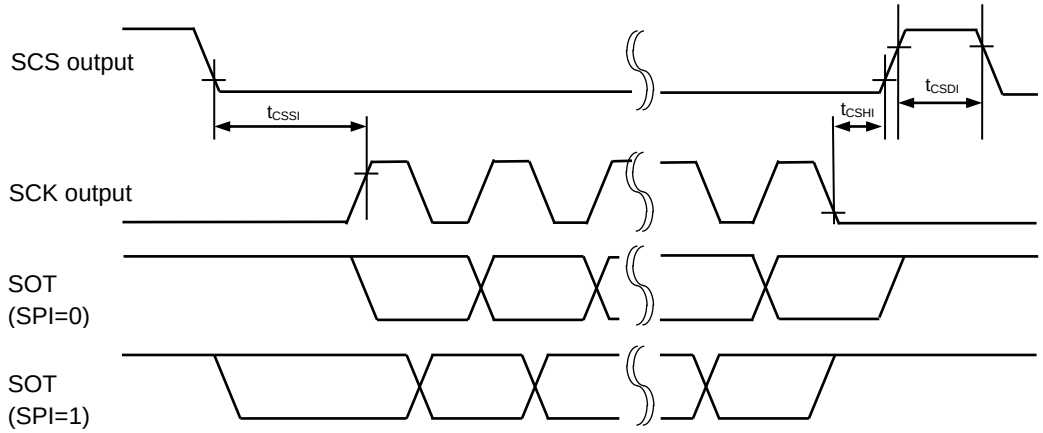
(4-1-6) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used : SCSCR:CSEN = 1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV = 1,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL = 1
($T_A$:-40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↓→SCK↑ setup time | $t_{CSSI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $t_{CSSU}$-50 *1 | $t_{CSSU}$+0 *1 | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSSU}$-50 *1 | $t_{CSSU}$+300 *1 | ns | |
| SCK↓→SCS↑ hold time | $t_{CSHI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSHD}$-10 *2 | $t_{CSHD}$+50 *2 | ns | |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSHD}$-300 *2 | $t_{CSHD}$+50 *2 | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSDS}$-50 *3 | $t_{CSDS}$+50 *3 | ns | |

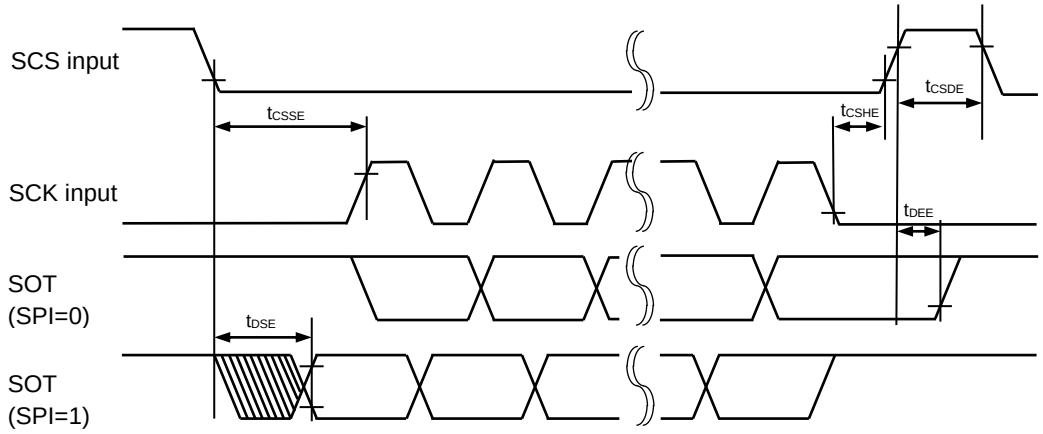
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↓→SCK↑ setup time | $t_{CSSE}$ | SCK1 to SCK11<br>SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$+30 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↓→SCS↑ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | | $3t_{CPP}$+30 | - | ns | |
| SCS↓→SOT delay time | $t_{DSE}$ | SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 , SOT2,<br>SOT5 to SOT11 | | - | 40 | ns | |
| | | SCS3,<br>SCS40 to SCS43<br>SOT3 , SOT4 | | - | 300 | ns | |
| SCS↑→SOT delay time | $t_{DEE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↑→SCS↓ clock switch time | $t_{SCC}$ | SCK1 , SCK2,<br>SCK5 to SCK11<br>SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$-10 | $3t_{CPP}$+50 | ns | Internal shift clock mode Round operation output pin: $C_L$ = 50 pF |
| | | SCK3 , SCK4<br>SCS3 ,<br>SCS40 to SCS43 | | $3t_{CPP}$-300 | $3t_{CPP}$+50 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: $t_{CSHD}$ = SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: $t_{CSDS}$ = SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

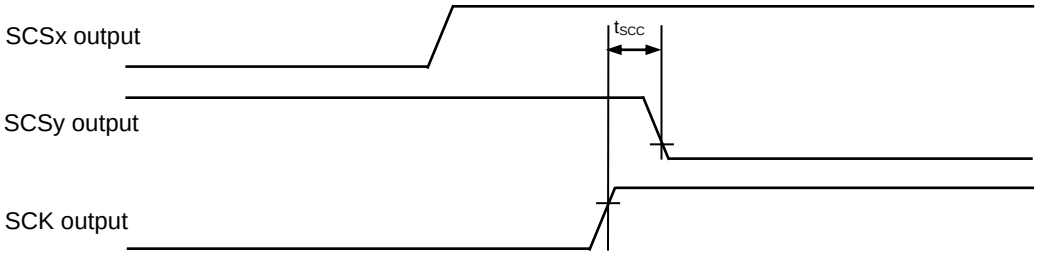
Please see the hardware manual for details of above-mentioned *1,*2, and *3




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

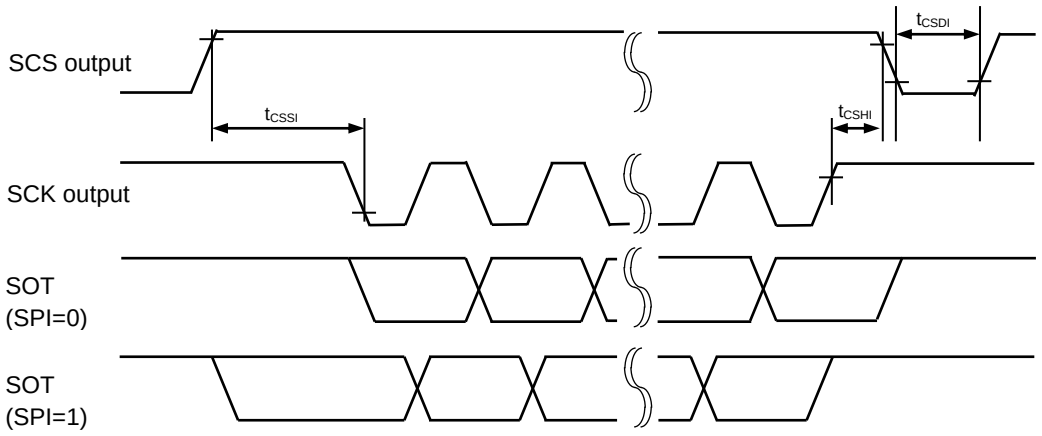
(4-1-7) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used : SCSCR:CSEN = 1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV = 0,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL = 0
($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3V±0.3V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↓ setup time | $t_{CSSI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $t_{CSSU}$-50 *1 | $t_{CSSU}$+0 *1 | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSSU}$-50 *1 | $t_{CSSU}$ +300 *1 | ns | |
| SCK↑→SCS↓ hold time | $t_{CSHI}$ | SCK1 to SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSHD}$-10 *2 | $t_{CSHD}$+50 *2 | ns | |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSHD}$-300 *2 | $t_{CSHD}$+50 *2 | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSDS}$-50 *3 | $t_{CSDS}$+50 *3 | ns | |

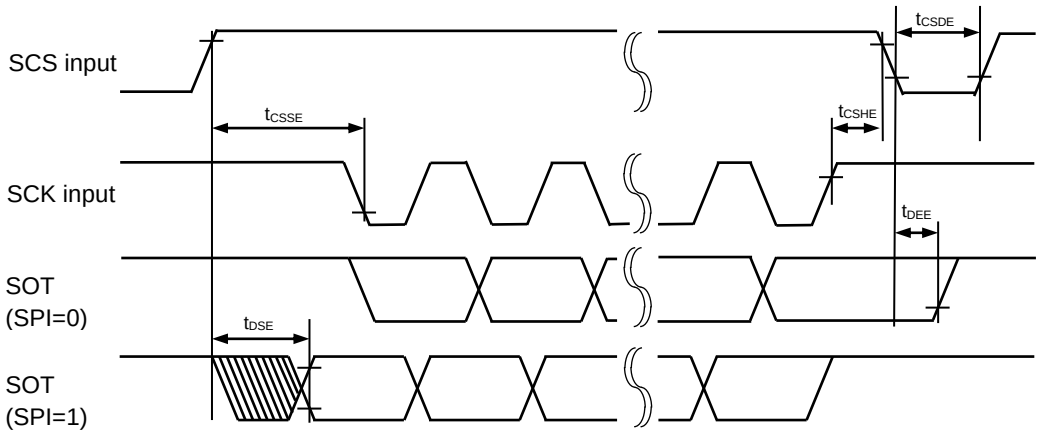
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↓ setup time | $t_{CSSE}$ | SCK1 to SCK11<br>SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$+30 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↑→SCS↓ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | | $3t_{CPP}$+30 | - | ns | |
| SCS↑→SOT delay time | $t_{DSE}$ | SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 , SOT2,<br>SOT5 to SOT11 | | - | 40 | ns | |
| | | SCS3 ,<br>SCS40 to SCS43<br>SOT3 , SOT4 | | - | 300 | ns | |
| SCS↓→SOT delay time | $t_{DEE}$ | SCS1 to ~SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↓→SCS↑ clock switch time | $t_{SCC}$ | SCK1 , SCK2,<br>SCK5 to SCK11<br>SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$-10 | $3t_{CPP}$+50 | ns | Internal shift clock mode Round operation output pin: $C_L$ = 50 pF |
| | | SCK3 , SCK4<br>SCS3 ,<br>SCS40 to SCS43 | | $3t_{CPP}$-300 | $3t_{CPP}$+50 | ns | |

*1: $t_{CSSU}$ = SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: $t_{CSHD}$ = SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: $t_{CSDS}$ = SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

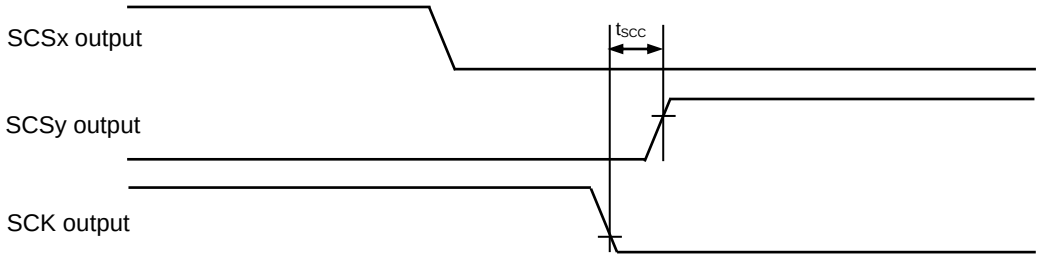
Please see the hardware manual for details of above-mentioned *1,*2, and *3.




When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode




When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode




When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

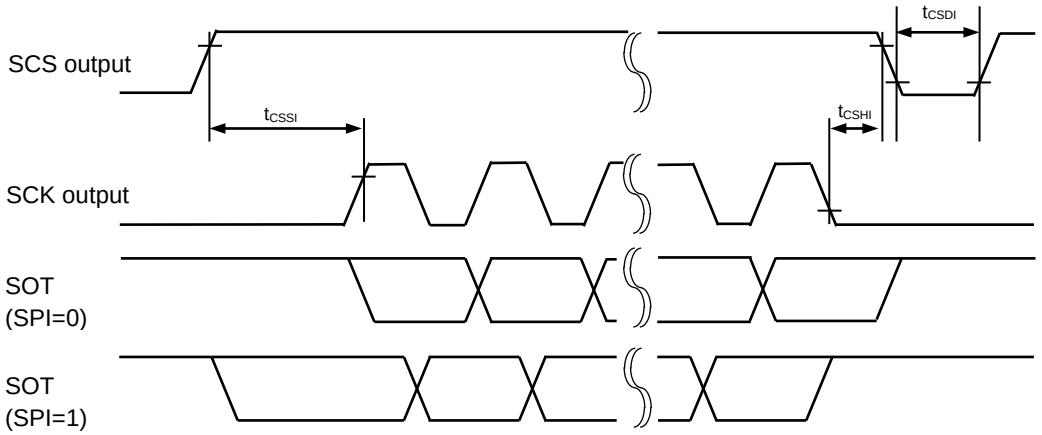
(4-1-8) Bit setting: SMR:MD2 = 0, SMR:MD1 = 1, SMR:MD0 = 0,
When Serial chip select is used: SCSCR:CSEN = 1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV = 1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL = 0
($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↑ setup time | $t_{CSSI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $t_{CSSU}$-50 *1 | $t_{CSSU}$+0 *1 | ns | Internal shift clock mode output pin : $C_L$ = 50 pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSSU}$-50 *1 | $t_{CSSU}$+300 *1 | ns | |
| SCK↓→SCS↓ hold time | $t_{CSHI}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSHD}$-10 *2 | $t_{CSHD}$+50 *2 | ns | |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $t_{CSHD}$-300 *2 | $t_{CSHD}$+50 *2 | ns | |
| SCS deselect time | $t_{CSDI}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $t_{CSDS}$-50 *3 | $t_{CSDS}$+50 *3 | ns | |

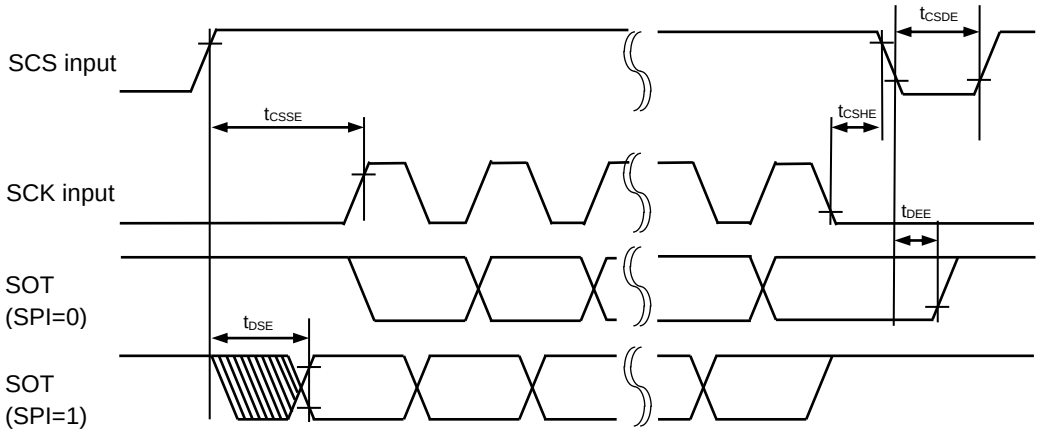
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↑ setup time | $t_{CSSE}$ | SCK1 to SCK11<br>SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$+30 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↓→SCS↓ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | | $3t_{CPP}$+30 | - | ns | |
| SCS↑→SOT delay time | $t_{DSE}$ | SCS1 , SCS2,<br>SCS50~SCS53,<br>SCS60~SCS63,<br>SCS70~SCS73,<br>SCS8~SCS11<br>SOT1 , SOT2,<br>SOT5~SOT11 | | - | 40 | ns | |
| | | SCS3 ,<br>SCS40~SCS43<br>SOT3 ,SOT4 | | - | 300 | ns | |
| SCS↓→SOT delay time | $t_{DEE}$ | SCS1 to SCS3,<br>SCS40 to SCS43,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$ = 50 pF |
| SCK↑→SCS↑ clock switch time | $t_{SCC}$ | SCK1 , SCK2,<br>SCK5 to SCK11<br>SCS1 , SCS2,<br>SCS50 to SCS53,<br>SCS60 to SCS63,<br>SCS70 to SCS73,<br>SCS8 to SCS11 | - | $3t_{CPP}$-10 | $3t_{CPP}$+50 | ns | Internal shift clock mode Round operation output pin: $C_L$ = 50 pF |
| | | SCK3 , SCK4<br>SCS3 ,<br>SCS40 to SCS43 | | $3t_{CPP}$-300 | $3t_{CPP}$+50 | | |

*1: $t_{CSSU}$ = SCSTR:CSSU7-0 × Serial chip select timing operating clock
*2: $t_{CSHD}$ = SCSTR:CSHD7-0 × Serial chip select timing operating clock
*3: $t_{CSDS}$ = SCSTR:CSDS15-0 × Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

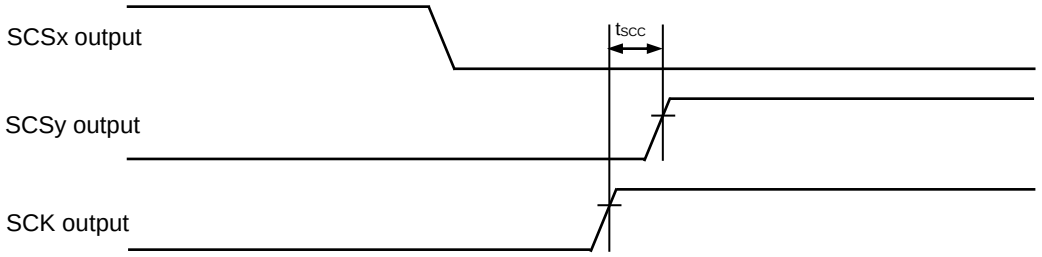
Please see the hardware manual for details of above-mentioned *1,*2, and *3.




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode



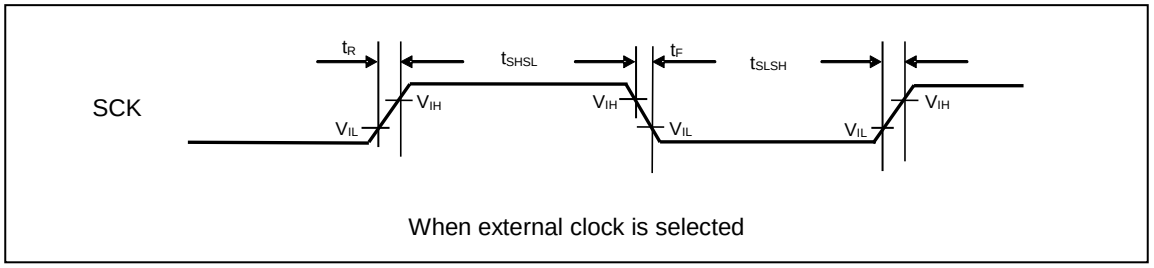

When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Slave mode




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(4-2) UART (Asynchronous serial interface) timing
Bit setting: SMR : MD2 = 0, SMR:MD1 = 0, SMR : MD0 = 0
Bit setting: SMR : MD2 = 0, SMR:MD1 = 0, SMR : MD0 = 1
When external clock is selected (BGR:EXT = 1)
($T_A$: -40 °C to +125°C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0V)

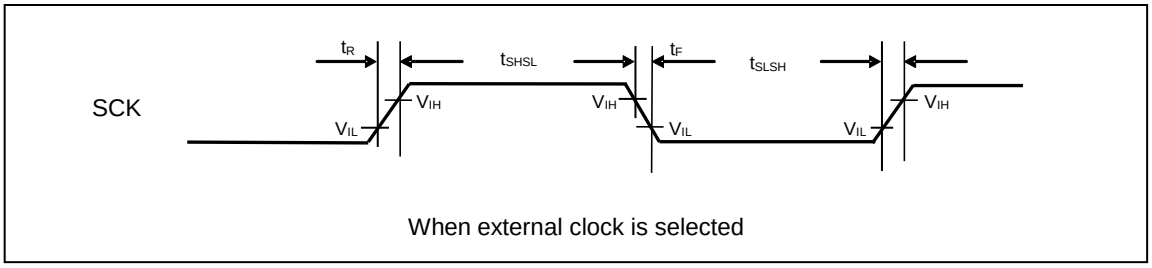
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | output pin: $C_L$ = 50 pF |
| Serial clock "H"pulse width | $t_{SHSL}$ | | | $t_{CPP}$+10 | - | ns | |
| SCK fall time | $t_F$ | | | - | 5 | ns | |
| SCK rise time | $t_R$ | | | - | 5 | ns | |




When external clock is selected

(4-3) LIN Interface (v2.1)( Asynchronous Serial Interface for LIN (v2.1)) timing
Bit setting: SMR : MD2 = 0, SMR:MD1 = 1, SMR : MD0 = 1
($T_A$:-40°C to +125°C, $V_{CC}$ = $AV_{CC}$ = 5.0 V±10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | output pin: $C_L$ = 50 pF |
| Serial clock "H"pulse width | $t_{SHSL}$ | | | $t_{CPP}$+10 | - | ns | |
| SCK fall time | $t_F$ | | | - | 5 | ns | |
| SCK rise time | $t_R$ | | | - | 5 | ns | |




When external clock is selected

(4-4) $I^2C$ timing

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Standard Mode | | Fast Mode*3 | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | | |
| SCL clock frequency | $f_{SCL}$ | SCK3 to SCK11 | $C_L$ = 50 pF<br>R = ($V_P$/$I_{OL}$) *1 | 0 | 100 | 0 | 400 | kHz | |
| Repeat "start" condition hold time<br>SDA ↓ → SCL ↓ | $t_{HDSTA}$ | SOT3 to SOT11, (SDA)<br>SCK3 to SCK11, (SCL) | | 4.0 | – | 0.6 | – | µs | |
| Period of "L" for SCL clock | $t_{LOW}$ | SCK3 to SCK11, (SCL) | | 4.7 | – | 1.3 | – | µs | |
| Period of "H" for SCL clock | $t_{HIGH}$ | SCK3 to SCK11, (SCL) | | 4.0 | – | 0.6 | – | µs | |
| Repeat "start" condition setup time<br>SCL ↑ → SDA ↓ | $t_{SUSTA}$ | SCK3 to SCK11, (SCL) | | 4.7 | – | 0.6 | – | µs | |
| Data hold time<br>SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | SOT3 to SOT11, (SDA)<br>SCK3 to SCK11, (SCL) | | 0 | 3.45*2 | 0 | 0.9*3 | µs | |
| Data setup time<br>SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | SOT3 to SOT11, (SDA)<br>SCK3 to SCK11, (SCL) | | 250 | – | 100 | – | ns | |
| "Stop" condition setup time<br>SCL ↑ → SDA ↑ | $t_{SUSTO}$ | SOT3 to SOT11, (SDA)<br>SCK3 to SCK11, (SCL) | | 4.0 | – | 0.6 | – | µs | |
| Bus-free time between "stop" condition and "start" condition | $t_{BUF}$ | – | | 4.7 | – | 1.3 | – | µs | |
| Noise filter | $t_{SP}$ | – | – | $2t_{CPP}$*4 | – | $2t_{CPP}$*4 | – | ns | |

Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence. In ch.5-ch.8, ch.10, and ch.11, only a standard mode is correspondences.

*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
Vp shows that the power-supply voltage of the pull-up resistor and $I_{OL}$ shows the $V_{OL}$ guarantee current.

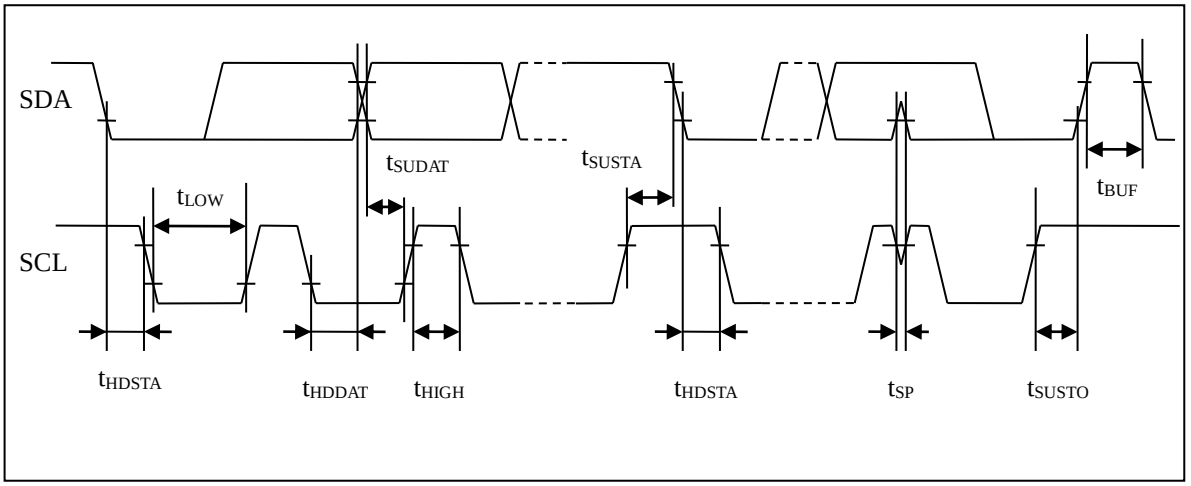
*2: The maximum $t_{HDDAT}$ only has to be met if the device does not extend the "L" width ($t_{LOW}$) of the SCL signal.

*3: A fast mode $I^2C$ bus device can be used on a standard mode $I^2C$ bus system as long as the device satisfies the requirement of

"$t_{SUDAT}$ ≥ 250 ns".

*4: $t_{CPP}$ is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8 MHz or more when use $I^2C$.

・ $I^2C$ timing

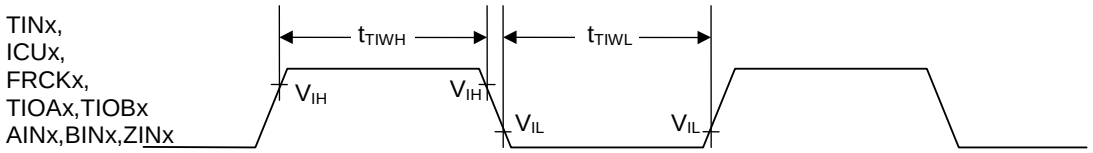


(5) Timer input timing

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | TIN0 to TIN7<br>ICU0 to ICU9<br>FRCK0 to FRCK5<br>TIOA0, TIOA1,<br>TIOB0, TIOB1,<br>AIN0, AIN1,<br>BIN0, BIN1,<br>ZIN0, ZIN1 | – | $4t_{CPP}$ | – | ns | |

• Timer input timing

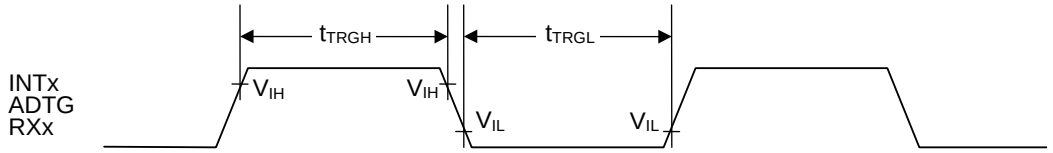



(6) Trigger input timing

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | INT0 to INT15, ADTG, RX0, RX1, RX2 | – | $5t_{CPP}$ | – | ns | |
| | | | | 1 | – | µs | At stop mode |

• Trigger input timing

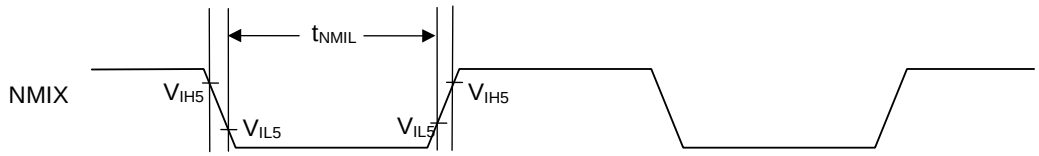


(7) NMI input timing

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{NMIL}$ | NMIX | – | $4t_{CPP}$ | – | ns | |

・ NMIX input timing




(8) Low voltage detection (External low-voltage detection)

($T_A$: -40 °C to +125 °C, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply voltage range | $V_{DP5}$ | VCC | - | 2.7 | - | 5.5 | V | |
| Detection voltage*3 | $V_{DL}$ | | *1 | -8% | LVD5F_SEL [3:0] | +8% | V | LVD5F_SEL[3:0] are programmable. Refer to the hardware manual. |
| Hysteresis width | $V_{HYS}$ | | - | - | 0.1 | - | V | When power-supply voltage rises |
| Low voltage detection time | Td | - | | - | - | 30 | µs | |
| Power supply voltage regulation | - | VCC | - | -2 | - | 2 | V/ms | *2 |

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage ($V_{DL}$).

*3: The initial detection voltage of the external low voltage detection is 2.8 V ± 8 % (2.576 V to 3.024 V).
This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7 V).
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(9) Low voltage detection (Internal low-voltage detection)
($T_A$: -40 °C to +125 °C, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply voltage range | $V_{RDP5}$ | - | - | 0.6 | - | 1.4 | V | |
| Detection voltage*2 | $V_{RDL}$ | | *1 | 0.8 | 0.9 | 1.0 | V | When power-supply voltage falls |
| Hysteresis width | $V_{RHYS}$ | | - | - | 0.1 | - | V | When power-supply voltage rises |
| Low voltage detection time | - | - | | - | - | 30 | µs | |

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.
*2: The detection voltage of the internal low voltage detection is 0.9 V ± 0.1 V.
This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing
($T_A$: -40 °C to +105 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)
(external load capacitance 50 pF)

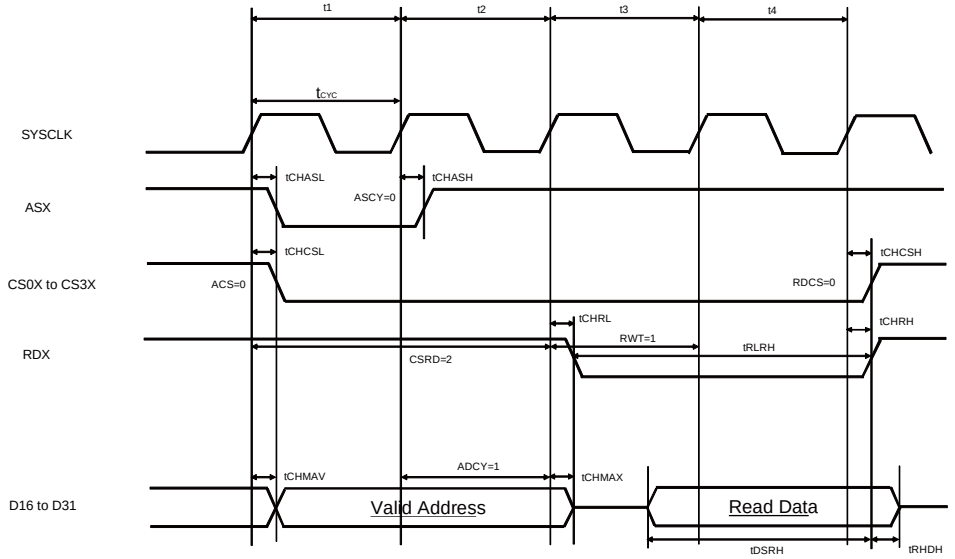
| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | SYSCLK | 25 | - | ns | $V_{CC}$ = 5.0 V ± 10 %*1 |
| | | | 31.25 | | | $V_{CC}$ = 3.3 V ± 0.3 V |
| ASX delay time | $t_{CHASL}$, $t_{CHASH}$ | SYSCLK ASX | 0.5 | 18 | ns | |
| CS0X to CS3X delay time | $t_{CHCSL}$, $t_{CHCSH}$ | SYSCLK CS0X to CS3X | 0.5 | 18 | ns | |
| A00 to A21 delay time | $t_{CHAV}$, $t_{CHAX}$ | SYSCLK A00 to A21 | 0.5 | 18 | ns | |
| RDX delay time | $t_{CHRL}$, $t_{CHRH}$ | SYSCLK RDX | 0.5 | 18 | ns | |
| RDX minimum pulse | $t_{RLRH}$ | RDX | $t_{CYC}$× 2 - 20 | - | ns | RWT = 1, set RWT to 1 or more.*2 |
| Data setup → RDX↑time | $t_{DSRH}$ | RDX D16 to D31 | 18+$t_{CYC}$ | - | ns | Same as above |
| RDX↑→ data hold | $t_{RHDH}$ | | 0 | - | ns | |

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| WRnX delay time | $t_{CHWL}$, $t_{CHWH}$ | SYSCLK WR0X, WR1X | 0.5 | 18 | ns | |
| WRnX minimum pulse | $t_{WLWH}$ | WR0X, WR1X | $t_{CYC}$ - 10 | - | ns | WWT = 0 *2 |
| SYSCLK↑→ data output time | $t_{CHDV}$ | SYSCLK D16 to D31 | 0.5 | 18 | ns | |
| SYSCLK↑→ data hold time | $t_{CHDX}$ | | - | 18 | ns | Set WRCS to 1 or more. |
| SYSCLK↑→ address output time | $t_{CHMAV}$ | SYSCLK D16 to D31 | 0.5 | 18 | ns | |
| SYSCLK↑→ address hold time | $t_{CHMAX}$ | | - | 18 | ns | In multiplex mode, set as follows:<br>□ Set CSWR and CSRD to 2 or more.<br>□ ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention.<br>ADCY +1 ≤ ACS + CSRD<br>ADCY +1 ≤ ACS + CSWR<br>ASCY + 1 ≤ ACS + CSRD<br>ASCY + 1 ≤ ACS + CSWR<br>See Hardware Manual for details. |

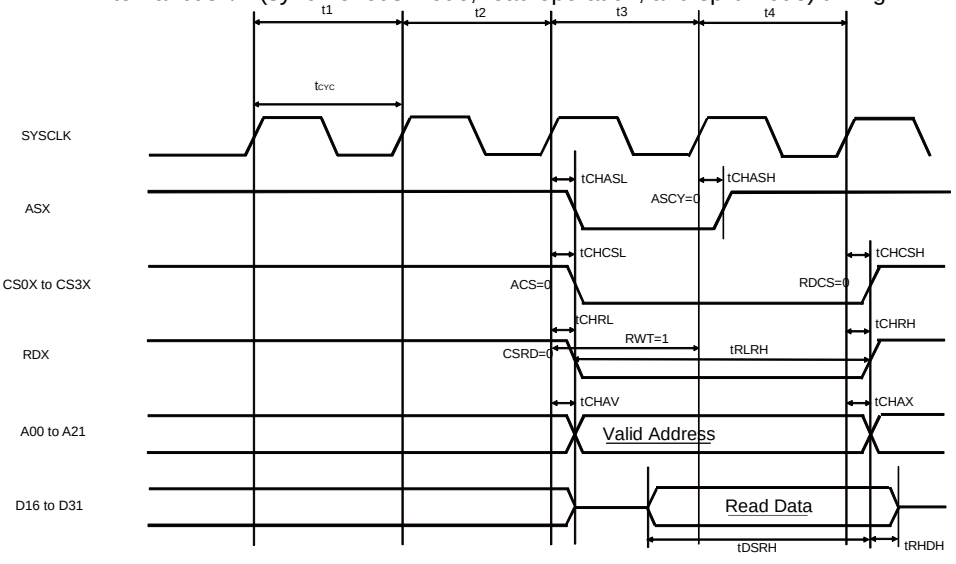
*1: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{CYC}$ × the number of expanded cycles) to the rated value.

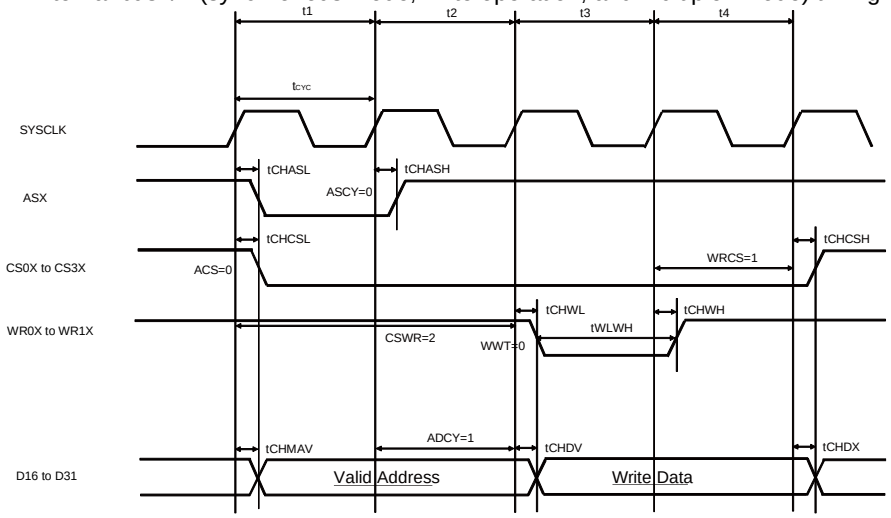
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



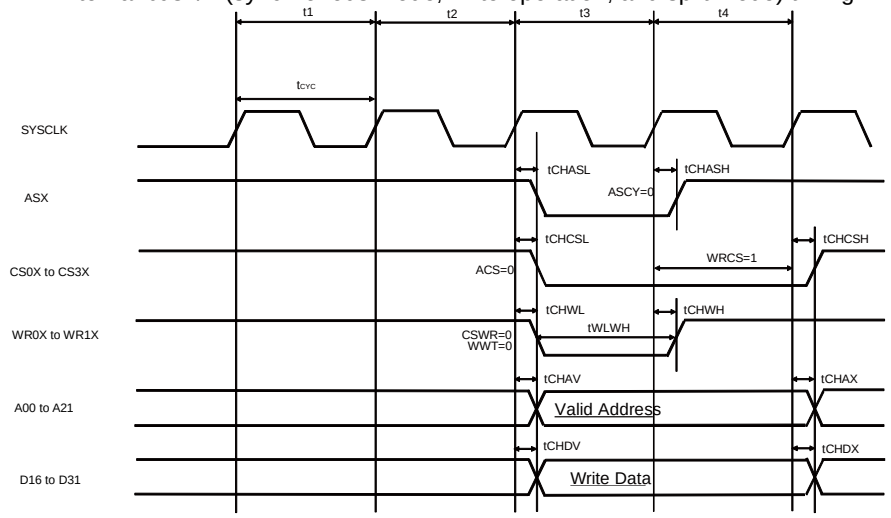

External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing




External bus I/F (synchronous mode, write operation, and split mode) timing

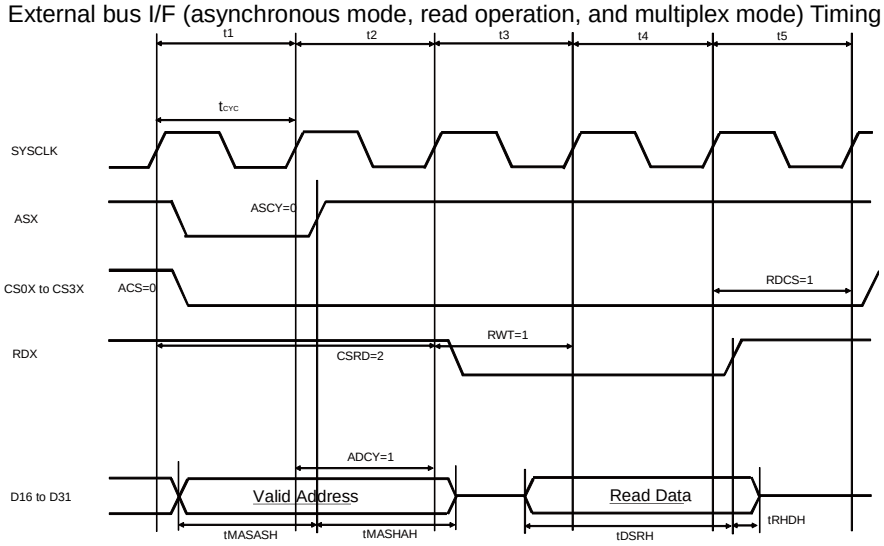


(11) External bus I/F (asynchronous mode) timing
($T_A$: -40 °C to +105 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)
(external load capacitance 50pF)

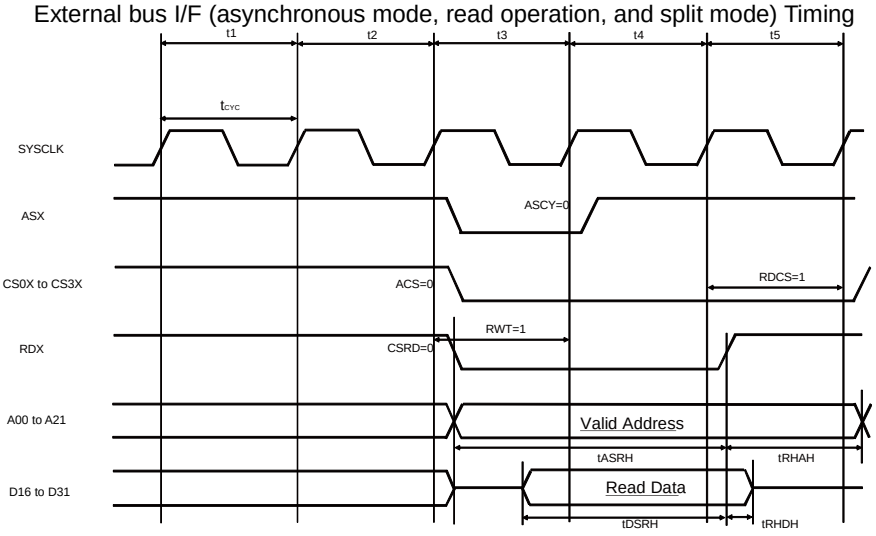
| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | SYSCLK | 25 | - | ns | $V_{CC}$ = 5.0 V ± 10 %*1 |
| | | | 31.25 | | | $V_{CC}$ = 3.3 V ± 0.3 V |
| Address setup → RDX↑time | $t_{ASRH}$ | RDX A00 to A21 | 2×$t_{CYC}$ - 12 | 2×$t_{CYC}$ + 12 | ns | RWT = 1, set RWT to 1 or more. *2 |
| RDX↑→ Address hold | $t_{RHAH}$ | | $t_{CYC}$ - 12 | $t_{CYC}$ + 12 | ns | Set RDCS to 1 or more. |
| Data setup→ RDX↑time | $t_{DSRH}$ | RDX D16 to D31 | 18 + $t_{CYC}$ | - | ns | RWT = 1, set RWT to 1 or more. |
| RDX↑→ Data hold | $t_{RHDH}$ | | 0 | - | ns | |
| Address setup→ WRnX↑time | $t_{ASWH}$ | WR0X to WR1X A00 to A21 | $t_{CYC}$ - 12 | $t_{CYC}$ + 12 | ns | WWT = 0 *2 |
| WRnX↑→ Address hold | $t_{WHAH}$ | | $t_{CYC}$ - 12 | $t_{CYC}$ + 12 | ns | Set WRCS to 1 or more. |
| Data setup→ WRnX↑time | $t_{DSWH}$ | WR0X to WR1X D16 to D31 | $t_{CYC}$ - 16 | $t_{CYC}$ + 16 | ns | WWT = 0 *2 |
| WRnX↑→ Data hold | $t_{WHDH}$ | | $t_{CYC}$ - 16 | $t_{CYC}$ + 16 | ns | Set WRCS to 1 or more. |
| Address setup → ASX↑time | $t_{MASASH}$ | ASX D16 to D31 | $t_{CYC}$-16 | $t_{CYC}$+ 16 | ns | ASCY = 0 |
| ASX↑→Address hold | $t_{MASHAH}$ | | $t_{CYC}$-16 | $t_{CYC}$ + 16 | ns | In multiplex mode, set as follows:<br>□ Set CSWR and CSRD to 2 or more.<br>□ ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention.<br>ADCY +1 ≤ ACS + CSRD<br>ADCY +1 ≤ ACS + CSWR<br>ASCY + 1 ≤ ACS + CSRD<br>ASCY + 1 ≤ ACS + CSWR<br>See Hardware Manual for details. |

*1: Please use it with external load capacity 12 pF or less for VCC = 3.3 V ± 0.3 V (40 MHz operation).
*2: If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{CYC}$ × the number of expanded cycles) to the rated value.

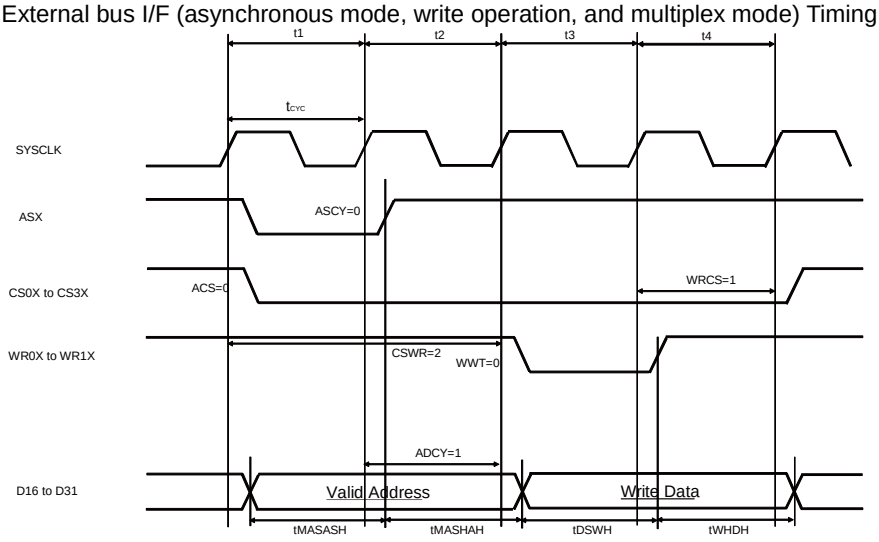
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



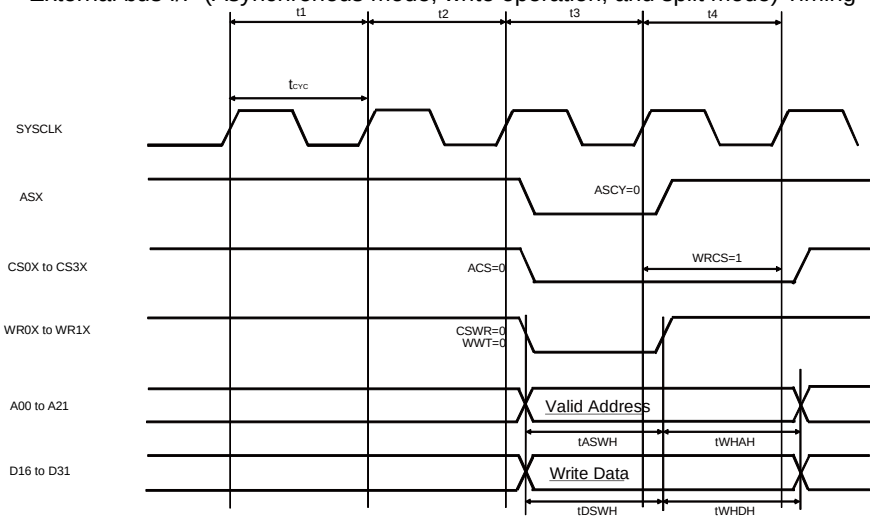

External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing




External bus I/F (Asynchronous mode, write operation, and split mode) Timing

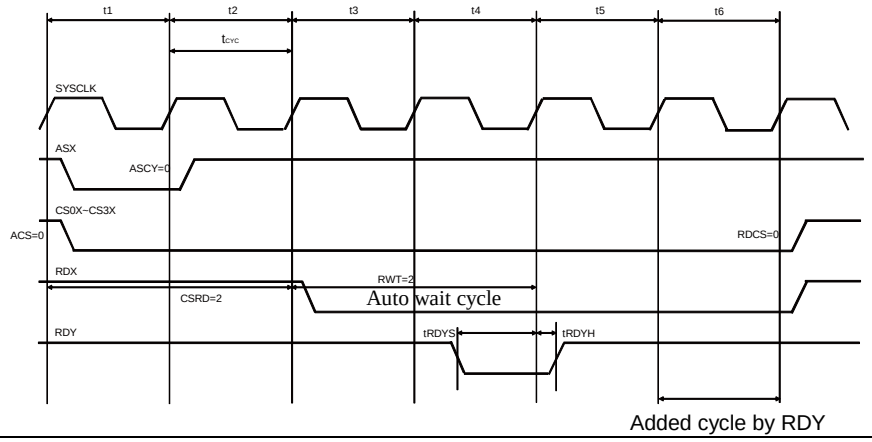


(12) External bus I/F (ready) Timing

($T_A$: -40 °C to +105 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)
(external load capacitance 50 pF)

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | SYSCLK | 50 | - | ns | If using RDY, set SYSCLK to 20 MHz or less. |
| RDY setup time → SYSCLK↑ | $t_{RDYS}$ | SYSCLK, RDY | 28 | - | ns | |
| SYSCLK↑→ RDY hold time | $t_{RDYH}$ | SYSCLK, RDY | 0 | - | ns | |

External bus I/F (ready) Timing



**A/D Converter**

(1) 12-bit A/D Converter Electrical Characteristics

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Total error | - | - | - | - | ±12 | LSB | |
| Linearity error | - | - | - | - | ± 4.0 | LSB | |
| Differential linearity error | - | - | - | - | ± 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN47 | AVRL-11.5LSB | - | AVRL+12.5LSB | V | 1LSB = ($V_{FST}$-$V_{OT}$)/4094 |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN47 | AVRH-13.5LSB | - | AVRH+10.5LSB | V | |
| Sampling time | $t_{SMP}$ | - | 0.7 | - | - | µs | *1 |
| Compare time | $t_{CMP}$ | - | 0.7 | - | - | µs | *1 |
| A/D conversion time | $t_{CNV}$ | - | 1.4 | - | - | µs | *1 |
| Analog port input current | $I_{AIN}$ | AN0 to AN47 | -1.0 | - | +1.0 | µA | $V_{AVSS} \le V_{AIN} \le V_{AVCC}$ |
| Analog input voltage | $V_{AIN}$ | AN0 to AN47 | AVRL | - | AVRH | V | |
| Reference voltage | AVRH | AVRH | 3.0 | - | 5.5 | V | |
| | AVRL | AVSS/AVRL | - | 0.0 | - | V | |
| Power supply current | $I_A$ | AVCC*3 | - | 0.47 | 0.63 | mA | Per unit $T_A$: +105 °C |
| | | | - | 0.47 | 0.7 | mA | Per unit $T_A$: +125 °C |
| | $I_{AH}$ | | - | - | 2.5 | µA | *2 |
| | $I_R$ | AVRH | - | 1 | 1.96 | mA | Per unit |
| | $I_{RH}$ | | - | - | 1.6 | µA | *2 |
| Variation between channels | - | AN0 to AN47 | - | - | 4 | LSB | |

*1: Time for each channel.

*2: Power supply current ($V_{CC}$ = $AV_{CC}$ = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

*3: The power supply current described only current value on A/D converter.
The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.

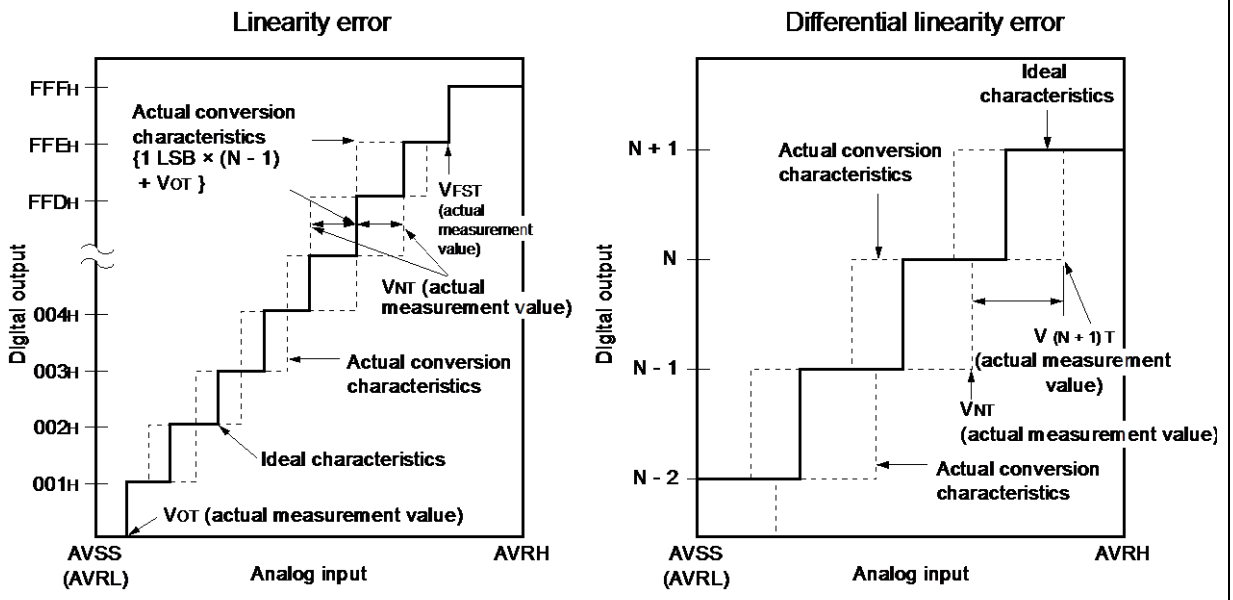
(Note) Please use the clock of 0.5 MHz-20 MHz for the output clock of A/D converter to guarantee accuracy.

(2) Definition of A/D Converter Terms

Resolution : Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"← →"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"← →"1111 1111 1111").

Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by LSB.




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ LSB} \quad \text{[LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \text{ [V]}$$

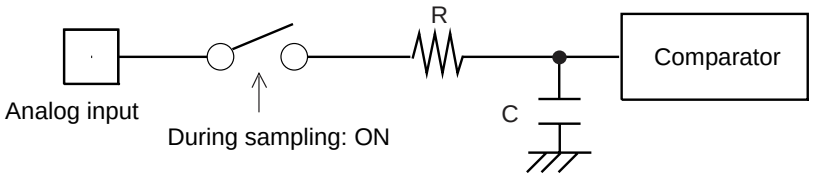
$V_{OT}$ : Voltage at which the digital output changes from "$000_H$" to "$001_H$".
$V_{FST}$ : Voltage at which the digital output changes from "$FFE_H$" to "$FFF_H$".

(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

- Analog input circuit model




| | R | C | |
|---|---|---|---|
| 12-bit A/D | 1.9 kΩ (Max) | 8.30 pF (Max) | (4.5 V ≤ $AV_{CC}$ ≤ 5.5 V) |
| | 4.3 kΩ (Max) | 8.30 pF (Max) | (3.0 V ≤ $AV_{CC}$ ≤ 3.6 V) |

**Note:** Listed values must be considered as reference values.

**Flash Memory**

(1) Electrical Characteristics

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | – | 200 | 800 | ms | 8 Kbytes sector*1, excluding internal preprogramming time |
| | – | 300 | 1100 | ms | 8 Kbytes sector*1, including internal preprogramming time |
| | – | 400 | 2000 | ms | 64 Kbytes sector*1, excluding internal preprogramming time |
| | – | 700 | 3700 | ms | 64 Kbytes sector*1, including internal preprogramming time |
| 8-bit writing time | – | 9 | 288 | µs | Exclusive of overhead time at system level*1 |
| 16-bit writing time | – | 12 | 384 | µs | Exclusive of overhead time at system level*1 |
| ECC writing time | – | 9 | 288 | µs | Exclusive of overhead time at system level*1 |
| Erase cycle*2/ Data retain time | 1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years | – | – | – | Average $T_A$ = +85 °C*3 |

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc) is prohibited.

In the application system where Vcc might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage ($V_{DL}$*), hold Vcc at 2.7 V or more within the duration calculated by the following expression:

$$Td^{*}[\mu s] + (\text{period of PCLK } [\mu s] \times 257) + 50\ [\mu s]$$

*: See “4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) ”

**D/A Converter**

($T_A$: -40 °C to +125 °C, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10 %/$V_{CC}$ = $AV_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

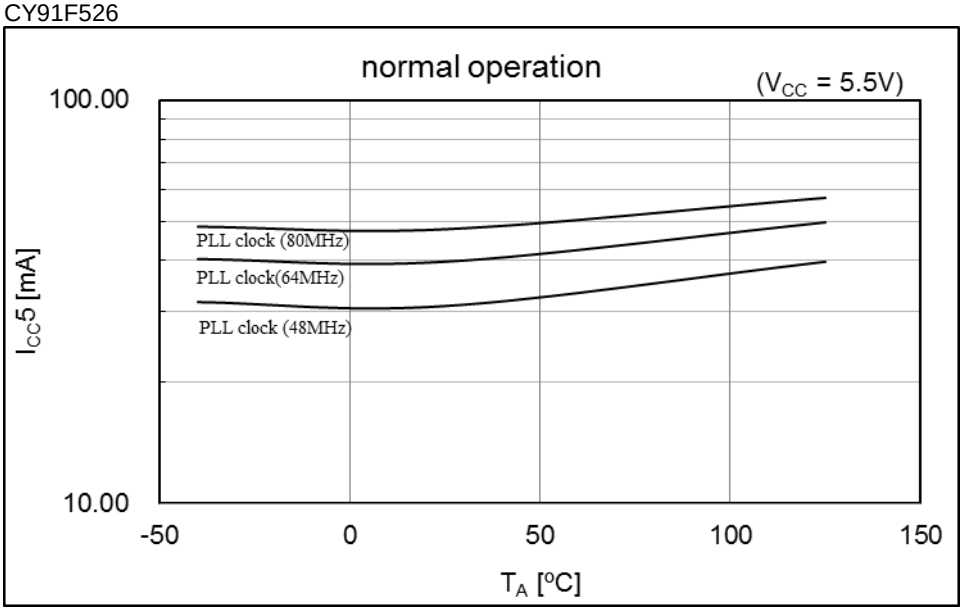
| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Resolution | - | - | – | – | – | 8 | bit | |
| Differential linearity error | - | - | – | – | – | ± 3.0 | LSB | |
| Conversion time | - | - | – | 0.47 | 0.58 | 0.69 | µs | $C_L$ = 20 |
| | | | – | 2.37 | 2.90 | 3.43 | µs | $C_L$ = 100 |
| Output impedance | Ro | DA0, DA1 | – | 3.1 | 3.8 | 4.5 | kΩ | |
| Power supply current *1 | IA | AVCC | – | – | 475 | 580 | µA | Each channel |
| | IAH | AVCC | – | – | – | 7.5 | µA | When powerdown Each channel |

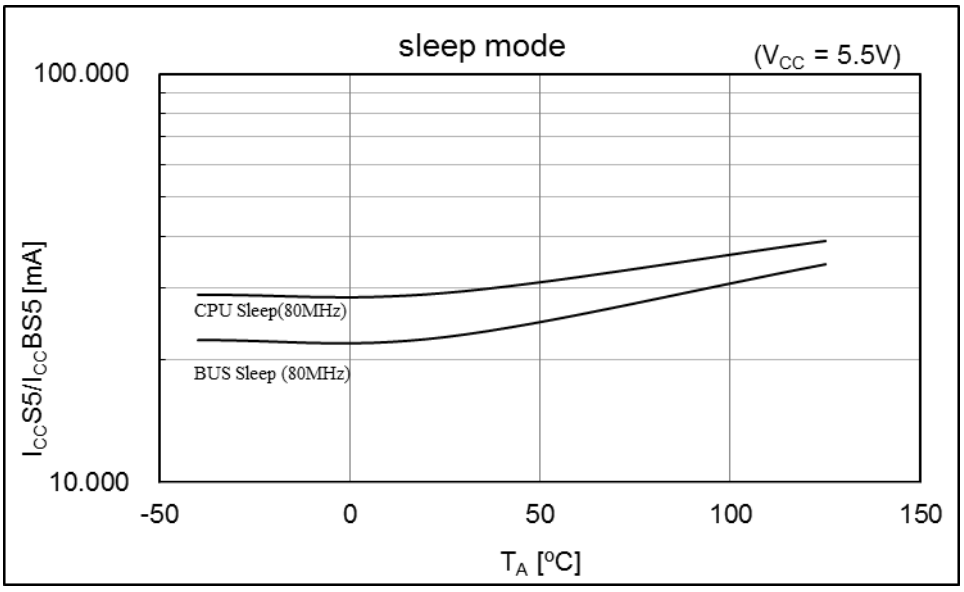
*1: The power supply current described only current value on D/A converter.
The total AVcc current value must be calculated the power supply current for D/A converter and A/D converter.

## 12. Example Characteristics

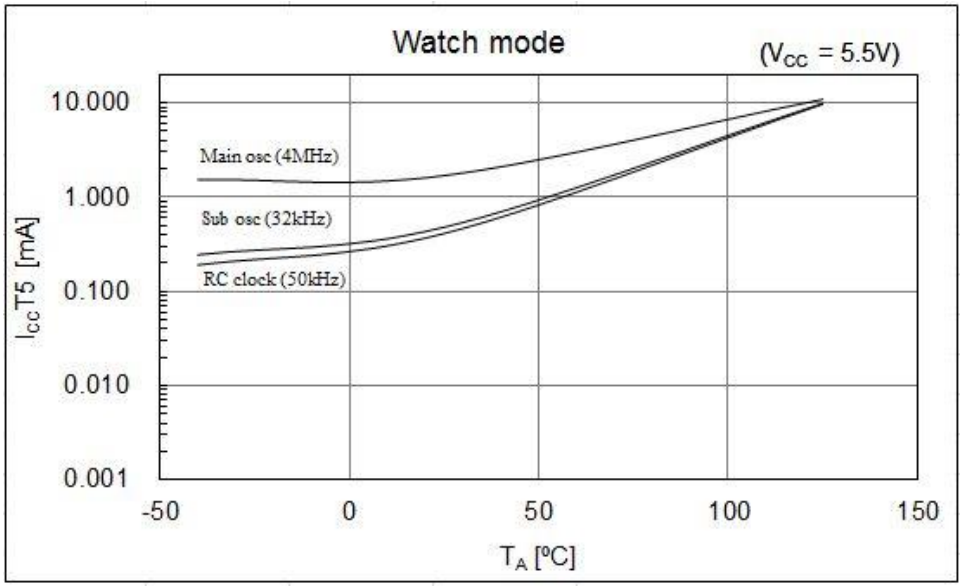
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

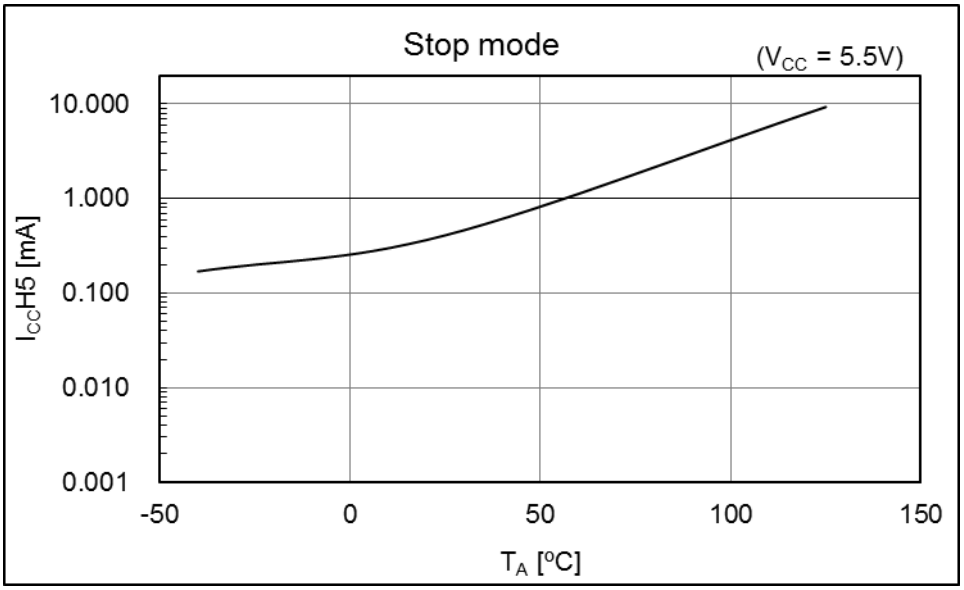
CY91F526



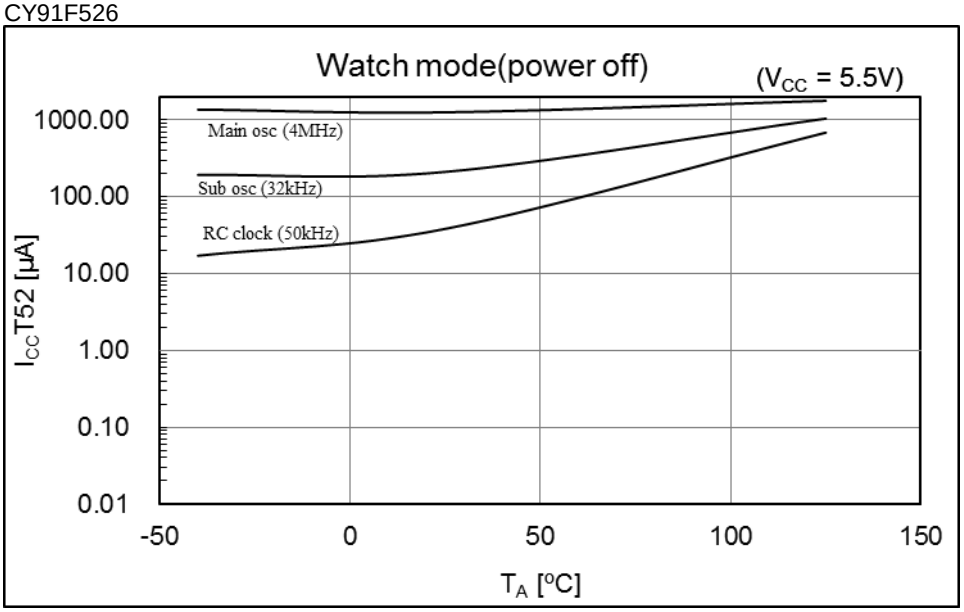



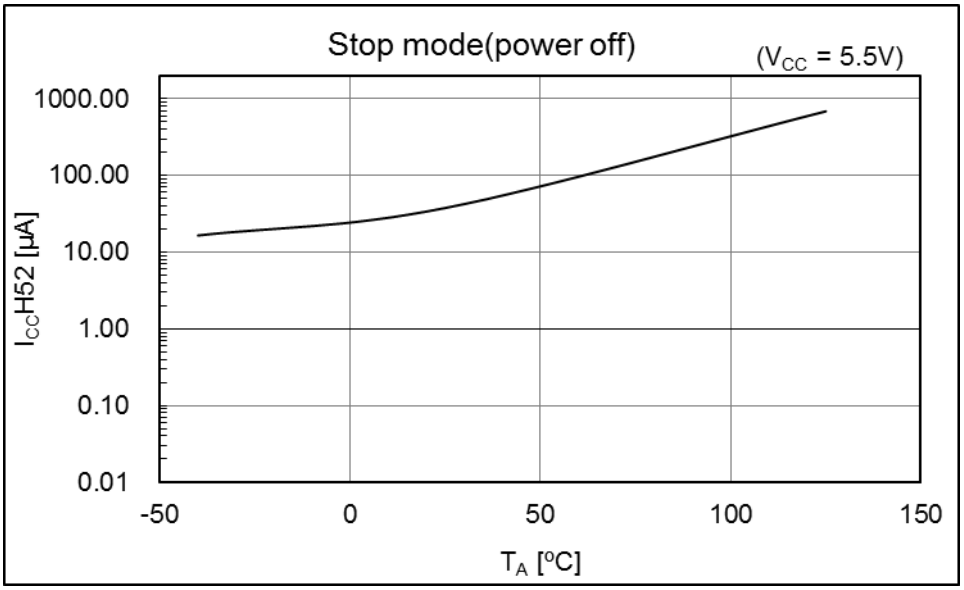
CY91F526


Watch mode
($V_{CC}$ = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}$T5 [mA]
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
-50
0
50
100
150
$T_A$ [°C]


Stop mode
($V_{CC}$ = 5.5V)
10.000
1.000
0.100
0.010
0.001
$I_{CC}$H5 [mA]
-50
0
50
100
150
$T_A$ [°C]

CY91F526


Watch mode(power off)
($V_{CC}$ = 5.5V)
Main osc (4MHz)
Sub osc (32kHz)
RC clock (50kHz)
1000.00
100.00
10.00
1.00
0.10
0.01
$I_{CC}$T52 [µA]
-50
0
50
100
150
$T_A$ [ºC]


Stop mode(power off)
($V_{CC}$ = 5.5V)
1000.00
100.00
10.00
1.00
0.10
0.01
$I_{CC}$H52 [µA]
-50
0
50
100
150
$T_A$ [ºC]

## 13. Ordering Information CY91F52xxxB[*1]

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package[*2] |
|---|---|---|---|---|
| CY91F526LWBPMC | Yes | ON | ON | LQP・176 pin, Plastic |
| CY91F526LYBPMC | | | OFF | |
| CY91F526LJBPMC | | OFF | ON | |
| CY91F526LLBPMC | | | OFF | |
| CY91F525LWBPMC | | ON | ON | |
| CY91F525LYBPMC | | | OFF | |
| CY91F525LJBPMC | | OFF | ON | |
| CY91F525LLBPMC | | | OFF | |
| CY91F524LWBPMC | | ON | ON | |
| CY91F524LYBPMC | | | OFF | |
| CY91F524LJBPMC | | OFF | ON | |
| CY91F524LLBPMC | | | OFF | |
| CY91F523LWBPMC | | ON | ON | |
| CY91F523LYBPMC | | | OFF | |
| CY91F523LJBPMC | | OFF | ON | |
| CY91F523LLBPMC | | | OFF | |
| CY91F522LWBPMC | | ON | ON | |
| CY91F522LYBPMC | | | OFF | |
| CY91F522LJBPMC | | OFF | ON | |
| CY91F522LLBPMC | | | OFF | |
| CY91F526LSBPMC | None | ON | ON | |
| CY91F526LUBPMC | | | OFF | |
| CY91F526LHBPMC | | OFF | ON | |
| CY91F526LKBPMC | | | OFF | |
| CY91F525LSBPMC | | ON | ON | |
| CY91F525LUBPMC | | | OFF | |
| CY91F525LHBPMC | | OFF | ON | |
| CY91F525LKBPMC | | | OFF | |
| CY91F524LSBPMC | | ON | ON | |
| CY91F524LUBPMC | | | OFF | |
| CY91F524LHBPMC | | OFF | ON | |
| CY91F524LKBPMC | | | OFF | |
| CY91F523LSBPMC | | ON | ON | |
| CY91F523LUBPMC | | | OFF | |
| CY91F523LHBPMC | | OFF | ON | |
| CY91F523LKBPMC | | | OFF | |
| CY91F522LSBPMC | | ON | ON | |
| CY91F522LUBPMC | | | OFF | |
| CY91F522LHBPMC | | OFF | ON | |
| CY91F522LKBPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526KWBPMC | Yes | ON | ON | LQS・144 pin, (Lead pitch 0.5 mm) Plastic |
| CY91F526KYBPMC | | | OFF | |
| CY91F526KJBPMC | | OFF | ON | |
| CY91F526KLBPMC | | | OFF | |
| CY91F525KWBPMC | | ON | ON | |
| CY91F525KYBPMC | | | OFF | |
| CY91F525KJBPMC | | OFF | ON | |
| CY91F525KLBPMC | | | OFF | |
| CY91F524KWBPMC | | ON | ON | |
| CY91F524KYBPMC | | | OFF | |
| CY91F524KJBPMC | | OFF | ON | |
| CY91F524KLBPMC | | | OFF | |
| CY91F523KWBPMC | | ON | ON | |
| CY91F523KYBPMC | | | OFF | |
| CY91F523KJBPMC | | OFF | ON | |
| CY91F523KLBPMC | | | OFF | |
| CY91F522KWBPMC | | ON | ON | |
| CY91F522KYBPMC | | | OFF | |
| CY91F522KJBPMC | | OFF | ON | |
| CY91F522KLBPMC | | | OFF | |
| CY91F526KSBPMC | None | ON | ON | |
| CY91F526KUBPMC | | | OFF | |
| CY91F526KHBPMC | | OFF | ON | |
| CY91F526KKBPMC | | | OFF | |
| CY91F525KSBPMC | | ON | ON | |
| CY91F525KUBPMC | | | OFF | |
| CY91F525KHBPMC | | OFF | ON | |
| CY91F525KKBPMC | | | OFF | |
| CY91F524KSBPMC | | ON | ON | |
| CY91F524KUBPMC | | | OFF | |
| CY91F524KHBPMC | | OFF | ON | |
| CY91F524KKBPMC | | | OFF | |
| CY91F523KSBPMC | | ON | ON | |
| CY91F523KUBPMC | | | OFF | |
| CY91F523KHBPMC | | OFF | ON | |
| CY91F523KKBPMC | | | OFF | |
| CY91F522KSBPMC | | ON | ON | |
| CY91F522KUBPMC | | | OFF | |
| CY91F522KHBPMC | | OFF | ON | |
| CY91F522KKBPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526KWBPMC1 | Yes | ON | ON | LQN・144 pin, (Lead pitch 0.4 mm) Plastic |
| CY91F526KYBPMC1 | | | OFF | |
| CY91F526KJBPMC1 | | OFF | ON | |
| CY91F526KLBPMC1 | | | OFF | |
| CY91F525KWBPMC1 | | ON | ON | |
| CY91F525KYBPMC1 | | | OFF | |
| CY91F525KJBPMC1 | | OFF | ON | |
| CY91F525KLBPMC1 | | | OFF | |
| CY91F524KWBPMC1 | | ON | ON | |
| CY91F524KYBPMC1 | | | OFF | |
| CY91F524KJBPMC1 | | OFF | ON | |
| CY91F524KLBPMC1 | | | OFF | |
| CY91F523KWBPMC1 | | ON | ON | |
| CY91F523KYBPMC1 | | | OFF | |
| CY91F523KJBPMC1 | | OFF | ON | |
| CY91F523KLBPMC1 | | | OFF | |
| CY91F522KWBPMC1 | | ON | ON | |
| CY91F522KYBPMC1 | | | OFF | |
| CY91F522KJBPMC1 | | OFF | ON | |
| CY91F522KLBPMC1 | | | OFF | |
| CY91F526KSBPMC1 | None | ON | ON | |
| CY91F526KUBPMC1 | | | OFF | |
| CY91F526KHBPMC1 | | OFF | ON | |
| CY91F526KKBPMC1 | | | OFF | |
| CY91F525KSBPMC1 | | ON | ON | |
| CY91F525KUBPMC1 | | | OFF | |
| CY91F525KHBPMC1 | | OFF | ON | |
| CY91F525KKBPMC1 | | | OFF | |
| CY91F524KSBPMC1 | | ON | ON | |
| CY91F524KUBPMC1 | | | OFF | |
| CY91F524KHBPMC1 | | OFF | ON | |
| CY91F524KKBPMC1 | | | OFF | |
| CY91F523KSBPMC1 | | ON | ON | |
| CY91F523KUBPMC1 | | | OFF | |
| CY91F523KHBPMC1 | | OFF | ON | |
| CY91F523KKBPMC1 | | | OFF | |
| CY91F522KSBPMC1 | | ON | ON | |
| CY91F522KUBPMC1 | | | OFF | |
| CY91F522KHBPMC1 | | OFF | ON | |
| CY91F522KKBPMC1 | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526JWBPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| CY91F526JYBPMC | | | OFF | |
| CY91F526JJBPMC | | OFF | ON | |
| CY91F526JLBPMC | | | OFF | |
| CY91F525JWBPMC | | ON | ON | |
| CY91F525JYBPMC | | | OFF | |
| CY91F525JJBPMC | | OFF | ON | |
| CY91F525JLBPMC | | | OFF | |
| CY91F524JWBPMC | | ON | ON | |
| CY91F524JYBPMC | | | OFF | |
| CY91F524JJBPMC | | OFF | ON | |
| CY91F524JLBPMC | | | OFF | |
| CY91F523JWBPMC | | ON | ON | |
| CY91F523JYBPMC | | | OFF | |
| CY91F523JJBPMC | | OFF | ON | |
| CY91F523JLBPMC | | | OFF | |
| CY91F522JWBPMC | | ON | ON | |
| CY91F522JYBPMC | | | OFF | |
| CY91F522JJBPMC | | OFF | ON | |
| CY91F522JLBPMC | | | OFF | |
| CY91F526JSBPMC | None | ON | ON | |
| CY91F526JUBPMC | | | OFF | |
| CY91F526JHBPMC | | OFF | ON | |
| CY91F526JKBPMC | | | OFF | |
| CY91F525JSBPMC | | ON | ON | |
| CY91F525JUBPMC | | | OFF | |
| CY91F525JHBPMC | | OFF | ON | |
| CY91F525JKBPMC | | | OFF | |
| CY91F524JSBPMC | | ON | ON | |
| CY91F524JUBPMC | | | OFF | |
| CY91F524JHBPMC | | OFF | ON | |
| CY91F524JKBPMC | | | OFF | |
| CY91F523JSBPMC | | ON | ON | |
| CY91F523JUBPMC | | | OFF | |
| CY91F523JHBPMC | | OFF | ON | |
| CY91F523JKBPMC | | | OFF | |
| CY91F522JSBPMC | | ON | ON | |
| CY91F522JUBPMC | | | OFF | |
| CY91F522JHBPMC | | OFF | ON | |
| CY91F522JKBPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526FWBPMC | Yes | ON | ON | LQI・100 pin, Plastic |
| CY91F526FYBPMC | | | OFF | |
| CY91F526FJBPMC | | OFF | ON | |
| CY91F526FLBPMC | | | OFF | |
| CY91F525FWBPMC | | ON | ON | |
| CY91F525FYBPMC | | | OFF | |
| CY91F525FJBPMC | | OFF | ON | |
| CY91F525FLBPMC | | | OFF | |
| CY91F524FWBPMC | | ON | ON | |
| CY91F524FYBPMC | | | OFF | |
| CY91F524FJBPMC | | OFF | ON | |
| CY91F524FLBPMC | | | OFF | |
| CY91F523FWBPMC | | ON | ON | |
| CY91F523FYBPMC | | | OFF | |
| CY91F523FJBPMC | | OFF | ON | |
| CY91F523FLBPMC | | | OFF | |
| CY91F522FWBPMC | | ON | ON | |
| CY91F522FYBPMC | | | OFF | |
| CY91F522FJBPMC | | OFF | ON | |
| CY91F522FLBPMC | | | OFF | |
| CY91F526FSBPMC | None | ON | ON | |
| CY91F526FUBPMC | | | OFF | |
| CY91F526FHBPMC | | OFF | ON | |
| CY91F526FKBPMC | | | OFF | |
| CY91F525FSBPMC | | ON | ON | |
| CY91F525FUBPMC | | | OFF | |
| CY91F525FHBPMC | | OFF | ON | |
| CY91F525FKBPMC | | | OFF | |
| CY91F524FSBPMC | | ON | ON | |
| CY91F524FUBPMC | | | OFF | |
| CY91F524FHBPMC | | OFF | ON | |
| CY91F524FKBPMC | | | OFF | |
| CY91F523FSBPMC | | ON | ON | |
| CY91F523FUBPMC | | | OFF | |
| CY91F523FHBPMC | | OFF | ON | |
| CY91F523FKBPMC | | | OFF | |
| CY91F522FSBPMC | | ON | ON | |
| CY91F522FUBPMC | | | OFF | |
| CY91F522FHBPMC | | OFF | ON | |
| CY91F522FKBPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526DWBPMC | Yes | ON | ON | LQH・80 pin, Plastic |
| CY91F526DYBPMC | | | OFF | |
| CY91F526DJBPMC | | OFF | ON | |
| CY91F526DLBPMC | | | OFF | |
| CY91F525DWBPMC | | ON | ON | |
| CY91F525DYBPMC | | | OFF | |
| CY91F525DJBPMC | | OFF | ON | |
| CY91F525DLBPMC | | | OFF | |
| CY91F524DWBPMC | | ON | ON | |
| CY91F524DYBPMC | | | OFF | |
| CY91F524DJBPMC | | OFF | ON | |
| CY91F524DLBPMC | | | OFF | |
| CY91F523DWBPMC | | ON | ON | |
| CY91F523DYBPMC | | | OFF | |
| CY91F523DJBPMC | | OFF | ON | |
| CY91F523DLBPMC | | | OFF | |
| CY91F522DWBPMC | | ON | ON | |
| CY91F522DYBPMC | | | OFF | |
| CY91F522DJBPMC | | OFF | ON | |
| CY91F522DLBPMC | | | OFF | |
| CY91F526DSBPMC | None | ON | ON | |
| CY91F526DUBPMC | | | OFF | |
| CY91F526DHBPMC | | OFF | ON | |
| CY91F526DKBPMC | | | OFF | |
| CY91F525DSBPMC | | ON | ON | |
| CY91F525DUBPMC | | | OFF | |
| CY91F525DHBPMC | | OFF | ON | |
| CY91F525DKBPMC | | | OFF | |
| CY91F524DSBPMC | | ON | ON | |
| CY91F524DUBPMC | | | OFF | |
| CY91F524DHBPMC | | OFF | ON | |
| CY91F524DKBPMC | | | OFF | |
| CY91F523DSBPMC | | ON | ON | |
| CY91F523DUBPMC | | | OFF | |
| CY91F523DHBPMC | | OFF | ON | |
| CY91F523DKBPMC | | | OFF | |
| CY91F522DSBPMC | | ON | ON | |
| CY91F522DUBPMC | | | OFF | |
| CY91F522DHBPMC | | OFF | ON | |
| CY91F522DKBPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526BWBPMC1 | Yes | ON | ON | LQD・64 pin, Plastic |
| CY91F526BYBPMC1 | | | OFF | |
| CY91F526BJBPMC1 | | OFF | ON | |
| CY91F526BLBPMC1 | | | OFF | |
| CY91F525BWBPMC1 | | ON | ON | |
| CY91F525BYBPMC1 | | | OFF | |
| CY91F525BJBPMC1 | | OFF | ON | |
| CY91F525BLBPMC1 | | | OFF | |
| CY91F524BWBPMC1 | | ON | ON | |
| CY91F524BYBPMC1 | | | OFF | |
| CY91F524BJBPMC1 | | OFF | ON | |
| CY91F524BLBPMC1 | | | OFF | |
| CY91F523BWBPMC1 | | ON | ON | |
| CY91F523BYBPMC1 | | | OFF | |
| CY91F523BJBPMC1 | | OFF | ON | |
| CY91F523BLBPMC1 | | | OFF | |
| CY91F522BWBPMC1 | | ON | ON | |
| CY91F522BYBPMC1 | | | OFF | |
| CY91F522BJBPMC1 | | OFF | ON | |
| CY91F522BLBPMC1 | | | OFF | |
| CY91F526BSBPMC1 | None | ON | ON | |
| CY91F526BUBPMC1 | | | OFF | |
| CY91F526BHBPMC1 | | OFF | ON | |
| CY91F526BKBPMC1 | | | OFF | |
| CY91F525BSBPMC1 | | ON | ON | |
| CY91F525BUBPMC1 | | | OFF | |
| CY91F525BHBPMC1 | | OFF | ON | |
| CY91F525BKBPMC1 | | | OFF | |
| CY91F524BSBPMC1 | | ON | ON | |
| CY91F524BUBPMC1 | | | OFF | |
| CY91F524BHBPMC1 | | OFF | ON | |
| CY91F524BKBPMC1 | | | OFF | |
| CY91F523BSBPMC1 | | ON | ON | |
| CY91F523BUBPMC1 | | | OFF | |
| CY91F523BHBPMC1 | | OFF | ON | |
| CY91F523BKBPMC1 | | | OFF | |
| CY91F522BSBPMC1 | | ON | ON | |
| CY91F522BUBPMC1 | | | OFF | |
| CY91F522BHBPMC1 | | OFF | ON | |
| CY91F522BKBPMC1 | | | OFF | |

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see Package Dimensions.

## 14. Ordering Information CY91F52xxxC[*1]

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package[*2] |
|---|---|---|---|---|
| CY91F526LWCPMC | Yes | ON | ON | LQP・176 pin, Plastic |
| CY91F526LYCPMC | | | OFF | |
| CY91F526LJCPMC | | OFF | ON | |
| CY91F526LLCPMC | | | OFF | |
| CY91F525LWCPMC | | ON | ON | |
| CY91F525LYCPMC | | | OFF | |
| CY91F525LJCPMC | | OFF | ON | |
| CY91F525LLCPMC | | | OFF | |
| CY91F524LWCPMC | | ON | ON | |
| CY91F524LYCPMC | | | OFF | |
| CY91F524LJCPMC | | OFF | ON | |
| CY91F524LLCPMC | | | OFF | |
| CY91F523LWCPMC | | ON | ON | |
| CY91F523LYCPMC | | | OFF | |
| CY91F523LJCPMC | | OFF | ON | |
| CY91F523LLCPMC | | | OFF | |
| CY91F522LWCPMC | | ON | ON | |
| CY91F522LYCPMC | | | OFF | |
| CY91F522LJCPMC | | OFF | ON | |
| CY91F522LLCPMC | | | OFF | |
| CY91F526LSCPMC | None | ON | ON | |
| CY91F526LUCPMC | | | OFF | |
| CY91F526LHCPMC | | OFF | ON | |
| CY91F526LKCPMC | | | OFF | |
| CY91F525LSCPMC | | ON | ON | |
| CY91F525LUCPMC | | | OFF | |
| CY91F525LHCPMC | | OFF | ON | |
| CY91F525LKCPMC | | | OFF | |
| CY91F524LSCPMC | | ON | ON | |
| CY91F524LUCPMC | | | OFF | |
| CY91F524LHCPMC | | OFF | ON | |
| CY91F524LKCPMC | | | OFF | |
| CY91F523LSCPMC | | ON | ON | |
| CY91F523LUCPMC | | | OFF | |
| CY91F523LHCPMC | | OFF | ON | |
| CY91F523LKCPMC | | | OFF | |
| CY91F522LSCPMC | | ON | ON | |
| CY91F522LUCPMC | | | OFF | |
| CY91F522LHCPMC | | OFF | ON | |
| CY91F522LKCPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526KWCPMC | Yes | ON | ON | LQS・144 pin, (Lead pitch 0.5 mm) Plastic |
| CY91F526KYCPMC | | | OFF | |
| CY91F526KJCPMC | | OFF | ON | |
| CY91F526KLCPMC | | | OFF | |
| CY91F525KWCPMC | | ON | ON | |
| CY91F525KYCPMC | | | OFF | |
| CY91F525KJCPMC | | OFF | ON | |
| CY91F525KLCPMC | | | OFF | |
| CY91F524KWCPMC | | ON | ON | |
| CY91F524KYCPMC | | | OFF | |
| CY91F524KJCPMC | | OFF | ON | |
| CY91F524KLCPMC | | | OFF | |
| CY91F523KWCPMC | | ON | ON | |
| CY91F523KYCPMC | | | OFF | |
| CY91F523KJCPMC | | OFF | ON | |
| CY91F523KLCPMC | | | OFF | |
| CY91F522KWCPMC | | ON | ON | |
| CY91F522KYCPMC | | | OFF | |
| CY91F522KJCPMC | | OFF | ON | |
| CY91F522KLCPMC | | | OFF | |
| CY91F526KSCPMC | None | ON | ON | |
| CY91F526KUCPMC | | | OFF | |
| CY91F526KHCPMC | | OFF | ON | |
| CY91F526KKCPMC | | | OFF | |
| CY91F525KSCPMC | | ON | ON | |
| CY91F525KUCPMC | | | OFF | |
| CY91F525KHCPMC | | OFF | ON | |
| CY91F525KKCPMC | | | OFF | |
| CY91F524KSCPMC | | ON | ON | |
| CY91F524KUCPMC | | | OFF | |
| CY91F524KHCPMC | | OFF | ON | |
| CY91F524KKCPMC | | | OFF | |
| CY91F523KSCPMC | | ON | ON | |
| CY91F523KUCPMC | | | OFF | |
| CY91F523KHCPMC | | OFF | ON | |
| CY91F523KKCPMC | | | OFF | |
| CY91F522KSCPMC | | ON | ON | |
| CY91F522KUCPMC | | | OFF | |
| CY91F522KHCPMC | | OFF | ON | |
| CY91F522KKCPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526KWCPMC1 | Yes | ON | ON | LQN・144 pin, (Lead pitch 0.4 mm) Plastic |
| CY91F526KYCPMC1 | | | OFF | |
| CY91F526KJCPMC1 | | OFF | ON | |
| CY91F526KLCPMC1 | | | OFF | |
| CY91F525KWCPMC1 | | ON | ON | |
| CY91F525KYCPMC1 | | | OFF | |
| CY91F525KJCPMC1 | | OFF | ON | |
| CY91F525KLCPMC1 | | | OFF | |
| CY91F524KWCPMC1 | | ON | ON | |
| CY91F524KYCPMC1 | | | OFF | |
| CY91F524KJCPMC1 | | OFF | ON | |
| CY91F524KLCPMC1 | | | OFF | |
| CY91F523KWCPMC1 | | ON | ON | |
| CY91F523KYCPMC1 | | | OFF | |
| CY91F523KJCPMC1 | | OFF | ON | |
| CY91F523KLCPMC1 | | | OFF | |
| CY91F522KWCPMC1 | | ON | ON | |
| CY91F522KYCPMC1 | | | OFF | |
| CY91F522KJCPMC1 | | OFF | ON | |
| CY91F522KLCPMC1 | | | OFF | |
| CY91F526KSCPMC1 | None | ON | ON | |
| CY91F526KUCPMC1 | | | OFF | |
| CY91F526KHCPMC1 | | OFF | ON | |
| CY91F526KKCPMC1 | | | OFF | |
| CY91F525KSCPMC1 | | ON | ON | |
| CY91F525KUCPMC1 | | | OFF | |
| CY91F525KHCPMC1 | | OFF | ON | |
| CY91F525KKCPMC1 | | | OFF | |
| CY91F524KSCPMC1 | | ON | ON | |
| CY91F524KUCPMC1 | | | OFF | |
| CY91F524KHCPMC1 | | OFF | ON | |
| CY91F524KKCPMC1 | | | OFF | |
| CY91F523KSCPMC1 | | ON | ON | |
| CY91F523KUCPMC1 | | | OFF | |
| CY91F523KHCPMC1 | | OFF | ON | |
| CY91F523KKCPMC1 | | | OFF | |
| CY91F522KSCPMC1 | | ON | ON | |
| CY91F522KUCPMC1 | | | OFF | |
| CY91F522KHCPMC1 | | OFF | ON | |
| CY91F522KKCPMC1 | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526JWCPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| CY91F526JYCPMC | | | OFF | |
| CY91F526JJCPMC | | OFF | ON | |
| CY91F526JLCPMC | | | OFF | |
| CY91F525JWCPMC | | ON | ON | |
| CY91F525JYCPMC | | | OFF | |
| CY91F525JJCPMC | | OFF | ON | |
| CY91F525JLCPMC | | | OFF | |
| CY91F524JWCPMC | | ON | ON | |
| CY91F524JYCPMC | | | OFF | |
| CY91F524JJCPMC | | OFF | ON | |
| CY91F524JLCPMC | | | OFF | |
| CY91F523JWCPMC | | ON | ON | |
| CY91F523JYCPMC | | | OFF | |
| CY91F523JJCPMC | | OFF | ON | |
| CY91F523JLCPMC | | | OFF | |
| CY91F522JWCPMC | | ON | ON | |
| CY91F522JYCPMC | | | OFF | |
| CY91F522JJCPMC | | OFF | ON | |
| CY91F522JLCPMC | | | OFF | |
| CY91F526JSCPMC | None | ON | ON | |
| CY91F526JUCPMC | | | OFF | |
| CY91F526JHCPMC | | OFF | ON | |
| CY91F526JKCPMC | | | OFF | |
| CY91F525JSCPMC | | ON | ON | |
| CY91F525JUCPMC | | | OFF | |
| CY91F525JHCPMC | | OFF | ON | |
| CY91F525JKCPMC | | | OFF | |
| CY91F524JSCPMC | | ON | ON | |
| CY91F524JUCPMC | | | OFF | |
| CY91F524JHCPMC | | OFF | ON | |
| CY91F524JKCPMC | | | OFF | |
| CY91F523JSCPMC | | ON | ON | |
| CY91F523JUCPMC | | | OFF | |
| CY91F523JHCPMC | | OFF | ON | |
| CY91F523JKCPMC | | | OFF | |
| CY91F522JSCPMC | | ON | ON | |
| CY91F522JUCPMC | | | OFF | |
| CY91F522JHCPMC | | OFF | ON | |
| CY91F522JKCPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526FWCPMC | Yes | ON | ON | LQI・100 pin, Plastic |
| CY91F526FYCPMC | | | OFF | |
| CY91F526FJCPMC | | OFF | ON | |
| CY91F526FLCPMC | | | OFF | |
| CY91F525FWCPMC | | ON | ON | |
| CY91F525FYCPMC | | | OFF | |
| CY91F525FJCPMC | | OFF | ON | |
| CY91F525FLCPMC | | | OFF | |
| CY91F524FWCPMC | | ON | ON | |
| CY91F524FYCPMC | | | OFF | |
| CY91F524FJCPMC | | OFF | ON | |
| CY91F524FLCPMC | | | OFF | |
| CY91F523FWCPMC | | ON | ON | |
| CY91F523FYCPMC | | | OFF | |
| CY91F523FJCPMC | | OFF | ON | |
| CY91F523FLCPMC | | | OFF | |
| CY91F522FWCPMC | | ON | ON | |
| CY91F522FYCPMC | | | OFF | |
| CY91F522FJCPMC | | OFF | ON | |
| CY91F522FLCPMC | | | OFF | |
| CY91F526FSCPMC | None | ON | ON | |
| CY91F526FUCPMC | | | OFF | |
| CY91F526FHCPMC | | OFF | ON | |
| CY91F526FKCPMC | | | OFF | |
| CY91F525FSCPMC | | ON | ON | |
| CY91F525FUCPMC | | | OFF | |
| CY91F525FHCPMC | | OFF | ON | |
| CY91F525FKCPMC | | | OFF | |
| CY91F524FSCPMC | | ON | ON | |
| CY91F524FUCPMC | | | OFF | |
| CY91F524FHCPMC | | OFF | ON | |
| CY91F524FKCPMC | | | OFF | |
| CY91F523FSCPMC | | ON | ON | |
| CY91F523FUCPMC | | | OFF | |
| CY91F523FHCPMC | | OFF | ON | |
| CY91F523FKCPMC | | | OFF | |
| CY91F522FSCPMC | | ON | ON | |
| CY91F522FUCPMC | | | OFF | |
| CY91F522FHCPMC | | OFF | ON | |
| CY91F522FKCPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526DWCPMC | Yes | ON | ON | LQH・80 pin, Plastic |
| CY91F526DYCPMC | | | OFF | |
| CY91F526DJCPMC | | OFF | ON | |
| CY91F526DLCPMC | | | OFF | |
| CY91F525DWCPMC | | ON | ON | |
| CY91F525DYCPMC | | | OFF | |
| CY91F525DJCPMC | | OFF | ON | |
| CY91F525DLCPMC | | | OFF | |
| CY91F524DWCPMC | | ON | ON | |
| CY91F524DYCPMC | | | OFF | |
| CY91F524DJCPMC | | OFF | ON | |
| CY91F524DLCPMC | | | OFF | |
| CY91F523DWCPMC | | ON | ON | |
| CY91F523DYCPMC | | | OFF | |
| CY91F523DJCPMC | | OFF | ON | |
| CY91F523DLCPMC | | | OFF | |
| CY91F522DWCPMC | | ON | ON | |
| CY91F522DYCPMC | | | OFF | |
| CY91F522DJCPMC | | OFF | ON | |
| CY91F522DLCPMC | | | OFF | |
| CY91F526DSCPMC | None | ON | ON | |
| CY91F526DUCPMC | | | OFF | |
| CY91F526DHCPMC | | OFF | ON | |
| CY91F526DKCPMC | | | OFF | |
| CY91F525DSCPMC | | ON | ON | |
| CY91F525DUCPMC | | | OFF | |
| CY91F525DHCPMC | | OFF | ON | |
| CY91F525DKCPMC | | | OFF | |
| CY91F524DSCPMC | | ON | ON | |
| CY91F524DUCPMC | | | OFF | |
| CY91F524DHCPMC | | OFF | ON | |
| CY91F524DKCPMC | | | OFF | |
| CY91F523DSCPMC | | ON | ON | |
| CY91F523DUCPMC | | | OFF | |
| CY91F523DHCPMC | | OFF | ON | |
| CY91F523DKCPMC | | | OFF | |
| CY91F522DSCPMC | | ON | ON | |
| CY91F522DUCPMC | | | OFF | |
| CY91F522DHCPMC | | OFF | ON | |
| CY91F522DKCPMC | | | OFF | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package*2 |
|---|---|---|---|---|
| CY91F526BWCPMC1 | Yes | ON | ON | LQD・64 pin, Plastic |
| CY91F526BYCPMC1 | | | OFF | |
| CY91F526BJCPMC1 | | OFF | ON | |
| CY91F526BLCPMC1 | | | OFF | |
| CY91F525BWCPMC1 | | ON | ON | |
| CY91F525BYCPMC1 | | | OFF | |
| CY91F525BJCPMC1 | | OFF | ON | |
| CY91F525BLCPMC1 | | | OFF | |
| CY91F524BWCPMC1 | | ON | ON | |
| CY91F524BYCPMC1 | | | OFF | |
| CY91F524BJCPMC1 | | OFF | ON | |
| CY91F524BLCPMC1 | | | OFF | |
| CY91F523BWCPMC1 | | ON | ON | |
| CY91F523BYCPMC1 | | | OFF | |
| CY91F523BJCPMC1 | | OFF | ON | |
| CY91F523BLCPMC1 | | | OFF | |
| CY91F522BWCPMC1 | | ON | ON | |
| CY91F522BYCPMC1 | | | OFF | |
| CY91F522BJCPMC1 | | OFF | ON | |
| CY91F522BLCPMC1 | | | OFF | |
| CY91F526BSCPMC1 | None | ON | ON | |
| CY91F526BUCPMC1 | | | OFF | |
| CY91F526BHCPMC1 | | OFF | ON | |
| CY91F526BKCPMC1 | | | OFF | |
| CY91F525BSCPMC1 | | ON | ON | |
| CY91F525BUCPMC1 | | | OFF | |
| CY91F525BHCPMC1 | | OFF | ON | |
| CY91F525BKCPMC1 | | | OFF | |
| CY91F524BSCPMC1 | | ON | ON | |
| CY91F524BUCPMC1 | | | OFF | |
| CY91F524BHCPMC1 | | OFF | ON | |
| CY91F524BKCPMC1 | | | OFF | |
| CY91F523BSCPMC1 | | ON | ON | |
| CY91F523BUCPMC1 | | | OFF | |
| CY91F523BHCPMC1 | | OFF | ON | |
| CY91F523BKCPMC1 | | | OFF | |
| CY91F522BSCPMC1 | | ON | ON | |
| CY91F522BUCPMC1 | | | OFF | |
| CY91F522BHCPMC1 | | OFF | ON | |
| CY91F522BKCPMC1 | | | OFF | |

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
*2: For details of the package, see Package Dimensions.

## 15. Ordering Information CY91F52xxxD

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526LWDPMC | Yes | ON | ON | LQP・176 pin, Plastic |
| CY91F526LJDPMC | | OFF | ON | |
| CY91F525LWDPMC | | ON | ON | |
| CY91F525LJDPMC | | OFF | ON | |
| CY91F524LWDPMC | | ON | ON | |
| CY91F524LJDPMC | | OFF | ON | |
| CY91F523LWDPMC | | ON | ON | |
| CY91F523LJDPMC | | OFF | ON | |
| CY91F522LWDPMC | | ON | ON | |
| CY91F522LJDPMC | | OFF | ON | |
| CY91F526LSDPMC | None | ON | ON | |
| CY91F526LHDPMC | | OFF | ON | |
| CY91F525LSDPMC | | ON | ON | |
| CY91F525LHDPMC | | OFF | ON | |
| CY91F524LSDPMC | | ON | ON | |
| CY91F524LHDPMC | | OFF | ON | |
| CY91F523LSDPMC | | ON | ON | |
| CY91F523LHDPMC | | OFF | ON | |
| CY91F522LSDPMC | | ON | ON | |
| CY91F522LHDPMC | | OFF | ON | |
| CY91F526KWDPMC | Yes | ON | ON | LQS・144 pin, (Lead pitch 0.5 mm) Plastic |
| CY91F526KJDPMC | | OFF | ON | |
| CY91F525KWDPMC | | ON | ON | |
| CY91F525KJDPMC | | OFF | ON | |
| CY91F524KWDPMC | | ON | ON | |
| CY91F524KJDPMC | | OFF | ON | |
| CY91F523KWDPMC | | ON | ON | |
| CY91F523KJDPMC | | OFF | ON | |
| CY91F522KWDPMC | | ON | ON | |
| CY91F522KJDPMC | | OFF | ON | |
| CY91F526KSDPMC | None | ON | ON | |
| CY91F526KHDPMC | | OFF | ON | |
| CY91F525KSDPMC | | ON | ON | |
| CY91F525KHDPMC | | OFF | ON | |
| CY91F524KSDPMC | | ON | ON | |
| CY91F524KHDPMC | | OFF | ON | |
| CY91F523KSDPMC | | ON | ON | |
| CY91F523KHDPMC | | OFF | ON | |
| CY91F522KSDPMC | | ON | ON | |
| CY91F522KHDPMC | | OFF | ON | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526KWDPMC1 | Yes | ON | ON | LQN・144 pin, (Lead pitch 0.4 mm) Plastic |
| CY91F526KJDPMC1 | | OFF | ON | |
| CY91F525KWDPMC1 | | ON | ON | |
| CY91F525KJDPMC1 | | OFF | ON | |
| CY91F524KWDPMC1 | | ON | ON | |
| CY91F524KJDPMC1 | | OFF | ON | |
| CY91F523KWDPMC1 | | ON | ON | |
| CY91F523KJDPMC1 | | OFF | ON | |
| CY91F522KWDPMC1 | | ON | ON | |
| CY91F522KJDPMC1 | | OFF | ON | |
| CY91F526KSDPMC1 | None | ON | ON | |
| CY91F526KHDPMC1 | | OFF | ON | |
| CY91F525KSDPMC1 | | ON | ON | |
| CY91F525KHDPMC1 | | OFF | ON | |
| CY91F524KSDPMC1 | | ON | ON | |
| CY91F524KHDPMC1 | | OFF | ON | |
| CY91F523KSDPMC1 | | ON | ON | |
| CY91F523KHDPMC1 | | OFF | ON | |
| CY91F522KSDPMC1 | | ON | ON | |
| CY91F522KHDPMC1 | | OFF | ON | |
| CY91F526JWDPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| CY91F526JJDPMC | | OFF | ON | |
| CY91F525JWDPMC | | ON | ON | |
| CY91F525JJDPMC | | OFF | ON | |
| CY91F524JWDPMC | | ON | ON | |
| CY91F524JJDPMC | | OFF | ON | |
| CY91F523JWDPMC | | ON | ON | |
| CY91F523JJDPMC | | OFF | ON | |
| CY91F522JWDPMC | | ON | ON | |
| CY91F522JJDPMC | | OFF | ON | |
| CY91F526JSDPMC | None | ON | ON | |
| CY91F526JHDPMC | | OFF | ON | |
| CY91F525JSDPMC | | ON | ON | |
| CY91F525JHDPMC | | OFF | ON | |
| CY91F524JSDPMC | | ON | ON | |
| CY91F524JHDPMC | | OFF | ON | |
| CY91F523JSDPMC | | ON | ON | |
| CY91F523JHDPMC | | OFF | ON | |
| CY91F522JSDPMC | | ON | ON | |
| CY91F522JHDPMC | | OFF | ON | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526FWDPMC | Yes | ON | ON | LQI・100 pin, Plastic |
| CY91F526FJDPMC | | OFF | ON | |
| CY91F525FWDPMC | | ON | ON | |
| CY91F525FJDPMC | | OFF | ON | |
| CY91F524FWDPMC | | ON | ON | |
| CY91F524FJDPMC | | OFF | ON | |
| CY91F523FWDPMC | | ON | ON | |
| CY91F523FJDPMC | | OFF | ON | |
| CY91F522FWDPMC | | ON | ON | |
| CY91F522FJDPMC | | OFF | ON | |
| CY91F526FSDPMC | None | ON | ON | |
| CY91F526FHDPMC | | OFF | ON | |
| CY91F525FSDPMC | | ON | ON | |
| CY91F525FHDPMC | | OFF | ON | |
| CY91F524FSDPMC | | ON | ON | |
| CY91F524FHDPMC | | OFF | ON | |
| CY91F523FSDPMC | | ON | ON | |
| CY91F523FHDPMC | | OFF | ON | |
| CY91F522FSDPMC | | ON | ON | |
| CY91F522FHDPMC | | OFF | ON | |
| CY91F526DWDPMC | Yes | ON | ON | LQH・80 pin, Plastic |
| CY91F526DJDPMC | | OFF | ON | |
| CY91F525DWDPMC | | ON | ON | |
| CY91F525DJDPMC | | OFF | ON | |
| CY91F524DWDPMC | | ON | ON | |
| CY91F524DJDPMC | | OFF | ON | |
| CY91F523DWDPMC | | ON | ON | |
| CY91F523DJDPMC | | OFF | ON | |
| CY91F522DWDPMC | | ON | ON | |
| CY91F522DJDPMC | | OFF | ON | |
| CY91F526DSDPMC | None | ON | ON | |
| CY91F526DHDPMC | | OFF | ON | |
| CY91F525DSDPMC | | ON | ON | |
| CY91F525DHDPMC | | OFF | ON | |
| CY91F524DSDPMC | | ON | ON | |
| CY91F524DHDPMC | | OFF | ON | |
| CY91F523DSDPMC | | ON | ON | |
| CY91F523DHDPMC | | OFF | ON | |
| CY91F522DSDPMC | | ON | ON | |
| CY91F522DHDPMC | | OFF | ON | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526BWDPMC1 | Yes | ON | ON | LQD・64 pin, Plastic |
| CY91F526BJDPMC1 | | OFF | ON | |
| CY91F525BWDPMC1 | | ON | ON | |
| CY91F525BJDPMC1 | | OFF | ON | |
| CY91F524BWDPMC1 | | ON | ON | |
| CY91F524BJDPMC1 | | OFF | ON | |
| CY91F523BWDPMC1 | | ON | ON | |
| CY91F523BJDPMC1 | | OFF | ON | |
| CY91F522BWDPMC1 | | ON | ON | |
| CY91F522BJDPMC1 | | OFF | ON | |
| CY91F526BSDPMC1 | None | ON | ON | |
| CY91F526BHDPMC1 | | OFF | ON | |
| CY91F525BSDPMC1 | | ON | ON | |
| CY91F525BHDPMC1 | | OFF | ON | |
| CY91F524BSDPMC1 | | ON | ON | |
| CY91F524BHDPMC1 | | OFF | ON | |
| CY91F523BSDPMC1 | | ON | ON | |
| CY91F523BHDPMC1 | | OFF | ON | |
| CY91F522BSDPMC1 | | ON | ON | |
| CY91F522BHDPMC1 | | OFF | ON | |

*: For details of the package, see Package Dimensions.

## 16. Ordering Information CY91F52xxxE

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526LWEPMC | Yes | ON | ON | LQP・176 pin, Plastic |
| CY91F526LJEPMC | | OFF | ON | |
| CY91F525LWEPMC | | ON | ON | |
| CY91F525LJEPMC | | OFF | ON | |
| CY91F524LWEPMC | | ON | ON | |
| CY91F524LJEPMC | | OFF | ON | |
| CY91F523LWEPMC | | ON | ON | |
| CY91F523LJEPMC | | OFF | ON | |
| CY91F522LWEPMC | | ON | ON | |
| CY91F522LJEPMC | | OFF | ON | |
| CY91F526LSEPMC | None | ON | ON | |
| CY91F526LHEPMC | | OFF | ON | |
| CY91F526LKEPMC | | OFF | OFF | |
| CY91F525LSEPMC | | ON | ON | |
| CY91F525LHEPMC | | OFF | ON | |
| CY91F524LSEPMC | | ON | ON | |
| CY91F524LHEPMC | | OFF | ON | |
| CY91F523LSEPMC | | ON | ON | |
| CY91F523LHEPMC | | OFF | ON | |
| CY91F522LSEPMC | | ON | ON | |
| CY91F522LHEPMC | | OFF | ON | |
| CY91F526KWEPMC | Yes | ON | ON | LQS・144 pin, (Lead pitch 0.5 mm) Plastic |
| CY91F526KJEPMC | | OFF | ON | |
| CY91F525KWEPMC | | ON | ON | |
| CY91F525KJEPMC | | OFF | ON | |
| CY91F524KWEPMC | | ON | ON | |
| CY91F524KJEPMC | | OFF | ON | |
| CY91F523KWEPMC | | ON | ON | |
| CY91F523KJEPMC | | OFF | ON | |
| CY91F522KWEPMC | | ON | ON | |
| CY91F522KJEPMC | | OFF | ON | |
| CY91F526KSEPMC | None | ON | ON | |
| CY91F526KHEPMC | | OFF | ON | |
| CY91F525KSEPMC | | ON | ON | |
| CY91F525KHEPMC | | OFF | ON | |
| CY91F524KSEPMC | | ON | ON | |
| CY91F524KHEPMC | | OFF | ON | |
| CY91F523KSEPMC | | ON | ON | |
| CY91F523KHEPMC | | OFF | ON | |
| CY91F522KSEPMC | | ON | ON | |
| CY91F522KHEPMC | | OFF | ON | |

| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526KWEPMC1 | Yes | ON | ON | LQN・144 pin, (LeaE pitch 0.4 mm) Plastic |
| CY91F526KJEPMC1 | | OFF | ON | |
| CY91F525KWEPMC1 | | ON | ON | |
| CY91F525KJEPMC1 | | OFF | ON | |
| CY91F524KWEPMC1 | | ON | ON | |
| CY91F524KJEPMC1 | | OFF | ON | |
| CY91F523KWEPMC1 | | ON | ON | |
| CY91F523KJEPMC1 | | OFF | ON | |
| CY91F522KWEPMC1 | | ON | ON | |
| CY91F522KJEPMC1 | | OFF | ON | |
| CY91F526KSEPMC1 | None | ON | ON | |
| CY91F526KHEPMC1 | | OFF | ON | |
| CY91F525KSEPMC1 | | ON | ON | |
| CY91F525KHEPMC1 | | OFF | ON | |
| CY91F524KSEPMC1 | | ON | ON | |
| CY91F524KHEPMC1 | | OFF | ON | |
| CY91F523KSEPMC1 | | ON | ON | |
| CY91F523KHEPMC1 | | OFF | ON | |
| CY91F522KSEPMC1 | | ON | ON | |
| CY91F522KHEPMC1 | | OFF | ON | |
| CY91F526JWEPMC | Yes | ON | ON | LQM・120 pin, Plastic |
| CY91F526JJEPMC | | OFF | ON | |
| CY91F525JWEPMC | | ON | ON | |
| CY91F525JJEPMC | | OFF | ON | |
| CY91F524JWEPMC | | ON | ON | |
| CY91F524JJEPMC | | OFF | ON | |
| CY91F523JWEPMC | | ON | ON | |
| CY91F523JJEPMC | | OFF | ON | |
| CY91F522JWEPMC | | ON | ON | |
| CY91F522JJEPMC | | OFF | ON | |
| CY91F526JSEPMC | None | ON | ON | |
| CY91F526JHEPMC | | OFF | ON | |
| CY91F525JSEPMC | | ON | ON | |
| CY91F525JHEPMC | | OFF | ON | |
| CY91F524JSEPMC | | ON | ON | |
| CY91F524JHEPMC | | OFF | ON | |
| CY91F523JSEPMC | | ON | ON | |
| CY91F523JHEPMC | | OFF | ON | |
| CY91F522JSEPMC | | ON | ON | |
| CY91F522JHEPMC | | OFF | ON | |

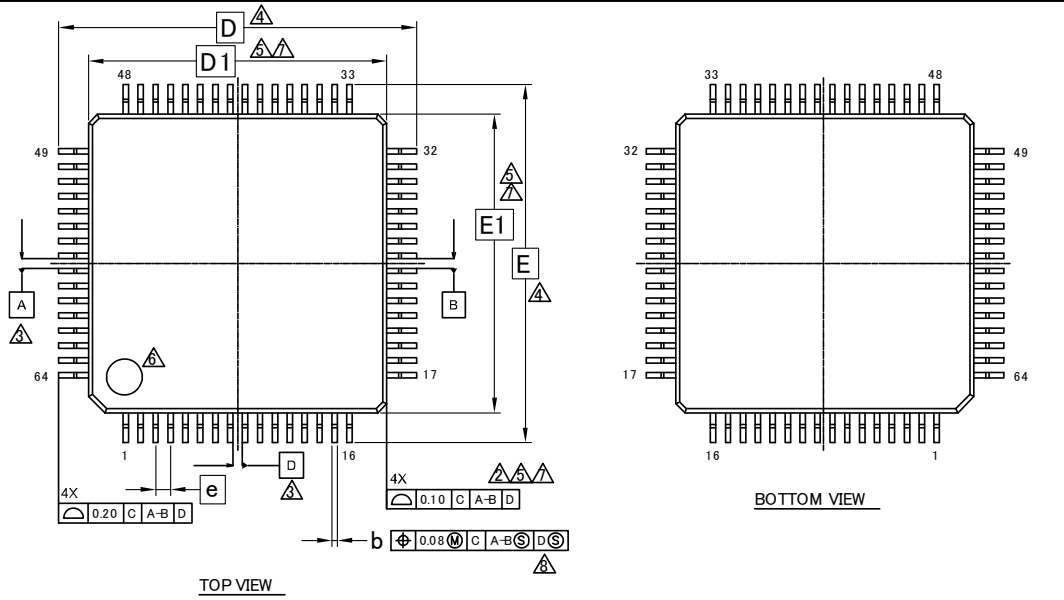
| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526FWEPMC | Yes | ON | ON | LQI・100 pin, Plastic |
| CY91F526FJEPMC | | OFF | ON | |
| CY91F525FWEPMC | | ON | ON | |
| CY91F525FJEPMC | | OFF | ON | |
| CY91F524FWEPMC | | ON | ON | |
| CY91F524FJEPMC | | OFF | ON | |
| CY91F523FWEPMC | | ON | ON | |
| CY91F523FJEPMC | | OFF | ON | |
| CY91F522FWEPMC | | ON | ON | |
| CY91F522FJEPMC | | OFF | ON | |
| CY91F526FSEPMC | None | ON | ON | |
| CY91F526FHEPMC | | OFF | ON | |
| CY91F525FSEPMC | | ON | ON | |
| CY91F525FHEPMC | | OFF | ON | |
| CY91F524FSEPMC | | ON | ON | |
| CY91F524FHEPMC | | OFF | ON | |
| CY91F523FSEPMC | | ON | ON | |
| CY91F523FHEPMC | | OFF | ON | |
| CY91F522FSEPMC | | ON | ON | |
| CY91F522FHEPMC | | OFF | ON | |
| CY91F526DWEPMC | Yes | ON | ON | LQH・80 pin, Plastic |
| CY91F526DJEPMC | | OFF | ON | |
| CY91F525DWEPMC | | ON | ON | |
| CY91F525DJEPMC | | OFF | ON | |
| CY91F524DWEPMC | | ON | ON | |
| CY91F524DJEPMC | | OFF | ON | |
| CY91F523DWEPMC | | ON | ON | |
| CY91F523DJEPMC | | OFF | ON | |
| CY91F522DWEPMC | | ON | ON | |
| CY91F522DJEPMC | | OFF | ON | |
| CY91F526DSEPMC | None | ON | ON | |
| CY91F526DHEPMC | | OFF | ON | |
| CY91F525DSEPMC | | ON | ON | |
| CY91F525DHEPMC | | OFF | ON | |
| CY91F524DSEPMC | | ON | ON | |
| CY91F524DHEPMC | | OFF | ON | |
| CY91F523DSEPMC | | ON | ON | |
| CY91F523DHEPMC | | OFF | ON | |
| CY91F522DSEPMC | | ON | ON | |
| CY91F522DHEPMC | | OFF | ON | |

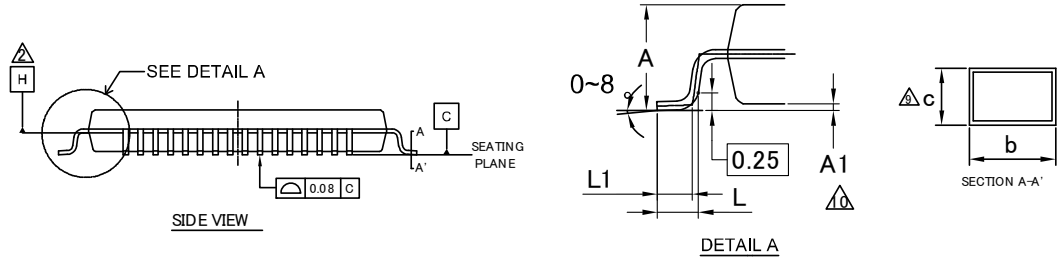
| Part Number | Sub Clock | CSV Initial Value | LVD Initial Value | Package* |
|---|---|---|---|---|
| CY91F526BWEPMC1 | Yes | ON | ON | LQD・64 pin, Plastic |
| CY91F526BJEPMC1 | | OFF | ON | |
| CY91F525BWEPMC1 | | ON | ON | |
| CY91F525BJEPMC1 | | OFF | ON | |
| CY91F524BWEPMC1 | | ON | ON | |
| CY91F524BJEPMC1 | | OFF | ON | |
| CY91F523BWEPMC1 | | ON | ON | |
| CY91F523BJEPMC1 | | OFF | ON | |
| CY91F522BWEPMC1 | | ON | ON | |
| CY91F522BJEPMC1 | | OFF | ON | |
| CY91F526BSEPMC1 | None | ON | ON | |
| CY91F526BHEPMC1 | | OFF | ON | |
| CY91F525BSEPMC1 | | ON | ON | |
| CY91F525BHEPMC1 | | OFF | ON | |
| CY91F524BSEPMC1 | | ON | ON | |
| CY91F524BHEPMC1 | | OFF | ON | |
| CY91F523BSEPMC1 | | ON | ON | |
| CY91F523BHEPMC1 | | OFF | ON | |
| CY91F522BSEPMC1 | | ON | ON | |
| CY91F522BHEPMC1 | | OFF | ON | |

*: For details of the package, see Package Dimensions.

## 17. Package Dimensions

| Package Type | Package Code |
|---|---|
| LQFP 64pin | LQD064 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.00 | — | 0.20 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 12.00 BSC. | | |
| D1 | 10.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC. | | |
| E1 | 10.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

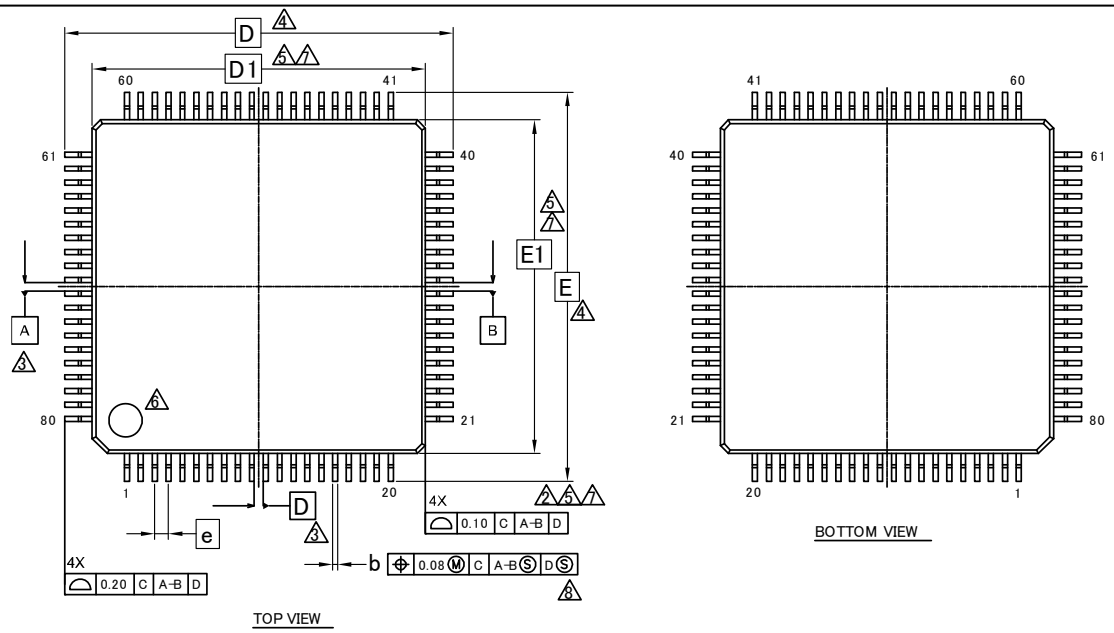
NOTES

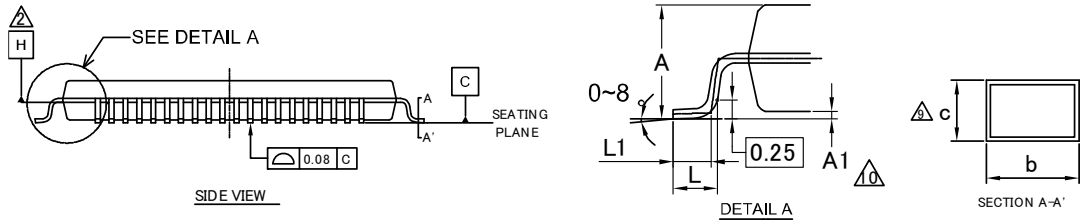
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

| Package Type | Package Code |
|---|---|
| LQFP 80pin | LQH080 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.70 |
| A1 | 0.05 | —— | 0.15 |
| b | 0.15 | —— | 0.27 |
| c | 0.09 | —— | 0.20 |
| D | 14.00 BSC. | | |
| D1 | 12.00 BSC. | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC. | | |
| E1 | 12.00 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

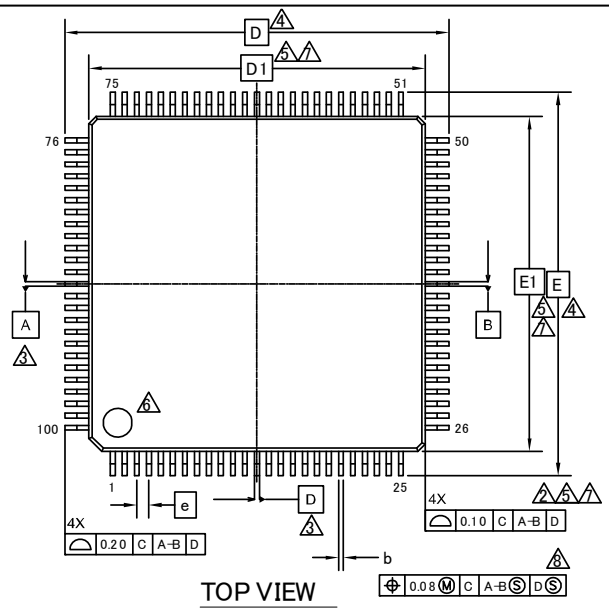
NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

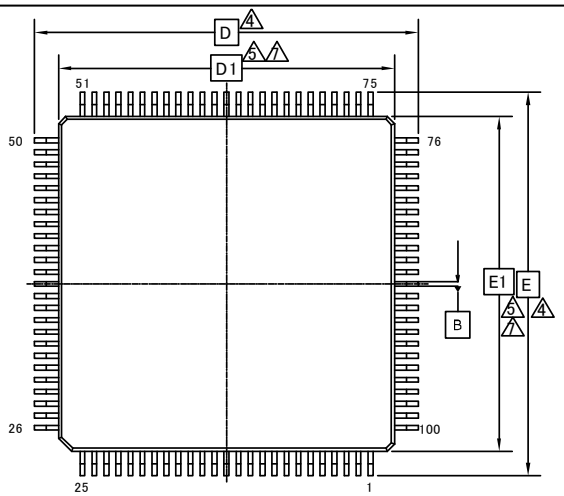
002-11501 **

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

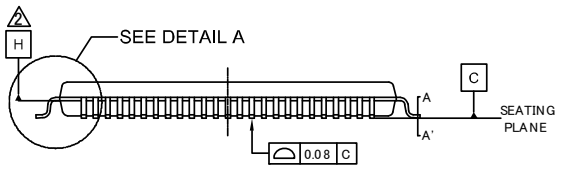
| Package Type | Package Code |
|---|---|
| LQFP 100pin | LQI100 |



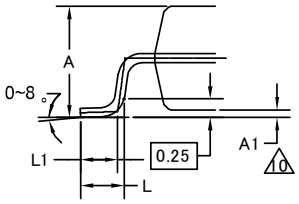

TOP VIEW



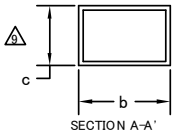

BOTTOM VIEW




SIDE VIEW




DETAIL A




SECTION A-A'

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.15 | — | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| e | 0.50 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

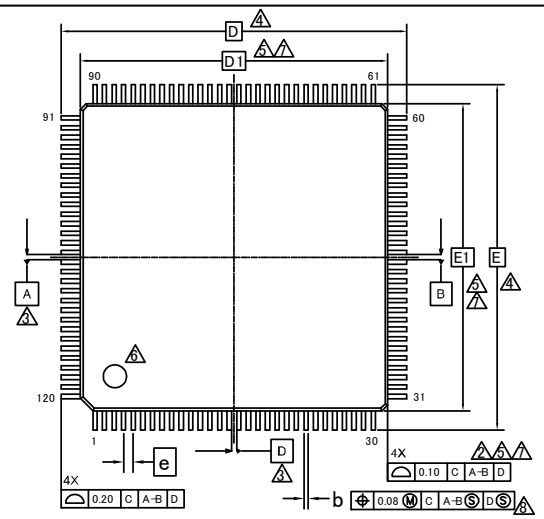
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

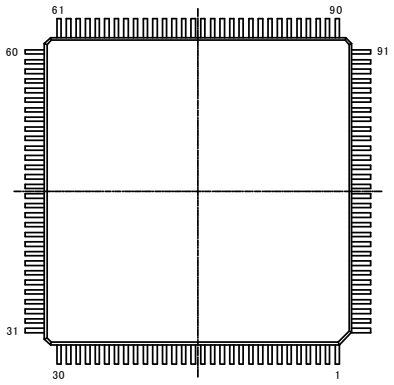
002-11500 *A

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

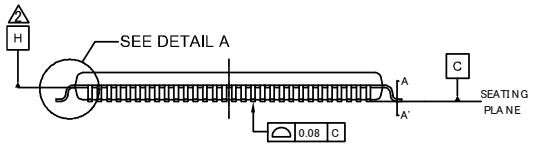
| Package Type | Package Code |
|---|---|
| LQFP 120pin | LQM120 |



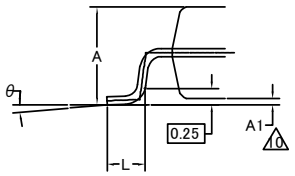

TOP VIEW



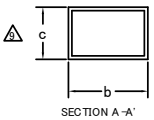

BOTTOM VIEW




SIDE VIEW




DETAIL A




SECTION A-A'

| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.115 | — | 0.195 |
| D | 18.00 BSC | | |
| D1 | 16.00 BSC | | |
| e | 0.50 BSC | | |
| E | 18.00 BSC | | |
| E1 | 16.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | — | 8° |

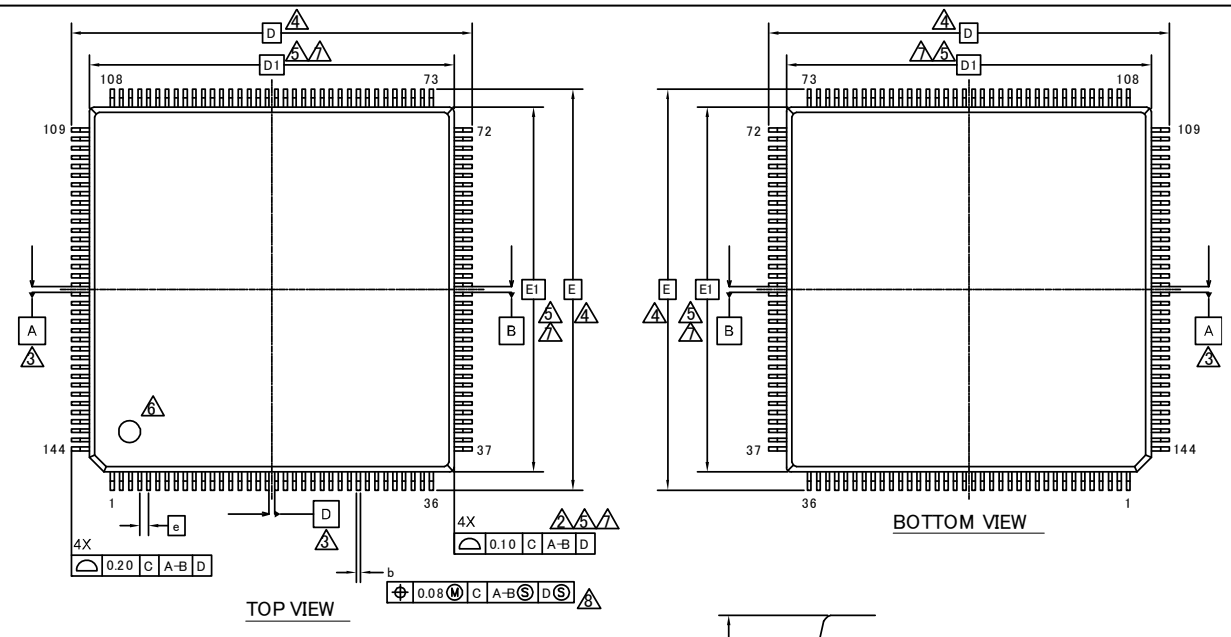
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

| Package Type | Package Code |
|---|---|
| LQFP 144pin | LQS144 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 22.00 BSC | | |
| D1 | 20.00 BSC | | |
| e | 0.50 BSC | | |
| E | 22.00 BSC | | |
| E1 | 20.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |

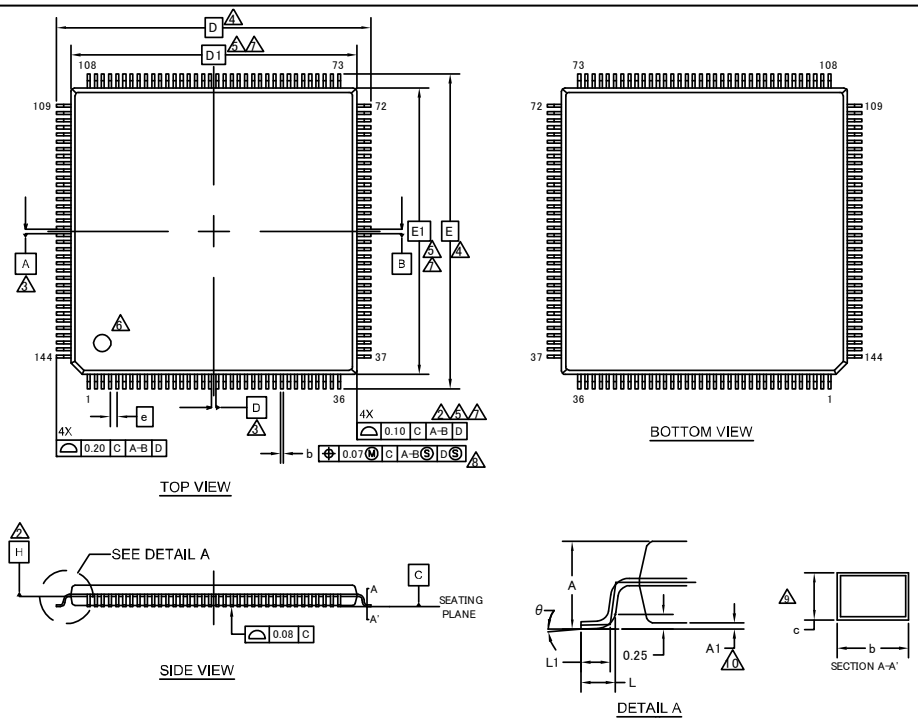
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *A

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

| Package Type | Package Code |
|---|---|
| LQFP 144pin | LQN144 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.70 |
| A1 | 0.05 | —— | 0.15 |
| b | 0.145 | 0.18 | 0.215 |
| c | 0.115 | —— | 0.195 |
| D | 18.00 BSC | | |
| D1 | 16.00 BSC | | |
| e | 0.40 BSC | | |
| E | 18.00 BSC | | |
| E1 | 16.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | —— | 8° |

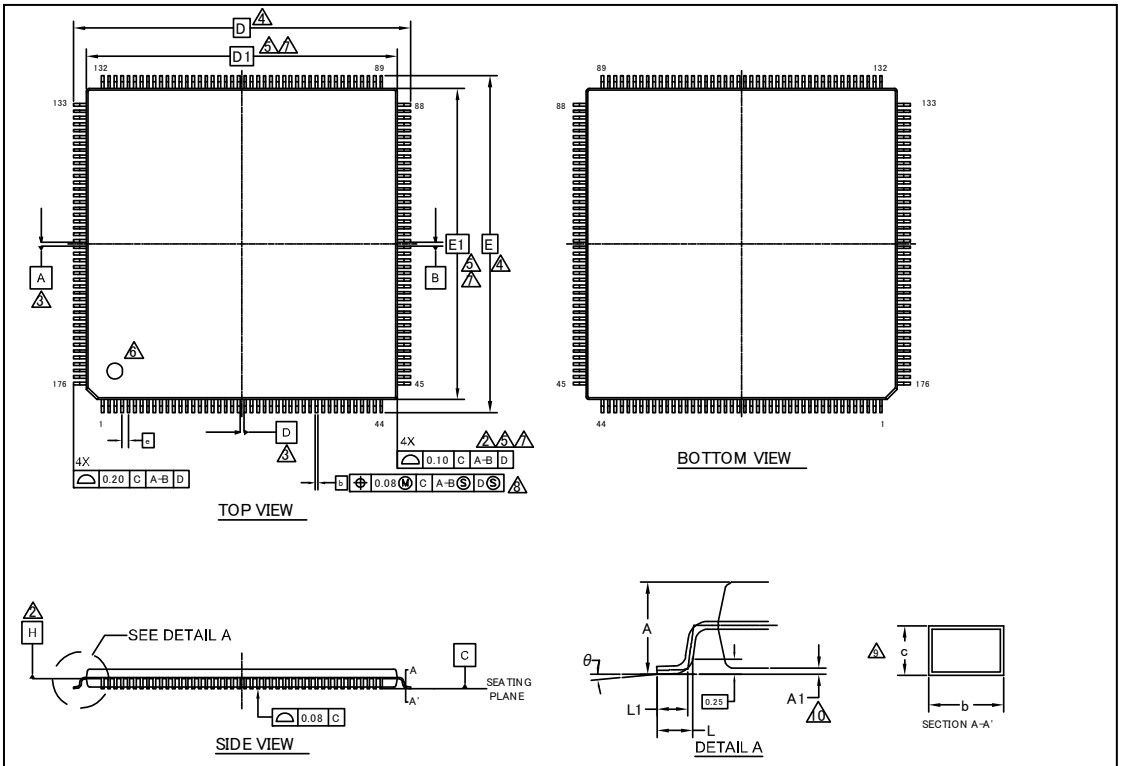
## NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-14045 **

PACKAGE OUTLINE, 144 LEAD LQFP
16.0X16.0X1.7 MM LQN144 REV**

| Package Type | Package Code |
|---|---|
| LQFP 176pin | LQP176 |




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 26.00 BSC | | |
| D1 | 24.00 BSC | | |
| e | 0.50 BSC | | |
| E | 26.00 BSC | | |
| E1 | 24.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 0.30 | 0.50 | 0.70 |
| θ | 0° | — | 8° |

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

# 18. Errata

This section describes the errata for the CY91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

**Part Numbers Affected**

| Part Number |
|---|
| CY91F522B/D/F/J/K/L<br>CY91F523B/D/F/J/K/L<br>CY91F524B/D/F/J/K/L<br>CY91F525B/D/F/J/K/L<br>CY91F526B/D/F/J/K/L |

**CY91F522/3/4/5/6 Qualification Status**

Product Status: Production

**Errata Summary**

The following table defines the errata applicability to available CY91520 Series devices.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| [1]. Power-on Conditions is not enough in the Datasheet Specification | CY91F522B/D/F/J/K/L<br>CY91F523B/D/F/J/K/L<br>CY91F524B/D/F/J/K/L<br>CY91F525B/D/F/J/K/L<br>CY91F526B/D/F/J/K/L | B, C | Will be fixed in production silicon version D, E |
| [2]. Limitation for Watch mode (power off) | | B, C, D, E | - |

**1. Power-on Conditions is not enough in the Datasheet Specification**

**■ Problem Definition**

If the Power-On-Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

**■ Parameters Affected**

$t_{OFF}$ for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

**■ Trigger Condition**

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

(1) The VCC voltage is less than 200 mV for 50 ms or longer ($t_{OFF}$)

(2) VCC Power ramp rate less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

■ **Scope of Impact**

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ **Workaround**

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

(1) The VCC voltage is less than 200 mV for 50 ms or longer ($t_{OFF}$)

(2) VCC Power ramp rate is less than 4 mV/µs (dV/dt) until a voltage level for a safe Power-On detection is reached

(3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will releases new version D, so Cypress recommends the version D for CY91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ **Fix Status**

Will be fixed in production silicon version D, E

**2. Limitation for Watch mode (power off)**

■ **Problem Definition**

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ **Trigger Conditions**

(1) Using the watch mode (power off)

(2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘16’ to ‘30’, or using NMIX pin as source for recovering from the watch mode (power off)

(3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
(*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 µs to 100 µs

■ **Scope of Impact**

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL

CSELR.SCEN

CMONR.SCRDY

CCRTSELR.CST

CCRTSELR.CSC

■ **Workaround**

It is necessary to satisfy the below both conditions of (1) and (2).

(1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are ‘31’, before CPU state changes to the watch mode (power off)

(2) Don’t use NMIX pin as source for recovering from the watch mode (power off)

■ **Fix Status**

Will not be planned

## 19. Major Changes

**Spansion Publication Number: MB91F526L_DS705-00011**

| Page | Section | Change Results |
|---|---|---|
| Revision 1.0 | | |
| - | - | Initial release |
| Revision 2.0 | | |
| 3 | ■FEATURES | Corrected the following description.<br>5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input<br>↓<br>5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input |
| 33 to 36 | ■I/O CIRCUIT TYPE | Corrected the following description to "Type F, G, I, J, K, M".<br>Schmitt input → CMOS hysteresis input<br>Corrected the following description to "Type D, E".<br>$I^2C$ Schmitt input → $I^2C$ hysteresis input |
| 44 to 49 | ■BLOCK DIAGRAM | Corrected the following description.<br>●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B<br>●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D<br>●MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F<br>●MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J<br>●MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K<br>●MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L |
| 138 | ■ELECTRICAL CHARACTERISTICS<br>2. Recommended operating conditions | Added the following description.<br>*1 : When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset |
| 139,140 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C ". Max 1420µA → Max 2000µA |
| 139 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of "Power supply voltage range".<br>(TA:-40°C to +105°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V)<br>↓<br>($T_A$:-40°C to +105°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,$V_{SS}$=$AV_{SS}$=0.0V) |
| 140,141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of "Power supply voltage range".<br>($T_A$:-40°C to +125°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V)<br>↓<br>($T_A$:-40°C to +125°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,$V_{SS}$=$AV_{SS}$=0.0V) |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of " Pull-up resistance $R_{UP1}$".<br>Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140 |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the following description.<br>Pull-up resistance $R_{UP2}$<br>Port pin other than P035,041,093,122 → P073,074,076,077 |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Corrected the value of " Pull-up resistance $R_{UP2}$".<br>VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60<br>VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90 |
| 141 | ■ELECTRICAL CHARACTERISTICS<br>3.DC characteristics | Added the value of " Pull-up resistance $R_{UP3}$".<br>Pin name : Port pin other than P035,041,073,074,076,077,093,122<br>VCC=5.0V±10% Min 25 Max 100<br>VCC=3.3V±0.3V Min 45 Max 140 |

| Page | Section | Change Results |
|---|---|---|
| 150,152, 154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVI}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min -30 Max 30<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min -30 Max 30<br>Pin name: SCK3,SCK4<br>SOT3,SOT4<br>Value: Min -300 Max 300 |
| 150,152, 154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time $t_{IVSHI}$<br>(4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time $t_{IVSLI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11 SIN0 to SIN11<br>Value: Min 34 Max -<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11<br>Value: Min 34 Max -<br>Pin name: SCK3,SCK4,SIN3,SIN4<br>Value: Min 300 Max - |
| 150,152, 154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVE}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVE}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min - Max 33<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min - Max 33<br>Pin name: SCK3,SCK4 SOT3,SOT4<br>Value: Min - Max 300 |
| 150,152, 154,156 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4) | (4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time $t_F$<br>Corrected the following description.<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>Value: Min - Max 5<br>Pin name: SCK3,SCK4<br>Value: Min - Max 250<br>↓<br>Pin name: SCK0 to SCK11<br>Value: Min - Max 5 |

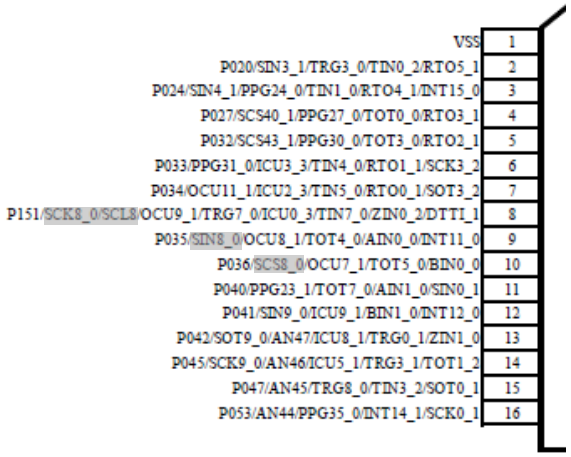
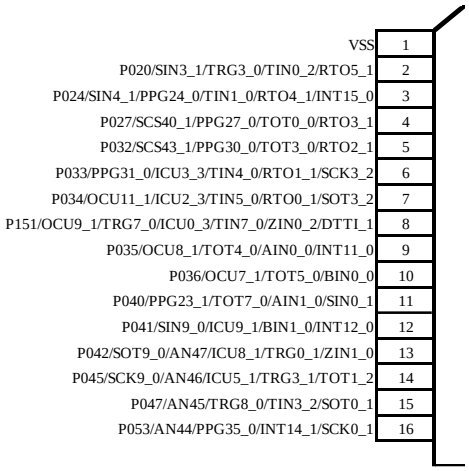
| Page | Section | Change Results |
|---|---|---|
| 158,161,<br>164,167 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-5),(4-1-6),(4-1-7),(4-1-8) | (4-1-5)SCS↓⇒SCK↓ setup time $t_{CSSI}$<br>(4-1-6)SCS↓⇒SCK↑ setup time $t_{CSSI}$<br>(4-1-7)SCS↑⇒SCK↓ setup time $t_{CSSI}$<br>(4-1-8)SCS↑⇒SCK↑ setup time $t_{CSSI}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSSU}$+0 Max $t_{CSSU}$+50<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSSU}$-50 Max $t_{CSSU}$+0<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $t_{CSSU}$-50 Max $t_{CSSU}$+300 |
| 158,161,<br>164,167 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-5),(4-1-6),(4-1-7),(4-1-8) | (4-1-5)SCK↑⇒SCS↑hold time $t_{CSHI}$<br>(4-1-6)SCK↓⇒SCS↑hold time $t_{CSHI}$<br>(4-1-7)SCK↑⇒SCS↓hold time $t_{CSHI}$<br>(4-1-8)SCK↓⇒SCS↓hold time $t_{CSHI}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-50 Max $t_{CSHD}$+0<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-10 Max $t_{CSHD}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $t_{CSHD}$-300 Max $t_{CSHD}$+50 |
| 158,161,<br>164,167 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-5),(4-1-6),(4-1-7),(4-1-8) | (4-1-5),(4-1-6)SCS↓⇒SOT delay time $t_{DSE}$<br>(4-1-7),(4-1-8)SCS↑⇒SOT delay time $t_{DSE}$<br>Corrected the following description.<br>Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>SOT1 to SOT11<br>Value: Min - Max 40<br>↓<br>Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>SOT1,SOT2,SOT5 to SOT11<br>Value: Min - Max 40<br>Pin name: SCS3,SCS40 to SCS43<br>SOT3,SOT4<br>Value: Min - Max 300 |

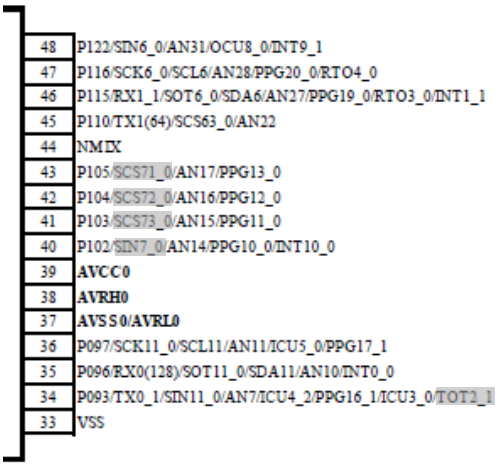
| Page | Section | Change Results |
|---|---|---|
| 159,162,<br>165,168 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-5),(4-1-6),(4-1-7),(4-1-8) | (4-1-5)SCK↓⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-6)SCK↑⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-7)SCK↓⇒SCS↑ clock switch time $t_{SCC}$<br>(4-1-8)SCK↑⇒SCS↑ clock switch time $t_{SCC}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $3t_{CPP}$+0 Max $3t_{CPP}$+50<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $3t_{CPP}$-10 Max $3t_{CPP}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $3t_{CPP}$-300 Max $3t_{CPP}$+50 |
| 159,162,<br>165,168 | ■ELECTRICAL CHARACTERISTICS<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-5),(4-1-6),(4-1-7),(4-1-8) | Added the following description.<br>Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again |
| 184 | ■ELECTRICAL CHARACTERISTICS<br>5.A/D Converter<br>(1) 12-bit A/D Converter<br>Electrical Characteristics | Added the value of "Total error".<br>Total error value Min – Typ – Max ±12 LSB |
| 184 | ■ELECTRICAL CHARACTERISTICS<br>5.A/D Converter<br>(1) 12-bit A/D Converter<br>Electrical Characteristics | Corrected the value of "Zero transition voltage".<br>Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV<br>↓<br>Min AVRL-11.5LSB Max AVRL+12.5LSB |
| 184 | ■ELECTRICAL CHARACTERISTICS<br>5.A/D Converter<br>(1) 12-bit A/D Converter<br>Electrical Characteristics | Corrected the value of "Full-scale transition voltage".<br>Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV<br>↓<br>Min AVRH-13.5LSB Max AVRH+10.5LSB |
| 184 | ■ELECTRICAL CHARACTERISTICS<br>5.A/D Converter<br>(1) 12-bit A/D Converter<br>Electrical Characteristics | Added the following description.<br>Parameter : Power supply current $I_A$ AVCC*3<br>*3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter. |
| 188 | ■ELECTRICAL CHARACTERISTICS<br>7.D/A Converter | Added the following description.<br>Parameter : Power supply current *1<br>*1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter. |
| 187 | ■ELECTRICAL CHARACTERISTICS<br>6.Flash memory | Parameter: Erase cycle*2/Data retain time<br>Deleted the following description.<br>Remarks :<br>"Temperature at writing/erasing Tj<+105°C" |

| Page | Section | Change Results |
|---|---|---|
| 188 | ■ELECTRICAL CHARACTERISTICS 7.D/A Converter | Corrected the following description.<br>Parameter : Power supply current<br>Symbol IA Pin name $AV_{CC}$<br>Symbol IAH Pin name $AV_{CC}$<br>↓<br>Symbol IA Pin name AVCC<br>Symbol IAH Pin name AVCC |
| 190 | ■EXAMPLE CHARACTERISTICS | Corrected the following description.<br>Watch mode |
| 192 | ■ORDERING INFORMATION | Corrected the following description.<br>■ORDERING INFORMATION<br>↓<br>■ORDERING INFORMATION MB91F52xxxB*1<br>Package<br>↓<br>Package*2 |
| 198 | ■ORDERING INFORMATION | Added the following description.<br>*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products. |
| 198 | ■ORDERING INFORMATION | Corrected the following description.<br>For details of the package, see "■ PACKAGE DIMENSIONS ".<br>↓<br>*2: For details of the package, see "■ PACKAGE DIMENSIONS ". |
| 199 to 205 | ■ORDERING INFORMATION | Added the following description.<br>■ORDERING INFORMATION MB91F52xxxC |
| - | - | Company name and layout design change |

| Page | Section | Change Results |
|---|---|---|
| Cypress Document Number: 002-04662 | | |
| Rev *B | | |
| 1 | ■Features | Corrected the following description.<br>· Clock generation (equipped with SSCG function)<br>· Main oscillation (4MHz to 16MHz)<br>· Sub oscillation (32kHz to 100kHz) or none sub oscillation<br>· PLL multiplication rate : 1 to 20 times<br>↓<br>· Clock generation (equipped with SSCG function)<br>· Main oscillation (4MHz to 16MHz)<br>· Sub oscillation (32kHz) or no sub oscillation<br>· PLL multiplication rate : 1 to 20 times<br>· Equipped with a 100kHz CR oscillator |
| 2 | ■Features | Corrected the following description.<br>· Base timer : Max. 2 channels<br>·16-bit timer<br>· Any of four PWM/PPG/PWC/reload timer functions can be selected and used<br>· A 32-bit timer can be used in 2 channels of cascade mode<br>↓<br>· Base timer : Max. 2 channels<br>· 16-bit timer<br>· Any of four PWM/PPG/PWC/reload timer functions can be selected and used<br>· As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascaded mode |
| 6 | ■Product Lineup | Corrected the following description for Product lineup comparison(64 pin).<br>Multi-Function Serial Interface: 8ch<br>↓<br>Multi-Function Serial Interface: 8ch*1 |
| 6 | ■Product Lineup | Added the following sentences under Product lineup comparison(64 pin)<br>*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode). |
| 7 | ■Product Lineup | Corrected the following description for Product lineup comparison(80 pin).<br>Multi-Function Serial Interface: 9ch<br>↓<br>Multi-Function Serial Interface: 9ch*1 |
| 7 | ■Product Lineup | Added the following sentences under Product lineup comparison(80 pin)<br>*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode). |
| 8 | ■Product Lineup | Corrected the following description for Product lineup comparison(100 pin).<br>Multi-Function Serial Interface: 12ch<br>↓<br>Multi-Function Serial Interface: 12ch*1 |
| 8 | ■Product Lineup | Added the following sentences under Product lineup comparison(100 pin)<br>*1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode). |

| Page | Section | Change Results |
|---|---|---|
| 9 | ■Product Lineup | Corrected the following description for Product lineup comparison(120 pin).<br>Multi-Function Serial Interface: 12ch<br>↓<br>Multi-Function Serial Interface: 12ch*1 |
| 9 | ■Product Lineup | Added the following sentences under Product lineup comparison(120 pin)<br>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).<br>Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode). |
| 10 | ■Product Lineup | Corrected the following description for Product lineup comparison(144 pin).<br>Multi-Function Serial Interface: 12ch<br>↓<br>Multi-Function Serial Interface: 12ch*1 |
| 10 | ■Product Lineup | Added the following sentences under Product lineup comparison(144 pin)<br>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).<br>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode). |
| 11 | ■Product Lineup | Corrected the following description for Product lineup comparison(176 pin).<br>Multi-Function Serial Interface: 12ch<br>↓<br>Multi-Function Serial Interface: 12ch*1 |
| 11 | ■Product Lineup | Added the following sentences under Product lineup comparison(176 pin)<br>*1: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).<br>Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I²C (standard mode). |

| Page | Section | Change Results |
|---|---|---|
| 13 | ■Pin Assignment MB91F52xB | Signals indicated by the shading below deleted in Figure.<br>- Left side<br>  <br><br>↓<br>  <br> |

| Page | Section | Change Results |
|---|---|---|
| 13 | ■Pin Assignment MB91F52xB | - Right side<br>  <br>48 P122/SIN6_0/AN31/OCU8_0/INT9_1<br>47 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0<br>46 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1<br>45 P110/TX1(64)/SCS63_0/AN22<br>44 NMIX<br>43 P105/SCS71_0/AN17/PPG13_0<br>42 P104/SCS72_0/AN16/PPG12_0<br>41 P103/SCS73_0/AN15/PPG11_0<br>40 P102/SIN7_0/AN14/PPG10_0/INT10_0<br>39 **AVCC0**<br>38 **AVRH0**<br>37 **AVSS0/AVRL0**<br>36 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1<br>35 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0<br>34 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT2_1<br>33 VSS<br>↓<br>48 P122/SIN6_0/AN31/OCU8_0/INT9_1<br>47 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0<br>46 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1<br>45 P110/TX1(64)/SCS63_0/AN22<br>44 NMIX<br>43 P105/AN17/PPG13_0<br>42 P104/AN16/PPG12_0<br>41 P103/AN15/PPG11_0<br>40 P102/AN14/PPG10_0/INT10_0<br>39 **AVCC0**<br>38 **AVRH0**<br>37 **AVSS0/AVRL0**<br>36 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1<br>35 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0<br>34 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0<br>33 VSS |

| Page | Section | Change Results |
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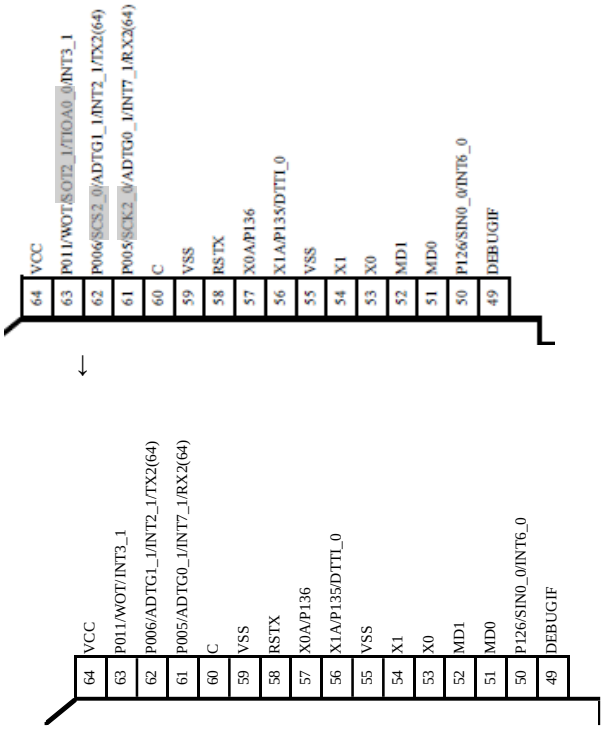
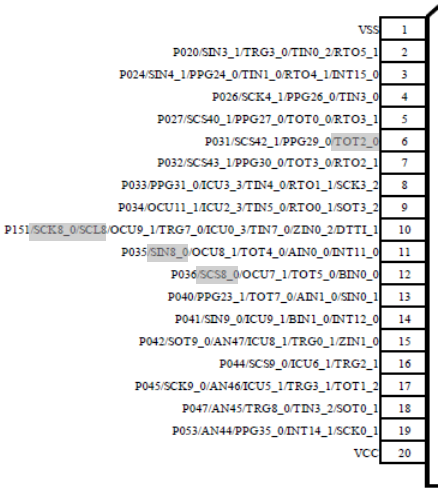
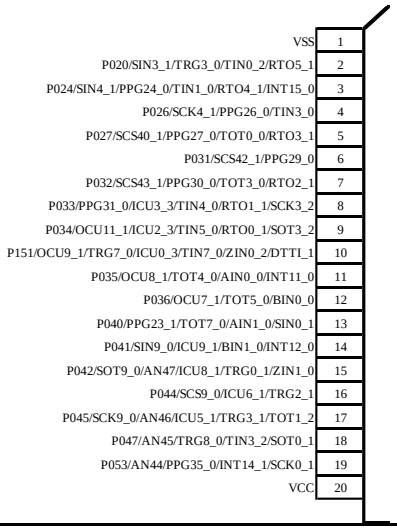
| 13 | ■Pin Assignment MB91F52xB | - Top<br>  <br> |
| 13 | ■Pin Assignment MB91F52xB | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 56 and pin 57 are the general-purpose ports. |

| Page | Section | Change Results |
|---|---|---|
| 14 | ■Pin Assignment MB91F52xD | Signals indicated by the shading below deleted in Figure.<br>- Left side<br>  <br><br>↓<br>  <br> |

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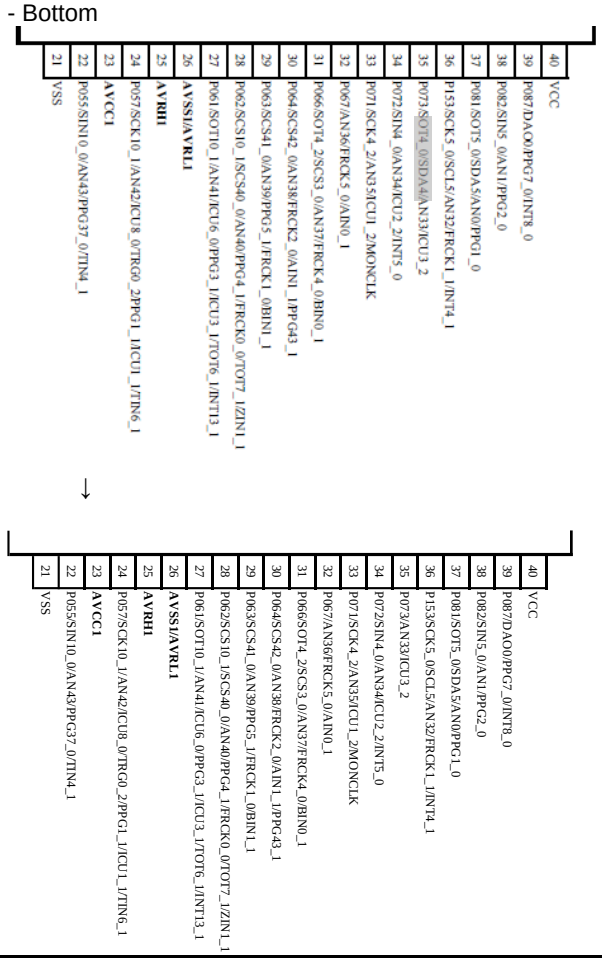
| 14 | ■Pin Assignment MB91F52xD | - Bottom<br>  <br> |

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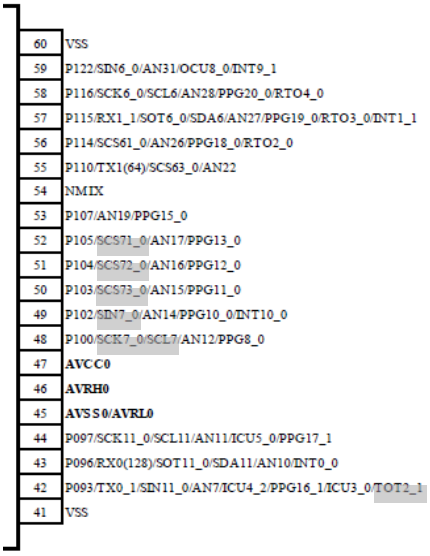
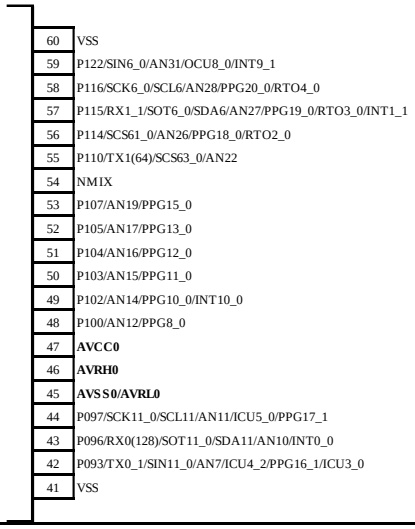
| 14 | ■Pin Assignment MB91F52xD | - Right side<br>  <br>60 VSS<br>59 P122/SIN6_0/AN31/OCU8_0/INT9_1<br>58 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0<br>57 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1<br>56 P114/SCS61_0/AN26/PPG18_0/RTO2_0<br>55 P110/TX1(64)/SCS63_0/AN22<br>54 NMIX<br>53 P107/AN19/PPG15_0<br>52 P105/SCS71_0/AN17/PPG13_0<br>51 P104/SCS72_0/AN16/PPG12_0<br>50 P103/SCS73_0/AN15/PPG11_0<br>49 P102/SIN7_0/AN14/PPG10_0/INT10_0<br>48 P100/SCK7_0/SCL7/AN12/PPG8_0<br>47 **AVCC0**<br>46 **AVRH0**<br>45 **AVSS0/AVRL0**<br>44 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1<br>43 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0<br>42 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT2_1<br>41 VSS<br>↓<br>  <br>60 VSS<br>59 P122/SIN6_0/AN31/OCU8_0/INT9_1<br>58 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0<br>57 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1<br>56 P114/SCS61_0/AN26/PPG18_0/RTO2_0<br>55 P110/TX1(64)/SCS63_0/AN22<br>54 NMIX<br>53 P107/AN19/PPG15_0<br>52 P105/AN17/PPG13_0<br>51 P104/AN16/PPG12_0<br>50 P103/AN15/PPG11_0<br>49 P102/AN14/PPG10_0/INT10_0<br>48 P100/AN12/PPG8_0<br>47 **AVCC0**<br>46 **AVRH0**<br>45 **AVSS0/AVRL0**<br>44 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1<br>43 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0<br>42 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0<br>41 VSS |

| Page | Section | Change Results |
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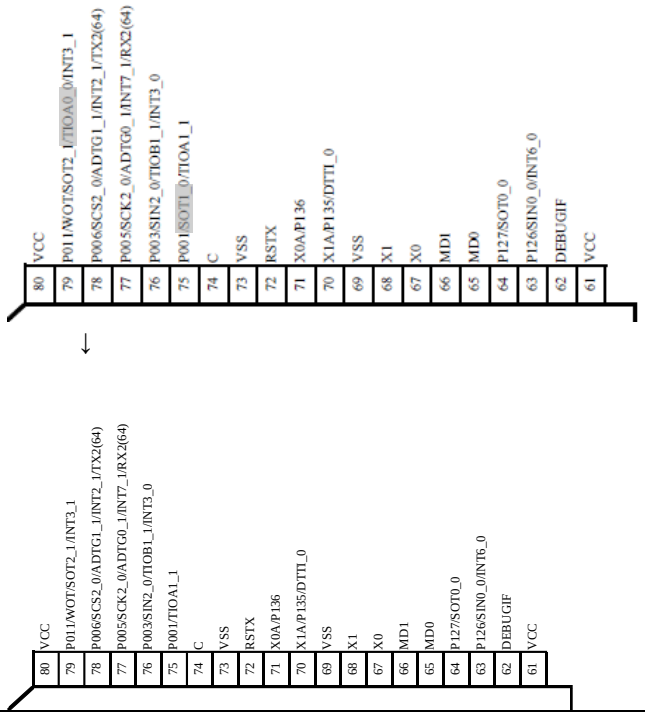
| 14 | ■Pin Assignment MB91F52xD | - Top<br>  <br>↓<br> |
| 14 | ■Pin Assignment MB91F52xD | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 71 and pin 72 are the general-purpose ports. |

| Page | Section | Change Results |
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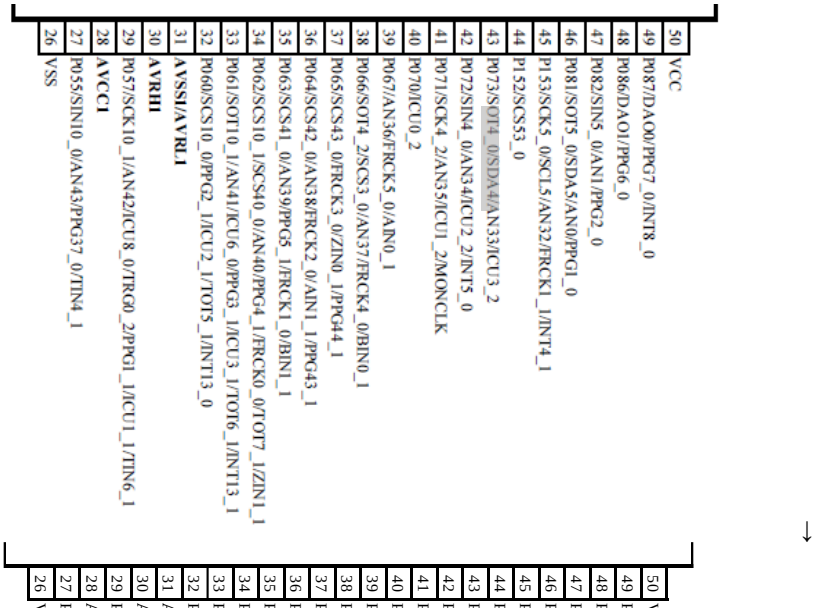
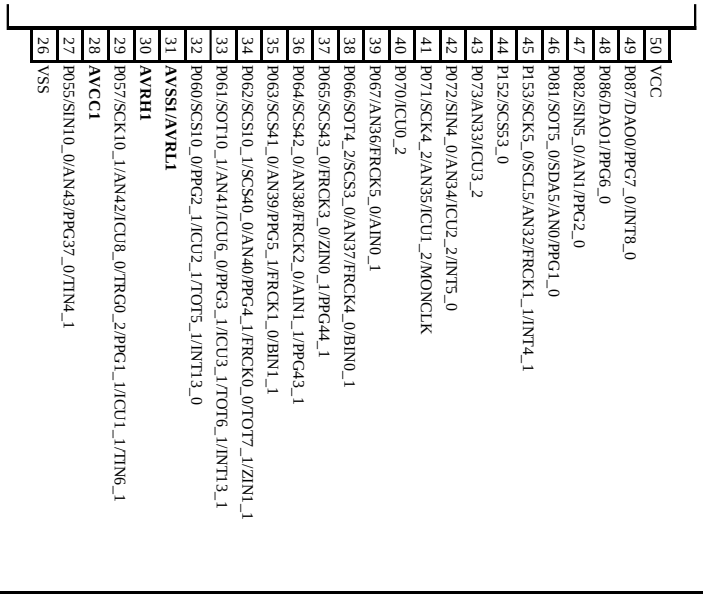
| 15 | ■Pin Assignment MB91F52xF | Signals indicated by the shading below deleted in Figure.<br><br>(Error)<br>- Bottom<br>  <br>↓<br>  |

| Page | Section | Change Results |
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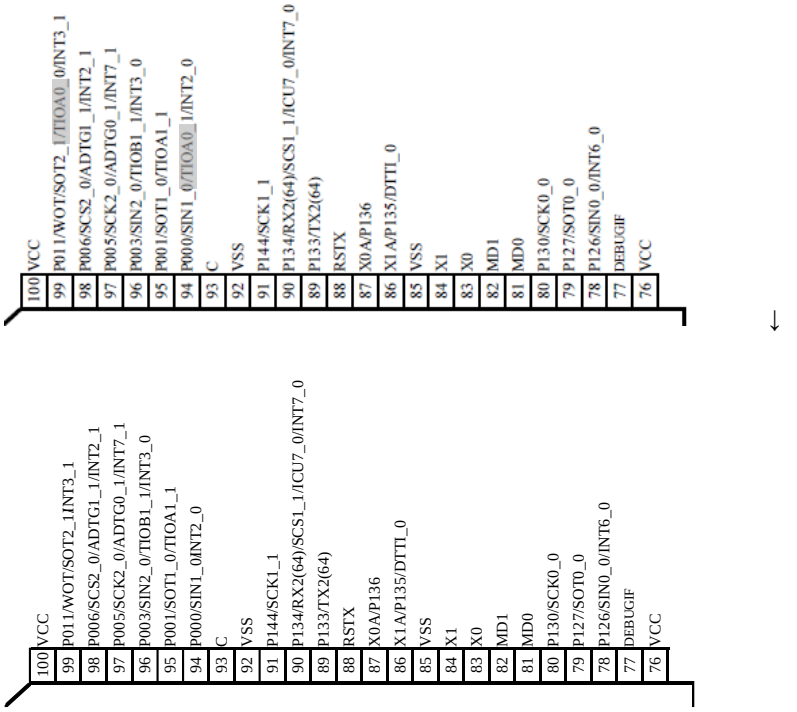
| 15 | ■Pin Assignment MB91F52xF | - Top<br>  <br><br>↓<br><br> |
| 15 | ■Pin Assignment MB91F52xF | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 86 and pin 87 are the general-purpose ports. |
| 16 | ■Pin Assignment MB91F52xJ | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 102 and pin 103 are the general-purpose ports. |
| 17 | ■Pin Assignment MB91F52xK | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 121 and pin 122 are the general-purpose ports. |
| 18 | ■Pin Assignment MB91F52xL | The following note added on the bottom left of Figure.<br>* In a single clock product, pin 149 and pin 150 are the general-purpose ports. |
| 19 to 35 | ■PIN Description | A List of "Pin Description" modified.<br><br>I/O Circuit types*1 \| Function*2<br>↓<br>I/O Circuit types*8 \| Function*9 |

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<tr><td>Function*2</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit21 I/O (0)</td></tr>
<tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 0 (1)</td></tr>
<tr><td>INT7 External interrupt input (1)</td></tr>
<tr><td>(CAN reception data 2 input<br>MB91F52xB ,MB91F52xD only)</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit22 I/O (0)</td></tr>
<tr><td>Serial chip select 2 I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 1 (1)</td></tr>
<tr><td>INT2 External interrupt input (1)</td></tr>
<tr><td>(CAN transmission data 2 output<br>MB91F52xB ,MB91F52xD only)</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Function*9</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit21 I/O (0)</td></tr>
<tr><td>Multi-function serial ch.2 clock I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 0 (1)</td></tr>
<tr><td>INT7 External interrupt input (1)</td></tr>
<tr><td>CAN reception data 2 input</td></tr>
<tr><td></td></tr>
<tr><td>General-purpose I/O port</td></tr>
<tr><td>External bus data bit22 I/O (0)</td></tr>
<tr><td>Serial chip select 2 I/O (0)</td></tr>
<tr><td>A/D converter external trigger input 1 (1)</td></tr>
<tr><td>INT2 External interrupt input (1)</td></tr>
<tr><td>CAN transmission data 2 output</td></tr>
</table>
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 36 | ■PIN Description | The following sentences modified under the Table of Pin description.<br><br>(Error)<br>*1: For the I/O circuit types, see "■I/O CIRCUIT TYPE".<br>*2: For switching, see "I/O Port" in HARDWARE MANUAL.<br><br>(Correct)<br>*1: There is a restriction of pin functions. See "Pin Name" of this table.<br>*2: not supported in 64pin<br>*3: not supported in 80pin<br>*4: not supported in 100pin<br>*5: not supported in 120pin<br>*6: not supported in 144pin<br>*7: not supported in 176pin<br>*8: For the I/O circuit types, see "■I/O CIRCUIT TYPE".<br>*9: For switching, see "I/O Port" in HARDWARE MANUAL. |
| 39 | ■I/O Circuit Type | Remarks for Type I in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- 3V pad power supply (5V tolerant),<br>General-purpose I/O port<br>- Output 4mA<br>- CMOS hysteresis input<br><br>(Correct)<br>- General-purpose I/O port (5V tolerant)<br>- Output 4mA<br>- CMOS hysteresis input |
| 40 | ■I/O Circuit Type | Remarks for Type J in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- 3V pad power supply (5V tolerant),<br>Analog input,General-purpose I/O port<br>- Output 4mA<br>- CMOS hysteresis input<br><br>(Correct)<br>- Analog input, General-purpose I/O port (5V tolerant)<br>- Output 4mA<br>- CMOS hysteresis input |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type L in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- Open-drain I/O<br>- Output 25mA (NOD)<br>- TTL input<br><br>(Correct)<br>- Open-drain I/O<br>- Output 25mA (Nch open-drain)<br>- TTL input</td></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type M in "I/O Circuit Types" modified as follows:<br><br>(Error)<br>- CMOS hysteresis input<br>- Pull-up resistor 50kΩ (5V cont)<br><br>(Correct)<br>- CMOS hysteresis input<br>- Pull-up resistor 50kΩ</td></tr>
<tr><td>121</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 64pins.<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>124</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 80pin modified as follows:<br><br>(Error)<br><table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308H</td><td rowspan="4">000FFF08H</td><td rowspan="4">45*5</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>–</td></tr><tr><td>–</td></tr></table><br>(Correct)<br><table><tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308H</td><td rowspan="4">000FFF08H</td><td rowspan="4">45</td></tr><tr><td>Base timer 1 IRQ1</td></tr><tr><td>–</td></tr><tr><td>–</td></tr></table></td></tr>
<tr><td>125</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 80pins.<br><br>(Error)<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 100pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 0 IRQ0<br>Base timer 0 IRQ1</td><td>60</td><td>3C</td><td>ICR44</td><td>30C<sub>H</sub></td><td>000FFF0C<sub>H</sub></td><td>44</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>–<br>–</td><td>60</td><td>3C</td><td>ICR44</td><td>30C<sub>H</sub></td><td>000FFF0C<sub>H</sub></td><td>44</td></tr>
</table>
</td></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 100pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>–<br>–</td><td>61</td><td>3D</td><td>ICR45</td><td>308<sub>H</sub></td><td>000FFF08<sub>H</sub></td><td>45 *5</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Base timer 1 IRQ0<br>Base timer 1 IRQ1<br>–<br>–</td><td>61</td><td>3D</td><td>ICR45</td><td>308<sub>H</sub></td><td>000FFF08<sub>H</sub></td><td>45</td></tr>
</table>
</td></tr>
<tr><td>129</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 100pins.<br><br>(Error)<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>131</td><td>■Interrupt Vector Table</td><td>"42" is deleted as shown below from the interrupt factor in Interrupt vector 120pin.<br><br>(Error)<br>
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/42/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25 *3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25 *3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 120pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>133</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 120pins.<br><br>(Error)<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>135</td><td>■Interrupt Vector Table</td><td>"42" is deleted as shown below from the interrupt factor in Interrupt vector 144pin.<br><br>(Error)<br>
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/42/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25*3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25*3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>
</td></tr>
<tr><td>137</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 144pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>137</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 144pins.<br><br>(Error)<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 176pin modified as follows:<br><br>(Error)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45 *5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>141</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 176pins.<br><br>(Error)<br>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>142</td><td>■Electrical Characteristics<br>1. Absolute Maximum Ratings</td><td>The remarks of "L" level average output current" and "H" level average output current" modified as follows.<br><br>(Error)<br>
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">"L" level average output current *4</td><td>$I_{OLAV1}$</td><td>-</td><td>4</td><td>mA</td><td rowspan="2"></td></tr>
<tr><td>$I_{OLAV2}$</td><td>-</td><td>12</td><td>mA</td></tr>
<tr><td rowspan="2">"H" level average output current *4</td><td>$I_{OHAV1}$</td><td>-</td><td>-4</td><td>mA</td><td rowspan="2"></td></tr>
<tr><td>$I_{OHAV2}$</td><td>-</td><td>-12</td><td>mA</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Max</th></tr>
<tr><td rowspan="2">"L" level average output current *4</td><td>$I_{OLAV1}$</td><td>-</td><td>4</td><td>mA</td><td>*9</td></tr>
<tr><td>$I_{OLAV2}$</td><td>-</td><td>12</td><td>mA</td><td>*10</td></tr>
<tr><td rowspan="2">"H" level average output current *4</td><td>$I_{OHAV1}$</td><td>-</td><td>-4</td><td>mA</td><td>*9</td></tr>
<tr><td>$I_{OHAV2}$</td><td>-</td><td>-12</td><td>mA</td><td>*10</td></tr>
</table>
</td></tr>
<tr><td>143</td><td>■Electrical Characteristics<br>1. Absolute Maximum Ratings</td><td>The following note added.<br><br>(Correct)<br>*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.<br>*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 155 | ■Electrical Characteristics<br>AC Characteristics<br>(2) Reset Input | Added the At power-on*2 condition to the remarks in Reset input time. |
| 156 | ■Electrical Characteristics<br>AC Characteristics<br>(3) Power-on Conditions | Deleted the Slope detection undetected specification.<br>Added the Power ramp rate and C pin voltage at Power-on.<br>*1, *2: Changed the sentence.<br>Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on. |
| 6 to 11, 203 to 216 | ■Product lineup<br>■Ordering information | Package description modified to JEDEC description. |
| 47 | ■During Power-on | The following sentence modified as fdeleted from Interrupt<br>(Error)<br>To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.<br><br>(Correct)<br>To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on.<br>Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. |
| 49, 50 | ■Block Diagram | The following Block diagram modified as follows:<br>●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B<br>●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D<br>(Error)<br>CAN (2ch).<br><br>(Correct)<br>CAN (3ch) |
| 217 to 220 | ■Ordering Information | Added the following description.<br>■ORDERING INFORMATION MB91F52xxxD |
| 221 to 227 | ■Package Dimensions | Package Dimensions modified to JEDEC description. |

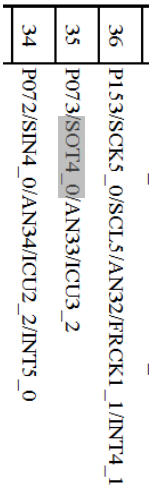
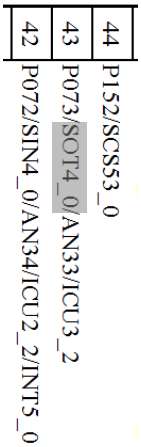
| Page | Section | Change Results |
|---|---|---|
| Rev *C | | |
| 2 | Features<br>Peripheral Functions | The following sentence modified in I2C as following:<br><br>(Error)<br>< I2C ><br>2 channels ch.3 , ch.4 Standard mode/high-speed mode supported.<br><br>Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported<br><br>(Correct)<br>< I2C ><br>2 channels ch.3 , ch.4 Standard mode/fast mode supported.<br><br>Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported |
| 5,6,7,8,9 ,10 | 1. Product Lineup | The following *2 added as follows:<br><br>(Error)<br>Power supply \| 2.7 V to 5.5 V<br><br>(Correct)<br>Power supply \| 2.7 V to 5.5 V *2 |
| 5,6,7,8,9 ,10 | 1. Product Lineup | The following sentence added as follows:<br><br>(Correct)<br>*2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).<br>This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).<br>Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector.<br>Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. |
| 8, 9, 10, | 1. Product Lineup | The following sentence modified in the bottom of Product lineup comparison table as following:<br><br>(Error)<br>*1: Only channel 3 and channel 4 support the I2C (high-speed mode/standard mode).<br><br>(Correct)<br>*1: Only channel 3 and channel 4 support the I2C (fast mode/standard mode). |
| 11 | 1. Product Lineup | Added silicon version E |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>46</td><td>■During Power-on</td><td>The following sentence modified as following:<br><br>(Error)<br>To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on.<br>Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.<br><br>(Correct)<br>To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.</td></tr>
<tr><td>142,143</td><td>11. Electrical Characteristics<br>Recommended operating conditions</td><td>The following sentence modified as following:<br><br>(Error)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset.<br><br>(Correct)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.<br>Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V).<br>This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V).<br>Between this detection voltage and the minimum operation guarantee voltage,<br>MCU functions are not guaranteed except for the low voltage detector.<br>Note that although the detection level is below the minimum operation guarantee voltage,<br>the LVD reset factor flag is set as the voltage drops below the detection level.</td></tr>
<tr><td>156, 157</td><td>11. Electrical Characteristics<br>AC Characteristics</td><td>Added (3-2) Power-on Conditions for MB91F52xxxE</td></tr>
<tr><td>184</td><td>11. Electrical Characteristics<br>AC Characteristics<br>(4-4) I2C timing</td><td>The following sentence modified as following:<br><br>(Error)<br><table><tr><th colspan="2">High-speed mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table><br>Notes: Only ch.3 and ch.4 are standard mode/high-speed mode correspondence.<br><br>*3: A high-speed mode I²C bus device can be used<br><br>(Correct)<br><table><tr><th colspan="2">Fast mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table><br>Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence.<br><br>*3: A fast mode I²C bus device can be used</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>187</td><td>11. Electrical Characteristics<br>(8) Low voltage detection (External low-voltage detection)</td><td>The following sentence modified in the Detection voltage as following:<br><br>(Error)<br>
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr>
<tr><td>-8%</td><td>2.8</td><td>+8%</td><td>V</td><td>When power-supply voltage falls and detection level is set initially</td></tr>
</table>
<br>(Correct)<br>
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr>
<tr><td>-8%</td><td>LVD5F_SEL[3:0]</td><td>+8%</td><td>V</td><td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td></tr>
</table>
</td></tr>
<tr><td>188</td><td>11. Electrical Characteristics<br>(9) Low voltage detection (RAM retention low-voltage detection)</td><td>The following sentence modified as following:<br><br>(Error)<br>(9) Low voltage detection (Internal low-voltage detection)<br><br>(Correct)<br>(9) Low voltage detection (RAM retention low-voltage detection)</td></tr>
<tr><td>220 to 223</td><td>16. Ordering Information</td><td>Added the following description.<br>■ORDERING INFORMATION MB91F52xxxE</td></tr>
<tr><td>Rev *D</td><td></td><td></td></tr>
<tr><td>1</td><td>Features</td><td>The following sentence should be modified as follows:<br><br>(Error)<br>Conversion time : 1µs<br><br>(Correct)<br>Conversion time : 1.4µs</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| 5,6,7,8,9,10 | 1. Product Lineup | The following sentence should be modified as follows:<br><br>(Error)<br>*2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.<br><br>(Correct)<br>*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting<br>and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation<br>voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum<br>guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD. |
| 142,143 | 11. Electrical Characteristics Recommended operating conditions | The following sentence should be modified as follows:<br><br>(Error)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.<br>Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.<br><br>(Correct)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.<br>The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting<br>and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD. |
| 146 | 11. Electrical Characteristics DC Characteristics | Pin name of $R_{UP3}$ should be modified as follows:<br><br>(Error)<br>Port pin other than P035,041,093,122<br><br>(Correct)<br>Port pin other than P035,041,073,074,076,077,093,122 |

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>187</td><td>11. Electrical Characteristics<br>(8) Low voltage detection<br>(External low-voltage detection)</td><td>Note of Detection voltage should be added as follows:<br><br>(Correct)<br>Detection voltage *3<br><br>*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</td></tr>
<tr><td>188</td><td>11. Electrical Characteristics<br>(9) Low voltage detection<br>(Internal low-voltage detection)</td><td>The following sentence modified as following:<br><br>(Error)<br>(9) Low voltage detection (RAM retention low-voltage detection)<br><br>(Correct)<br>(9) Low voltage detection (Internal low-voltage detection)</td></tr>
<tr><td></td><td></td><td>The following symbol should be modified as follows:<br><br>(Error)<br>*<br><br>(Correct)<br>*1</td></tr>
<tr><td></td><td></td><td>Note of Detection voltage should be added as follows:<br><br>(Correct)<br>Detection voltage *2<br><br>*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</td></tr>
<tr><td>233 to 235</td><td>18. Errata</td><td>Limitation for Watch mode (power off) should be added in Errata.</td></tr>
<tr><td>Rev *F</td><td></td><td></td></tr>
<tr><td>222</td><td>16. Ordering Information<br>MB91F52xxxE</td><td>The shading part added as below.<br><br>
<table>
<tr><th>Part number</th><th>Sub clock</th><th>CSV Initial value</th><th>LVD Initial value</th><th>Package*</th></tr>
<tr><td>MB91F526LSEPMC</td><td rowspan="3">None</td><td>ON</td><td>ON</td><td rowspan="3">LQP・176 pin, Plastic</td></tr>
<tr><td>MB91F526LHEPMC</td><td>OFF</td><td>ON</td></tr>
<tr><td>MB91F526LKEPMC</td><td>OFF</td><td>OFF</td></tr>
</table>
</td></tr>
</table>

| Page | Section | Change Results |
|---|---|---|
| Rev *G | | |
| - | Marketing Part Numbers changed from an MB prefix to a CY prefix. | |
| Rev *H | | |
| 13 | 2. Pin Assignment | The shading part added for LQH080 as below.<br>  |
| 14 | 2. Pin Assignment | The shading part added for LQI100 as below.<br>  |
| 217 | 16. Ordering Information<br>CY91F52xxxE | The shading part modified as below.<br>Error)<br>LQE・64 pin, Plastic<br><br>Correct)<br>LQD・64 pin, Plastic |

## Document History

**Document Title: CY91520 Series 32-bit FR81S Microcontroller**
**Document Number: 002-04662**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | – | – | – | Initial release |
| ** | – | – | 2/20/2014 | Features:<br>Corrected the following description.<br>5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 Automotive input<br>↓<br>5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input<br><br>I/O CIRCUIT TYPE:<br>Corrected the following description to "Type F, G, I, J, K, M".<br>Schmitt input → CMOS hysteresis input<br>Corrected the following description to "Type D, E".<br>$I^2C$ Schmitt input → $I^2C$ hysteresis input<br><br>Block Diagram<br>Corrected the following description.<br>• MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B<br>• MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D<br>• MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F<br>• MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J<br>• MB91F522K, MB91F523K, MB91F524K, MB91F525K, MB91F526K<br>• MB91F522L, MB91F523L, MB91F524L, MB91F525L, MB91F526L<br><br>Electrical Characteristics<br>2. Recommended operating conditions:<br>*1 : When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset<br><br>Electrical Characteristics<br>3.DC characteristics<br>Corrected the value of "ICCT5 When using sub clock 32kHz TA=+25°C<br>". Max 1420µA → Max 2000µA<br>Corrected the value of "Power supply voltage range".<br>(TA:-40°C to +105°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V)<br>↓<br>($T_A$:-40°C to +105°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,$V_{SS}$=$AV_{SS}$=0.0V)<br>Corrected the value of "Power supply voltage range".<br>($T_A$:-40°C to +125°C,Vcc=AVcc=2.7V to 5.5V,VSS=AVSS=0.0V)<br>↓<br>($T_A$:-40°C to +125°C,Vcc=AVcc=5.0V±10%/3.3V±0.3V,$V_{SS}$=$AV_{SS}$=0.0V)<br>Corrected the value of " Pull-up resistance $R_{UP1}$".<br>Vcc=3.3V±0.3V Min 49 Max 140 →Min 45 Max 140<br>Corrected the following description.<br>Pull-up resistance $R_{UP2}$<br>Port pin other than P035,041,093,122 → P073,074,076,077<br>Corrected the value of " Pull-up resistance $R_{UP2}$". |

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | VCC=5.0V±10% Min 25 Max 100 →Min 25 Max 60<br>VCC=3.3V±0.3V Min 49 Max 140 →Min 33 Max 90<br>Added the value of " Pull-up resistance $R_{UP3}$".<br>Pin name : Port pin other than P035,041,073,074,076,077,093,122<br>VCC=5.0V±10% Min 25 Max 100<br>VCC=3.3V±0.3V Min 45 Max 140<br><br>Electrical Characteristics<br>4. AC characteristics<br>(4) Multi-function Serial<br>(4-1) CSIO timing<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4)<br>(4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVI}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min -30 Max 30<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min -30 Max 30<br>Pin name: SCK3,SCK4<br>SOT3,SOT4<br>Value: Min -300 Max 300<br>(4-1-1),(4-1-4)Valid SIN⇒SCK↑ setup time $t_{IVSHI}$<br>(4-1-2),(4-1-3)Valid SIN⇒SCK↓ setup time $t_{IVSLI}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11 SIN0 to SIN11<br>Value: Min 34 Max -<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11 SIN0 to SIN2,SIN5 to SIN11<br>Value: Min 34 Max -<br>Pin name: SCK3,SCK4,SIN3,SIN4<br>Value: Min 300 Max –<br>(4-1-1),(4-1-4)SCK↓⇒SOT delay time $t_{SLOVE}$<br>(4-1-2),(4-1-3)SCK↑⇒SOT delay time $t_{SHOVE}$<br>Corrected the following description.<br>Pin name: SCK0 to SCK11<br>SOT0 to SOT11<br>Value: Min - Max 33<br>↓<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>SOT0 to SOT2,SOT5 to SOT11<br>Value: Min - Max 33<br>Pin name: SCK3,SCK4 SOT3,SOT4<br>Value: Min - Max 300<br>(4-1-1),(4-1-2),(4-1-3),(4-1-4)SCK fall time $t_F$<br>Corrected the following description.<br>Pin name: SCK0 to SCK2,SCK5 to SCK11<br>Value: Min - Max 5<br>Pin name: SCK3,SCK4<br>Value: Min - Max 250<br>↓<br>Pin name: SCK0 to SCK11 |

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | Value: Min - Max 5<br>(4-1-5)SCS↓⇒SCK↓ setup time $t_{CSSI}$<br>(4-1-6)SCS↓⇒SCK↑ setup time $t_{CSSI}$<br>(4-1-7)SCS↑⇒SCK↓ setup time $t_{CSSI}$<br>(4-1-8)SCS↑⇒SCK↑ setup time $t_{CSSI}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSSU}$+0 Max $t_{CSSU}$+50<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSSU}$-50 Max $t_{CSSU}$+0<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $t_{CSSU}$-50 Max $t_{CSSU}$+300<br>(4-1-5)SCK↑⇒SCS↑hold time $t_{CSHI}$<br>(4-1-6)SCK↓⇒SCS↑hold time $t_{CSHI}$<br>(4-1-7)SCK↑⇒SCS↓hold time $t_{CSHI}$<br>(4-1-8)SCK↓⇒SCS↓hold time $t_{CSHI}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-50 Max $t_{CSHD}$+0<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $t_{CSHD}$-10 Max $t_{CSHD}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $t_{CSHD}$-300 Max $t_{CSHD}$+50<br>(4-1-5),(4-1-6)SCS↓⇒SOT delay time $t_{DSE}$<br>(4-1-7),(4-1-8)SCS↑⇒SOT delay time $t_{DSE}$<br>Corrected the following description.<br>Pin name: SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>SOT1 to SOT11<br>Value: Min - Max 40<br>↓<br>Pin name: SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,<br>SCS8 to SCS11<br>SOT1,SOT2,SOT5 to SOT11<br>Value: Min - Max 40<br>Pin name: SCS3,SCS40 to SCS43<br>SOT3,SOT4<br>Value: Min - Max 300<br>(4-1-5)SCK↓⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-6)SCK↑⇒SCS↓ clock switch time $t_{SCC}$<br>(4-1-7)SCK↓⇒SCS↑ clock switch time $t_{SCC}$<br>(4-1-8)SCK↑⇒SCS↑ clock switch time $t_{SCC}$<br>Corrected the following description.<br>Pin name: SCK1 to SCK11<br>SCS1 to SCS3,SCS40 to SCS43,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11 |

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | Value: Min $3t_{CPP}$+0 Max $3t_{CPP}$+50<br>↓<br>Pin name: SCK1,SCK2,SCK5 to SCK11<br>SCS1,SCS2,SCS50 to SCS53,SCS60 to SCS63,SCS70 to SCS73,SCS8 to SCS11<br>Value: Min $3t_{CPP}$-10 Max $3t_{CPP}$+50<br>Pin name: SCK3,SCK4 SCS3,SCS40 to SCS43<br>Value: Min $3t_{CPP}$-300 Max $3t_{CPP}$+50<br>Added the following description.<br>Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again<br><br>Electrical Characteristics<br>5.A/D Converter<br>(1) 12-bit A/D Converter Electrical Characteristics:<br>Added the value of "Total error".<br>Total error value Min – Typ – Max ±12 LSB<br>Corrected the value of "Zero transition voltage".<br>Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV<br>↓<br>Min AVRL-11.5LSB Max AVRL+12.5LSB<br>Corrected the value of "Full-scale transition voltage".<br>Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV<br>↓<br>Min AVRH-13.5LSB Max AVRH+10.5LSB<br>Added the following description.<br>Parameter : Power supply current $I_A$ AVCC*3<br>*3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.<br><br>Electrical Characteristics<br>7.D/A Converter:<br>Added the following description.<br>Parameter : Power supply current *1<br>*1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter.<br><br>Electrical Characteristics<br>6.Flash memory:<br>Parameter: Erase cycle*2/Data retain time<br>Deleted the following description.<br>Remarks :<br>"Temperature at writing/erasing Tj<+105°C"<br><br>Electrical Characteristics<br>7.D/A Converter:<br>Corrected the following description.<br>Parameter : Power supply current<br>Symbol IA Pin name $AV_{CC}$<br>Symbol IAH Pin name $AV_{CC}$<br>↓<br>Symbol IA Pin name AVCC |

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| | | | | Symbol IAH Pin name AVCC<br><br>Example Characteristics<br>Corrected the following description.<br>Watch mode<br><br>Ordering Information<br>Corrected the following description.<br>• ORDERING INFORMATION<br>↓<br>• ORDERING INFORMATION MB91F52xxxB*1<br>Package<br>↓<br>Package*2<br>Added the following description.<br>*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.<br>Corrected the following description.<br>For details of the package, see "■ PACKAGE DIMENSIONS ".<br>↓<br>*2: For details of the package, see "■ PACKAGE DIMENSIONS ".<br>Added the following description.<br>• ORDERING INFORMATION MB91F52xxxC<br>Company name and layout design change |
| *A | 4999456 | JHMU | 11/13/2015 | Updated to Cypress template.<br>Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in “Absolute Maximum Ratings” of “ELECTRICAL CHARACTERISTICS”.<br>*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.<br>*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.<br>Added Errata section. |
| *B | 5112138 | KUME | 01/28/2016 | Fixed some clerical errors.<br>For details, please see the chapter 18. Major Changes. |
| *C | 5196285 | KUME | 04/28/2016 | For details, please see the chapter 19. Major Changes. |
| *D | 5318862 | KUME | 06/23/2016 | For details, please see the chapter 19. Major Changes. |
| *E | 5711679 | AESATMP7 | 04/25/2017 | Updated Cypress Logo and Copyright. |
| *F | 5984090 | KUME | 12/05/2017 | For details, please see the chapter 19. Major Changes. |
| *G | 5990912 | KUME | 12/12/2017 | Marketing Part Numbers changed from an MB prefix to a CY prefix. |
| *H | 6216567 | KUME | 06/25/2018 | Fixed LQD064 package for Ordering Information CY91F52xxxE.<br>For details, please see the chapter 19. Major Changes. |

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