

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) DIPs

description

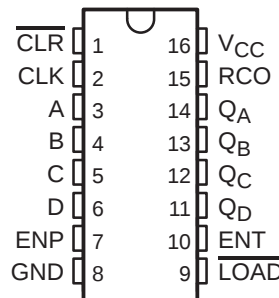
These synchronous, presettable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they can be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

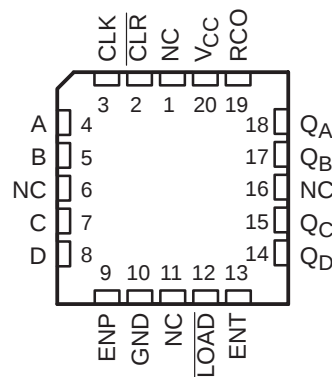
The clear function for the 'ALS161B and 'AS161 devices is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, LOAD, or enable inputs. The clear function for the SN54ALS162B, 'ALS163B, and 'AS163 devices is synchronous, and a low level at CLR sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{\text{CLR}}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled,

SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 ... J PACKAGE
SN74ALS161B, SN74AS161,
SN74AS163 ... D OR N PACKAGE
SN74ALS163B ... D, DB, OR N PACKAGE
(TOP VIEW)



SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

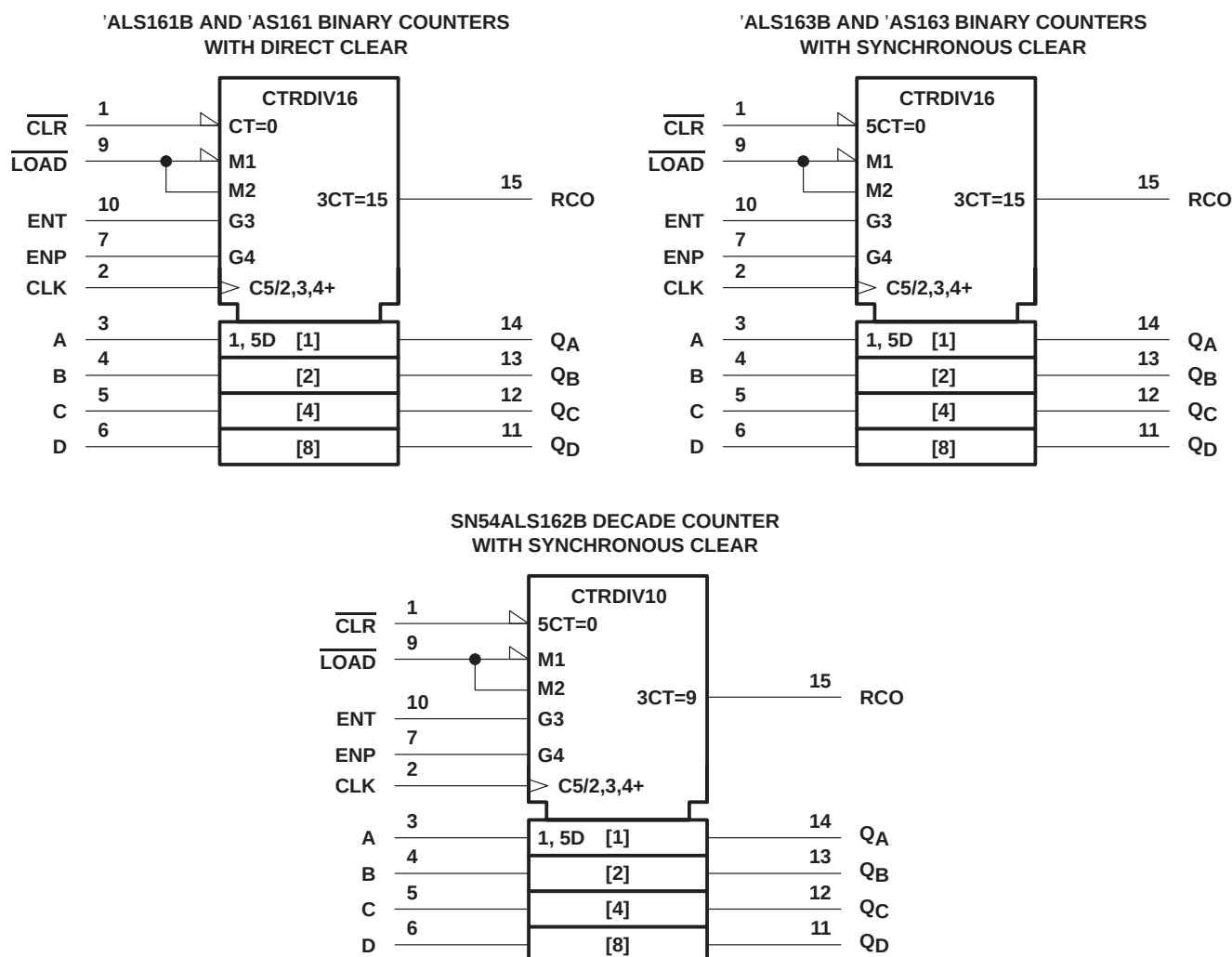
description (continued)

produces a high-level pulse while the count is maximum (9 or 15, with Q_A high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from 0°C to 70°C .

logic symbols†

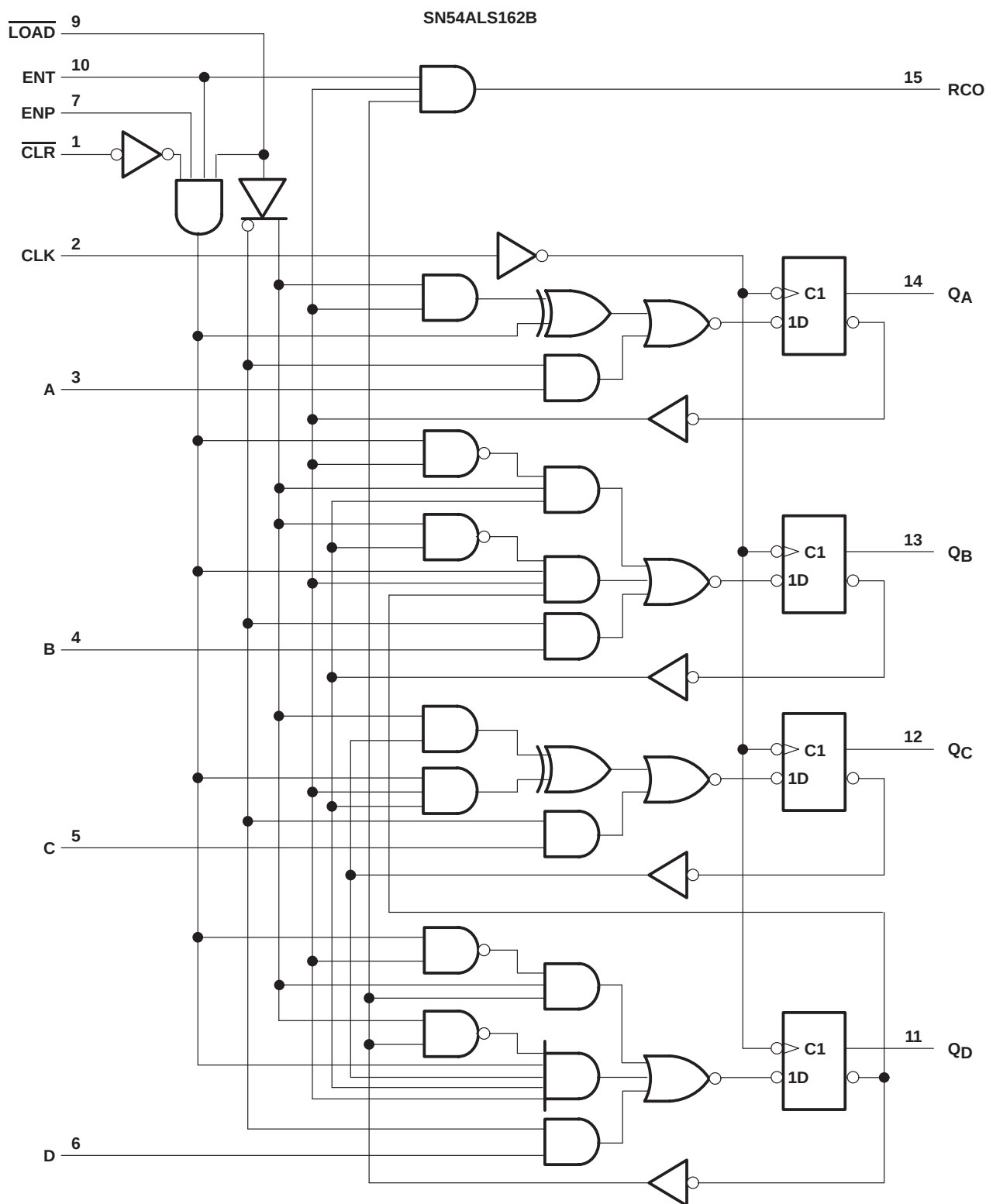


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, and N packages.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

logic diagram (positive logic)

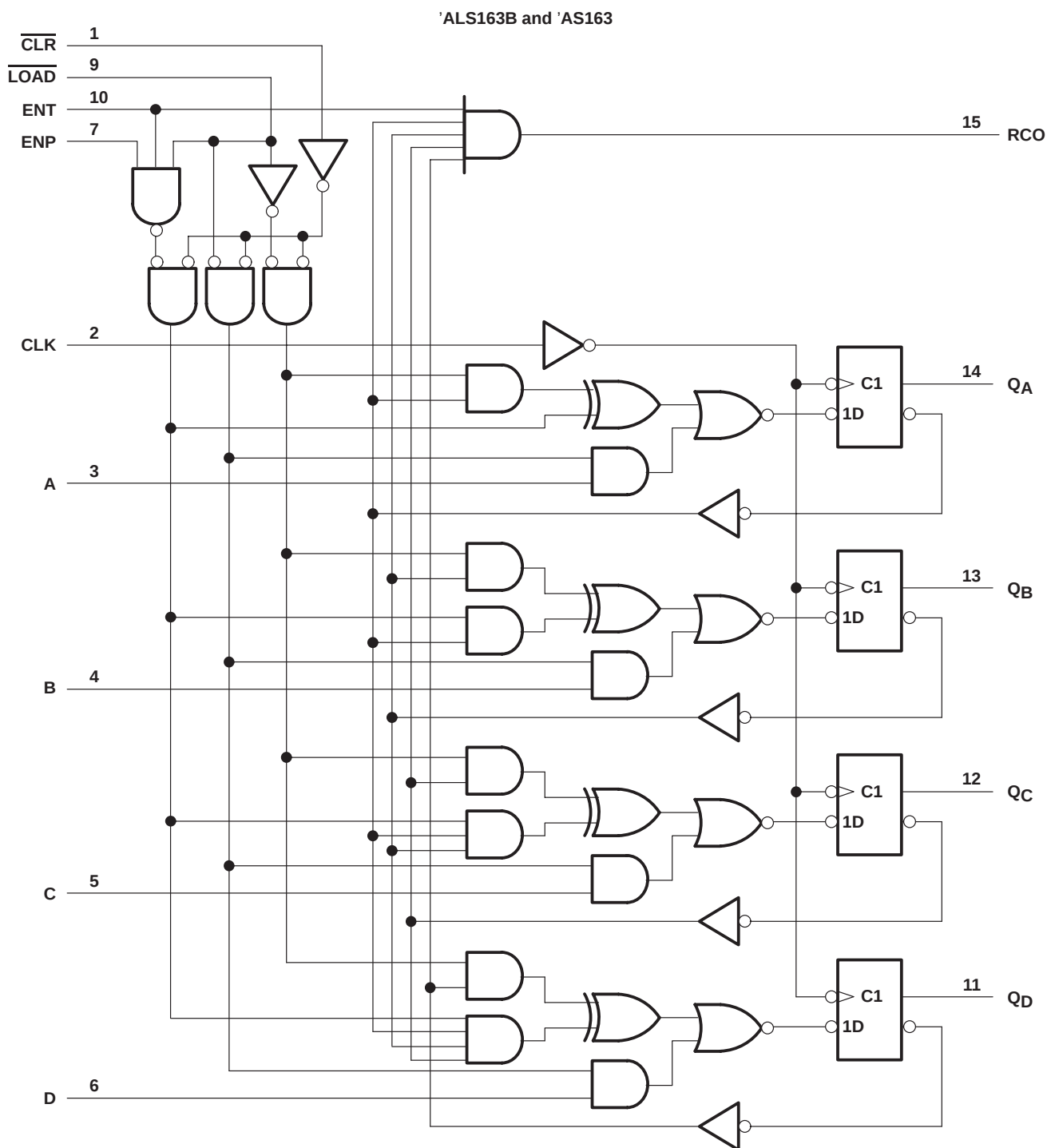


Pin numbers shown are for the J package.

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.

'ALS161B and 'AS161 synchronous binary counters are similar; however, $\overline{\text{CLR}}$ is asynchronous.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

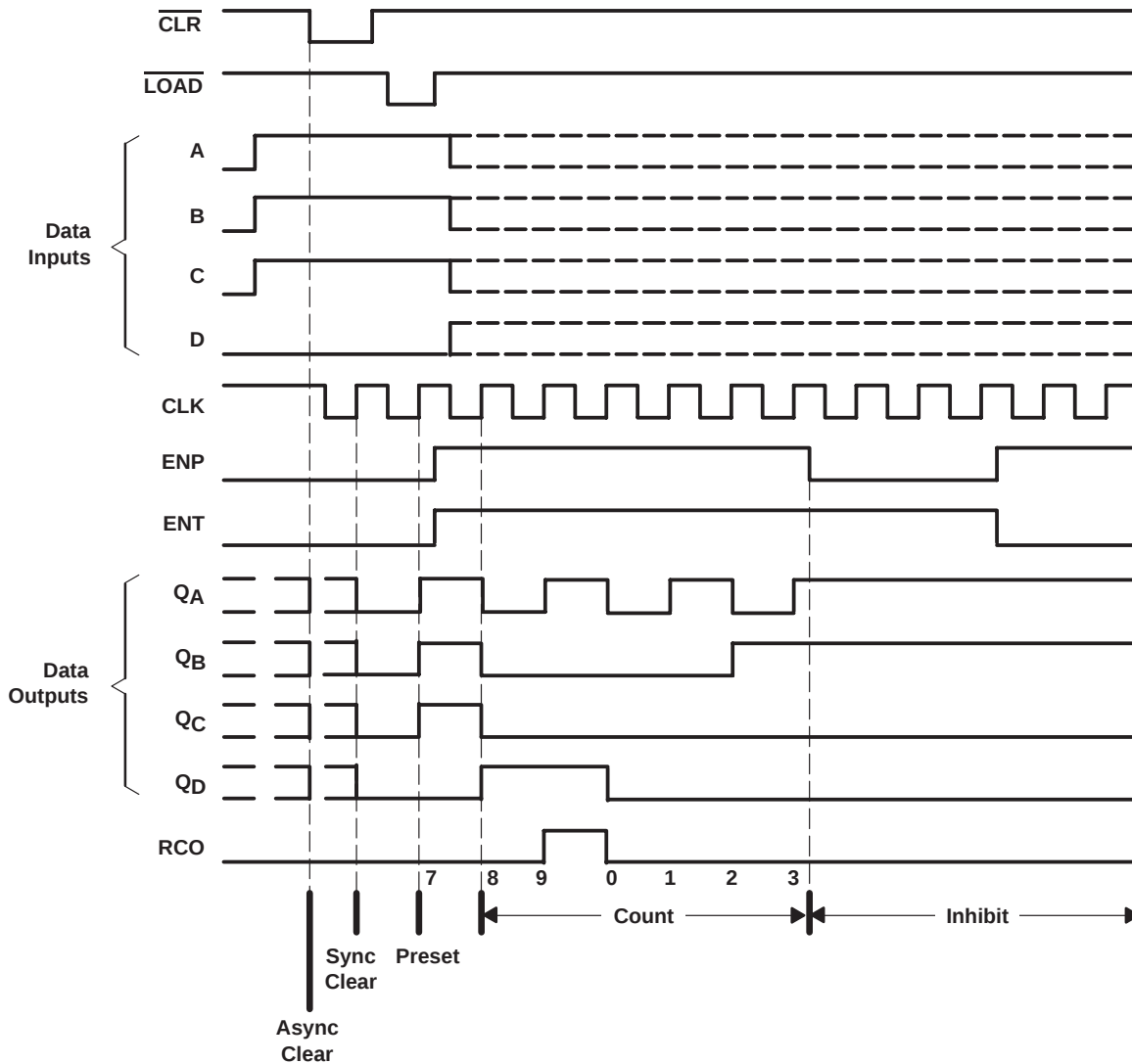
SDAS276A – DECEMBER 1994 – REVISED JULY 2000

typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

1. Clear outputs to zero (SN54ALS162B is synchronous)
2. Preset to BCD 7
3. Count to 8, 9, 0, 1, 2, and 3
4. Inhibit



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

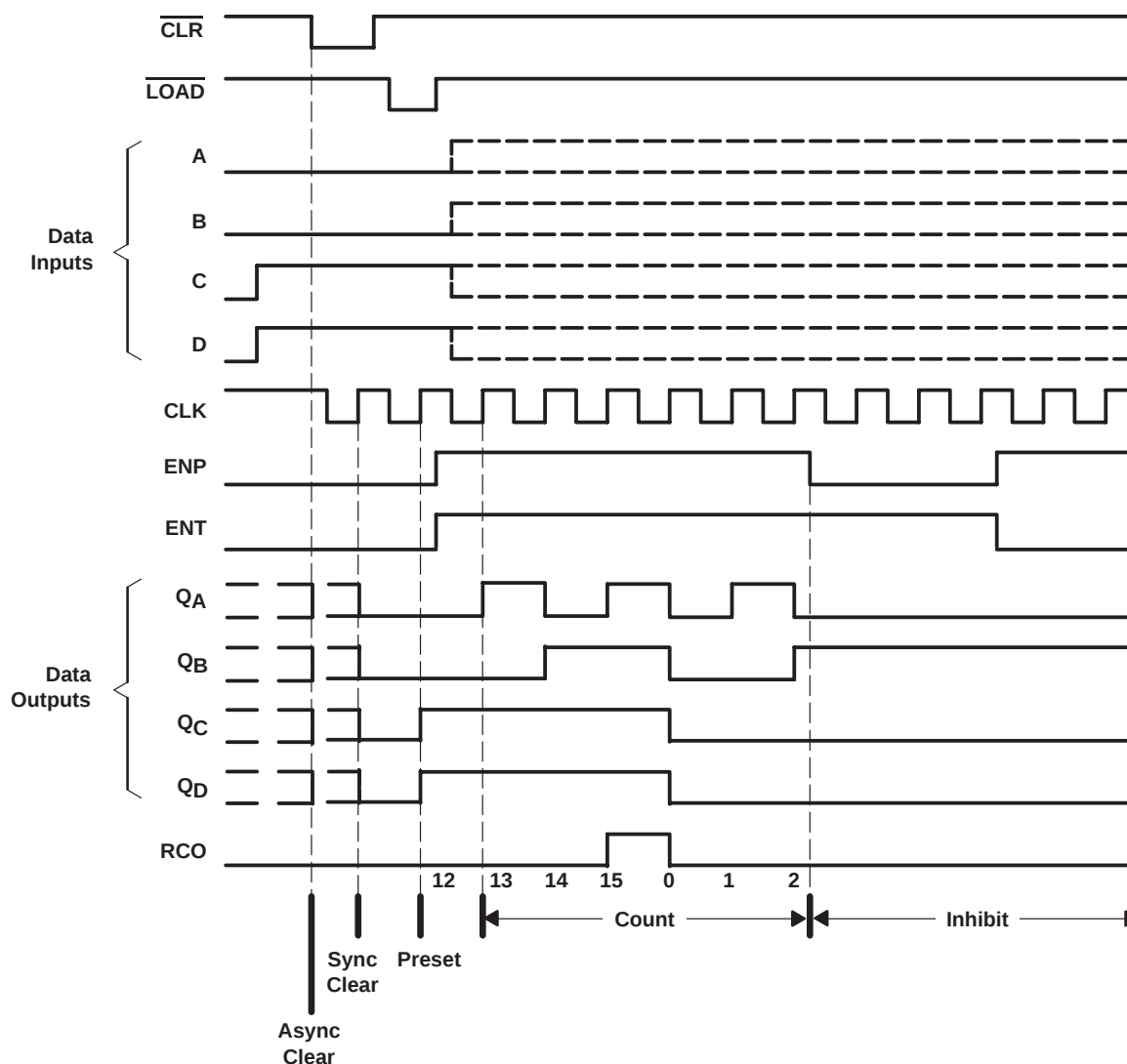
SDAS276A – DECEMBER 1994 – REVISED JULY 2000

typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, and 'AS163

The following sequence is illustrated below:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous.)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I	–0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.5			–1.5	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 4$ mA	0.25		0.4	0.25		0.4	V
		$I_{OL} = 8$ mA				0.35		0.5	
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.2			–0.2	mA
$I_{O}^{\S}$	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–20		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V			12	21		12	21	mA

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

				SN54ALS161B SN54ALS162B SN54ALS163B		SN74ALS161B SN74ALS163B		UNIT			
				MIN	MAX	MIN	MAX				
f _{clock}	Clock frequency			22		40		MHz			
t _w	Pulse duration		CLR high or low		20		12.5		ns		
			'ALS161B	CLR low	20		15				
t _{su}	Setup time, before CLK↑		A, B, C, D		50		15		ns		
			LOAD		20		15				
			ENP, ENT		'ALS161B		25			15	
					SN54ALS162B, 'ALS163B		20			15	
			'ALS161B		CLR inactive		10			10	
			SN54ALS162B, 'ALS163B		CLR low		20			15	
					CLR high		20			10	
t _h	Hold time, all synchronous inputs after CLK↑			0		0		ns			

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS161B		SN74ALS161B		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			22		40		MHz
t _{PLH}	CLK	RCO	5	34	5	20	ns
t _{PHL}			5	27	5	20	
t _{PLH}	CLK	Any Q	4	19	4	15	ns
t _{PHL}			6	25	6	20	
t _{PLH}	ENT	RCO	3	18	3	13	ns
t _{PHL}			3	17	3	13	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	8	27	8	24	ns
		RCO	11	32	11	23	

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS162B SN54ALS163B		SN74ALS163B		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			22		40		MHz
t _{PLH}	CLK	RCO	5	25	5	20	ns
t _{PHL}			5	25	5	20	
t _{PLH}	CLK	Any Q	4	18	4	15	ns
t _{PHL}			6	25	6	20	
t _{PLH}	ENT	RCO	3	16	3	13	ns
t _{PHL}			3	16	3	13	



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

recommended operating conditions

		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–2			–2	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = –18 mA			–1.2			–1.2	V
V _{OH}		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = –2 mA	V _{CC} – 2			V _{CC} – 2			V
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I _I	LOAD	V _{CC} = 5.5 V,	V _I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All others					0.1			0.1	
I _{IH}	LOAD	V _{CC} = 5.5 V,	V _I = 2.7 V			60			60	μA
	ENT					40			40	
	All others					20			20	
I _{IL}	LOAD	V _{CC} = 5.5 V,	V _I = 0.4 V			–1.5			–1.5	mA
	ENT					–1			–1	
	All others					–0.5			–0.5	
I _O ‡		V _{CC} = 5.5 V,	V _O = 2.25 V	–30		–112	–30		–112	mA
I _{CC}		V _{CC} = 5.5 V			35	53		35	53	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

timing requirements over recommended operating conditions (see Figure 1)

				SN54AS161 SN54AS163		SN74AS161 SN74AS163		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			65		75		MHz
t _w	Pulse duration	$\overline{\text{CLR}}$ high or low		7.7		6.7		ns
		'AS161	$\overline{\text{CLR}}$ low	10		8		
t _{su}	Setup time, before CLK↑	A, B, C, D		10		8		ns
		$\overline{\text{LOAD}}$		10		8		
		ENP, ENT		10		8		
		'AS161	$\overline{\text{CLR}}$ inactive	10		8		
		'AS163	$\overline{\text{CLR}}$ low	14		12		
			$\overline{\text{CLR}}$ high (inactive)	10		9		
t _h	Hold time, all synchronous inputs after CLK↑			2		0		ns

switching characteristics over recommended operating conditions (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS161		SN74AS161		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			65*		75		MHz
t _{PLH}	CLK	RCO (with LOAD high)	1	8.5	1	8	ns
		RCO (with LOAD low)	3	17.5	3	16.5	
t _{PHL}	CLK	RCO	2	14	2	12.5	ns
t _{PLH}	CLK	Any Q	1	7.5	1	7	ns
t _{PHL}			2	14	2	13	
t _{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t _{PHL}			1	9.5	1	8.5	
t _{PHL}	CLR	Any Q	2	14	2	13	ns
		RCO	2	14	2	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating conditions (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS163		SN74AS163		UNIT
			MIN	MAX	MIN	MAX	
f _{max}			65*		75		MHz
t _{PLH}	CLK	RCO (with LOAD high)	1	8.5	1	8	ns
		RCO (with LOAD low)	3	17.5	3	16.5	
t _{PHL}	CLK	RCO	2	14	2	12.5	ns
t _{PLH}	CLK	Any Q	1	7.5	1	7	ns
t _{PHL}			2	14	2	13	
t _{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t _{PHL}			1	9.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

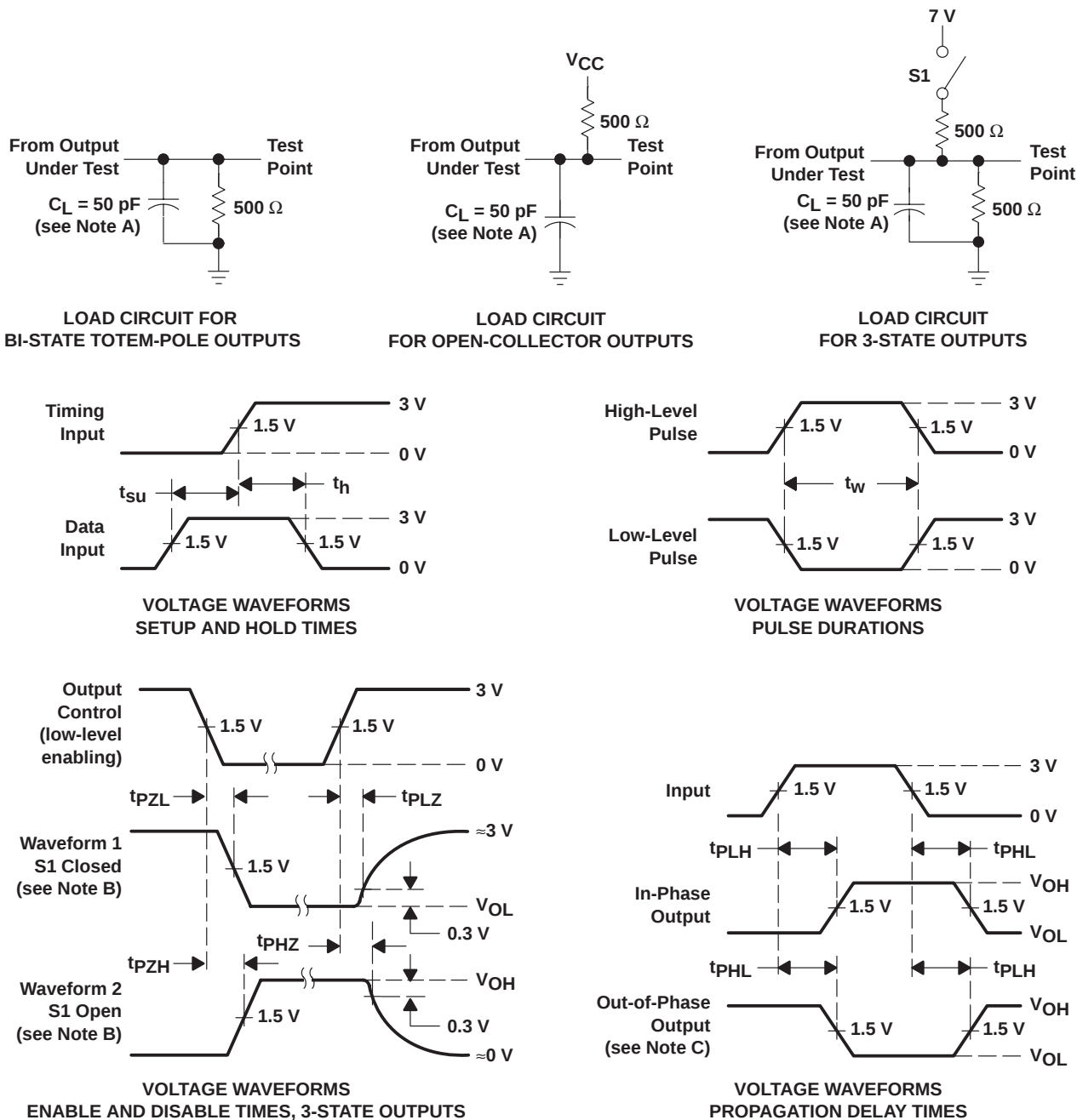


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

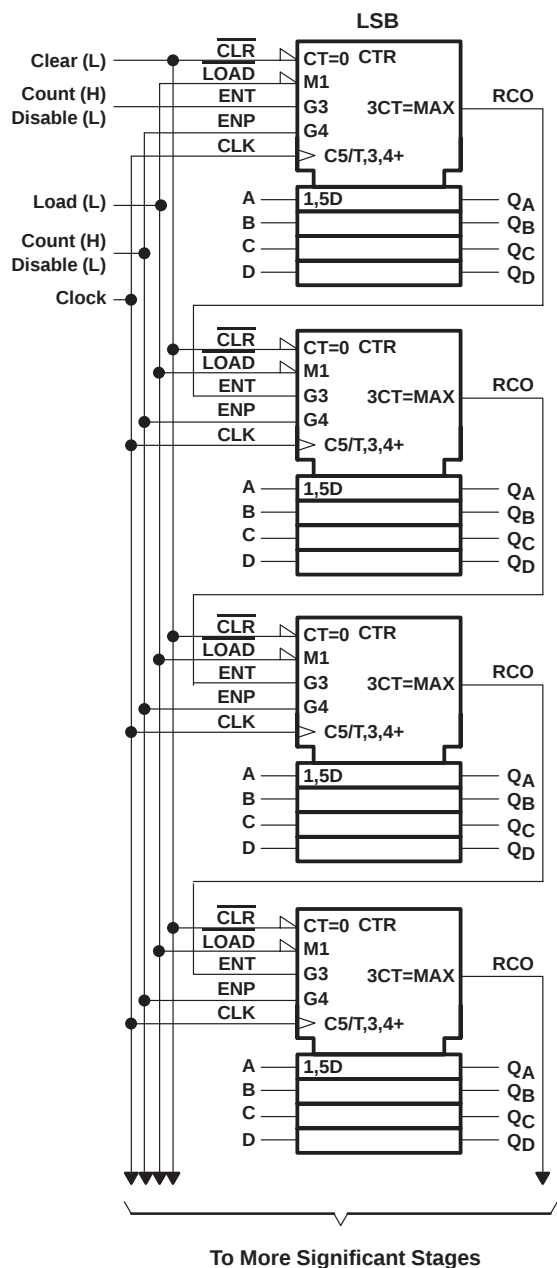
SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

APPLICATION INFORMATION

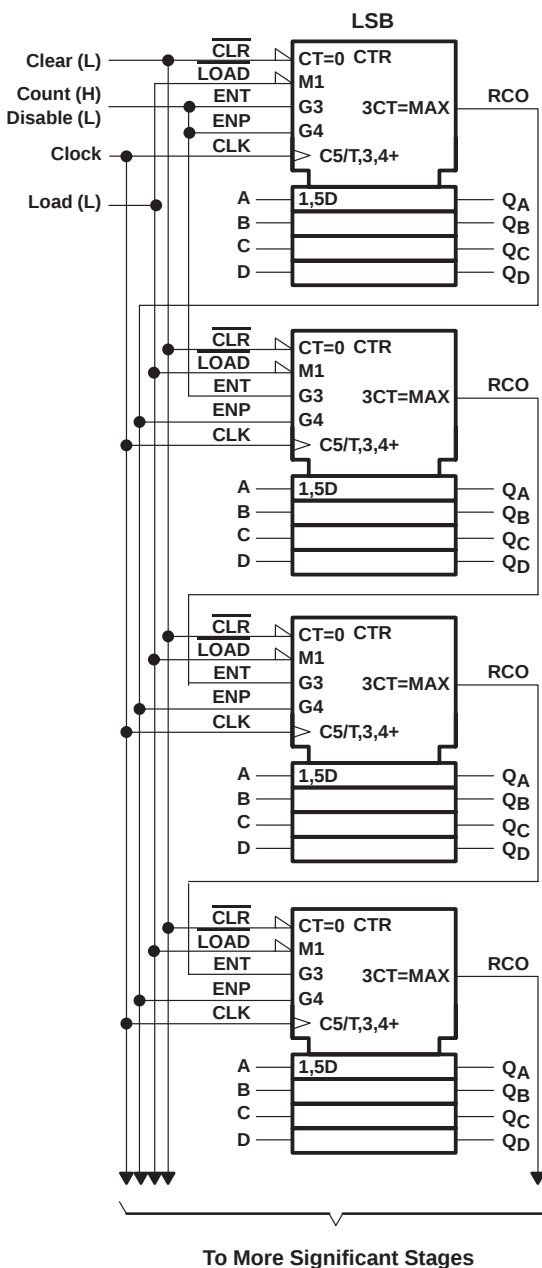
n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 2) and the carry look-ahead circuit (see Figure 3) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The 'ALS161B, 'AS161, 'ALS163B, and 'AS163 devices count in binary. When additional stages are added, the $f_{\max}$ decreases in Figure 2, but remains unchanged in Figure 3.



$$f_{\max} = 1/(\text{CLK to RCO } t_{\text{PLH}}) + (\text{ENT to RCO } t_{\text{PLH}}) (N - 2) + (\text{ENT } t_{\text{su}})$$

Figure 2. Ripple-Mode Carry Circuit



$$f_{\max} = 1/(\text{CLK to RCO } t_{\text{PLH}}) + (\text{ENP } t_{\text{su}})$$

Figure 3. Carry Look-Ahead Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
83022012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302201EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8302201FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
83022022A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8302202EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
8302202FA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	
JM38510/38001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/38001BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
JM38510/38002B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/38002BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/38001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/38001BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
M38510/38002B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/38002BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54ALS161BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54ALS163BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54AS163J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	
SN74ALS161BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS161BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74ALS161BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS161BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS161BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS163BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74ALS163BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS163BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS163BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS161N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS161NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS161NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS161NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AS161NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS163D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS163DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS163DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS163N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS163NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNJ54ALS161BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS161BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS161BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS163BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS163BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54AS161FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS161J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54AS163J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS161B, SN54ALS163B, SN54AS161, SN54AS163, SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 :

- Catalog: [SN74ALS161B](#), [SN74ALS163B](#), [SN74AS161](#), [SN74AS163](#)
- Military: [SN54ALS161B](#), [SN54ALS163B](#), [SN54AS161](#), [SN54AS163](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS161BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS161BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ALS163BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS163BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS161NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS161BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS161BNSR	SO	NS	16	2000	367.0	367.0	38.0
SN74ALS163BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS163BNSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AS161NSR	SO	NS	16	2000	367.0	367.0	38.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

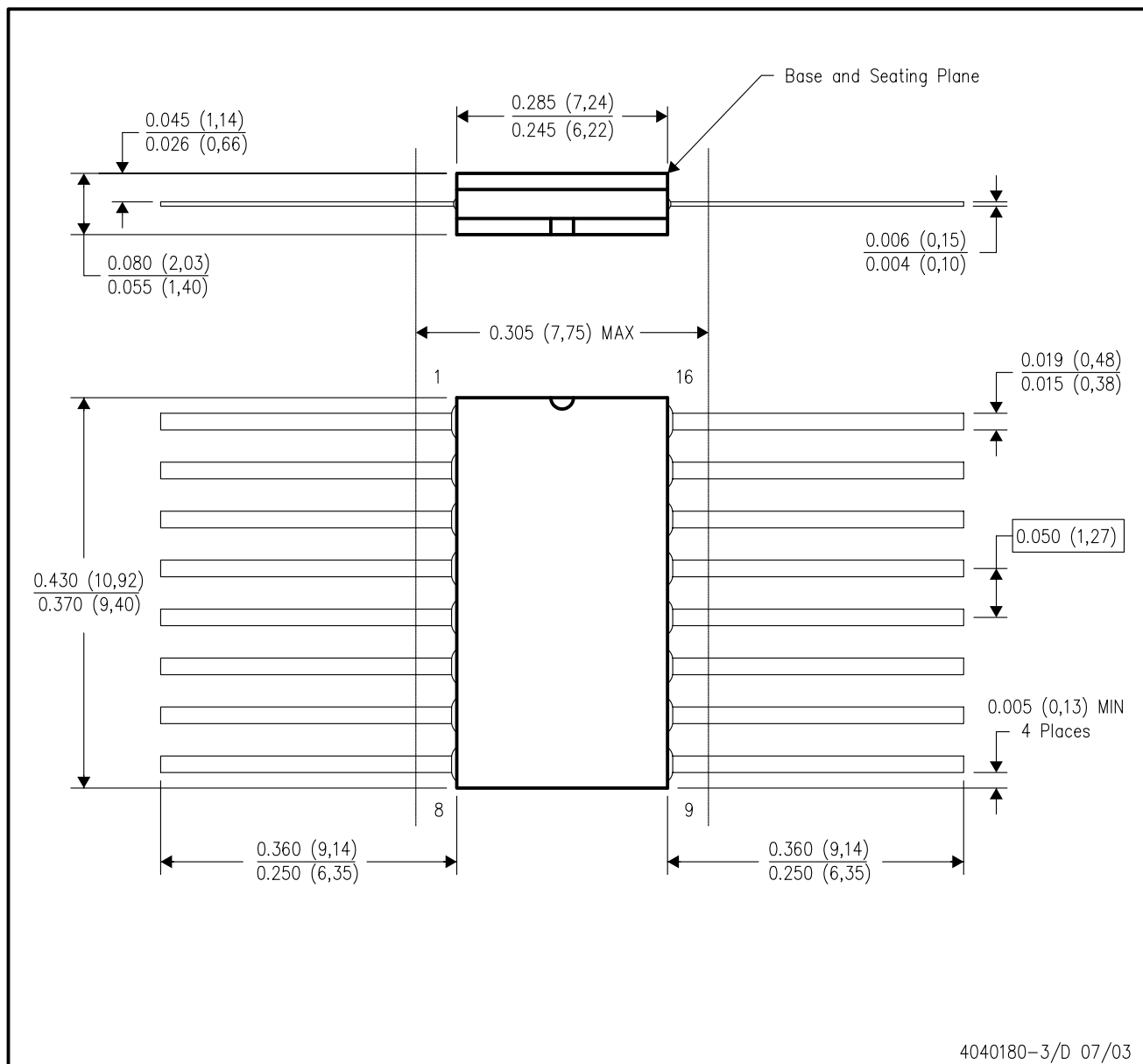


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9