To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT2140H

Silicon N Channel Power MOS FET
Power Switching

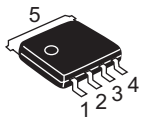
REJ03G1192-0400
(Previous: ADE-208-1581B)
Rev.4.00
Sep 07, 2005

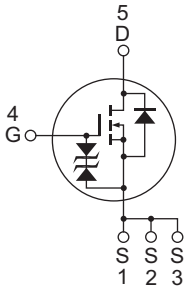
Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS\ (on)}$ = 12.5 mΩ typ. (at V_{GS} = 10 V)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)





1, 2, 3	Source
4	Gate
5	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	25	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} Note 3	25	A
Avalanche energy	E_{AR} Note 3	62.5	mJ
Channel dissipation	Pch Note 2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Tc = 25 °C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

(Ta = 25°C)

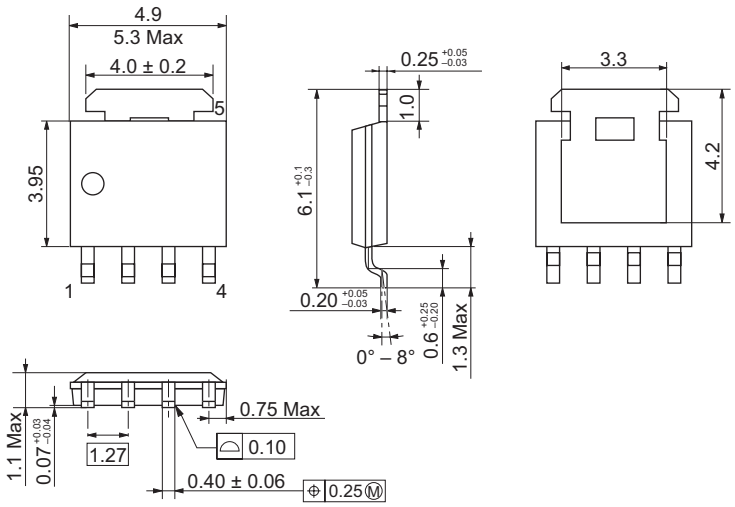
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	2.0	—	3.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS\ (on)}$	—	12.5	16.0	mΩ	I_D = 12.5 A, V_{GS} = 10 V Note 4
	$R_{DS\ (on)}$	—	13.5	18.0	mΩ	I_D = 12.5 A, V_{GS} = 7 V Note 4
Forward transfer admittance	$\|y_{fs}\|$	27	45	—	S	I_D = 12.5 A, V_{DS} = 10 V Note 4
Input capacitance	Ciss	—	6500	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	210	—	pF	f = 1 MHz
Total gate charge	Qg	—	105	—	nC	V_{DD} = 50 V
Gate to source charge	Qgs	—	20	—	nC	V_{GS} = 10 V
Gate to drain charge	Qgd	—	22	—	nC	I_D = 25 A
Turn-on delay time	$t_{d\ (on)}$	—	25	—	ns	V_{GS} = 10 V, I_D = 12.5 A
Rise time	t_r	—	24	—	ns	V_{DD} ≅ 30 V
Turn-off delay time	$t_{d\ (off)}$	—	100	—	ns	R_L = 2.4 Ω
Fall time	t_f	—	12	—	ns	Rg = 4.7 Ω
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	I_F = 25 A, V_{GS} = 0 Note 4
Body-drain diode reverse recovery time	t_{rr}	—	55	—	ns	I_F = 25 A, V_{GS} = 0 di_F/dt = 100 A/µs

Note: 4. Pulse test

Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-100	PTZZ0005DA-A	LFPAK	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part Name	Quantity	Shipping Container
HAT2140H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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