

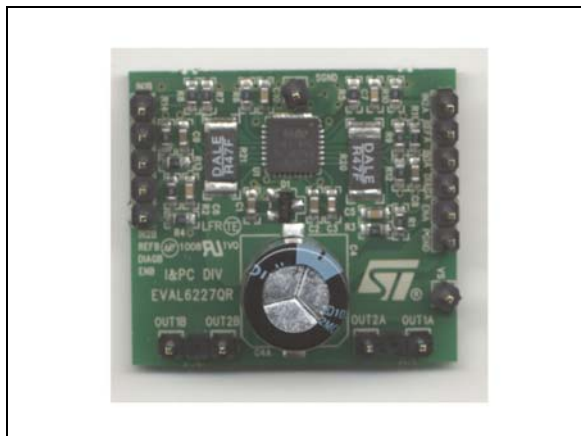


## Demonstration board mounting the L6227Q dual full-bridge driver

Data brief

### Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A DC)
- $R_{DS(on)}$  0.73  $\Omega$  typ. value @  $T_J = 25^\circ\text{C}$
- Operating frequency up to 100 kHz
- Non dissipative overcurrent protection
- Dual independent constant  $t_{OFF}$  PWM current controllers
- Slow decay synchronous rectification
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast free wheeling diodes



### Description

The L6227Q is a DMOS dual full-bridge designed for motor control applications, realized in BCD multipower technology.

The L6227Q features thermal shutdown and a non-dissipative overcurrent protection on the high-side power MOSFETs plus a diagnostic output that can be easily used to implement the overcurrent protection.

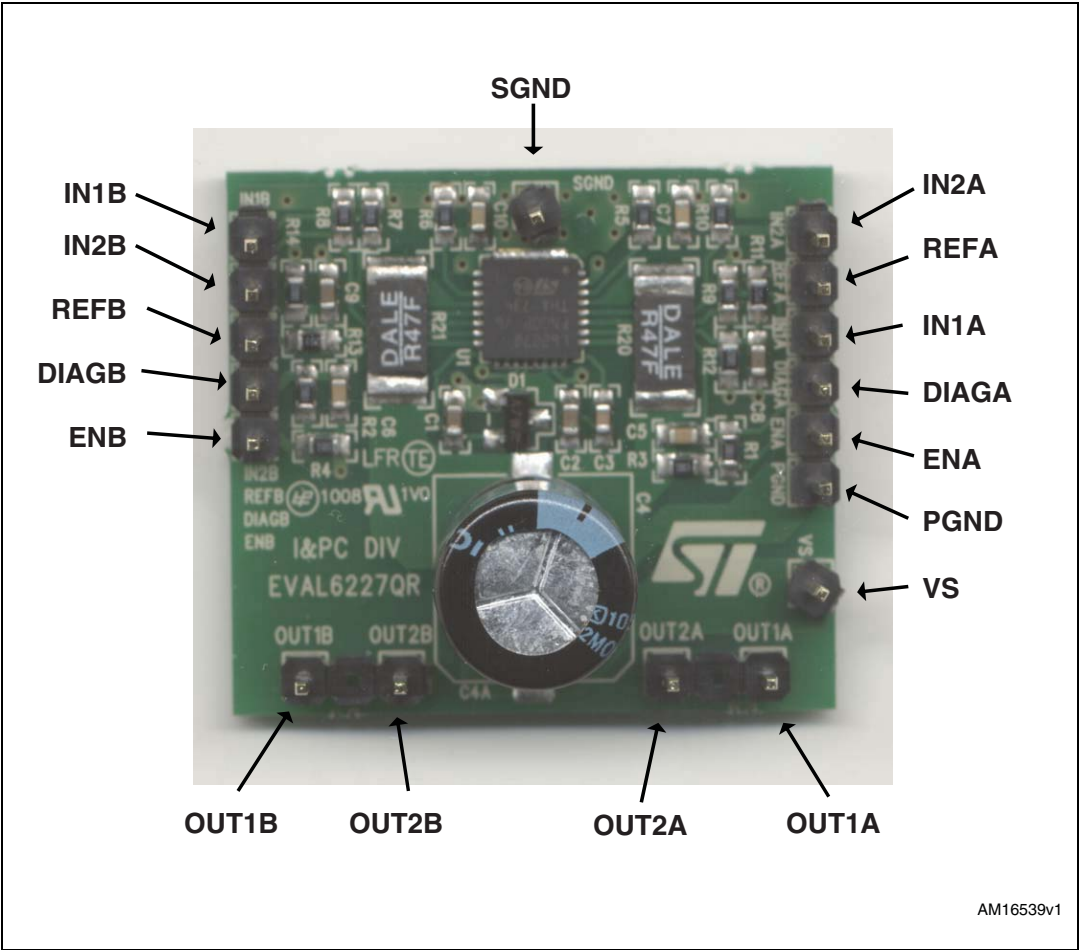
The device also includes two independent constant off-time PWM current controllers which perform the chopping regulation.

# 1 Board description

Table 1. EVAL6227QR electrical specifications (recommended values)

| Parameter                                     | Value                         |
|-----------------------------------------------|-------------------------------|
| Supply voltage range (VS)                     | 8 to 52 Vdc                   |
| Output current rating (OUTx)                  | up to 1.4 A <sub>r.m.s.</sub> |
| Switching frequency                           | up to 100 kHz                 |
| Input and enable voltage range                | 0 to + 5 V                    |
| Voltage reference range (REFA, REFB)          | 0 to + 5 V                    |
| L6227Q thermal resistance junction-to-ambient | 42 °C/W                       |

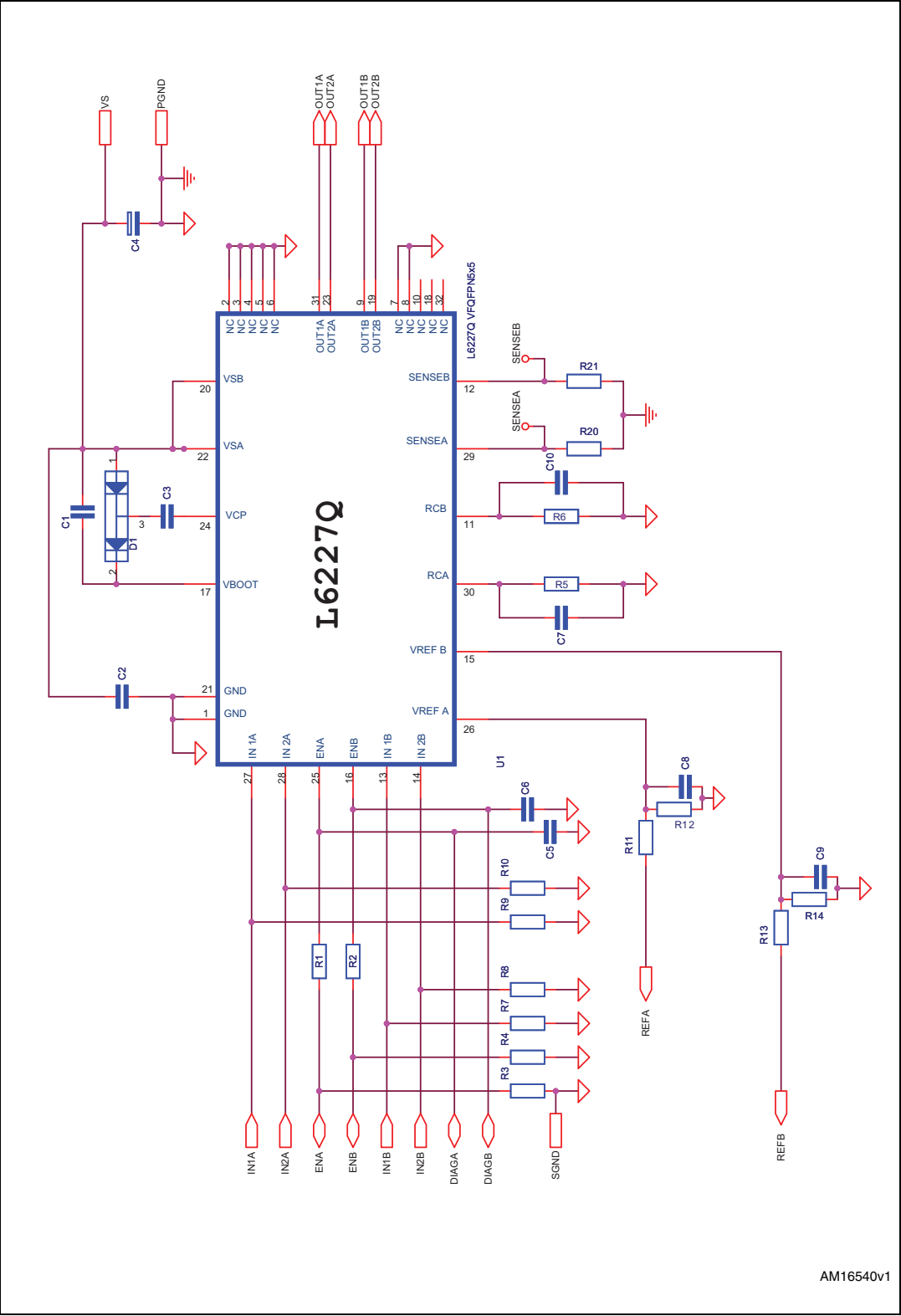
Figure 1. EVAL6227QR demonstration board description



**Table 2. EVAL6227QR pin connections**

| Name  | Type              | Function                                                                                            |
|-------|-------------------|-----------------------------------------------------------------------------------------------------|
| VS    | Power supply      | Bridge A and bridge B power supply                                                                  |
| PGND  | Ground            | Power ground terminal                                                                               |
| IN1A  | Logic input       | Bridge A logic input 1                                                                              |
| IN2A  | Logic input       | Bridge A logic input 2                                                                              |
| ENA   | Logic input       | Bridge A enable (active high). When low, the power DMOSs of bridge A are switched OFF.              |
| IN1B  | Logic input       | Bridge B logic input 1                                                                              |
| IN2B  | Logic input       | Bridge B logic input 2                                                                              |
| ENB   | Logic input       | Bridge B enable (active high). When low, the power DMOSs of bridge B are switched OFF.              |
| DIAGA | Open drain output | Bridge A diagnostic pin. When low, an overcurrent or overtemperature event of bridge A is signaled. |
| DIAGB | Open drain output | Bridge B diagnostic pin. When low, an overcurrent or overtemperature event of bridge B is signaled. |
| SGND  | Ground            | Signal ground terminal                                                                              |
| REFA  | Analog input      | Bridge A current controller reference voltage                                                       |
| REFB  | Analog input      | Bridge B current controller reference voltage                                                       |
| OUT1A | Power output      | Bridge A output 1                                                                                   |
| OUT2A | Power output      | Bridge A output 2                                                                                   |
| OUT1B | Power output      | Bridge B output 1                                                                                   |
| OUT2B | Power output      | Bridge B output 2                                                                                   |

Figure 2. EVAL6227QR demonstration board schematic



**Table 3. EVAL6227QR part list**

| Part reference                     | Part value                  | Part description              |
|------------------------------------|-----------------------------|-------------------------------|
| C1                                 | 220 nF/25 V                 | Capacitor                     |
| C2                                 | 220 nF/63 V                 | Capacitor                     |
| C3                                 | 10 nF/25 V                  | Capacitor                     |
| C4                                 | 100 $\mu$ F/63 V            | Capacitor                     |
| C5, C6                             | 5.6 nF                      | Capacitor                     |
| C7, C10                            | 820 pF                      | Capacitor                     |
| C8, C9                             | 220 nF                      | Capacitor                     |
| D1                                 | BAT46SW                     | Diode                         |
| R1, R2, R3, R4, R7,<br>R8, R9, R10 | 100 k $\Omega$ , 5%, 0.25 W | Resistor                      |
| R5, R6                             | 100 k $\Omega$ , 1%, 0.25 W | Resistor                      |
| R11, R13                           | 20 k $\Omega$ , 5 %, 0.25 W | Resistor                      |
| R12, R14                           | 2 k $\Omega$ , 5 %, 0.25 W  | Resistor                      |
| R20, R21                           | 0.4 $\Omega$ , 1 W          | Resistor                      |
| U1                                 | L6227Q                      | Dual full-bridge in VFQFPN5x5 |

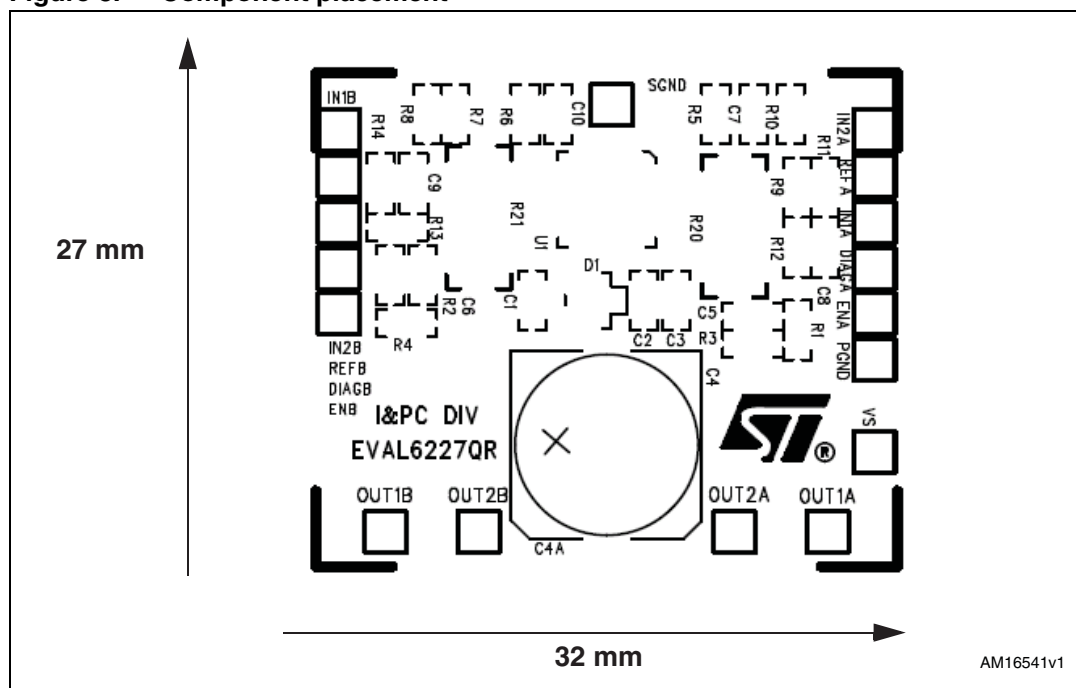
**Figure 3. Component placement**

Figure 4. Top layer layout

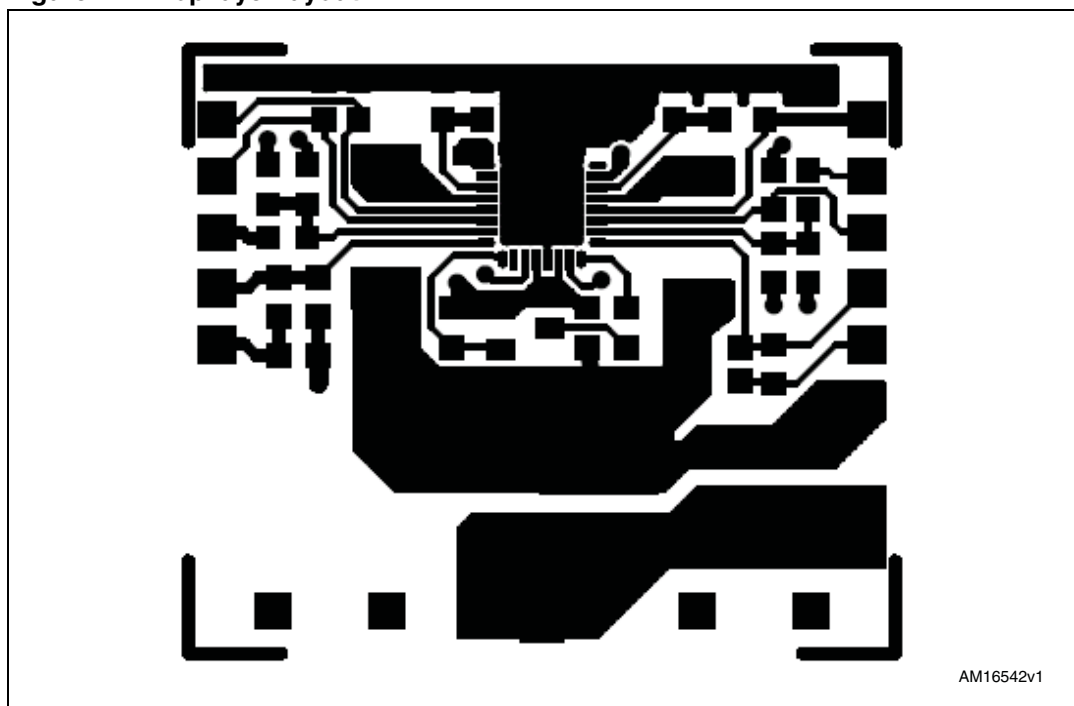
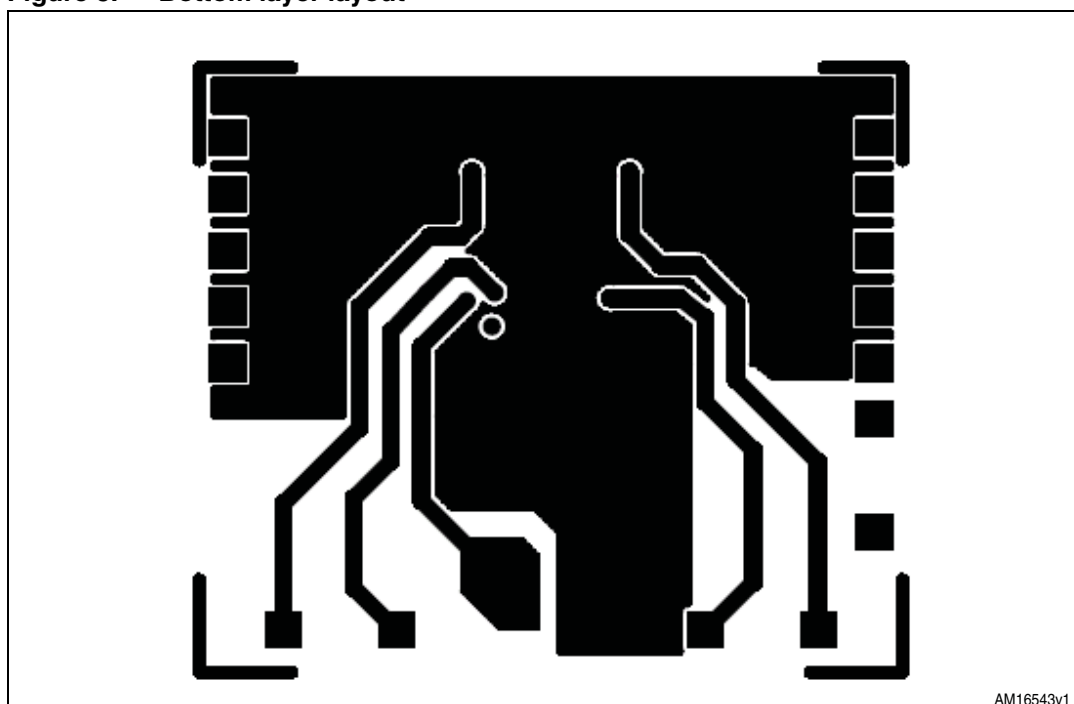


Figure 5. Bottom layer layout



## 2 Revision history

**Table 4. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 09-Jan-2013 | 1        | Initial release. |

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