Z8FS040

ZMOTION™ Detection and Control Family Featuring Zilog's PIR Technology

Product Specification

PS028506-1110

PRELIMINARY

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Revision History

Each instance in the Revision History table reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the following table.

Date	Revision	Description	Page No.
November 2010	5	Updated for new Zilog/IXYS logo	All
October 2010	4	Changed verbatim instances of ePIR to PIR as appropriate.	All
September 2010	3	Added MCU-only version. Removed ePIR.	3, 38
August 2010	2	Added ZMOTION product logo.	i
June 2010	1	Original Issue	All

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Overview

Zilog's ZMOTION™ Detection and Control Product Family provides an integrated and flexible solution for Passive Infra Red (PIR) based motion detection applications. The family includes a series of high-performance microcontrollers with integrated motion detection algorithms and a selection of lenses and PIR sensors to fit a wide range of application requirements. Optimized configuration parameters for the MCU are provided for each lens/sensor combination ensuring the best possible performance while significantly reducing development risk and minimizing time to market.

The Z8FS040 ZMOTION™ Detection MCU combines the programmability and rich peripheral set of Zilog's Flash Z8F082A Z8 Encore! XP® MCU with built-in motion detection software algorithms to provide the functions necessary for PIR motion detection applications. These motion detection algorithms comprise Zilog's PIR technology and run in the background while control and status of the Engine is accessed through a software API (Application Programmer Interface). This allows the designer to create their own application specific software while taking advantage of Zilog's ZMOTION™ Motion Detection Technology.

API settings are provided to match the Engine operation to each of the lens and pyroelectric sensor combinations provided.

The Flash in-circuit programming capability of the Z8FS040 allows for faster development time, more flexible manufacturing and firmware changes in the field.

Zilog's PIR motion detection technology provides a dramatic improvement in both sensitivity and stability over traditional designs and is scalable to many market segments including Lighting Control, HVAC, Access Control, Vending, Display, Proximity, Power Management, Occupancy Sensing and many others.

Features

- High performance eZ8® MCU core
- 4 KB in-circuit programmable Flash available for application code
- Single pin debug with unlimited breakpoints
- Flexible clocking scheme
- Internal precision oscillator running at 5.53 MHz
- External oscillator operating up to 20 MHz
- Sigma Delta ADC
- Up to 6 channels single ended or 3 channels differential available
- On-chip analog comparator with independent programmable reference voltage
- Full-duplex UART with dedicated BRG
- Two 16-bit timers with input capture, output compare, and PWM capability (11 modes total)
- Watchdog timer (WDT) with dedicated internal oscillator
- Up to 20 vectored interrupts
- 6 to 25 I/O pins depending upon package

- 2.7 V to 3.6 V operating voltage with extended operating temperature range -40^0 C to +105^0 C
- Zilog's PIR technology controlled and monitored through software API registers
- Select from an assortment of lenses and pyroelectric sensors to best fit your application
- API settings provided for each lens and pyroelectric sensor combination
- Directly supports 1 or 2 pyroelectric sensors
- Sensitivity control, range control and directionality detection
- Extended detection modes for Occupancy sensing
- Low power modes

Block Diagram

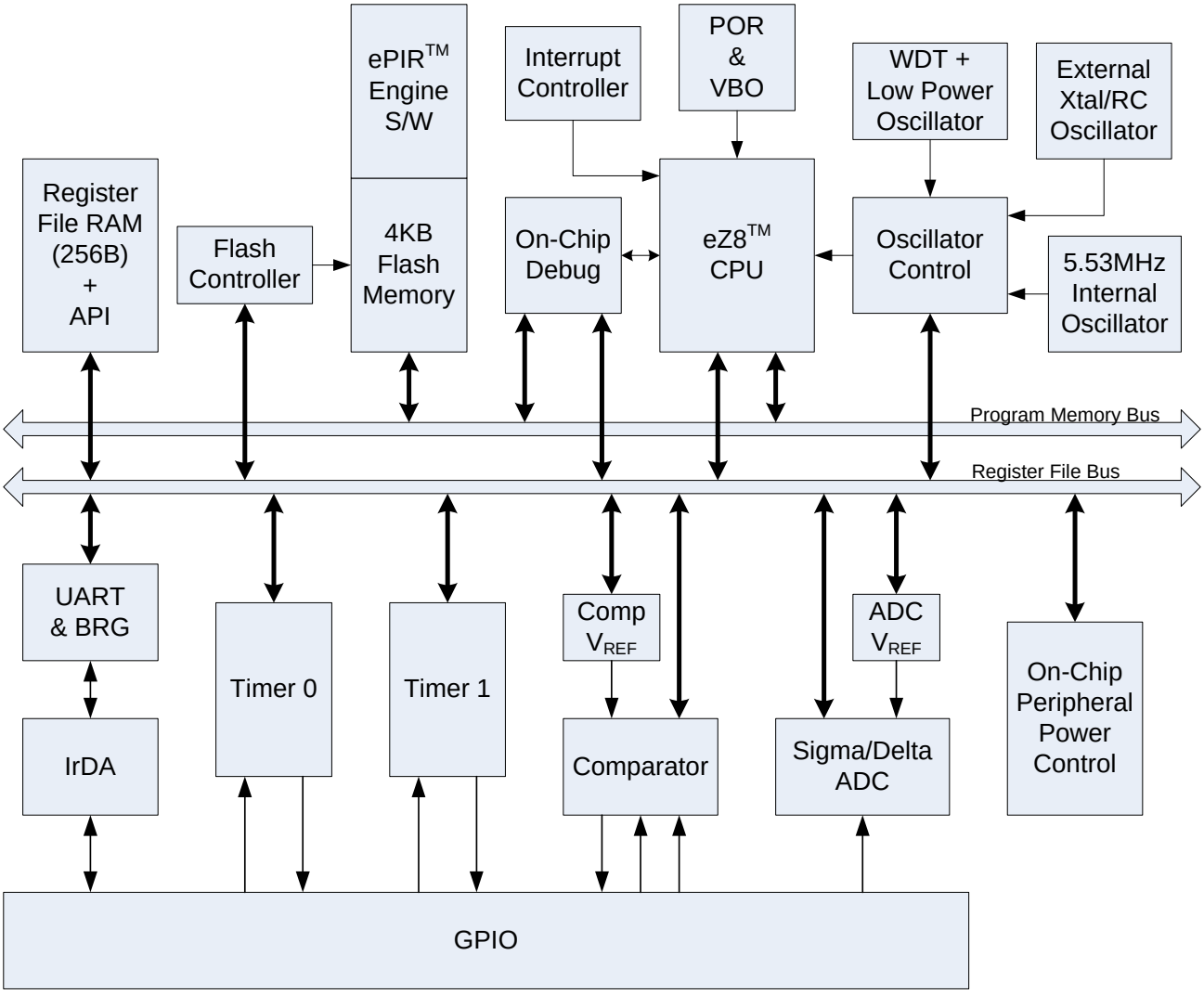


Figure 1 shows the architectural block diagram of the Z8FS040.

MCU Part Selection Guide and Reference

Table 1 displays the basic features and package styles available for each device within the Z8FS040 ZMOTION™ MCU devices.

The ZMOTION™ MCU is available on its own or as a package which includes the MCU, lens and pyroelectric sensor together. The part numbers for the ZMOTION MCU are shown below.

See Ordering Information for full ZMOTION™ Product Family part numbers.

ZMOTION MCU Part Number	Z8 Encore XP Base Part Number	Flash Memory	GP I/O	ADC Channels	Package	Pin Configuration Diagram
Z8FS040xSB20EG	Z8F082ASB020EG	4 KB	5	3	8 pin SOIC	Figure 2
Z8FS040xHH20EG	Z8F082AHH020EG	4 KB	16	4	20 pin SSOP	Figure 3
Z8FS040xHJ20EG	Z8F082AHJ020EG	4 KB	22	6	28 pin SSOP	Figure 4
Where x = PIR Technology Revision Identifier (see Table 2)						

Table 1 - Z8FS040 ZMOTION™ MCU Series Part Selection Guide

Please refer to the base part number in **Product Specification - PS0228 "***Z8 Encore! XP® F082A Series Product Specification***"** for all MCU functions, features, and specifications not covered in this document.

PIR Technology Revisions

Version	Part Number Engine Revision Identifier	Description
1.00	A	Initial release for ZEPIR0AAS01SBCG. 8-pin version only
2.00	B	ZMOTION™ MCU Series release. Improved detection/stability. Added Range, Low Power, Extended Detection, Dual Pyro, Advanced API features

Table 2 - PIR Technology Revision Identifiers

Pin Configurations

Overview

Zilog's Z8FS040 products are available in a variety of package styles and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information on the physical package specifications, see Packaging on Page 35.

Figure 2, Figure 3, and Figure 4 display the pin configurations of all the packages available for the ZMOTION™ MCU Series. For a description of the signals, see Tables 6, 7, and 8.

At reset, all port pins are set to GPIO input state except /RESET/DE0/T1OUT (8 pin) which is configured to /RESET, PA0/T0IN/T0OUT/XIN/DBG (8 pin) which is configured to DBG and RESET/PD0 (20 and 28 pin) which are configured to /RESET.

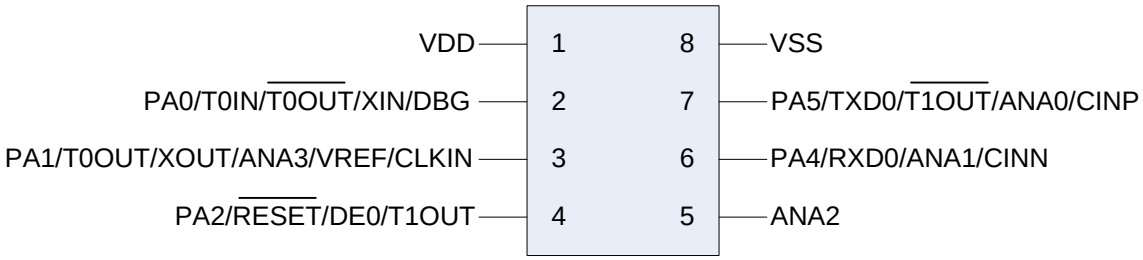


Figure 2 – 8 Pin SOIC Package Pin-Out – Z8FS040xSB20EG

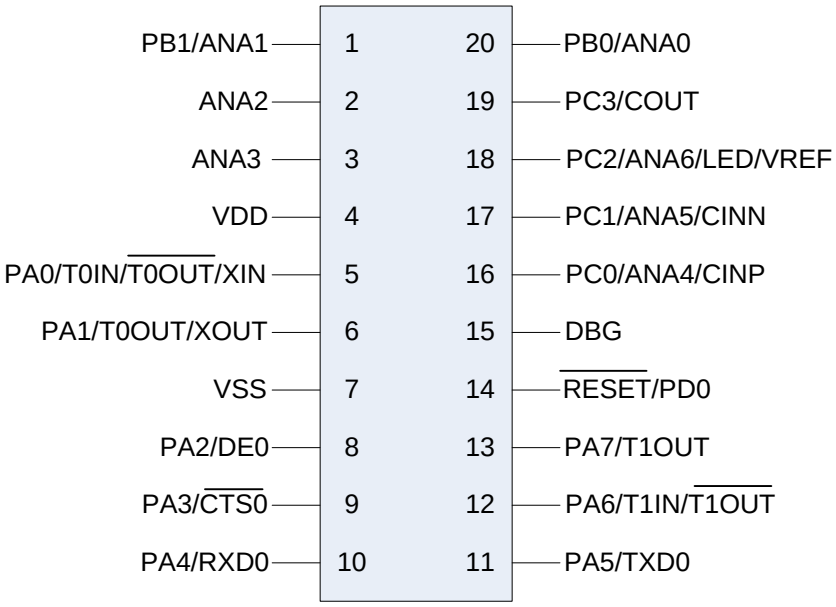


Figure 3 – 20 Pin SSOP Package Pin-Out – Z8FS040xHH20EG

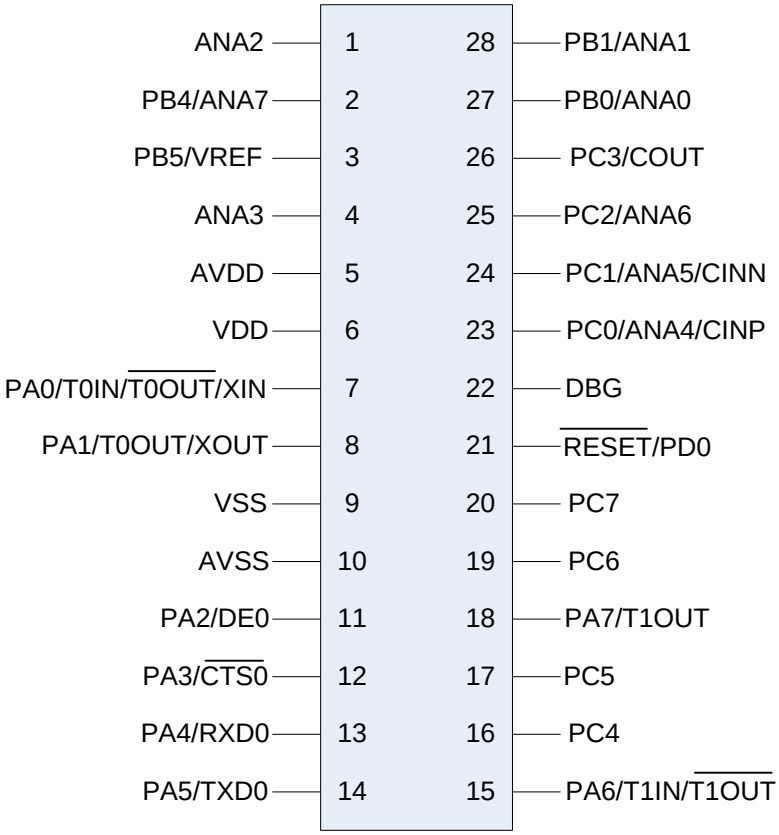


Figure 4 – 28 Pin SSOP Package Pin-Out – Z8FS040xHJ20EG

Signal Descriptions

Table 3 below describes the Z8FS040 Series signals.

Table 3 - Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A–D		
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[5:0]	I/O	These pins are used for general-purpose I/O.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
PD[0]	I/O	Port D. This pin is used for general-purpose output only.
UART Controllers		
TXD0	O	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	I	Clear To Send. This signal is the flow control input for the UART.
DE	O	Driver Enable. This signal allows automatic control of external RS-485 drivers. This signal is approximately the inverse of the TXE (Transmit Empty) bit in the UART Status 0 register. The DE signal may be used to ensure the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0OUT/T1OUT	O	Timer Output 0–1. These signals are outputs from the timers.
T0OUT/T1OUT	O	Timer Complement Output 0–1. These signals are output from the timers in PWM Dual Output mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs.

Table 3 - Signal Descriptions (continued…)

Comparator		
CINP/CINN	I	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
COUT	O	Comparator Output.
Analog		
ANA[7:0]	I	Analog Port. These signals are used as inputs to the analog-to-digital converter (ADC).
VREF	I/O	Analog-to-digital converter reference voltage input, or buffered output for internal reference.
Oscillators		
XIN	I	External Crystal Input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the **XOUT** pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
XOUT	O	External Crystal Output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the **XIN** pin to form the oscillator.
Clock Input		
CLKIN	I	Clock Input Signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	O	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger.

Caution: *The DBG pin is open-drain and requires a pull-up resistor to ensure proper operation.*

Table 3 - Signal Descriptions (continued…)

Reset		
RESET	I/O	RESET. Generates a Reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V_{DD}	I	Digital Power Supply.
AV_{DD}	I	Analog Power Supply.
V_{SS}	I	Digital Ground.
AV_{SS}	I	Analog Ground.

Memory Map

Flash Memory (Code Space)

The Z8FS040 is based on Zilog's Z8F082A device which contains a total of 8KB Flash memory. Zilog's PIR technology is located in the 4-KB address range from 1000h to 1FFFh leaving 4 KB from 0000h to 0FFFh available for user application code.

Zilog's PIR technology is locked and can not be erased by the user or by Zilog Debug Interface (ZDI) mass or page erase commands.

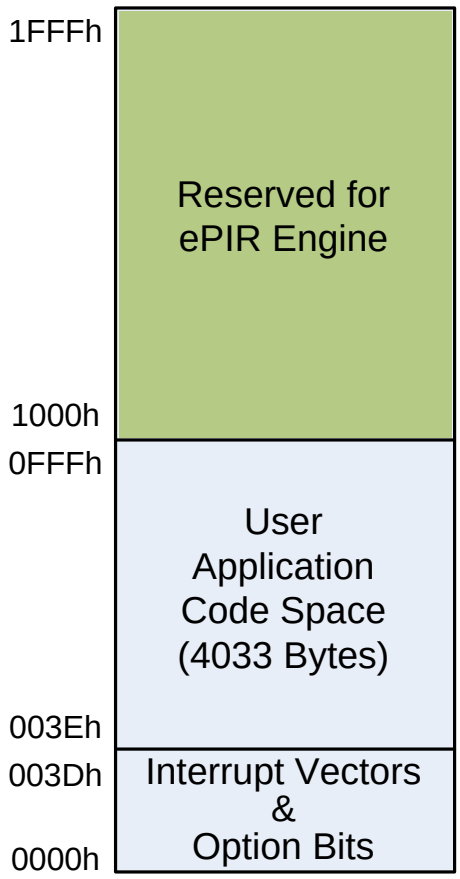


Figure 5 - Z8FS040 Program Memory Map

RAM Memory Map (Register Files)

There is a total of 1 KB of RAM available on the base Z8F082A device. Some of this RAM (from 080h to 0EFh and 190h to 3FFh) is used by Zilog's PIR technology. The remainder of the RAM from 000h to 07Fh and 110h to 18Fh (256 bytes) is available to the application. The MCU Control Registers are located at the top of memory from F00h to FFFh and are also available to the application. The area from 400h to EFFh contains no device memory.

The PIR Motion Detection API is a series of registers located in RAM memory space from 0F0h to 10Fh. It is through these memory locations that configuration and status are passed between the PIR technology and the user application. Advanced API registers are located from address 0F0h to 0FFh. See PIR Engine and API section for details on the API registers and setting up the project memory environment.

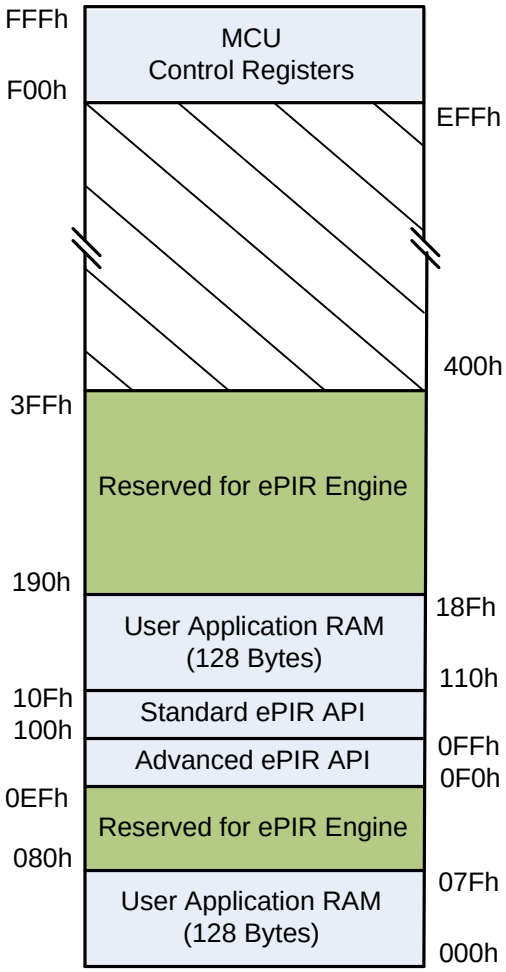


Figure 6 - Z8FS040 RAM Memory Map

Peripherals

The following sections describe the differences, changes, or limitations placed on any of the Z8FS040 peripherals or other functions from the base Z8F082A device. For more information on the operation of each peripheral please refer to the appropriate section of PS0228.

Peripheral Availability

Table 4 - Peripheral Availability shows how the peripherals are used by Zilog's PIR technology and the differences from the base Z8F082A device. The peripherals used by the PIR technology should not be used by the application unless the engine is disabled through the PIR Engine Enable register.

	Device		
	Z8FS040xSB20EG	**Z8FS040xHH20EG**	**Z8FS040xHJ20EG**
Base MCU Device	**Z8F082ASB020EG**	**Z8F082AHH020EG**	**Z8F082AHJ020EG**
Pins/Package	8 pin SOIC	20 Pin SSOP	28 Pin SSOP
ADC	ANA2 used for PIR sensor input. ANA3 is used for second sensor input in dual pyro mode.	ANA2 used for PIR sensor input. ANA3 connected to ANA6/V_{REF}. ANA3 is used for second sensor input and ANA6 becomes available in Dual Pyro Mode.	ANA2 used for PIR sensor input. ANA3 connected to V_{REF}. ANA3 is used for second sensor in Dual Pyro Mode
V_{REF}	Internal V_{REF} used by the PIR engine and set to 1 V.	Internal V_{REF} used by the PIR engine and set to 1 V.	Internal V_{REF} used by the PIR engine and set to 1 V.
Timer 0	Available to application	Available to application	Available to application
Timer 1	Available to application	Available to application	Available to application
GP I/O	PA3/PA1 are multiplexed with ANA2/ANA3 and used for PIR sensor input (ANA2 for single pyro mode and ANA2/ANA3 for dual pyro mode).	PB2, PB3 & PC2 used for PIR functions. In dual pyro mode PC2 becomes available.	PB2, PB3 & PB5 are used for PIR functions. In dual pyro mode PB5 becomes available.
Low Power Op Amp	Not Available	Not Available	Not Available
Comparator	Available to application	Available to application	Available to application
UART	Available to application – No CTS	Available to application	Available to application
Temperature Sensor	Not Available	Not Available	Not Available
LED Drive	—	Available to application	Available to application
WDT	Available to application	Available to application	Available to application

Table 4 - Peripheral Availability

ADC

Zilog's PIR technology requires exclusive access to the ADC peripheral in order to detect motion. However, ADC conversions can be requested by the application through the API (PIR Status/Control Register 3). If it is necessary for the user application to utilize the ADC peripheral directly, the PIR engine must first be disabled via the PIR Engine Enable Register in the API. Motion detection is not possible while the PIR engine is disabled. When the user application is finished with the ADC peripheral, it must re-enable the PIR engine.

8 Pin Device: PA3 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. Therefore ANA2 is not available for user applications. Additionally ANA3 is used for second sensor input in dual pyro mode. All other channels are available to the user application.

ADC Channel	Available to Application
0	Yes
1	Yes
2	No
3	Only in Single Pyro Mode

20 Pin Device: PB2 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. Therefore ANA2 is not available for user applications. Also, ANA3 and ANA6 are not available since PB3 (ANA3) must be tied directly to PC2 (ANA6/ V_{REF}). PC2 is configured as V_{REF} output by the PIR engine. In dual pyro mode ANA3 is used for second sensor input – rather than being tied to V_{REF} and therefore ANA6/ V_{REF} becomes available. All other channels are available to the user application.

ADC Channel	Available to Application
0	Yes
1	Yes
2	No
3	No
4	Yes
5	Yes
6	Only in Dual Pyro Mode

28 Pin Device: PB2 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. Therefore ANA2 is not available for user applications. Also, ANA3 is not available since it is tied directly to PB5/ V_{REF}. PB5 will be configured as V_{REF} output by the PIR engine. In dual pyro mode ANA3 is used for second sensor input – rather than being tied to V_{REF} and therefore PB5 becomes available. All other channels are available to the user application.

ADC Channel	Available to Application
0	Yes
1	Yes
2	No
3	No
4	Yes
5	Yes
6	Yes
7	Yes

Timers

There are two independent and identical 16 bit multi-function timers available – Timer 0 and Timer 1.

Timer 0

This timer is available to the user application.

8 Pin Device: T0OUT not available in Dual Pyro Mode – configured as ANA3 to support second sensor input. All other external Timer 0 functions are available for the user application.

20 Pin Device: All external Timer 0 functions are available for the user application.

28 Pin Device: All external Timer 0 functions are available for the user application.

Timer 1

This timer is available to the user application.

8 Pin Device: T1IN is configured as ANA2 to support the signal input from the pyroelectric sensor and is not available to the user application. All other Timer 1 functions are available.

20 Pin Device: All external Timer 1 functions are available for the user application.

28 Pin Device: All external Timer 1 functions are available for the user application.

Watchdog Timer

No changes or limitations are placed on these functions by Zilog's PIR technology. This is available to the user application.

Comparator

8 Pin Device: The external pin that carries COUT is configured as ANA2 to support the signal input from the Pyroelectric sensor. However, the Comparator is still able to generate an interrupt internally without COUT.

20 Pin Device: All external Comparator functions are available for the user application.

28 Pin Device: All external Comparator functions are available for the user application.

UART

8 Pin Device: /CTS0 is configured as ANA2 to support the signal input from the Pyroelectric sensor. It is therefore not available to the user application. The UART is still able to function correctly without /CTS when CTSE in the U0CTL0 register set to 0.

20 Pin Device: All external UART functions are available for the user application.

28 Pin Device: All external UART functions are available for the user application.

Oscillator Control

All devices can be operated with the internal 5.54 MHz IPO. For applications that require more processing power or a more accurate time base, an external crystal oscillator or ceramic resonator may be used.

For the 8 pin device external oscillator support is limited to single pyro mode only since ANA3 (ADC input for second pyro sensor) is multiplexed with Xout. The 20 and 28 pin devices can be operated with an external oscillator in both single and dual pyro modes.

Do not operate at frequencies lower than the IPO frequency while the PIR engine is enabled or motion detection performance will be degraded.

No other changes or limitations are placed on these functions by the PIR engine.

Flash Memory

The control registers associated with the Flash memory are all available to the application. Zilog's PIR technolgoy uses the value programmed into the Flash Frequency registers (FFREQ) to determine its required sample timing. This register must be programmed prior to initializing the PIR engine. The Flash Frequency High (FFREQH) and Flash Frequency Low Byte (FFREQL) registers combine to form a 16-bit value FFREQ. This value is also used by the PIR engine to calculate the required sample rate of the ADC and other functions. The 16-bit value for FFREQ is the System Clock Frequency in KHz and is calculated using the following equation.

FFREQ[15:0] = {FFREQH[7:0],FFREQL[7:0]} = (System Clock Frequency)/1000

Interrupt Controller

No changes or limitations are placed on the interrupt controller functions by Zilog's PIR technology.

Temperature Sensor

The temperature sensor is not tested or calibrated (trim bits are not available). Therefore this peripheral is not available on any of the Z8FS040 devices.

Low-Power Operational Amplifier

The AMPINP signal is multiplexed with ANA2 which is used for the pyro sensor input. Therefore this peripheral is not available on any of the Z8FS040 devices.

Non-Volatile Data Storage

There is no dedicated non-volatile data storage on the Z8FS040 devices.

Pin Configurations

Although most pins on the ZMOTION™ MCU Series are available to the application, some pins are dedicated to supporting the PIR functions. The following section describes which pins are reserved and which are available to the application. The pins used by Zilog's PIR technology are automatically configured when the engine is initialized.

General-Purpose Input/Output

All of the General Purpose I/O's are available except for those used for the PIR circuit. See example application schematics, Appendix A for more information.

8 Pin Device: Pin 5 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. Any other functions multiplexed with Pin 5 (PA3//CTS0, COUT and T1IN) are not available for user applications.

In dual pyro mode (application uses 2 pyroelectric sensors) Pin 3 (ANA3) is used as an analog ADC input for second sensor and is therefore not available for other functions (T0OUT/Vref/CLKIN).

20 Pin Device: Pin 2 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. In single pyro mode, Pin 3 (ANA3) must be externally tied to V_{REF} on Pin 18 (PC2/ANA6/LED/V_{REF}). PC2 will be configured as the V_{REF} output by the PIR engine when it is enabled.

In dual pyro mode (supporting 2 pyroelectric sensors), Pin 3 (ANA3) is used for the second sensor. In this mode the Pin 18 V_{REF} signal is not connected externally to any other ADC inputs and is therefore available to the application (PC2/ANA6/LED/ V_{REF}).

28 Pin Device: Pin 1 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. In single pyro mode, Pin 4 (ANA3) must be externally tied to V_{REF} on Pin 3 (PB5/ V_{REF}). PB5 will be configured as V_{REF} output by the PIR engine when it is enabled.

In dual pyro mode (supporting 2 pyroelectric sensors), Pin 4 (ANA3) is used for second sensor. In this mode the Pin 3 V_{REF} signal is not connected externally to any other ADC inputs and is therefore available to the application (PB5/ V_{REF}).

Hardware Connection Requirements

This section describes the required external hardware connection for the ZMOTION™ MCU Series.

Pins are automatically configured to their required function when the PIR engine is initialized via the EPIR_INIT macro.

See Appendix A for example schematic diagrams showing the required connections.

The device can be operated in Single Pyro mode supporting one Pyroelectric sensor or Dual Pyro mode supporting two Pyroelectric sensors. Both of these modes can be operated in Normal or Low Scan Rate modes.

Depending on the application, there can be up to 3 connection requirements supporting these modes:

1. Pyroelectric Sensor (PIR Sensor)
   The signal from the PIR sensor is connected directly to the ANA2 input of the ADC. The ADC is configured for differential, buffered mode by Zilog's PIR technology. The sensor signal should be connected directly to the ADC input with no additional signal conditioning circuitry unless specified by the pyroelectric sensor manufacturer.

2. ADC V_{REF}
   The on chip V_{REF} is configured for 1V nominal. The PIR Sensor signal is connected to the '+' differential input of the ADC (ANA2) and the V_{REF} signal is connected to the '-' differential input (ANA3). The 8 pin device has an internal connection from V_{REF} to ANA3 to support this configuration therefore no external hardware connection is required. The 20 and 28 pin devices require an external connection from the V_{REF} out signal to the ADC '-' (ANA3) input.

3. Pyroelectric Passive Infrared Sensor #2
   In Dual Pyro mode, the ADC is still used in differential, buffered mode (same as Single Pyro mode). The signal from the second PIR sensor is connected to ANA3. The V_{REF} signal is no longer connected to ANA3 ('-' ADC input). The fist PIR sensor is connected to the '+' ADC input (ANA2) as it is in Single Pyro mode. The V_{REF} signal is still used internally for the ADC, but the external pin is unused in Dual Pyro mode.

Zilog's PIR Technology and API

General Operation

The ZMOTION™ MCU Series is based on the Z8 Encore! XP® Z8F082A MCU with the added functionality of a motion detection engine (PIR engine). The PIR engine is located in the upper 4KB area of the 8KB device leaving 4KB of code space to the user application. It operates in the background and is controlled and monitored through an Application Programmer Interface (API). The API is a series of reserved registers in memory.

There are two sections to the API – Standard API Registers and Advanced API Registers:

1. ***Standard API registers***: It includes all of the status and control functions needs for most applications. These include sensitivity control, motion detection/direction status and operational modes.
2. ***Advanced API registers***: It provides additional control over the PIR engine operation and allows it to be configured to support the pyroelectric sensor and lens being used in the application.

PIR Engine Timer Tick

Bit 7 of PIR Status/Control Register 1 provides a 1 second time base for the PIR engine to perform house keeping operations. This bit must be set to 1, once per second by the user application. The bit is checked and cleared during the EPIR_ADC_ISR routine.

PIR Engine Entry Points

There are two entry points to the PIR engine that are accessed through two predefined Macros. One is an initialization macro that is used to start the engine and the other is executed upon every ADC interrupt. Both macros save and initialize the Register Pointer, perform a call to the PIR engine entry point and then restore the Register Pointer before returning control to the application. It is the responsibility of the Application S/W to execute these Macro's at the appropriate time.

EPIR_INIT Macro

This macro is executed to initialize the PIR engine after reset. It is normally only executed once and is used in conjunction with the PIR Engine Enable register in the standard API section. The application should initialize all API registers, write the PIR Enable Pattern to the PIR Engine Enable register, and then execute this Macro. ADC conversions are started by this macro.

```
EPIR_INIT Macro:
      PUSHX       RP
      LDX         RP, #%E0
      CALL        %1FFD
      POPX        RP
```

CPU Cycles: 261
Peripherals Initialized:
ADC and GPIO depending on API selected options. ADC IRQ set for medium priority.

EPIR_ADC_ISR Macro

This macro is executed for each ADC conversion. The application handles the ADC interrupt and executes this macro. All motion detection processing is performed by this macro.

```
EPIR_ADC_ISR Macro:
      PUSHX       RP
      LDX         RP, #%E0
      CALL        %1000
      POPX        RP
```

The CPU cycles used by this Macro vary depending on Engine state and configuration.

PIR Engine CPU Stack Usage

The PIR engine shares the processor stack with the user application. There are no special requirements on the placement of the stack in memory, but it is essential that the user provide enough stack space for both the user application and the PIR engine.

The PIR engine requires maximum 6 bytes of stack.

Standard API Register Set

The Standard API Register Set is a series of registers implemented in the Z8FS040 RAM that allows the user code to configure and communicate with the PIR engine. The default values are loaded only when the PIR engine is enabled via the PIR Enable Register.

API Register Name	Address	Mnemonic	Description
PIR Engine Enable Register	100h	ePIR_Enable	Enable PIR Engine
PIR Sensitivity Register	101h	ePIR_Sensitivity	Motion Sensitivity
PIR Status/Control Register 0	102h	ePIR_SC0	Motion Status and Engine Mode Control
PIR Status/Control Register 1	103h	ePIR_SC1	Engine Status and Control
PIR Status/Control Register 2	104h	ePIR_SC2	Range Control
PIR Status/Control Register 3	105h	ePIR_SC3	ADC Scan Request
PIR ADC Result Value	10Ah/10Bh	ePIR_ADC_Result	ADC Scan Result
PIR Version	10Ch	ePIR_Version	PIR Engine Software Version

Table 5 - PIR Engine Standard API Registers

PIR Engine Enable Register (ePIR_Enable)

Bit	7	6	5	4	3	2	1	0
Field	PIR Enable/Disable Pattern							
Control	Read/Write							
Address	100H							

PIR Enable/Disable Pattern (Bits 0-7)

PIR Enable/Disable Register
Controlled by Application

The PIR Enable Register controls the overall operation of the PIR engine. As an added level of protection, there is a specific 8 bit enable value and 8 bit disable value. All other values are reserved. Reading this register returns the last value written. Once enabled, the PIR engine reads the application controlled Status/Control Register values and sets the engine controlled values to their default state.

To enable the PIR engine, first write the ePIR_ENABLE_PATTERN to the PIR Enable Register then execute the EPIR_INIT macro.

Pattern	Name	Description
00h	ePIR_DISABLE_PATTERN	Disables all Engine functions, including motion detection. Used to temporarily or permanently shut down the engine.
11h	ePIR_ENABLE_PATTERN	Enables the PIR engine. All primary engine functions as configured in Engine Status/Control Registers are enabled. Confirmation of enabled status is provided through Engine Disabled bit in Status/Control Register 0.

Table 6 - PIR Software Enable Patterns

PIR Sensitivity Register (ePIR_Sensitivity)

Bit	7	6	5	4	3	2	1	0
Field	Sensitivity							
Default	U	U	U	U	U	U	U	U
Control	Read/Write							
Address	101H							

Sensitivity (Bits 0-7)

PIR Sensitivity Setting
Controlled by Application

The PIR Sensitivity Register is used to adjust the sensitivity of the PIR engine to target motion. Lower values produce higher sensitivity to motion with 00h being the most sensitive and FFh being the least sensitive. The user application should load this register with the appropriate value to give the desired sensitivity.

Notes:

- The setting of this register also affects the range of detection. Lower values increase range and higher values decrease range.
- Depending on the lens and pyroelectric sensor used, values above 3Fh may result in very limited detection.

PIR Status/Control Register 0 (ePIR_SC0)

Bit	7	6	5	4	3	2	1	0
Field	Extended Detection		Engine Disabled	MD Suspend	Motion Direction Control	Motion Direction	Motion Detected	PIR Stable
Control	R/W		R	R/W	R/W	R	R/W	R
Address	102H							

Extended Detection Level (Bit 6-7)

Sets the sensitivity level of extended detector
Controlled by application

These 2 bits enhance the motion detection algorithms to detect slower, faster and/or more subtle motion. The Extended Detection level is selected to provide a balance between additional sensitivity while maintaining stability (no false detections). In certain applications such as lighting control the Extended Detection level can be increased once ‘normal’ motion has been detected. Extended detection is dependent on the lens pattern used. Smaller lens beams tend to provide more subtle motion detection.

The Extended Detection level effects user control over the range provided in ePIR_SC2. As the Extended Detection level is increased, the Range setting becomes less effective.

00 = Extended Detection Level 0 – Minimum (least sensitive)
01 = Extended Detection Level 1
10 = Extended Detection Level 2
11 = Extended Detection Level 3 – High (most sensitive)

Engine Disabled (Bit 5)

PIR Engine Disable/Suspend Acknowledged
Controlled by PIR engine

This bit indicates the operational status of and is controlled by the PIR engine. When the engine is initialized and enabled by loading the PIR Enable Register with the ePIR_ENABLE_PATTERN value, this bit is cleared to indicate that the Engine is ready. When the Engine is disabled by loading the PIR Enable Register with the ePIR_DISABLE_PATTERN, it will respond by setting this bit to 1 and perform no further operations until re-enabled. In order for the Engine to detect that it has been disabled, the user must allow the Engine ADC interrupt to run at least once after loading the PIR Enable Register with the ePIR_DISABLE_PATTERN.

0 = Engine is enabled and operational
1 = Engine is disabled and not operational

MD Suspend (Bit 4)

Motion Detection Suspend
Controlled by Application

Temporarily suspends the PIR engine from running. This puts it in a very low processing overhead state and can be used when the application requires significant CPU processing power. While suspended, motion detection is disabled, however to ensure fast recovery from this mode, ADC interrupts still occur and samples continue to be buffered. When the application clears this bit, suspend mode is exited upon the next ADC interrupt.

0 = Normal Motion Detection
1 = Suspended Motion Detection

Motion Direction Control (Bit 3)

Motion Direction Control Enable
Controlled by Application

This bit enables directional motion detection. The relative direction of the detected motion is indicated in bit 2 (Motion Direction) of this same register. When configured as a directional detector (bit 3 set to 1), direction is indicated in bit 2 as positive or negative relative to the PIR sensor.

0 = Standard Motion Detection Mode. Motion detected in any direction. Motion Direction status bit (Bit 2) is not valid.
1 = Directional Motion Detection Mode. Motion is detected in any direction; relative direction is indicated via Motion Direction status bit (Bit 2).

The directional polarity of PIR sensors is arbitrary at the time of manufacturing. Therefore it is necessary for the user application to calibrate to each individual PIR sensor using a controlled target (i.e. moving in a known direction) and internally record the polarity to identify which polarity represents that direction.

Motion Direction (Bit 2)

Relative Direction of Last Motion Detected
Controlled by PIR engine

When directional motion detection is enabled, this bit indicates the relative direction of the last motion detected. When the PIR engine sets the Motion Detected bit in PIR Status Register 0, this bit is set or cleared to indicate the direction of the motion. The status is latched until the user application clears the Motion Detected bit.

0 = Last detected motion was negative
1 = Last detected motion was positive

This status bit is undefined when Motion Direction Control is disabled.

Motion Detected (Bit 1)

Motion detected on PIR sensor
Set by PIR engine; cleared by application

This bit indicates that the Engine has detected a motion event. The user application should routinely check this bit to determine if motion has been detected. This bit is set by the Engine and must be cleared by the user application.

0 = No motion detected by the Engine
1 = Motion has been detected by the Engine

PIR Stable (Bit 0)

Passive Infrared (PIR) sensor signal stabilized bit
Controlled by PIR engine

After periods of non-use the PIR sensor will take some time to stabilize before it can be used reliably. The amount of time is dependant on the PIR Sensor being used and environmental conditions and can range from a few seconds up to a minute. To relieve the application S/W from having to assume the worst case stabilization time, the PIR engine automatically monitors the DC offset of the PIR sensor and sets this bit when it determines that it has become stable. This bit indicates that the PIR sensor has stabilized after one of the following conditions:

- After initial power on (cold start).
- After re-enabling the Engine via PIR Enable Register.
- After returning from sleep mode.

0 = PIR sensor signal is not stable, motion detected events are not valid
1 = PIR sensor signal is stable, motion detected events are valid

PIR Status/Control Register 1 (ePIR_SC1)

Bit	7	6	5	4	3	2	1	0
Field	Engine Timer Tick	Frequency Response				PIR Scan Rate	Reserved	Dual Pyro Enable
Control	R/W	Read/Write				R/W	0	R/W
Address	103H							

Engine Timer Tick (Bit 7)

PIR One Second Timer Tick
Set by Application; cleared by PIR engine

This bit must be set to 1 once per second by the user application. This provides the engine with a one-second tick to perform house keeping operations relating to the motion detection. The engine will routinely poll this bit to obtain a one-second tick. This bit is cleared by the engine.

0 = Cleared by PIR engine
1 = One-Second interval has occurred

Frequency Response (Bits 3-6)

Frequency Response of PIR engine
Controlled by Application
Range: 0h - Ch

This value determines the frequency response of the motion detection system. Higher values allow lower frequencies to be accepted by the PIR engine. Lower values cause the Engine to ignore targets that generate lower frequencies. These targets typically include horizontally oriented objects such as pets.

The frequency of the signal that is presented to the PIR engine is largely dependent on the structure of the PIR lens being used (number and dispersion of beams). A lens with several evenly distributed beams provides better frequency response performance than a lens with an uneven beam distribution.

Note: Lower programmed values also have the effect of reducing the relative range of detection.

PIR Scan Rate (Bit 2)

PIR ADC conversion rate for the Pyroelectric Sensor
Controlled by application

The PIR engine performs the necessary ADC conversions on the PIR sensor input. Each conversion generates an interrupt that is processed by the PIR engine from the EPIR_ADC_ISR macro. The PIR Scan Rate bit determines the rate at which the ADC conversions are generated.

In **Normal Scan Rate Mode** (PIR Scan Rate set to 0), the Z8FS040 ADC peripheral is set to continuous conversion mode which causes a conversion to be carried out automatically every 256 system clocks. In this mode, the application is only required to execute the EPIR_ADC_ISR macro for each ADC interrupt. The ADC continually runs and continuously generates interrupts.

When **Low Scan Rate Mode** is selected by setting this bit to a 1, continuous conversion mode is disabled and the ADC is operated in single-shot mode such that each conversion takes 5129 system clocks to complete. In this mode, the application S/W must initiate the ADC conversion request (set bit 7 of ADCCTL0) and execute the EPIR_ADC_ISR macro once every 5mS.

In Low Scan Rate Mode, the ADC is disabled between conversions to reduce power consumption. Power consumption can be reduced further if the application S/W uses this mode in conjunction with the CPU's Halt or Stop modes. Alternately, this mode can be used to provide the application S/W with additional CPU processing time.

Although the Low Scan Rate Mode provides the application with more processing power and the opportunity for the system to reduce power consumption, the normal scan rate will provide better sensitivity and range. While operating in Low Scan Rate Mode, sensitivity is reduced by approximately 20%. The performance of Direction Detection may also be reduced in this mode. EMC immunity is disabled while in Low Scan Rate Mode.

If the PIR Scan Rate bit is changed during engine operation, the engine will stop detecting motion for up to 200mS to avoid potential false motion detection. When changing the PIR Scan Rate mode, the Advanced API registers must first be updated with the appropriate values.

0 = Normal Scan Rate Mode
1 = Low Scan Rate Mode

Dual Pyro Mode (Bit 0)

Dual Pyroelectric Sensor Signaling Mode
Controlled by Application

This bit determines if the PIR engine should accept signals from one or two pyroelectric sensors. When configured for single pyro operation, only one sensor is used (connected to ANA2). When configured for dual pyro operation, the engine will scan two sensors simultaneously. Dual pyro mode is typically used to provide a larger area of coverage. The second pyroelectric sensor is connected to input ANA3. In Dual Pyro Mode, motion on either sensor will generate a motion detected event.

0 = Single pyroelectric sensor mode
1 = Dual pyroelectric sensor mode

PIR Status/Control Register 2 (ePIR_SC2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved					Range Control		
Control	0					Read/Write		
Address	104H							

Range Control (Bits 0-2)

Motion Detection Range Control
Controlled by application

These bits determine the relative range of motion detection. Larger values decrease the range of detection. Typical values used for Range are dependant on the lens and pyroelectric sensor being used. Range is also dependent on target size, speed, and relative temperature. For example, a range control setting that rejects one target of a particular size at a given distance does not guarantee that a larger target will be rejected at the same distance.

PIR Status/Control Register 3 (ePIR_SC3) - 28 Pin SSOP

Bit	7	6	5	4	3	2	1	0
Field	ANA7 Scan Request	ANA6 Scan Request	ANA5 Scan Request	ANA4 Scan Request	Reserved	Reserved	ANA1 Scan Request	ANA0 Scan Request
Control	R/W	R/W	R/W	R/W	0	0	R/W	R/W
Address	105H							

PIR Status/Control Register 3 (ePIR_SC3) - 20 Pin SSOP

Bit	7	6	5	4	3	2	1	0
Field	Reserved	ANA6 Scan Request	ANA5 Scan Request	ANA4 Scan Request	Reserved	Reserved	ANA1 Scan Request	ANA0 Scan Request
Control	0	R/W Reserved in Single Pyro Mode	R/W	R/W	0	0	R/W	R/W
Address	105H							

PIR Status/Control Register 3 (ePIR_SC3) - 8 Pin SOIC

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	ANA3 Scan Request	Reserved	ANA1 Scan Request	ANA0 Scan Request
Control	0	0	0	0	R/W Reserved in Dual Pyro Mode	0	R/W	R/W
Address	105H							

ANAx Scan Request

Analog Channel 0, 1, 3-7 Scan Requested Bits
Set by Application; cleared by PIR engine

These bits allow the user application to request the Engine to perform an A/D conversion on the non-reserved analog inputs. When requested, the Engine will reconfigure the appropriate I/O pin to a single-ended, unbuffered input using a 2 Volt reference. It will then take the next sample and store it in the PIR ADC Result Value Registers and clear all ANAx Scan Request bits. The I/O configuration for the ANAx pin is not returned to its previous configuration by the Engine. If needed, the user application must do this.

If multiple request bits are set simultaneously, the Engine will only scan the lowest numbered ADC channel requested and ignore any other requests. The user application should set one request bit then poll it to determine when the conversion is complete and the data is ready.

When ADC Scan requests are being serviced by the PIR engine, ADC conversions on the PIR sensor are suspended. Therefore the user application should be careful not to continuously request ADC Scan's. The Process Rate Register in the "Advanced PIR Engine" section can be monitored to ensure the Engine is receiving enough time to perform its required PIR Sensor ADC scans.

0 = no conversion requested/last conversion completed
1 = perform a conversion on this channel

PIR ADC Result Value (ePIR_ADC_Result)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ADC Result Value															
Control	Read															
Address	10AH								10BH							

PIR ADC Result Value (Bits 0-15)

ADC Scan Request Result Value
Controlled by PIR engine

The PIR ADC Result Value contains the result of the last application requested ADC conversion.

The data format is identical to that given in the Z8 Encore XP Product Specification (PS0228) for registers ADCD_H and ADCD_L.

Example for requesting an ANA0 Conversion:

- Set bit 0 (ANA0 Scan Request) in PIR Status/Control Register 3 (ePIR_SC3)
- Wait until the ANA0 Scan Request bit is cleared by the Engine
- Read the ADC conversion result from the PIR ADC Result Value register

Note: Even though the ADC Result Value is a 16 bit register, atomic operations are not required since the value is only updated at the request of the application.

PIR Version (ePIR_Version)

Bit	7	6	5	4	3	2	1	0
Field	Version							
Control	Read							
Address	10CH							

Version (Bits 0-7)

PIR engine software version
Controlled by PIR engine

The value stored in this register indicates the software version of the PIR engine.

Value	PIR Engine Software Version
03h	2.00

Advanced API Register Set

The following registers are for advanced configuration of the PIR engine. They include customization for lens and pyroelectric sensor configurations. These registers are not initialized by the PIR engine.

API Advanced Register Name	Address	Mnemonic	Description
PIR Advanced Status/Control Register 0	F0h	ePIR_ASC0	EM noise and MD origin status
PIR Advanced Status/Control Register 2	F2h	ePIR_ASC2	Window Size, Lock Level, and Window Update Rate
PIR Process Rate	F3h/F4h	ePIR_Process_Rate	Relative Processing available to PIR engine
PIR Sample Size Register	F5h	ePIR_Sample_Size	Controls amount of sensor signal averaging
PIR Debounce Time Register	F6h	ePIR_Debounce_Time	Controls time to Debounce motion signal
PIR Debounce Batch Size Register	F7h	ePIR_Debounce_Batch	Controls out of window samples needed for Debounce
PIR Transient Sensitivity Level	F8h	ePIR_Transient_Sense	Sets PIR engine sensitivity to transient detection
PIR Noise Sensitivity Level	F9h	ePIR_Noise_Sense	Sets PIR engine sensitivity to noise detection
PIR Signal	FAh/FBh	ePIR_Signal	Current Pyro Sensor signal sample
PIR Pyro DC Signal Level	FCh/FDh	ePIR_Signal_DC	Current calculated Pyro Sensor DC offset

Table 7 - PIR Engine Advanced Registers

PIR Advanced Status/Control Register 0 (ePIR_ASC0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Buffer Refresh	New Sample	MD Origin	EM Noise Detected	EM Transient Detected
Control	0	0	0	R/W	R/W	R	R/W	R/W
Address	F0H							

Buffer Refresh (Bit 4)

Uses fast fill algorithm to quickly refill the motion detection buffers.
Controlled by application

This bit is used to restart motion detection by quickly reinitializing and refilling the motion detection constructed sample buffers. This can be used as a method to restore motion detection after waking up from sleep mode or it can be used to help ignore external events that may cause false detections.

Waking up from Sleep Mode:
If this bit is set when the EPIR_INIT macro is executed the Engine re-fills the constructed sample buffers with a fast fill algorithm that allows it to quickly restore motion detection. Typically, a simple external wake-up circuit would be implemented that provides an unqualified motion detection signal to wake up the MCU from Sleep mode (SMR). Upon SMR, the application would set the Buffer Refresh bit, execute EPIR_INIT, and then continue with normal motion detection functions for some period of time before returning to Sleep mode. By setting this bit prior to EPIR_INIT, the Engine buffers are filled much faster enabling it to analyze the original signal seen by the external wake up circuit and determine if it is 'real' motion.

Ignoring False Detection Events:
If the MCU is used to control external components (LED's, relays, Lights, Triac's, etc) a fluctuation on the power supply can be created as the external device is turned on or off. The Buffer Refresh bit can be used to ignore any false detection that could be created by these fluctuations. When the external device is turned on or off, the application can set the Buffer Refresh bit to effectively reset the motion detection history and therefore ignore any effect from the external device.

New Sample (Bit 3)

New sample available from PIR Signal High/Low register
Set by PIR engine, cleared by application

This bit indicates that the PIR engine has a new sensor signal input sample available that may be read by the application. This status is available as an advanced feature as the application is not normally required to read the sampled PIR sensor signal. The application must clear this bit when the sample has been read.

MD Origin (Bit 2)

Origin of last motion detection event
Controlled by PIR engine

This bit indicates how the PIR engine detected the last Motion Detected Event. When the engine sets the Motion Detected bit in PIRStatus0, it also sets this bit according to which detection engine registered the event.

0 – Normal Motion Detector
1 – Extended Motion Detector

EM Noise Detected (Bit 1)

EM Noise Detected on PIR Signal
Set by PIR engine; cleared by application

This bit indicates if the engine has detected noise on the PIR signal. This event is provided to the user application to indicate that an EM noise event has occurred and associated motion event(s) may have been suppressed by the engine. This bit does not have to be read for normal operation and is provided as status only. The application must clear this bit after it has been read.

EM Transient Detected (Bit 0)

EM Transient Detected on PIR Signal
Set by PIR engine; cleared by application

This bit indicates if the Engine has detected a transient on the PIR signal. This event is provided to the user application to indicate that an EM transient event has occurred and associated motion event(s) may have been suppressed by the engine. This bit does not have to be read for normal operation and is provided as status only. The application must clear this bit after it has been read.

PIR Advanced Status/Control Register 2 (ePIR_ASC2)

Bit	7	6	5	4	3	2	1	0
Field	Lock level			Window Size		Window Update Rate		
Control	R/W			R/W		R/W		
Address	F2H							

Lock Level (Bits 5-7)

Controlled by application

This parameter sets the minimum slope change in the signal that can be considered valid motion. This prevents small signal changes caused by environmental or Vcc shifts from causing a false detection. Use this value in combination with PIR Sensitivity and Range Control settings to balance sensitivity and stability to the particular lens and pyroelectric sensor being used.

- Smaller values allow subtle signals with lower slopes to be considered motion events at the expense of potential false motion events.
- Larger values allow the system to ignore smaller signal slope changes at the expense of potentially missing smaller motion events.

Window Size (Bits 3-4)

Controlled by application

This register determines the size of the control limit window. A larger window size produces more stable control limits at the cost of additional CPU usage. If a smaller window size is used, the more frequently the window can be calculated which allows it to track the signal better.

00 – Reserved
01 – Small window
02 – Medium window
03 – Large window

Window Update Rate (Bits 0-2)

Controlled by application

This register determines how frequently the control limits are calculated. It is measured in PIR samples. A smaller number produces more frequent calculations which allow the control limits to track the signal better, at the cost of increased CPU usage. The valid range is 0 to 7.

The window is updated every 4 + (Window Update Rate * 2) PIR samples.

PIR Process Rate (ePIR_Process_Rate)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PIR Process Rate															
Control	Read															
Address	F3H								F4H							

PIR Process Rate (Bits 0-7)
Controlled by PIR engine

The PIR Process Rate Indicator is provided by the Engine to determine if the user application process and interrupts overhead is impacting the performance of the Engine. If the Engine process rate drops significantly, its ability to detect motion can be significantly reduced. This value is typically used at the application development stage. This number gives an indication of how much CPU time the Engine is receiving. Higher numbers are better. Generally, if the process rate drops below 0080h, the ability to detect motion could be compromised.

Note: The 16 bit value provided by these two 8 bit registers must be read as an atomic operation by the application. This can be ensured by either using the CPU's ATM instruction or by disabling interrupts while reading the two 8 bit registers.

PIR Sample Size Register (ePIR_Sample_Size)

Bit	7	6	5	4	3	2	1	0
Field	PIR Sample Size							
Control	Read/Write							
Address	F5H							

PIR Sample Size (Bits 0-7)
Controlled by application

This register controls the amount of averaging that the engine performs on the incoming PIR signal ADC samples. More averaging improves signal noise immunity at the cost of a slower sample rate.

PIR Debounce Time Register (ePIR_Debounce)

Bit	7	6	5	4	3	2	1	0
Field	PIR Debounce Time							
Control	Read/Write							
Address	F6H							

PIR Debounce Time (Bits 0-7)
Controlled by application

This register controls the amount of time that the engine will wait to fully debounce a motion signal. Longer times result in detection of subtle motion at the cost of more potential false motion detections. Valid range is from 01h to FFh.

Using a value less than the value in the PIR Sensitivity Register will result in no motion detection.

PIR Debounce Batch Size Register (ePIR_Debounce_Batch)

Bit	7	6	5	4	3	2	1	0
Field	PIR Debounce Batch Size							
Control	Read/Write							
Address	F7H							

Debounce Batch Size (Bits 0-7)

Controlled by application

This register determines the number of consecutive out-of-window samples required in order to consider the sequence a valid debounce count. The field works as a mask. Increasing the mask size (i.e. more bits set to 1) will increase the noise immunity of the engine but result in lower sensitivity to subtle motion signals.

Valid values are 01h, 03h, 07h, 0Fh, 1Fh, 3Fh, 7Fh, and FFh.

PIR Transient Sensitivity Level (ePIR_Transient_Sense)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PIR Transient Sensitivity						
Control	0	Read/Write						
Address	F8H							

Transient Sensitivity (Bits 0-6)

Controlled by application

This register determines how sensitive the transient detection part of the engine is to sudden changes in the PIR signal. A lower number makes the engine more sensitive, at the cost of potential rejection of large signal motion (ex. warm target very close to detector).

The valid range is 0 (disabled) to 64h.

PIR Noise Sensitivity Level (ePIR_Noise_Sense)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PIR Noise Sensitivity						
Control	0	Read/Write						
Address	F9H							

Noise Sensitivity (Bits 0-6)

Controlled by application

This register determines how sensitive the noise detection part of the engine is to random noise in the PIR signal. A lower number makes the noise detector more sensitive, at the cost of potential rejection of small-signal motion (ex. Small delta between ambient and target temperature or distant target). The valid range is 0 (disabled) to a maximum value determined by the Window Size selected in the PIR Advanced Status/Control Register 2.

Window Size	Max PIR Noise Sensitivity Value	Typical Value
Small	0Ch	08h

Medium	1Dh	12h
Large	46h	2D

PIR Signal (ePIR_Signal)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PIR Signal															
Control	Read															
Address	FAH								FBH							

PIR Signal (Bits 0-15)

Controlled by PIR engine

These registers contain the last PIR signal obtained by the engine. Each time the engine generates a new PIR signal sample it will place it in these registers and set the New Sample bit in the PIR Advanced Status/Control 0 Register. This gives the application direct visibility to the PIR generated signal for debugging purposes.

Note: The 16 bit value provided by these two 8 bit registers must be read as an atomic operation by the application. This can be ensured by either using the CPU's ATM instruction or by disabling interrupts while reading the two 8 bit registers.

PIR DC Signal Level (ePIR_Signal_DC)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PIR Signal DC															
Control	Read															
Address	FCH								FDH							

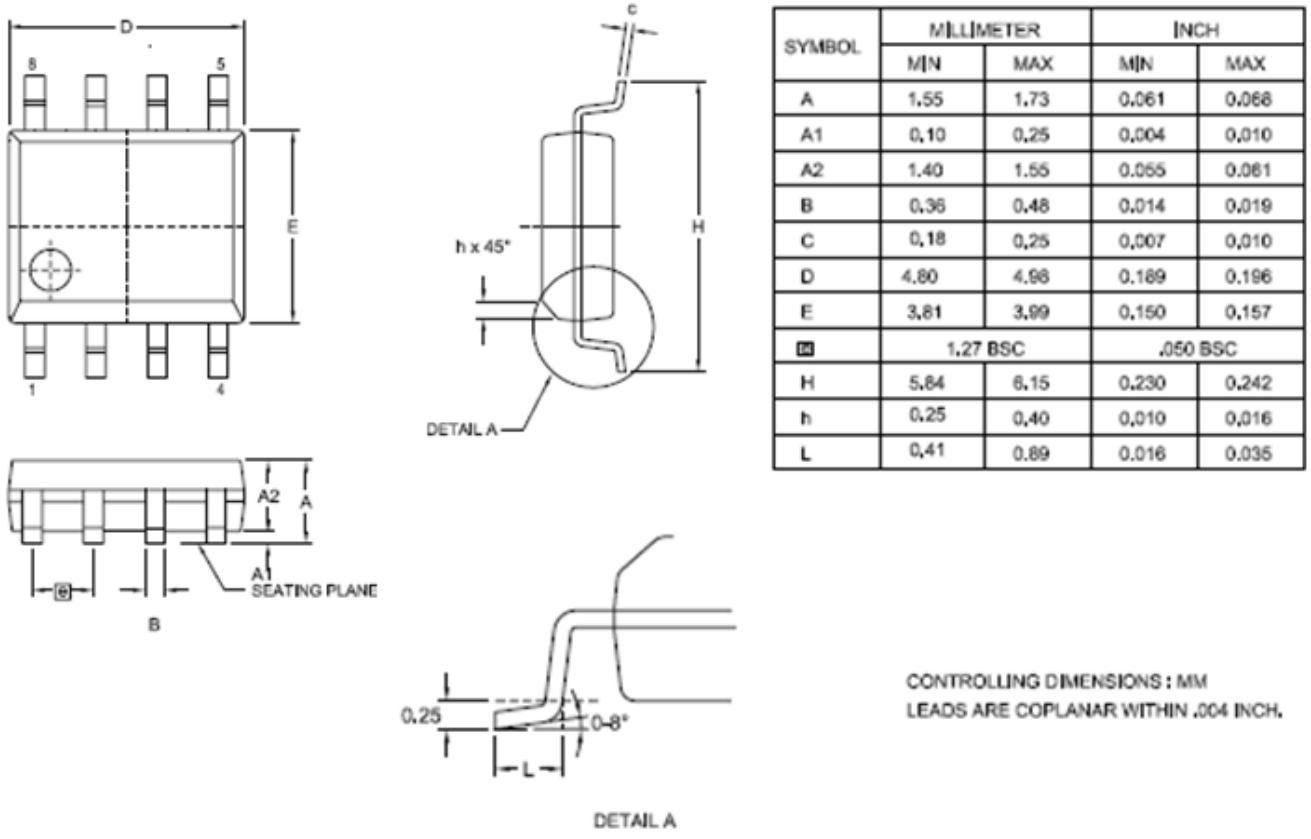
PIR Signal DC Level (Bits 0-15)

Controlled by PIR engine

These registers contain the last PIR signal DC Level calculated by the engine. Each time the engine generates new control limits it will place the DC component level in these registers.

Note: The 16 bit value provided by these two 8 bit registers must be read as an atomic operation by the application. This can be ensured by either using the CPU's ATM instruction or by disabling interrupts while reading the two 8 bit registers.

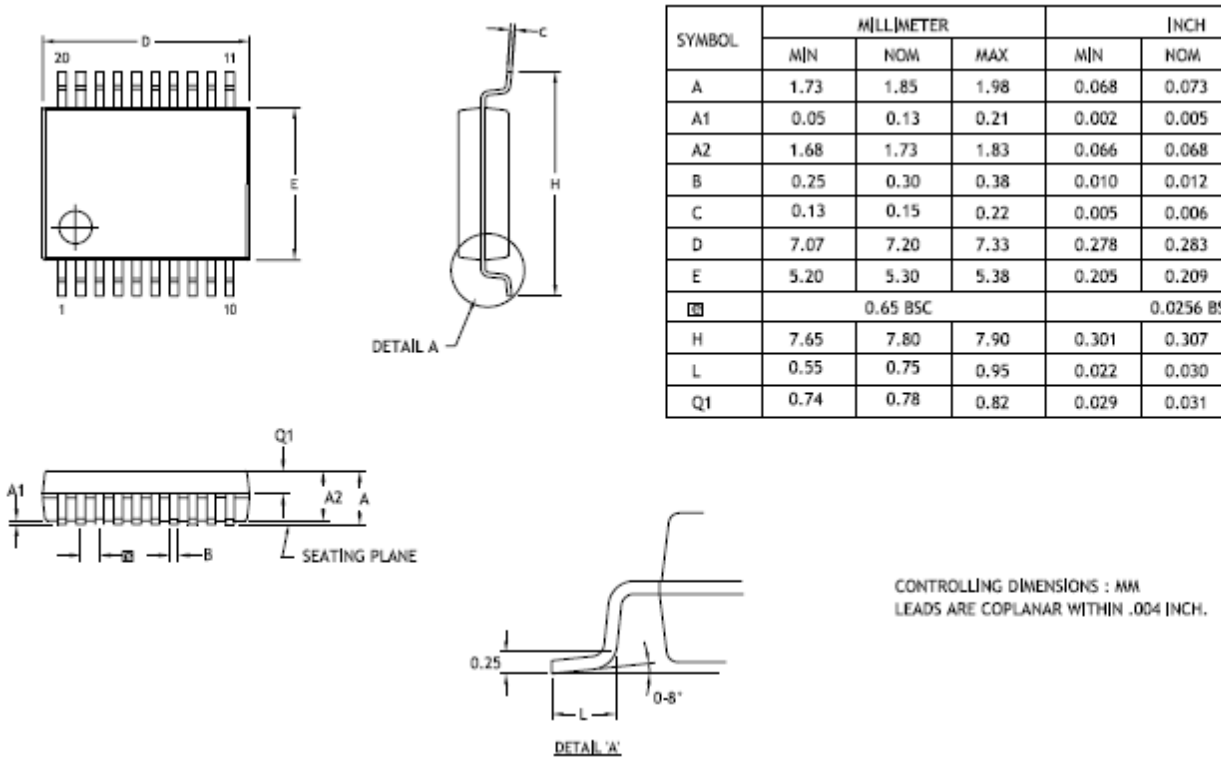
Packaging



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.55	1.73	0.061	0.068
A1	0.10	0.25	0.004	0.010
A2	1.40	1.55	0.055	0.061
B	0.36	0.48	0.014	0.019
C	0.18	0.25	0.007	0.010
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.27 BSC		.050 BSC	
H	5.84	6.15	0.230	0.242
h	0.25	0.40	0.010	0.016
L	0.41	0.89	0.016	0.035

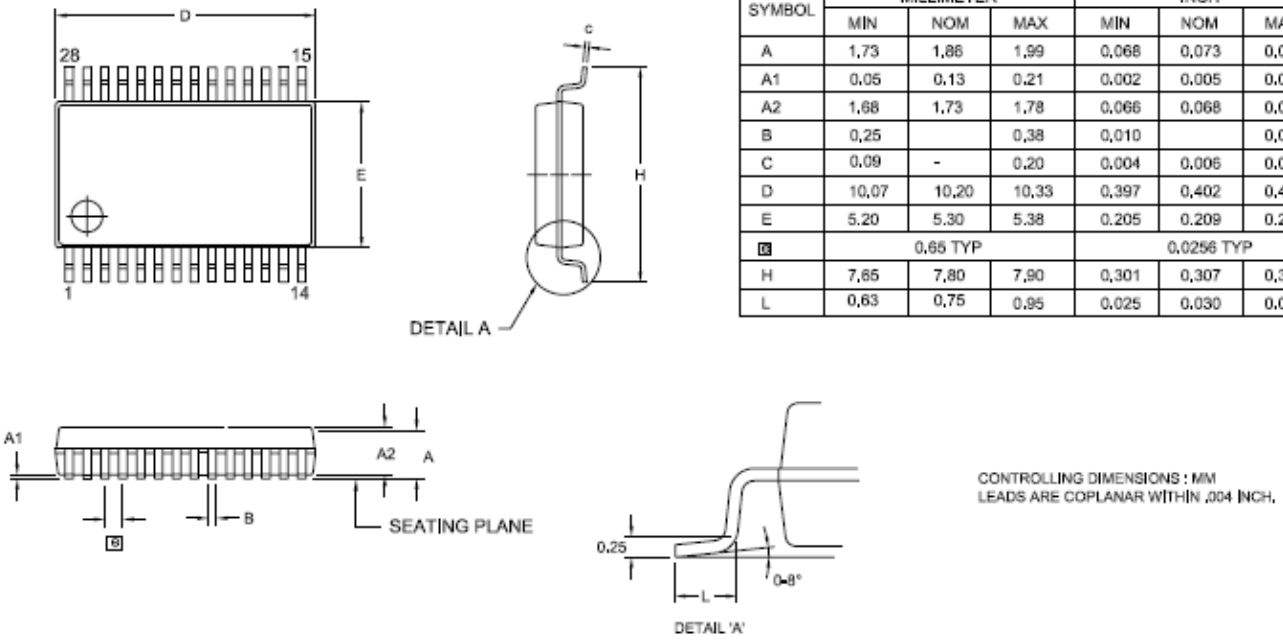
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 7 - 8-Pin Small Outline Integrated Circuit Package (SOIC)



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.55	0.75	0.95	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 8 - 20-Pin Small Shrink Outline Package (SSOP)



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1,73	1,86	1,99	0,068	0,073	0,078
A1	0,05	0,13	0,21	0,002	0,005	0,008
A2	1,68	1,73	1,78	0,066	0,068	0,070
B	0,25		0,38	0,010		0,015
C	0,09	-	0,20	0,004	0,006	0,008
D	10,07	10,20	10,33	0,397	0,402	0,407
E	5,20	5,30	5,38	0,205	0,209	0,212
e	0,65 TYP			0,0256 TYP		
H	7,65	7,80	7,90	0,301	0,307	0,311
L	0,63	0,75	0,95	0,025	0,030	0,037

Figure 9 - 28-Pin Small Shrink Outline Package (SSOP)

Ordering Information

The ZMOTION™ Detection and Control Family comprises the ZMOTION™ MCU, lens and pyroelectric sensor. Construct your part number based on the specific combination of MCU, lens and PIR sensor you wish to order. There are four fields in the part number that determine this combination.

Order the ZMOTION™ Detection and Control product from Zilog® using the following table.

Position:	1	2	3	4	5	6	7	8	9	10	11	12	13
Field	Z	M	O	T	MCU		MCU Package		Lens		PIR		G
					Selected Options								

Position 1 - 4: ZMOT - ZMOTION™ Product Family

To purchase the ZMOTION™ MCU alone, use the ZMOTION MCU part number in the following table.

Position 5, 6 & 7, 8 - MCU and MCU Package Selector:

MCU Part Number	Description	PIR Software Revision	MCU Field (Pos 5, 6)	MCU Package Field (Pos 7, 8)
Z8FS040xSB20EG	Occupancy, 8 pin SOIC	2.00	0B	SB
Z8FS040xHH20EG	Occupancy, 20 pin SSOP	2.00	0B	HH
Z8FS040xHJ20EG	Occupancy, 28 pin SSOP	2.00	0B	HJ

Note: The second digit of the MCU field refers to the PIR software engine revision

Position 9, 10 & 11, 12 - Lens and PIR Sensor Selector:

Manufacturer	Part Number	Description	Lens Field (Pos 9, 10)	PIR Sensor	PIR Field (Pos 11, 12)
Fresnel Technologies	AA 0.9 GI T1	Animal Alley Array (88°)	0A	RE200B-P	0A
				SDA02-54-P	0B
Fresnel Technologies	CM 0.77 GI V3	Ceiling Mount Array (360°)	0B	RE200B-P	0A
				SBDI46-504AA	0C
Fresnel Technologies	CM 0.77 GI V5	Ceiling Mount Array (360°)	0C	RE200B-P	0A
				SBDI46-504AA	0C
Fresnel Technologies	CWM 0.5 GI V1	Ceiling/Wall Mount Array (360°)	0D	RE200B-P	0A
				SBDI46-504AA	0C
Nicera	NCL-9(26)	Clip-on 15mm Array (360°)	1A	RE200B-P	0A
				SBDI46-504AA	0C

Position 13 – Environmental

'G' = RoHS Compliant

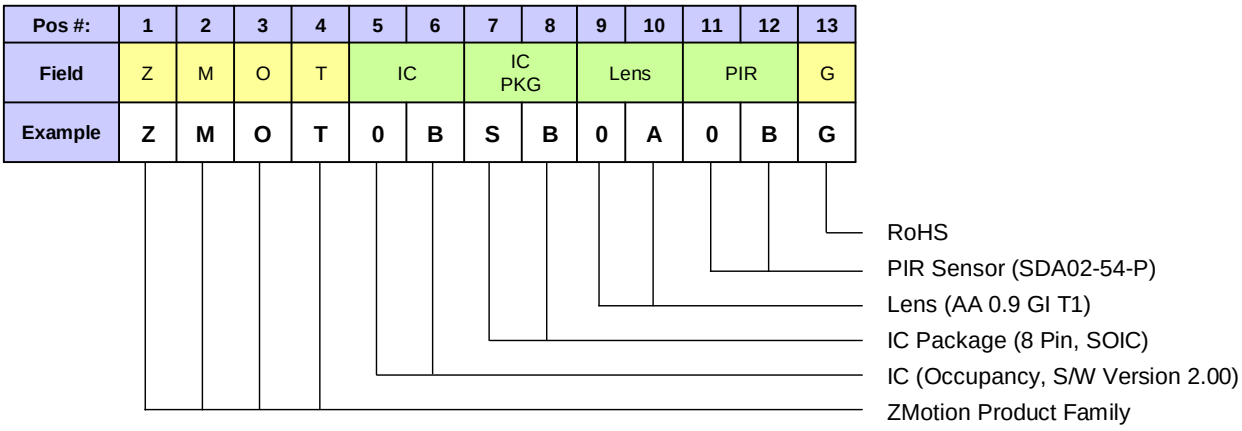
PIR Sensor Information:

Manufacturer	Part Number	Description
Nicera	RE200B-P	Basic Dual Element
Nicera	SDA02-54-P	Premium Dual Element
Nicera	SBDI46-504AA	Quad Element

Refer to Product Specification PS0286 for details on the Lens and Pyroelectric sensors.

Ordering Example:

Part Number: ZMOT0BSB0A0BG



For more information on ordering, please consult your local Zilog sales office. The Zilog website (www.zilog.com) lists all regional offices and provides additional product information.

Related Documents

Additional information can be found in the following documents. These are available from the Zilog website (www.zilog.com).

Document Number	Description
PS0286	ZMOTION™ Lens and Pyroelectric Sensor Product Specification
PB0225	ZMOTION™ Detection and Control Product Brief
PS0228	Z8 Encore! XP® F082A Series Product Specification
PB0223	ZMOTION™ Detection Module Product Brief
PS0284	ZMOTION™ Detection Module Product Specification
WP0017	A New PIR Motion Detection Architecture White Paper

Appendix A

Example Application Schematics

Z8FS040xSB20EG - (8 Pin)

Figure 10 shows an example circuit for the 8 pin device of the ZMOTION™ Detection and Control MCU Family. The interface to the pyroelectric sensor is via the dedicated input ANA2 (pin 5). The status LED is driven by pin 6 which is normally configured as a GPIO by the application to control the state of the LED. Pin 2 is used as the debug input to the chip, but can be used for other functions as required. Pin 4 is set up for the Reset function, but may also be used for other functions as the application requires. Pull-up resistors (10K) are provided on the Debug and Reset signals as required for the Debug interface. The signals on pins 3 and 7 can be used as needed. The power supply design is left to the application needs.

In Dual Pyro mode, the second Pyroelectric sensor is connected to Pin 3 (ANA3). All other connections remain the same.

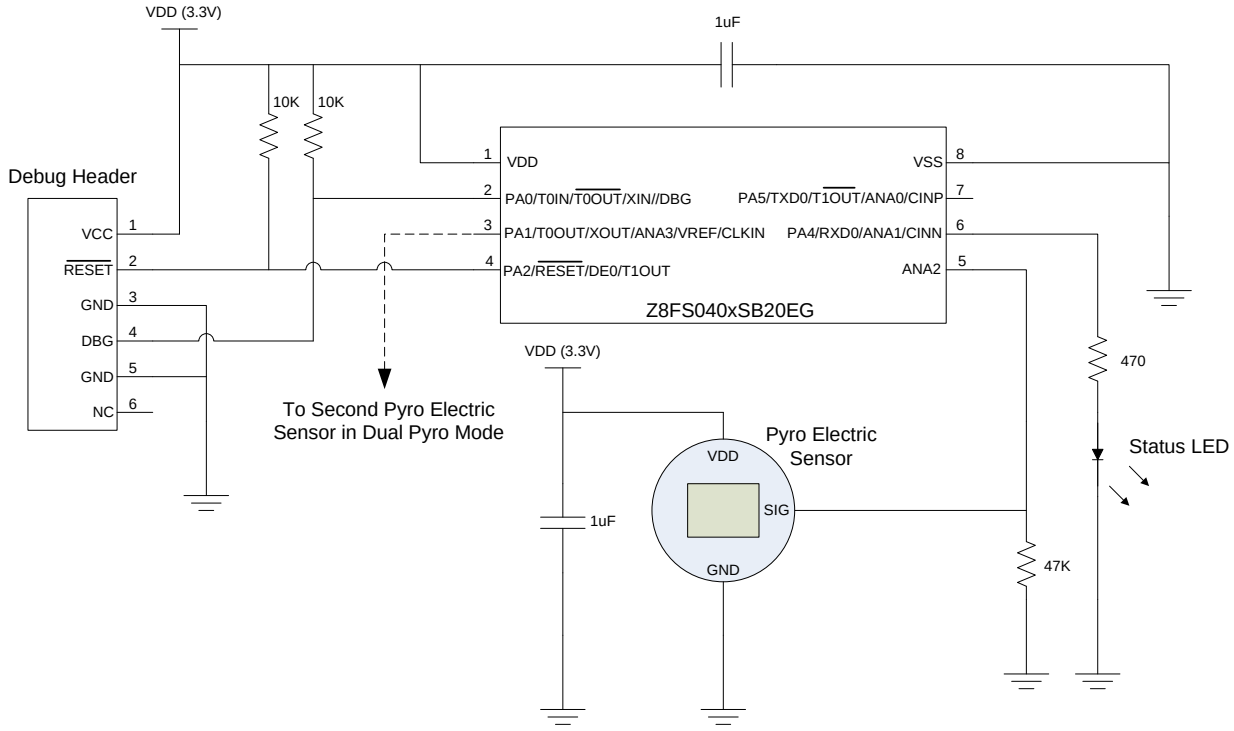


Figure 10 - Required Circuit Connections of Z8FS040xSB20EG (8 Pin) Motion Detection MCU

Z8FS040xHH20EG - (20 Pin)

Single Pyroelectric Sensor

Figure 11 shows an example circuit for the 20 pin device of the ZMOTION™ Detection and Control MCU Family with a single Pyro Electric sensor. The interface to the pyroelectric sensor is via the dedicated input ANA2 (pin 2). V_{REF} (pin 18) must be externally tied to ANA3 (pin 3). The status LED is driven by pin 19 (PC3/COUT) which is normally configured as a GPIO by the application to control the state of the LED. This pin provides a programmable constant current sink specifically for LED drive without using an external resistor. Pin 15 is dedicated as the Debug pin and is connected to pin 4 of the Debug Header. Pin 14 is set up for the Reset function, but may also be used as PD0 (general purpose I/O) as the application requires. Pull-up resistors (10K) are provided on the Debug and Reset signals as required for the Debug interface. All other signals may be used as needed. The power supply design is left to the application needs.

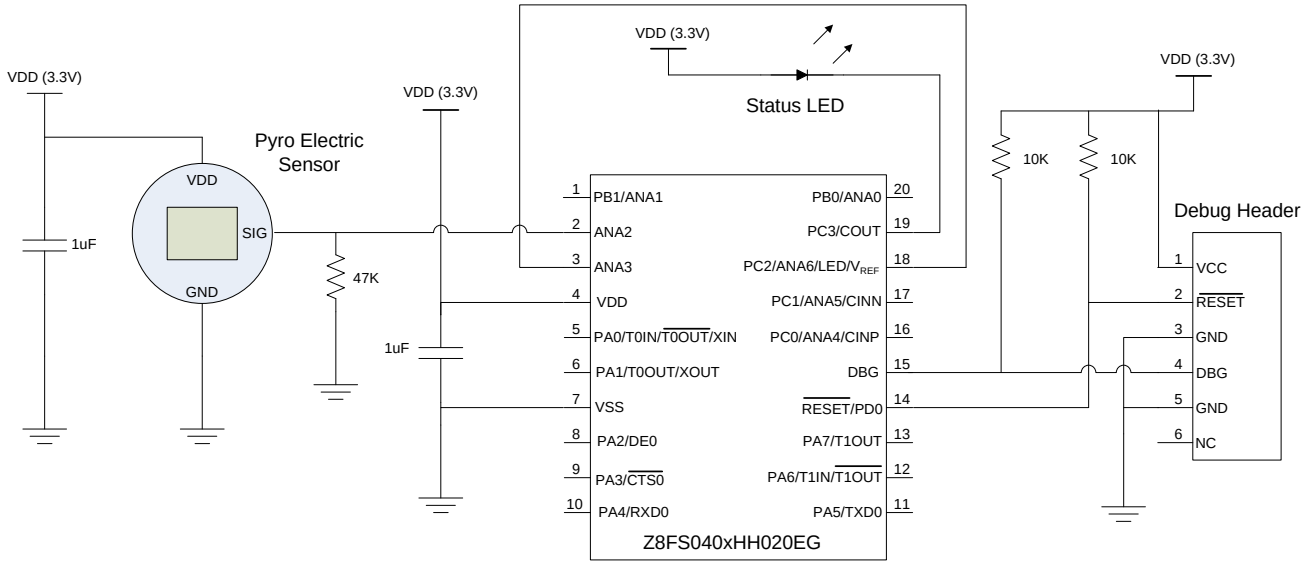


Figure 11 - Required Circuit Connections of Z8FS040xHH20EG (20 Pin) Motion Detection MCU – Single Pyro Mode

Dual Pyroelectric Sensors

In Dual Pyro mode, the second pyroelectric sensor is connected to ANA3. The signal from V_{REF} to ANA3 is not required. All other connections remain the same as Single Pyro Mode.

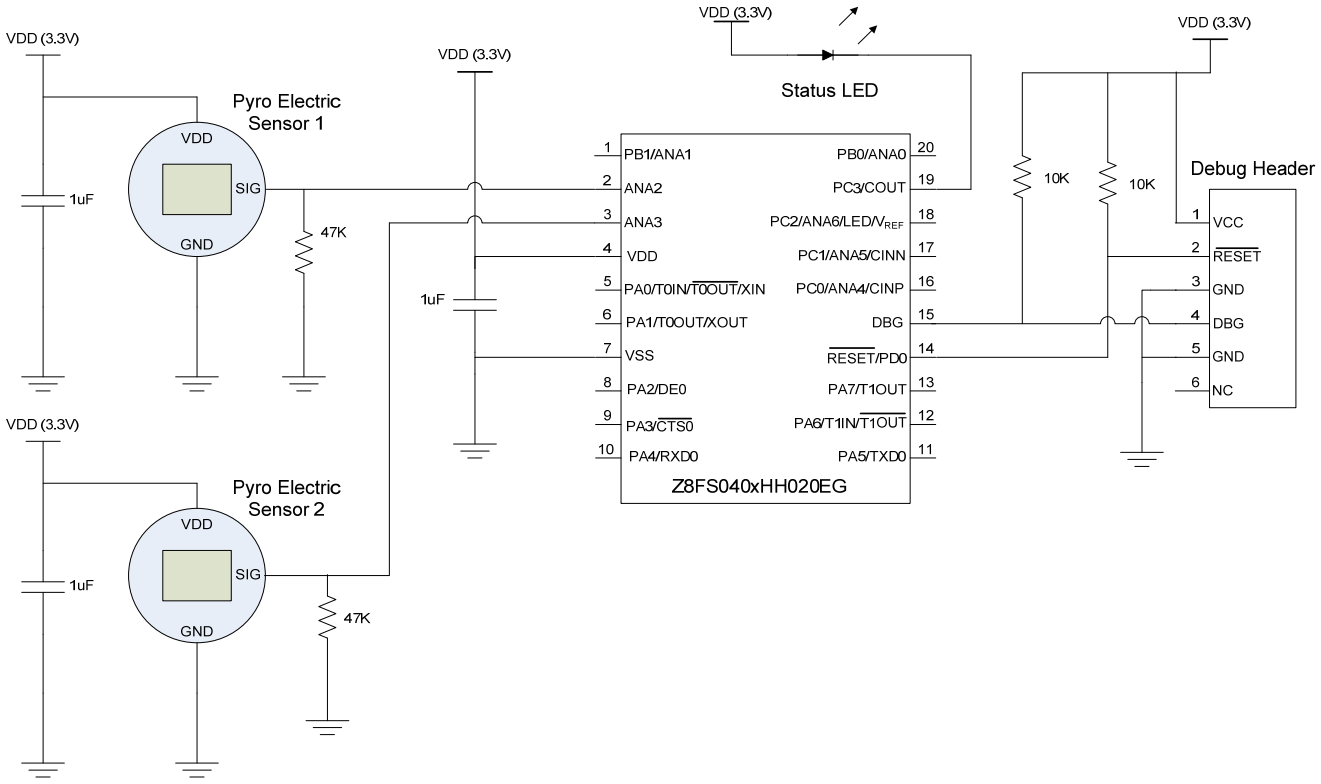


Figure 12 - Required Circuit Connections for Z8FS040xHH20EG (20 Pin) Motion Detection MCU – Dual Pyro Mode

Z8FS040xHJ20EG - (28 Pin)

Single Pyroelectric Sensor

Figure 13 shows an example circuit for the 28 pin device of the ZMOTION™ Detection and Control MCU Family with a single Pyroelectric sensor. The interface to the pyroelectric sensor is via the dedicated input ANA2 (pin 1). V_{REF} (pin 3) must be externally tied to ANA3 (pin 4). The status LED is driven by pin 26 (PC3/COUT) which is normally configured as a GPIO by the application to control the state of the LED. This pin provides a programmable constant current sink specifically for LED drive without using an external resistor. Pin 22 is dedicated as the Debug pin and is connected to pin 4 of the Debug Header. Pin 21 is set up for the Reset function, but may also be used as PD0 (general purpose I/O) as the application requires. Pull-up resistors (10K) are provided on the Debug and Reset signals as required for the Debug interface. All other signals may be used as needed. The power supply design is left to the application needs.

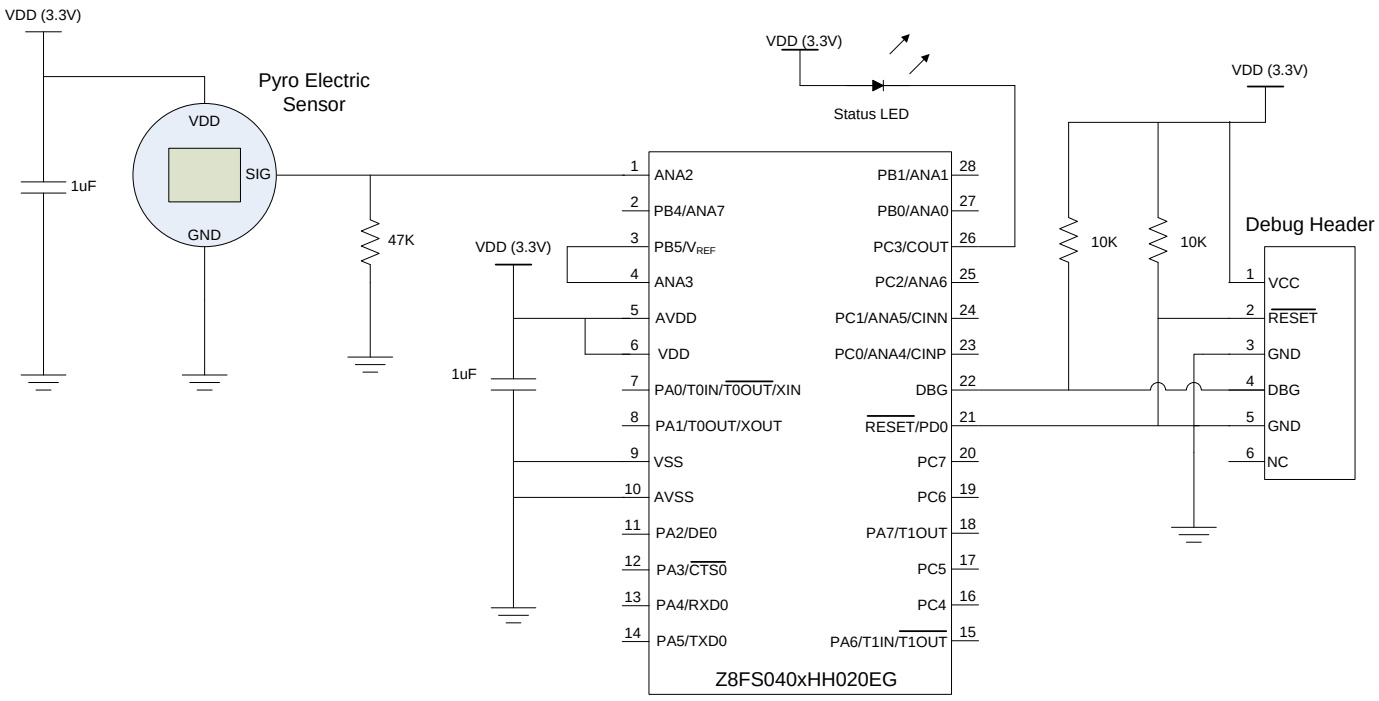


Figure 13 - Required Circuit Connections of Z8FS040xHJ20EG (28 Pin) Motion Detection MCU – Single Pyro Mode

Dual Pyroelectric Sensors

In Dual Pyro mode, the second pyroelectric sensor is connected to ANA3. The signal from V_{REF} to ANA3 is not required. All other connections remain the same as Single Pyro Mode.

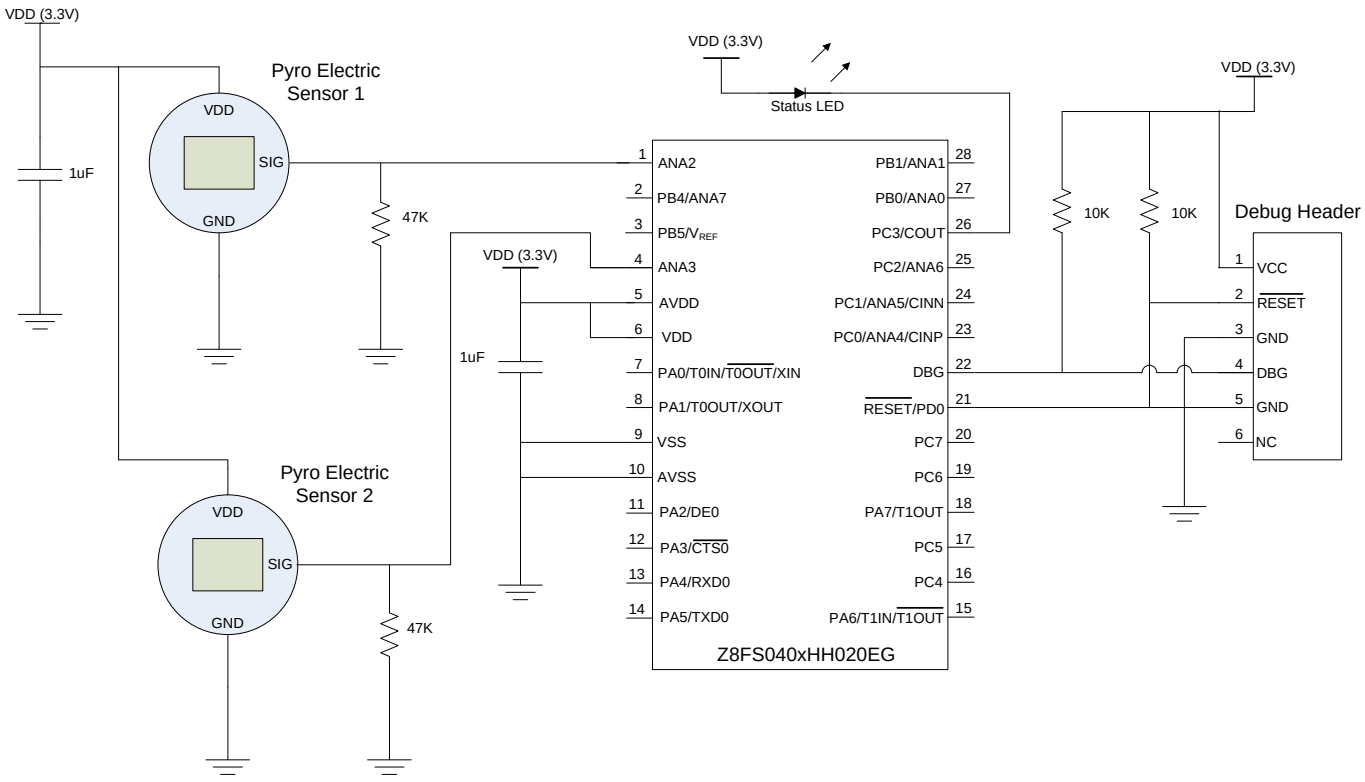


Figure 14 - Required Circuit Connections for Z8FS040xHJ20EG (28 Pin) Motion Detection MCU – Dual Pyro Mode

Appendix B

PIR Engine Initialization and Control

Description

The application software must execute an initialization procedure to enable the PIR engine. Once the PIR engine is enabled, it runs in the background from the ADC interrupt. Every ADC conversion generates an interrupt and the PIR engine performs its functions during this time. The user application code runs in the foreground and monitors the status through the API and performs any other functions required for the application.

The PIR engine also requires a one-second tick to perform several house-keeping operations and to keep track of its sampling rate. This needs to be provided by the user application through Status/Control Register 1 (Engine Timer Tick). This bit should be set to a 1-once per second by the application software to provide the engine with a 1-second time base. The accuracy of this time is not critical, but should be within +/- 10%.

There are two basic modes in which the PIR engine operates: Normal Scan Rate mode and Low Scan Rate mode. See description of the PIR Scan Rate bit in the PIR Status/Control Register 1 for more details.

The PIR engine runs in the background from the ADC interrupt (initiated by the application). Engine processing is done during the ADC interrupt. Therefore CPU loading is based on the sample rate of the ADC. To ensure a consistent sample rate the Engine needs to know the MCU operating frequency (System Clock Frequency). It uses the Flash Frequency Control Registers to determine the operating frequency which must be initialized prior to starting the Engine.

The Flash Frequency High (FFREQH) and Flash Frequency Low Byte (FFREQL) registers combine to form a 16-bit value FFREQ primarily to control timing for Flash program and erase functions. This value is also used by the PIR software engine to calculate the required sample rate of the ADC and other functions. The 16-bit value for FFREQ is the System Clock Frequency in KHz and is calculated using the following equation.

$$FFREQ[15:0] = \{FFREQH[7:0],FFREQL[7:0]\} = (\text{System Clock Frequency})/1000$$

Basic steps for initializing the PIR engine – this process is common to both Normal Scan Rate and Low Scan Rate modes:

1. Set up API control registers (standard and advanced)
2. Initialize FFREQH and FFREQL registers with MCU clock frequency
3. Write PIR Enable Pattern to PIR Enable Register
4. Call PIR Init
5. Initialize any Application specific I/O and peripherals
6. Enable interrupts
7. Ensure PIR Sensor Stable bit (ePIR_SC0:0) is set
8. Continue with application

The following flow diagram shows the general S/W operation for Normal Scan Rate mode.

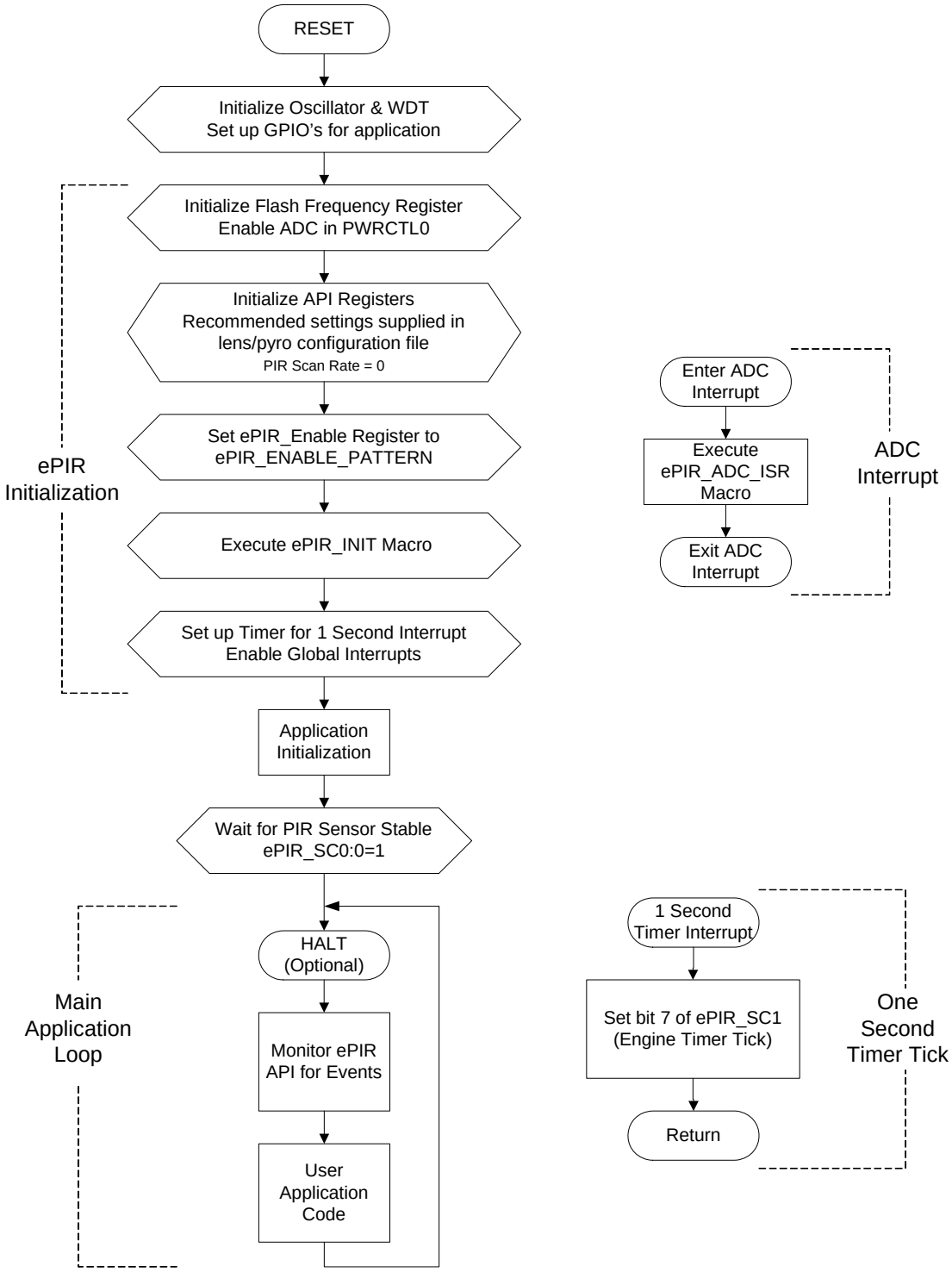


Figure 15 - Application Flow Diagram - Normal Scan Rate

The following flow diagram shows the general S/W operation for Low Scan Rate mode.

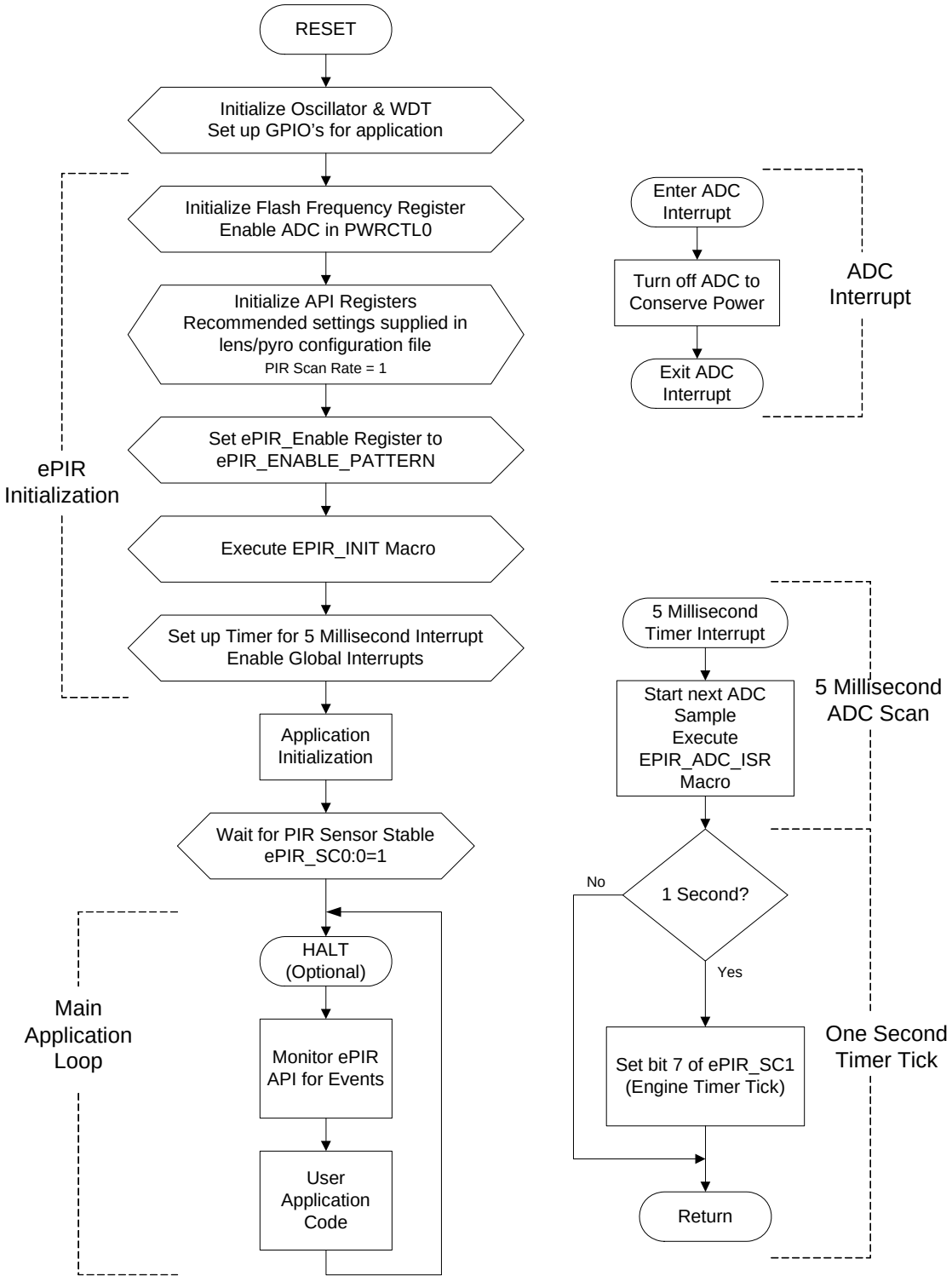


Figure 16 - Software Flow Diagram – Low Scan Mode

Appendix C

Software Support Files and Project Configuration

The following four files are provided to support the PIR engine:

1. **ePIR_API.c:** Contains the API register definitions and locates them at their appropriate places in memory.
2. **ePIR_API.h:** Provides the bit definitions for the API registers and also contains the macro definitions for EPIR_INIT and EPIR_ADC_ISR
3. **API_INIT_xx.h:** This header file contains the default API settings specific to the lens and pyroelectric sensor being used. The application code loads the API registers with these values prior to executing the EPIR_INIT macro. Several versions of this file are available from the zilog website with tested configurations supporting the available lenses and pyroelectric sensors. Refer to Appendix D to select the appropriate API_INIT_xx file for the selected lens.
4. **startupePIR.asm:** This is the C startup file that replaces startups.asm or startupl.asm in ZDS-II. It contains the environment initialization, stack and register pointer configurations required specifically for a PIR project.

ZDS-II Project Settings

Zilog Developer Studio (ZDS-II) is used for S/W development. Since the compiled application code has no vision into the operation of the PIR engine, it is important to ensure that the application working RAM area is not effected by engine operations. To facilitate this, the PIR engine uses working register group E (addresses E0h to EFh) as its working RAM area and the application code uses working register group 0 (as defined in startupePIR.asm). These operations are automatically handled by the compiler and examples are provided with the available sample projects.

The Small Memory Model must be used for the application S/W.

To support the defined memory map, ZDS-II project settings must be configured as follows (sample projects are available that have these settings already configured).

Application Project Settings (Small Model)

- RData: 20h-6Fh, F0h-FFh
  - Defined in ZDS-II Project Settings under Linker Address Spaces
  - This allows for 16 bytes of stack space starting at 7Fh. If more space is needed, reduce the 6Fh value.
  - The compiler uses address 00h to 0Fh for working registers
  - Address range 10h to 1Fh is the working register group reserved for first level interrupt
  - If more than 1 level of interrupt nesting is needed by the application, the 20h must be increased by 10h for every additional nesting level.

    - Address range F0h to FFh contains the Advanced API Registers

- EData: 100h-10Fh, 110h-18Fh
    - Defined in ZDS-II Project Settings under Linker Address Spaces
    - Address range 100h to 10Fh contains the Standard API Registers
- SP = 80h
    - Defined in startupePIR.asm
    - First stack location is 7Fh and it grows down
- RP = 00h
    - Defined in startupePIR.asm
    - The application code uses working register group 0
- __intrp = 10h
    - Defined in startupePIR.asm
    - First level interrupt uses working register group 1
- Engine RP = E0h
    - This is the working register group used by the PIR engine
    - Defined by the Engine Entry macro's EPIR_INIT and EPIR_ADC_ISR

Appendix D

Use the following table to help select the lens most appropriate to your application. The configuration file listed contains the optimal API settings for that particular lens and should be included with your ZMOTION™ project.

Refer to Product Specification PS0286 for lens usage and details.

Lens Selection Guide

Manufacturer	Part Number	Description	Typical Applications	Configuration Header File
Fresnel Technologies	AA 0.9 GI T1	Animal Alley Array (88°) 35.6mm x 49.9mm Flat Fresnel 22.9mm Focal Length 25 Meter Range 22 equal segments	Corner wall mount or very high ceiling with rectangular floor pattern • Warehouse Lighting (Bay Light) • Large area Lighting Control • HVAC	PIR_INIT_01.h
Fresnel Technologies	CM 0.77 GI V3	Ceiling Mount Array (360°) 37mm diameter circular lens 19.6mm focal length 3.7m radius at 2.4m height 3:1 floor coverage diameter to height ratio	Ceiling Mount for standard commercial heights • Lighting Control • HVAC Control • Meeting rooms	PIR_INIT_02.h
Fresnel Technologies	CM 0.77 GI V5	Ceiling Mount Array (360°) 37mm diameter circular lens 19.6mm focal length 12.2m radius at 12.2m height 2:1 floor coverage diameter to height ratio	High Ceiling mount for commercial and industrial applications • Commercial Lighting Control • Commercial HVAC Control	PIR_INIT_03.h
Fresnel Technologies	CWM 0.5 GI V1	Ceiling/Wall Mount Array (180°) Circular lens with 24mm x 24mm square base 14.2mm focal length Board mount clip-in	Wall or ceiling mount for office or meeting room lighting and HVAC control • Room Lighting Control HVAC Control	PIR_INIT_04.h
Nicera	NCL-9(26)	Clip-on 15mm Array (360°) Clips on to pyroelectric sensor 2.25m radius at 2m height 2.1:1 Floor coverage diameter to height ratio	Room Occupancy and Proximity Sensing • Lighting Control • HVAC Control • Appliance • Kiosk/Display Control • Vending Power Management Appliance • Kiosk • Power Management	PIR_INIT_05.h

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