

# MC74LVX259

## 8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74LVX259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The LVX259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the LVX259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74LVX259 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74LVX259 to be used to interface 5.0 V circuits to 3.0 V circuits.

### Features

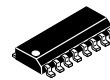
- High Speed:  $t_{PD} = 7.0$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- CMOS-Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



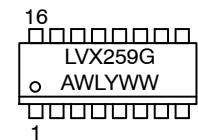
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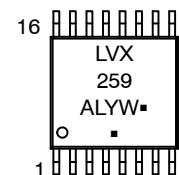
### MARKING DIAGRAMS



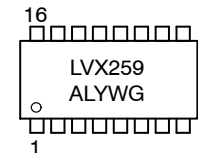
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
M SUFFIX  
CASE 966



LVX259 = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MC74LVX259

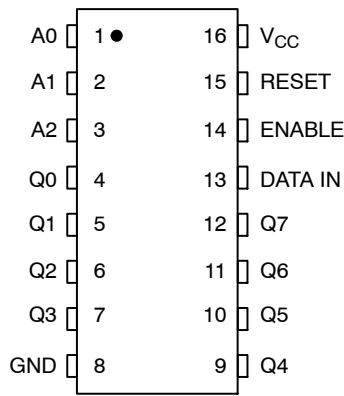


Figure 1. Pin Assignment

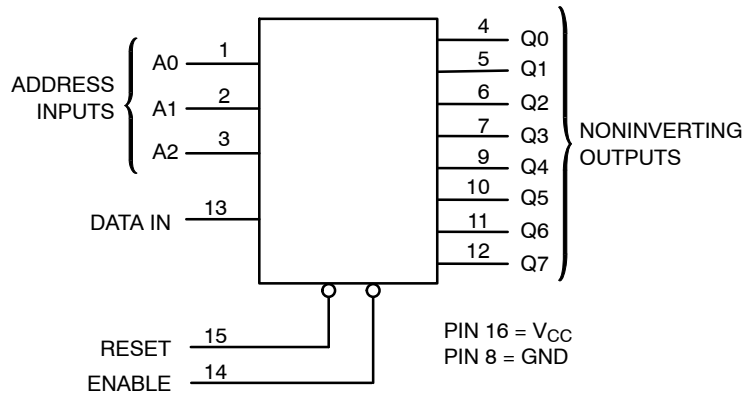


Figure 2. Logic Diagram

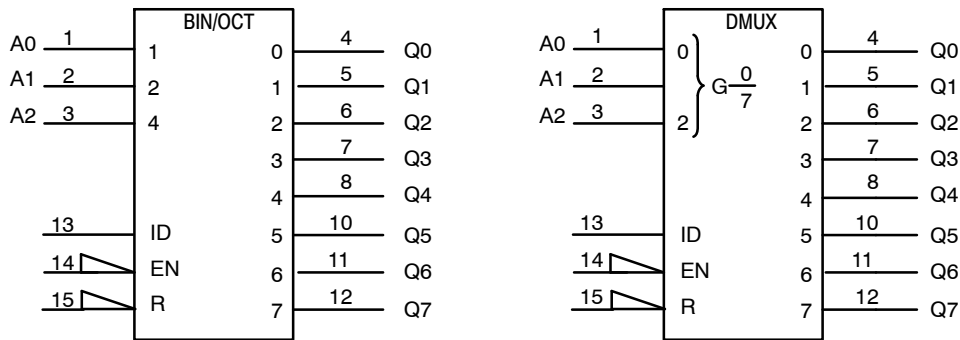


Figure 3. IEC Logic Symbol

MODE SELECTION TABLE

| Enable | Reset | Mode                 |
|--------|-------|----------------------|
| L      | H     | Addressable Latch    |
| H      | H     | Memory               |
| L      | L     | 8-Line Demultiplexer |
| H      | L     | Reset                |

LATCH SELECTION TABLE

| Address Inputs |   |   | Latch Addressed |
|----------------|---|---|-----------------|
| C              | B | A |                 |
| L              | L | L | Q0              |
| L              | L | H | Q1              |
| L              | H | L | Q2              |
| L              | H | H | Q3              |
| H              | L | L | Q4              |
| H              | L | H | Q5              |
| H              | H | L | Q6              |
| H              | H | H | Q7              |

# MC74LVX259

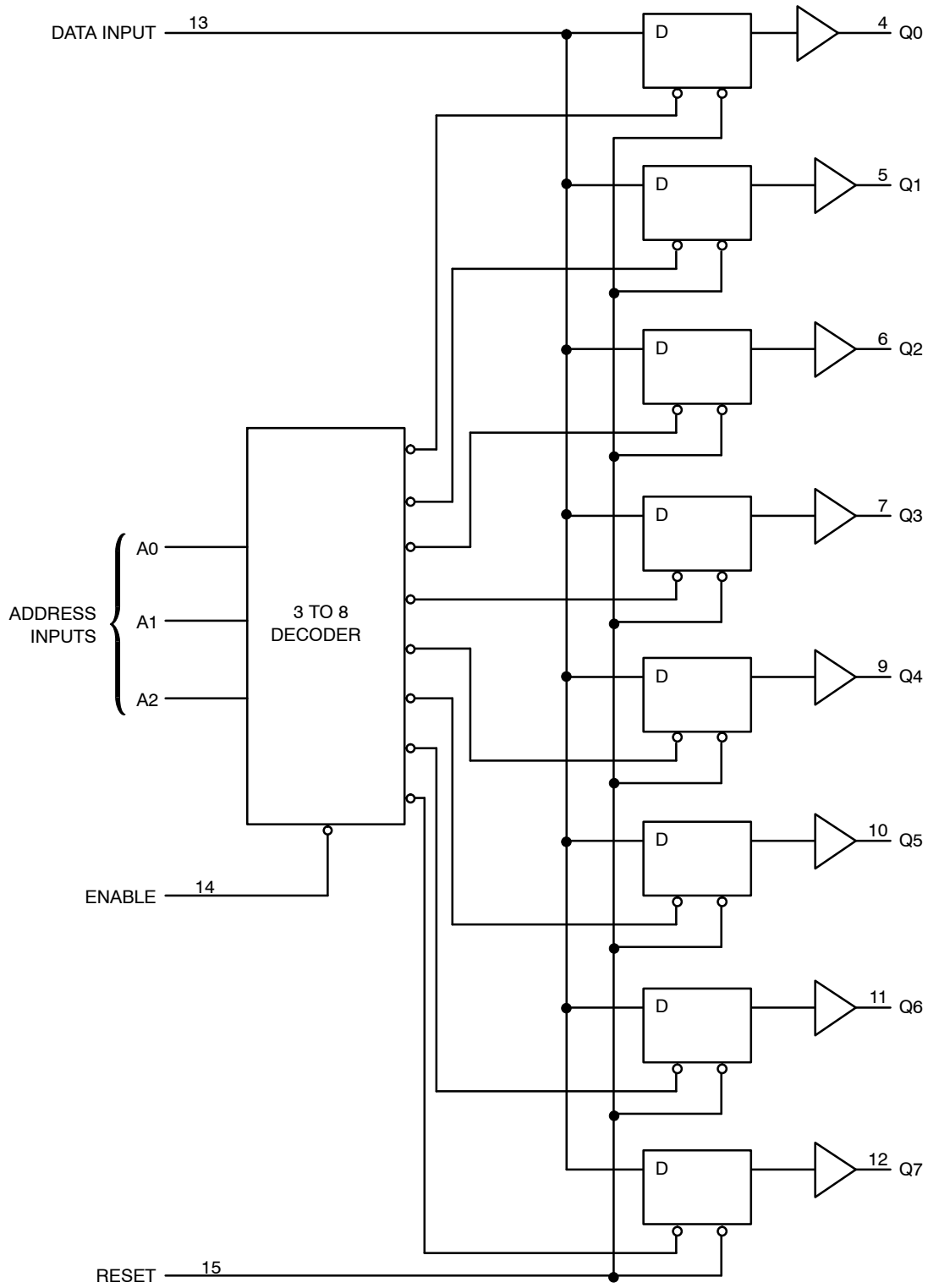


Figure 4. Expanded Logic Diagram

# MC74LVX259

## MAXIMUM RATINGS

| Symbol               | Parameter                                       | Value  | Unit        |
|----------------------|---|--|-------------|
| V <sub>CC</sub>      | Positive DC Supply Voltage                      | -0.5 to +7.0   | V           |
| V <sub>IN</sub>      | Digital Input Voltage                           | -0.5 to +7.0   | V           |
| V <sub>OUT</sub>     | DC Output Voltage                               | -0.5 to V <sub>CC</sub> +0.5   | V           |
| I <sub>IK</sub>      | Input Diode Current                             | -20  | mA          |
| I <sub>OK</sub>      | Output Diode Current                            | ± 20   | mA          |
| I <sub>OUT</sub>     | DC Output Current, per Pin                      | ± 25   | mA          |
| I <sub>CC</sub>      | DC Supply Current, V <sub>CC</sub> and GND Pins | ± 75   | mA          |
| P <sub>D</sub>       | Power Dissipation in Still Air                  | SOIC Package<br>200<br>TSSOP<br>180  | mW          |
| T <sub>STG</sub>     | Storage Temperature Range                       | -65 to +150  | °C          |
| V <sub>ESD</sub>     | ESD Withstand Voltage                           | Human Body Model (Note 1)<br>>2000<br>Machine Model (Note 2)<br>>200<br>Charged Device Model (Note 3)<br>>2000 | V           |
| I <sub>LATCHUP</sub> | Latchup Performance                             | Above V <sub>CC</sub> and Below GND at 125°C (Note 4)  | ± 300<br>mA |
| θ <sub>JA</sub>      | Thermal Resistance, Junction-to-Ambient         | SOIC Package<br>143<br>TSSOP<br>164  | °C/W        |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

| Symbol                          | Characteristics                                | Min                             | Max             | Unit |
|---------------------------------|--|---------------------------------|-----------------|------|
| V <sub>CC</sub>                 | DC Supply Voltage                              | 2.0                             | 3.6             | V    |
| V <sub>IN</sub>                 | DC Input Voltage                               | 0                               | 5.5             | V    |
| V <sub>OUT</sub>                | DC Output Voltage                              | 0                               | V <sub>CC</sub> | V    |
| T <sub>A</sub>                  | Operating Temperature Range, all Package Types | -40                             | 85              | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input Rise or Fall Time                        |                                 |                 |      |
|                                 |  | V <sub>CC</sub> = 3.3 V ± 0.3 V |                 |      |
|                                 |  | 0                               | 100             | ns/V |



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## TIMING REQUIREMENTS Input $t_r = t_f = 3.0$ ns

| Symbol     | Parameter  | Test Conditions                          | $T_A = 25^\circ\text{C}$ |     |     | $T_A \leq 85^\circ\text{C}$ |     | Unit |
|------------|--|--|--------------------------|-----|-----|-----------------------------|-----|------|
|            |  |  | Min                      | Typ | Max | Min                         | Max |      |
| $t_w$      | Minimum Pulse Width, Reset or Enable (Figure 8)              | $V_{CC} = 2.7\text{ V}$                  | 4.5                      | -   | -   | 5.0                         | -   | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 4.5                      | -   | -   | 5.0                         | -   |      |
| $t_{su}$   | Minimum Setup Time, Address or Data to Enable (Figure 8)     | $V_{CC} = 2.7\text{ V}$                  | 4.0                      | -   | -   | 4.0                         | -   | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 3.0                      | -   | -   | 3.0                         | -   |      |
| $t_h$      | Minimum Hold Time, Enable to Address or Data (Figure 7 or 8) | $V_{CC} = 2.7\text{ V}$                  | 2.0                      | -   | -   | 2.0                         | -   | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 2.0                      | -   | -   | 2.0                         | -   |      |
| $t_r, t_f$ | Maximum Input, Rise and Fall Times (Figure 5)                | $V_{CC} = 2.7\text{ V}$                  | -                        | -   | 400 | -                           | 300 | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | -                        | -   | 300 | -                           | 300 |      |

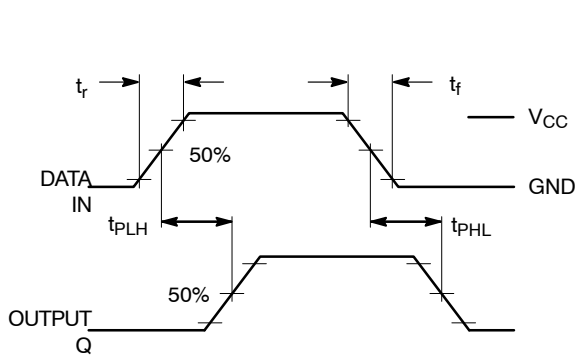


Figure 5. Switching Waveform

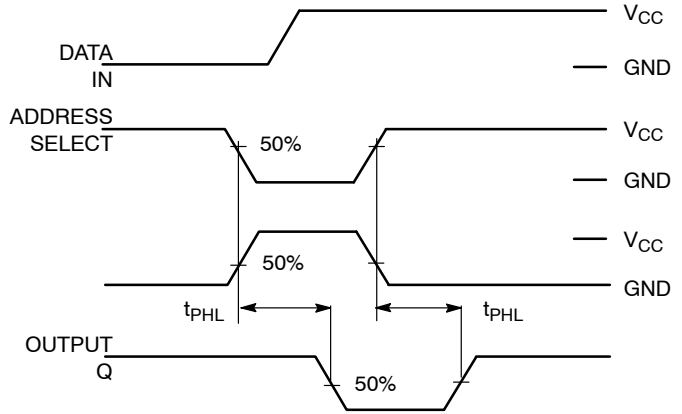


Figure 6. Switching Waveform

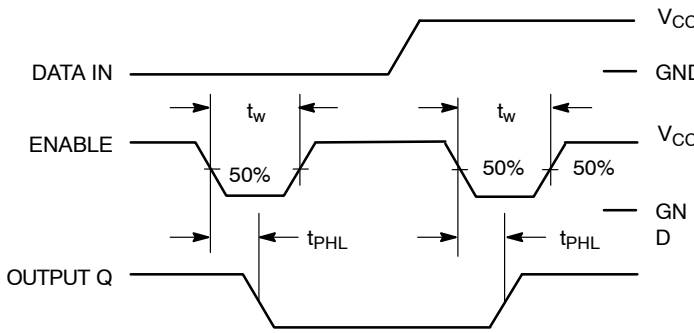


Figure 7. Switching Waveform

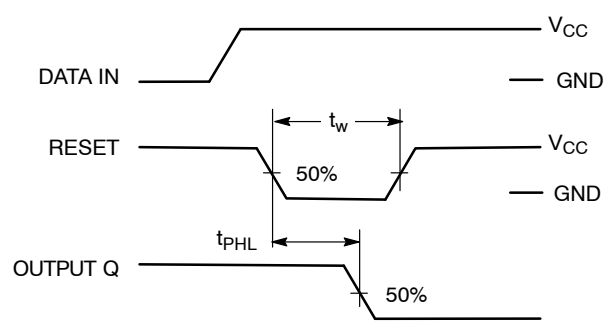


Figure 8. Switching Waveform

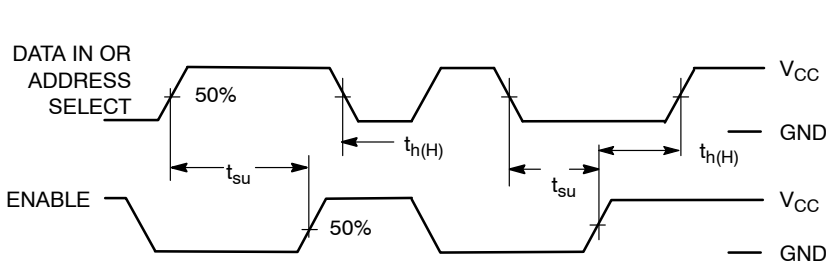
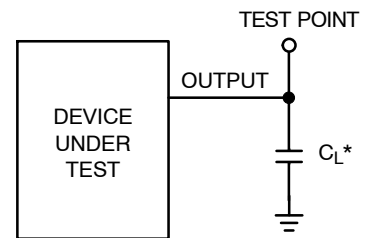


Figure 9. Switching Waveform



\*Includes all probe and jig capacitance

Figure 10. Test Circuit

# MC74LVX259

## ORDERING INFORMATION

| Device          | Package                | Shipping <sup>†</sup> |
|-----------------|------------------------|-----------------------|
| MC74LVX259DG    | SOIC-16<br>(Pb-Free)   | 48 Units / Rail       |
| MC74LVX259DR2G  | SOIC-16<br>(Pb-Free)   | 2500 Tape & Reel      |
| MC74LVX259DTG   | TSSOP-16*              | 96 Units / Rail       |
| MC74LVX259DTR2G | TSSOP-16*              | 2500 Tape & Reel      |
| MC74LVX259MG    | SOEIAJ-16<br>(Pb-Free) | 50 Units / Rail       |
| MC74LVX259MELG  | SOEIAJ-16<br>(Pb-Free) | 2000 Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

| Tape Size | B <sub>1</sub> Max  | D   | D <sub>1</sub>            | E                                     | F                                      | K                          | P  | P <sub>0</sub>                       | P <sub>2</sub>                       | R                | T                 | W                                     |
|-----------|---------------------|---|---------------------------|---------------------------------------|--|----------------------------|--|--------------------------------------|--------------------------------------|------------------|-------------------|---------------------------------------|
| 8 mm      | 4.35 mm<br>(0.179") | 1.5 mm<br>+ 0.1<br>-0.0<br>(0.059"<br>+0.004<br>-0.0) | 1.0 mm<br>Min<br>(0.179") | 1.75 mm<br>±0.1<br>(0.069<br>±0.004") | 3.5 mm<br>±0.5<br>(1.38<br>±0.002")    | 2.4 mm<br>Max<br>(0.094")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")  | 4.0 mm<br>±0.1<br>(0.157<br>±0.004") | 2.0 mm<br>±0.1<br>(0.079<br>±0.004") | 25 mm<br>(0.98") | 0.6 mm<br>(0.024) | 8.3 mm<br>(0.327)                     |
| 12 mm     | 8.2 mm<br>(0.323")  |   | 1.5 mm<br>Min<br>(0.060)  |                                       | 5.5 mm<br>±0.5<br>(0.217<br>±0.002")   | 6.4 mm<br>Max<br>(0.252")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")<br>8.0 mm<br>±0.10<br>(0.315<br>±0.004")   |                                      |                                      | 30 mm<br>(1.18") |                   | 12.0 mm<br>±0.3<br>(0.470<br>±0.012") |
| 16 mm     | 12.1 mm<br>(0.476") |   |                           |                                       | 7.5 mm<br>±0.10<br>(0.295<br>±0.004")  | 7.9 mm<br>Max<br>(0.311")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")<br>8.0 mm<br>±0.10<br>(0.315<br>±0.004")<br>12.0 mm<br>±0.10<br>(0.472<br>±0.004") |                                      |                                      |                  |                   | 16.3 mm<br>(0.642)                    |
| 24 mm     | 20.1 mm<br>(0.791") |   |                           |                                       | 11.5 mm<br>±0.10<br>(0.453<br>±0.004") | 11.9 mm<br>Max<br>(0.468") | 16.0 mm<br>±0.10<br>(0.63<br>±0.004")  |                                      |                                      |                  |                   | 24.3 mm<br>(0.957)                    |

6. Metric Dimensions Govern—English are in parentheses for reference only.

7. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

# MC74LVX259

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

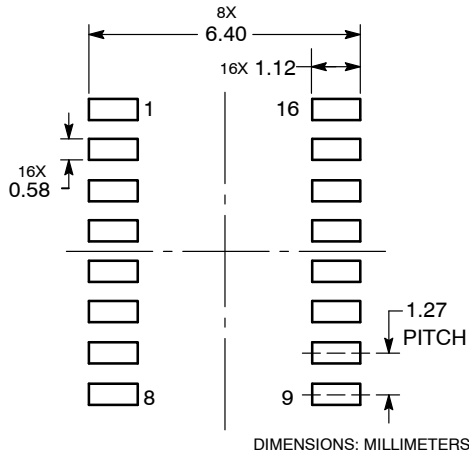


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0° 7°       |       | 0° 7°     |       |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

### SOLDERING FOOTPRINT

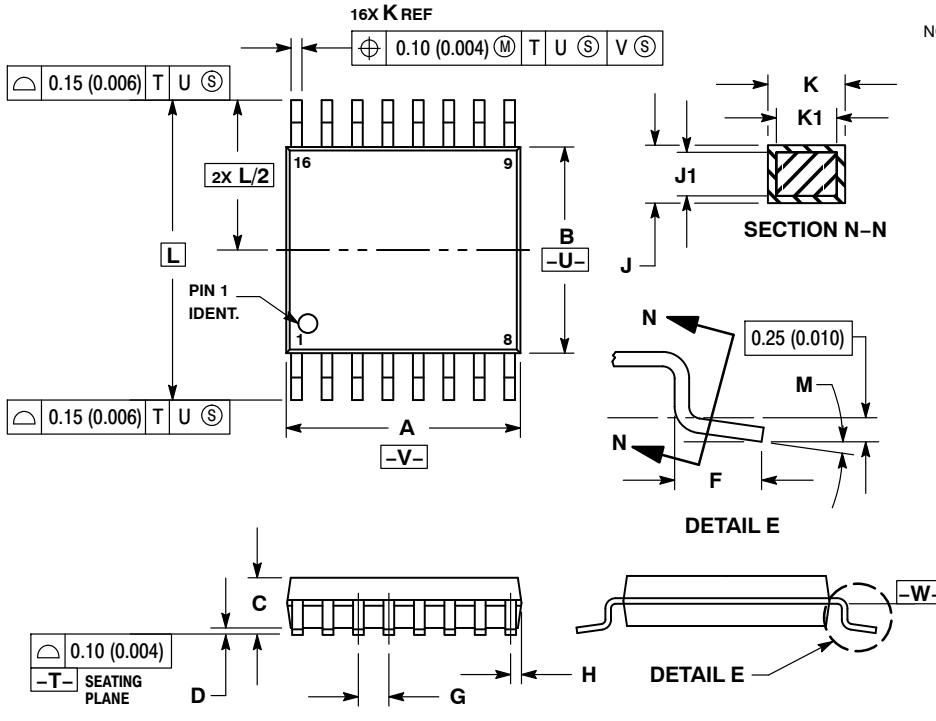




# MC74LVX259

## PACKAGE DIMENSIONS

TSSOP-16  
CASE 948F-01  
ISSUE B

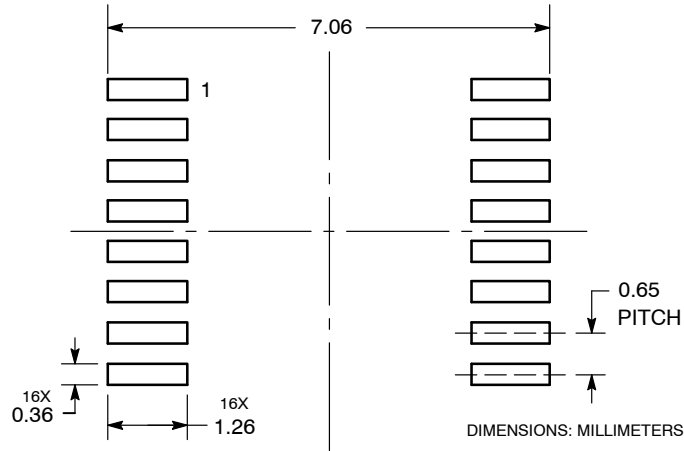


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

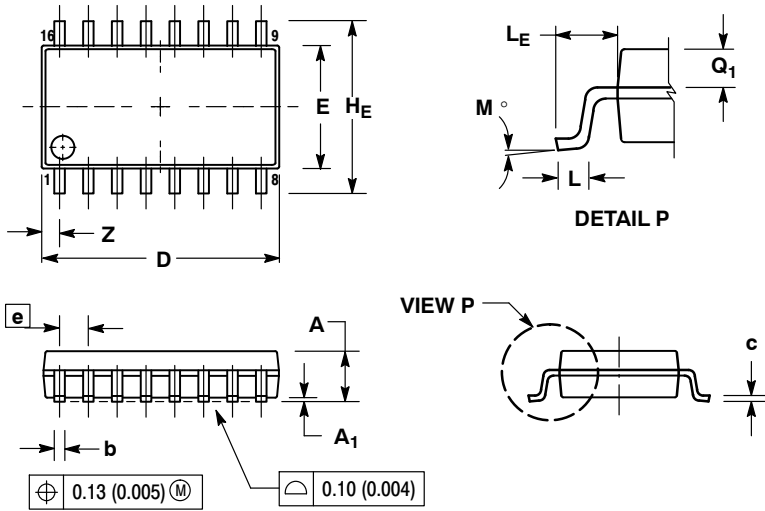
### SOLDERING FOOTPRINT



# MC74LVX259

## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.10        | 0.20  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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