



N-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold - 1.6V max.
- ▶ High input impedance
- ▶ Low input capacitance - 130pF typical
- ▶ Fast switching speeds
- ▶ Low on-resistance guaranteed at $V_{GS} = 2, 3, \text{ and } 5V$
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

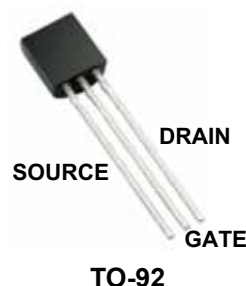
Part Number	Package Option	Packing
TN0702N3-G	TO-92	1000/Bag
TN0702N3-G P002	TO-92	2000/Reel
TN0702N3-G P003		
TN0702N3-G P005		
TN0702N3-G P013		
TN0702N3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availability.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)
20V	1.3Ω	0.5A	1.0V

Pin Configuration



Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

SiTN
0 7 0 2
YYWW

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

Typical Thermal Resistance

Package	θ_{JA}
TO-92	132°C/W

Thermal Characteristics

Package	I_D (continuous) [†]	I_D (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	I_{DR} [†]	I_{DRM}
TO-92	530mA	1.0A	1.0W	530mA	1.0A

Notes:
[†] I_D (continuous) is limited by max rated T_j .

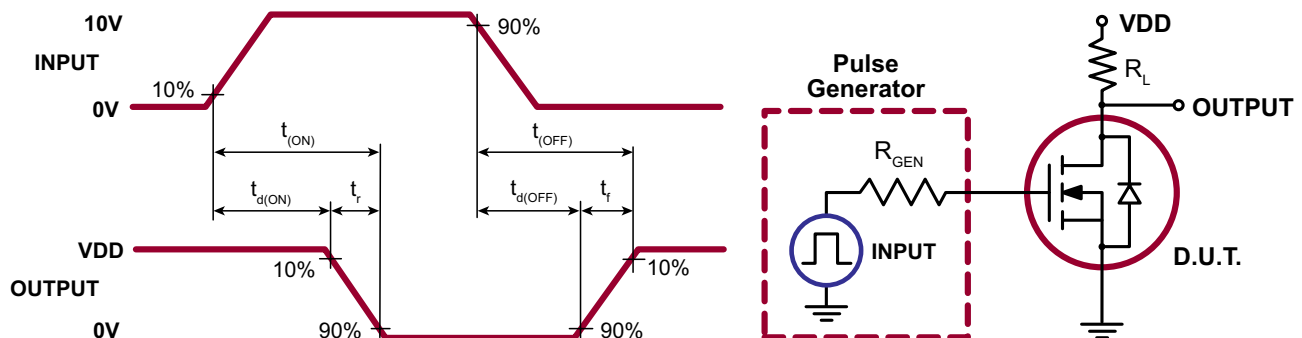
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	20	-	-	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate threshold voltage	0.5	0.8	1.0	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate body leakage	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	100	nA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	100	μA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.5	1.0	-	A	$V_{GS} = V_{DS} = 5.0V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	4.0	5.0	Ω	$V_{GS} = 2.0V, I_D = 50mA$
		-	1.9	2.5		$V_{GS} = 3.0V, I_D = 200mA$
		-	1.0	1.3		$V_{GS} = 5.0V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/ $^\circ\text{C}$	$V_{GS} = 5.0V, I_D = 500mA$
G_{FS}	Forward transductance	100	500	-	mmho	$V_{DS} = 5.0V, I_D = 500mA$
C_{ISS}	Input capacitance	-	130	200	pF	$V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz$
C_{OSS}	Common source output capacitance	-	70	125		
C_{RSS}	Reverse transfer capacitance	-	30	60		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	$V_{DD} = 20V, I_D = 0.5A, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	20		
$t_{d(OFF)}$	Turn-off delay time	-	-	30		
t_f	Fall time	-	-	20		
V_{SD}	Diode forward voltage drop	-	-	1.0	V	$V_{GS} = 0V, I_{SD} = 0.5A$

Notes:

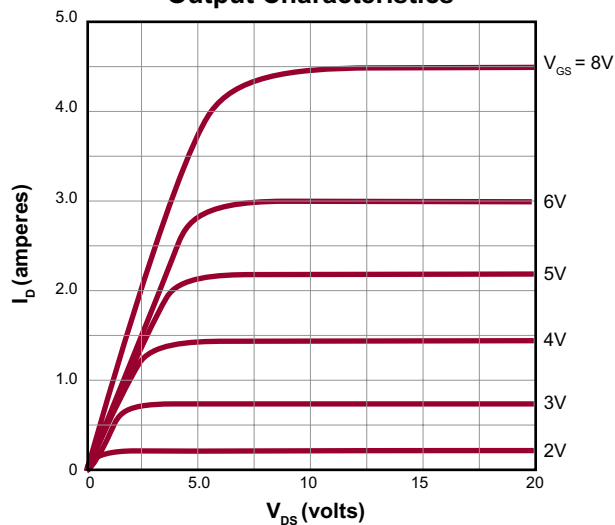
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

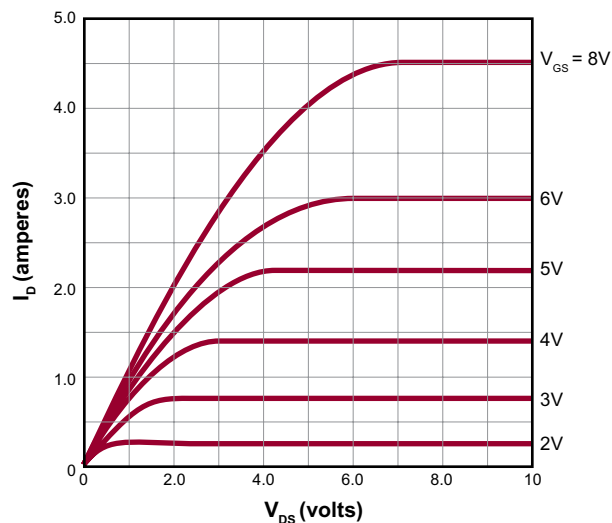


Typical Performance Curves

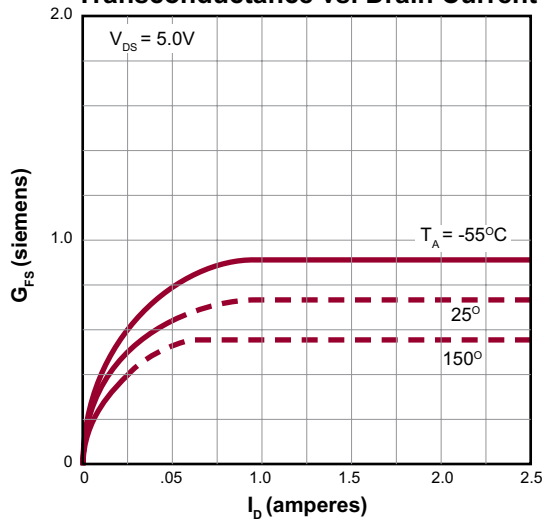
Output Characteristics



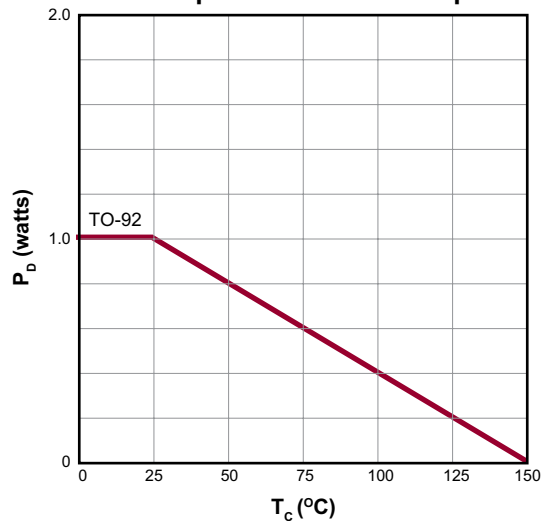
Saturation Characteristics



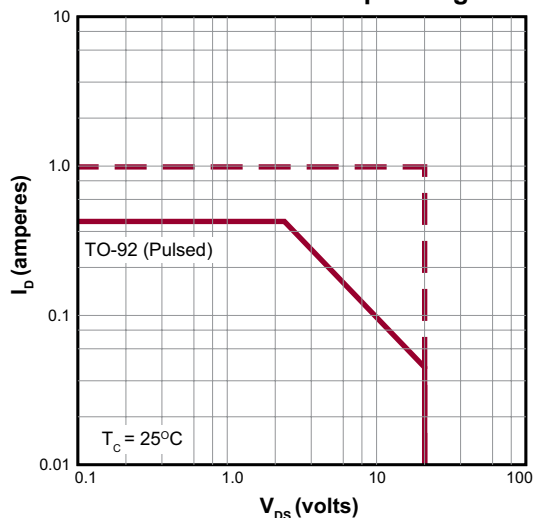
Transconductance vs. Drain Current



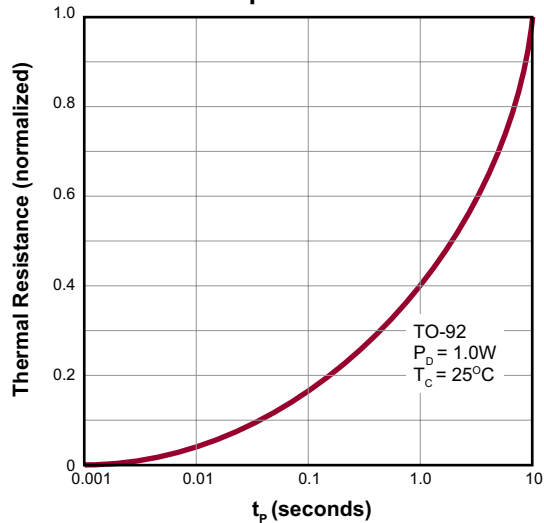
Power Dissipation vs. Case Temperature



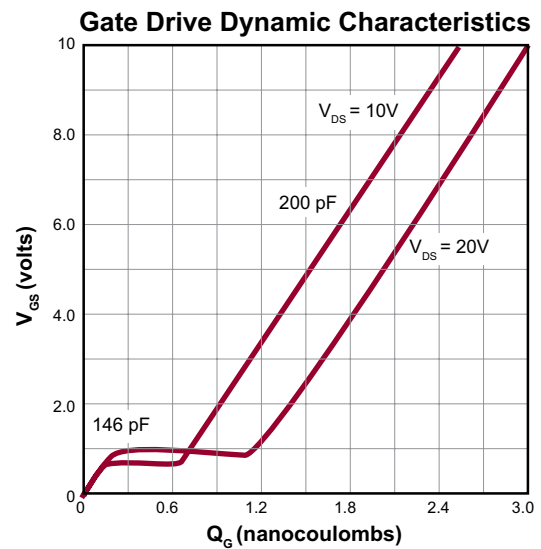
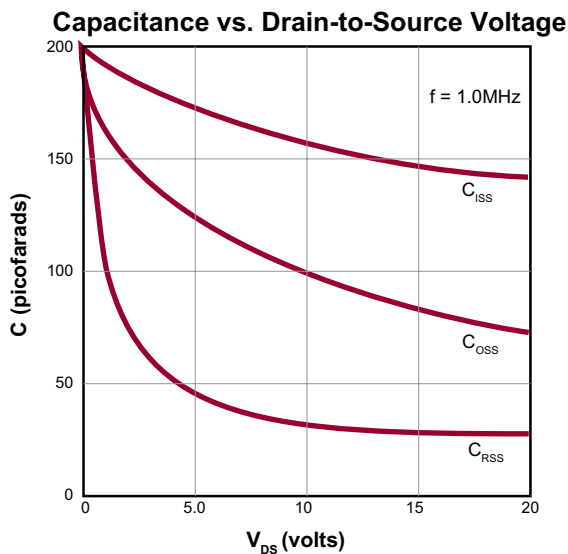
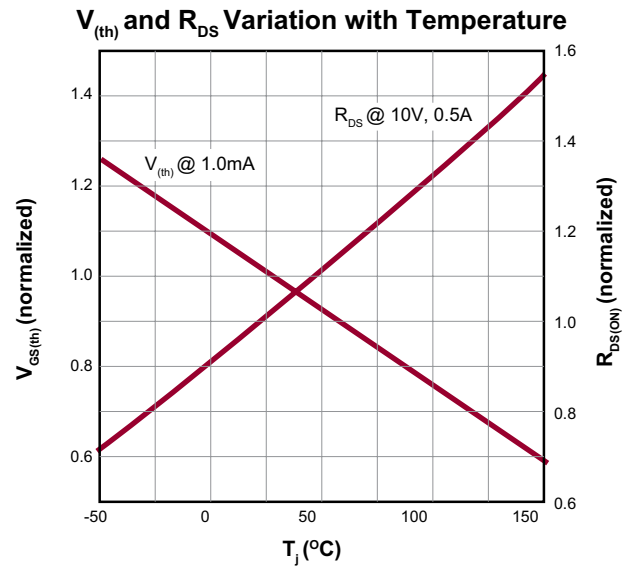
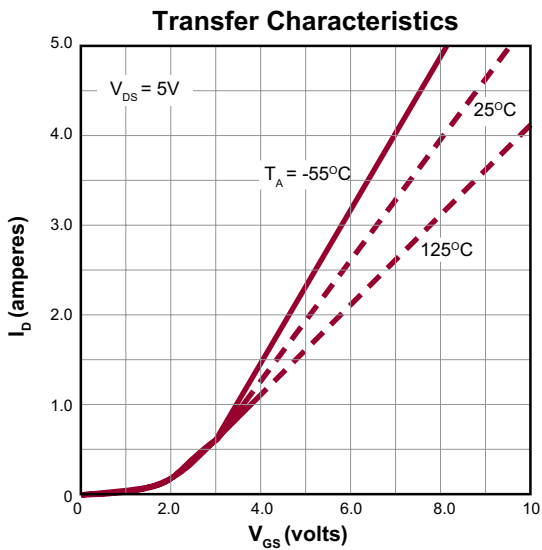
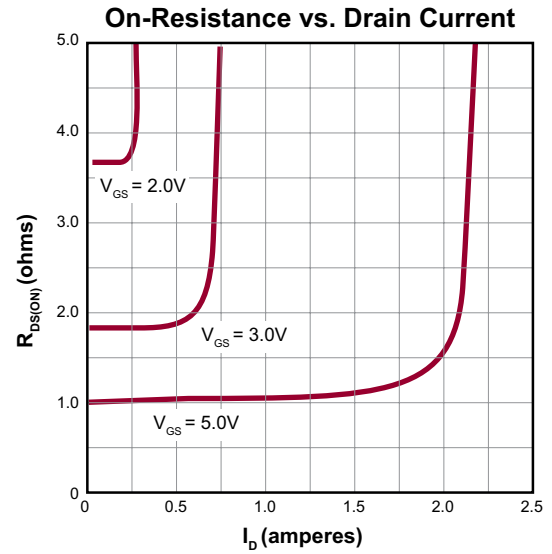
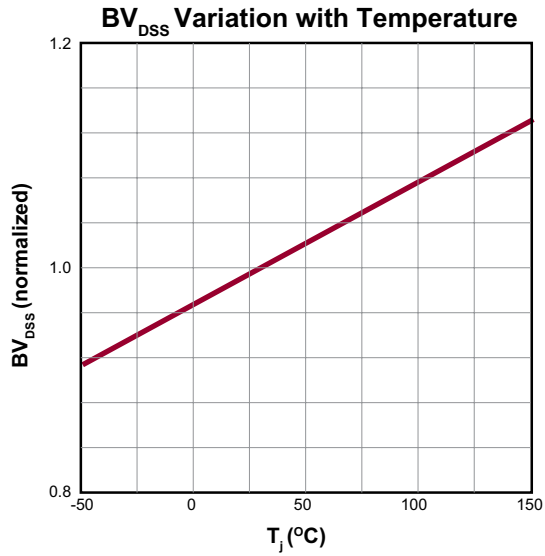
Maximum Rated Safe Operating Area



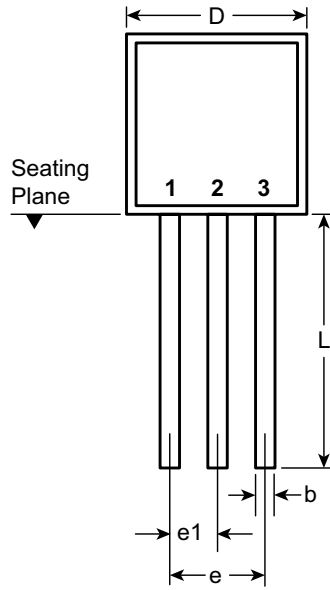
Thermal Response Characteristics



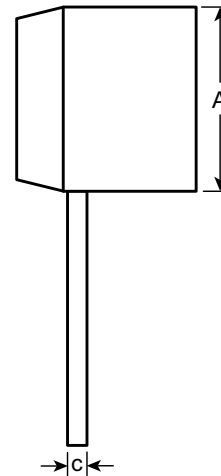
Typical Performance Curves (cont.)



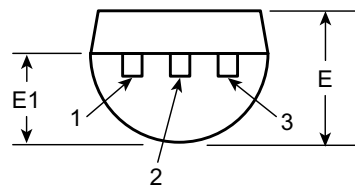
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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