

74LV04

Hex inverter

Rev. 4 — 8 December 2015

Product data sheet

1. General description

The 74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC04 and 74HCT04.

The 74LV04 provides six inverting buffers.

2. Features and benefits

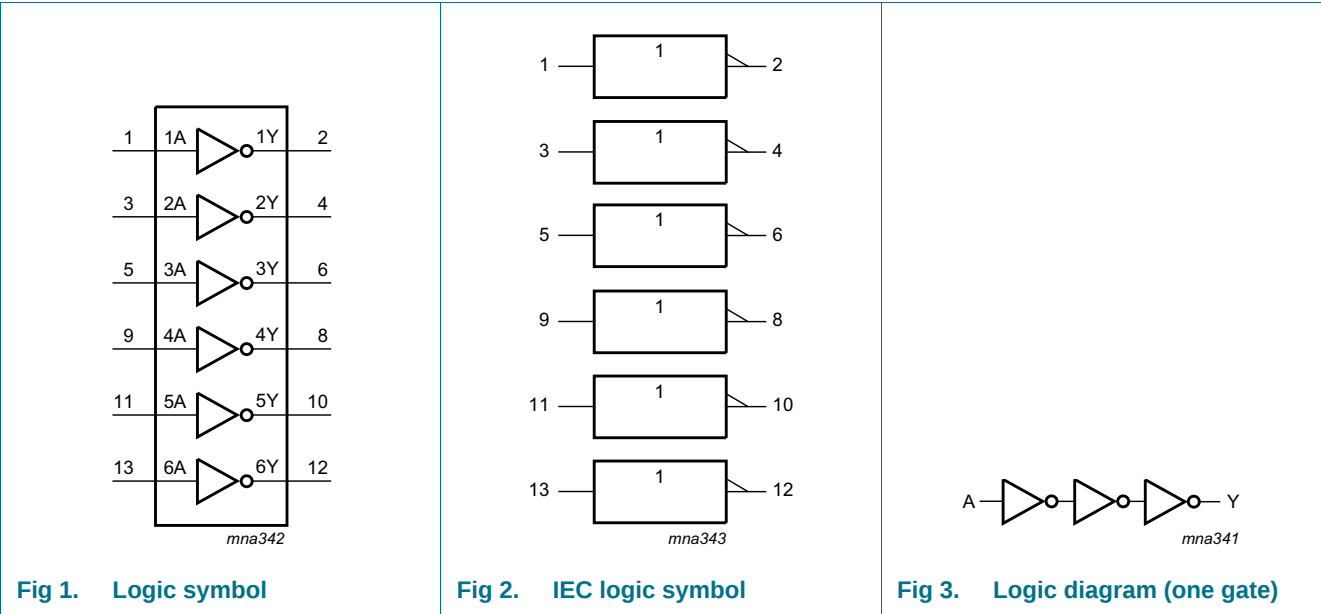
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

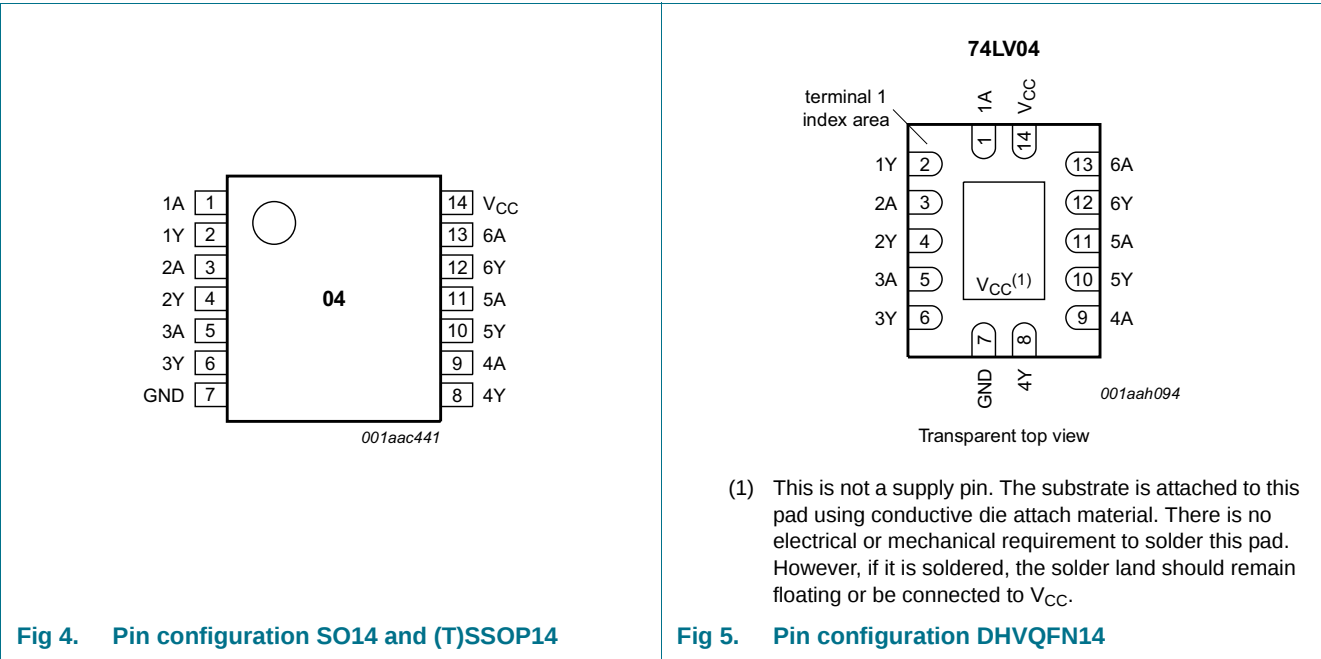
Type number	Package			
	Temperature range	Name	Description	Version
74LV04D	-40 °C to $+125$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV04DB	-40 °C to $+125$ °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV04PW	-40 °C to $+125$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV04BQ	-40 °C to $+125$ °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1 Pinning



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nA	Output nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
I _{IK}	input clamping current	V _I < −0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < −0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±50	mA
I _O	output current	V _O = −0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		−50	-	mA
T _{stg}	storage temperature		−65	+150	°C

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
	SO14 package	[2]	-	500	mW
	(T)SSOP14 package	[3]	-	500	mW
	DHVQFN14 package	[4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = –100 µA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = –100 µA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = –100 µA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = –100 µA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I _O = –100 µA; V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I _O = –6 mA; V _{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I _O = –12 mA; V _{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 µA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 µA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 µA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I _O = 100 µA; V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I _O = 6 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I _O = 12 mA; V _{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20.0	-	40	µA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} – 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6						
		$V_{CC} = 1.2\text{ V}$	-	40	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	14	20	-	25	ns
		$V_{CC} = 2.7\text{ V}$	-	10	15	-	19	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $C_L = 15\text{ pF}$	^[3]	6	-	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	^[3]	8	12	-	15	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	9	-	11	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_i = GND\text{ to }V_{CC}$	-	21	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

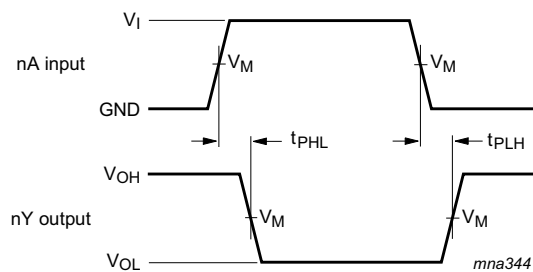
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

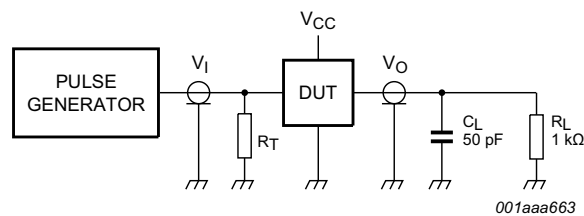


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
$< 2.7\text{ V}$	$0.5V_{CC}$	$0.5V_{CC}$
$2.7\text{ V to } 3.6\text{ V}$	1.5 V	1.5 V
$\geq 4.5\text{ V}$	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input	
V_{CC}	V_I	t_r, t_f
$< 2.7\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$
$2.7\text{ V to } 3.6\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$
$\geq 4.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

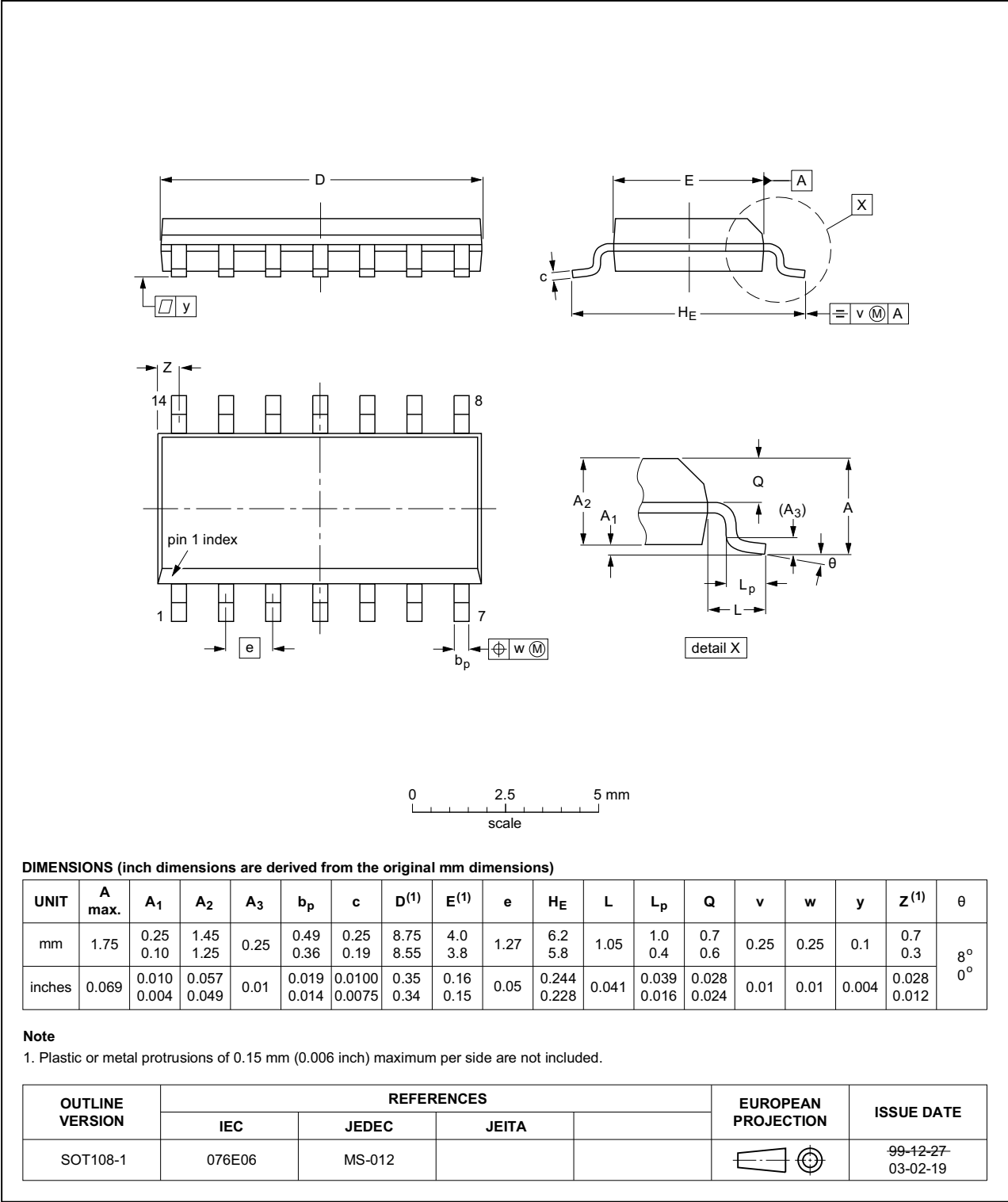


Fig 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

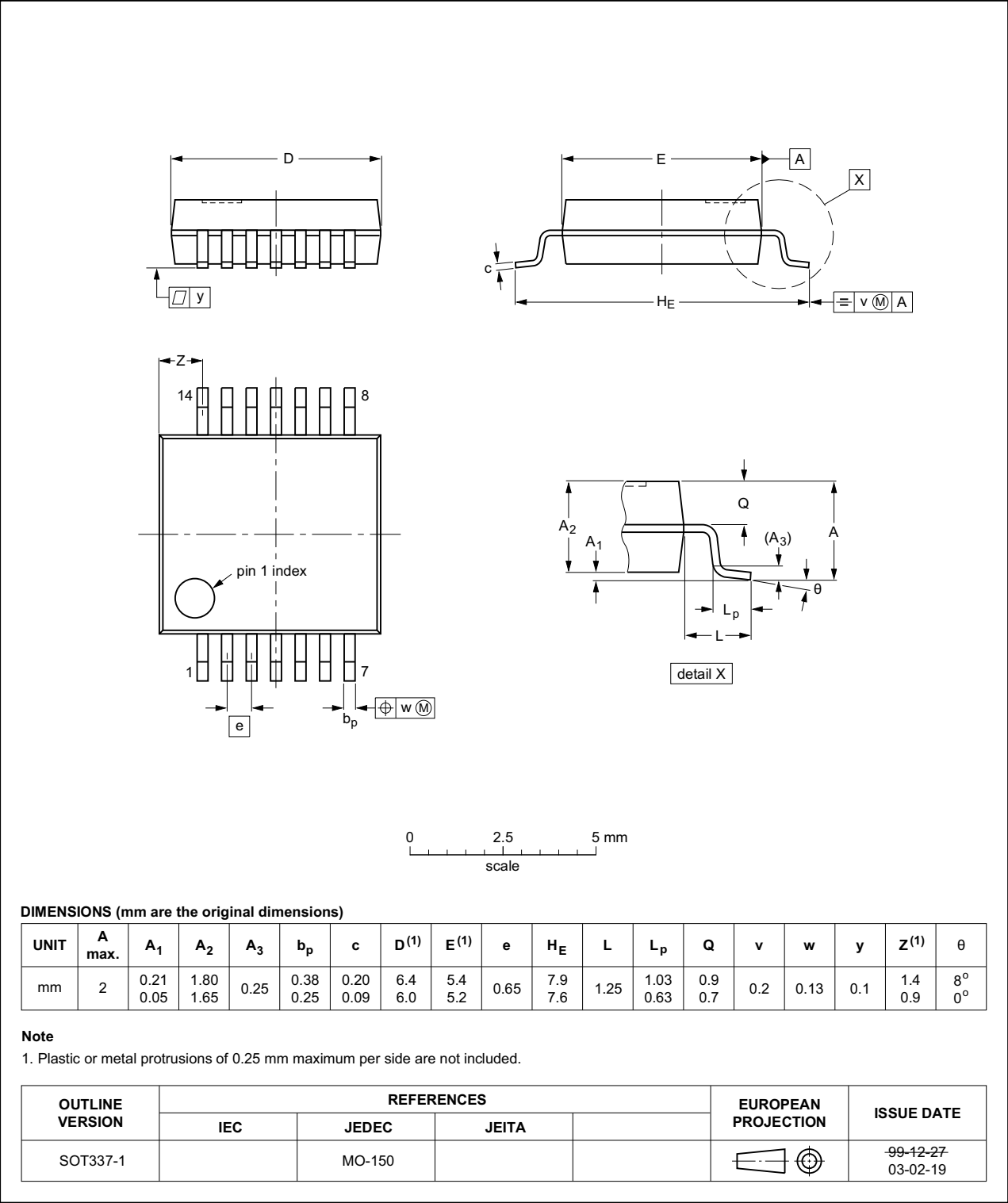
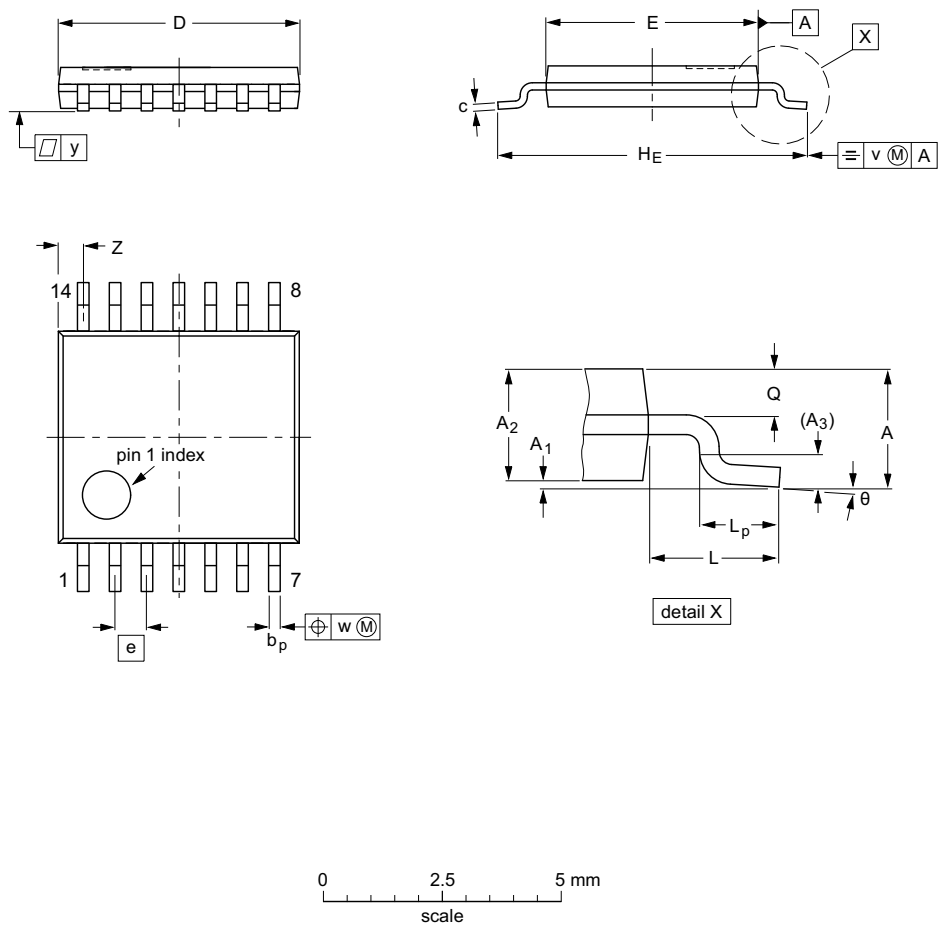


Fig 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

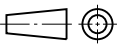
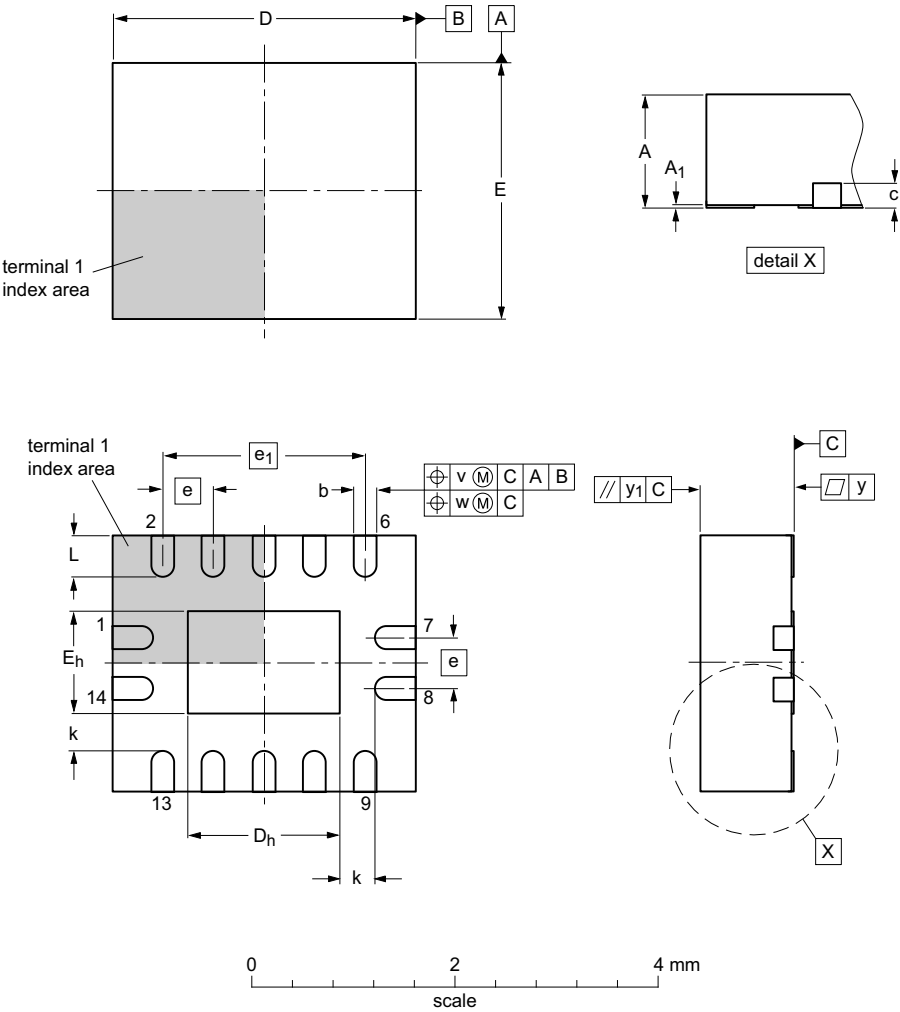
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30	3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18	2.9	1.35	2.4	0.85			0.2	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10- 15-05-05

Fig 11. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV04 v.4	20151208	Product data sheet	-	74LV04 v.3
Modifications:	Type number 74LV04N (SOT27-1) removed.			
74LV04 v.3	20071204	Product data sheet	-	74LV04 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors - Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN14 package added. Section 8: derating values added for DHVQFN14 package. Section 12: outline drawing added for DHVQFN14 package.			
74LV04 v.2	19980420	Product specification	-	74LV04 v.1
74LV04 v.1	19970203	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9