High Reliability Serial EEPROMs

Microwire BUS
BR93□□□family

BU9888FV-W

No.11001EAT20

●Description

BU9888FV-W is a serial EEPROM of serial 3-line interface method.

●Features

1) 256word×16bits architecture 4k bit serial EEPROM
2) Operating voltage range(3.0～3.6V)
3) Address auto increment function at read action
4) Write mistake prevention function
   Write prohibition at power on
   Write prohibition by command code
   Write mistake prevention function at low voltage
5) Program cycle auto delete and auto end function
6) Program condition display READY / $\overline{\text{BUSY}}$
7) Low current consumption
   At write action(3.6V): Icc1 = 3.5mA(Max.)
   At read action(3.6V): Icc2 = 2.0mA(Max.)
   At standby action (3.6V) : ISB = 2.0μA(Max.)
8) Compact package SSOP-B8pin
9) Data retention for 40 years
10) Data rewrite up to 100,000 times
11) Data at shipment all addresses FFFFh

●Absolute maximum rating (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vcc	-0.3～+6.5	V
Power Dissipation	Pd	300 *1	mW
Storage Temperature	Tstg	-65 ～+125	℃
Operating Temperature	Topr	-20 ～+85	℃
Terminal Voltage	—	-0.3～Vcc+0.3 *2	V

*1 Degradation is done at 3.0mW/℃ for operation above 25℃
*2 The Max value of Terminal Voltage is not over 6.5V

●EEPROM recommended operating condition

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vcc	3.0～3.6	V
Input Voltage	VIN	0 ～ Vcc	

●Memory cell characteristics(Ta=25℃, Vcc = 3.0～3.6V)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Erase/Write Cycle *1	100,000	—	—	Cycles
Data Retention *1	40	—	—	Years

*1 Not 100% TESTED

●**DC Operating Characteristics**(Unless otherwise specified Ta=-20～+85℃, Vcc=3.0～3.6V)

Parameter	Symbol	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
"L" Input Voltage	VIL	-0.3	—	0.2×Vcc	V	
"H" Input Voltage	VIH	0.8×Vcc	—	Vcc+0.3	V	
"L" Output Voltage	VOL	0	—	0.4	V	IOL=2.1mA
"H" Output Voltage	VOH	2.4	—	Vcc	V	IOH=-0.4mA
Input Leakage Current	ILI	-1	—	1	μA	VIN=0～Vcc
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0～Vcc, CS=0V
Operating Current	ICC1	—	—	3.5	mA	fSK=2MHz, tE/W=2ms(WRITE), TEST1=Vcc
	ICC2	—	—	2.0	mA	fSK=2MHz, (READ), TEST1=Vcc
Standby Current	ISB	—	—	2.0	μA	CS=0V, TEST1=Vcc, DO=OPEN

○This product is not designed for protection against radioactive rays.

●**EEPROM AC Operating Characteristics** (Ta=-20～+85℃, Vcc = 3.0～3.6V)

Paramete	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SK Clock Frequency	fSK	—	—	2	MHz
SK High Time	tSKH	230	—	—	ns
SK Low Time	tSKL	230	—	—	ns
CS Low Time	tCS	200	—	—	ns
CS Setup Time	tCSS	200	—	—	ns
DI Setup Time	tDIS	100	—	—	ns
CS Hold Time	tCSH	0	—	—	ns
DI Hold Time	tDIH	100	—	—	ns
Data "1" Output Delay Time	tPD1	—	—	200	ns
Data "0" Output Delay Time	tPD0	—	—	200	ns
CS to Status Valid	tSV	—	—	150	ns
CS to Output High-Z	tDF	—	—	150	ns
Write Cycle time	tE/W	—	—	2	ms

●**Synchronous data input/output timing**

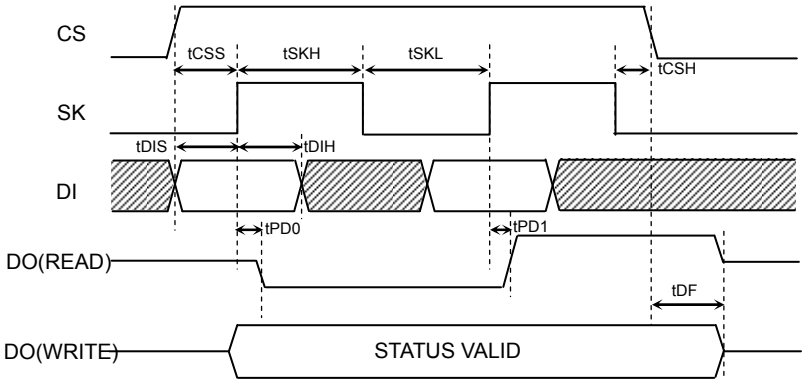


Fig.1 Sync data input / output timing

○Data is taken by DI in sync with the rise of SK.
○At read action, data is output from DO in sync with the rise of SK.
○The status signal at write (READY / $\overline{\text{BUSY}}$) is output after tCS from the fall of CS after write command input, at the area DO where CS is “H”, and valid until the next command start bit is input. And, while CS is “L”, DO becomes High-Z.
○After completion of each mode execution, set CS “L” once for internal circuit reset, and execute the following action mode.

●**Characteristic data** (The following characteristic data are Typ. Values.)

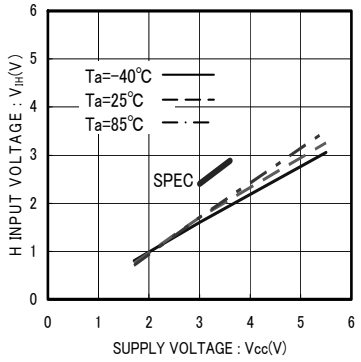


Fig.2 'H' input tvoltage
VIH(CS,SK,DI)

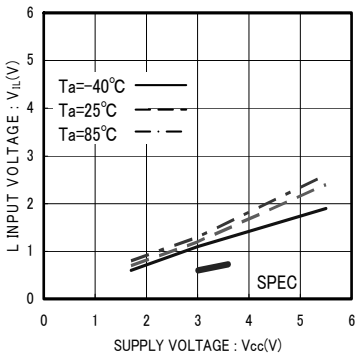


Fig.3 'L' input voltage
VIL (CS,SK,DI)

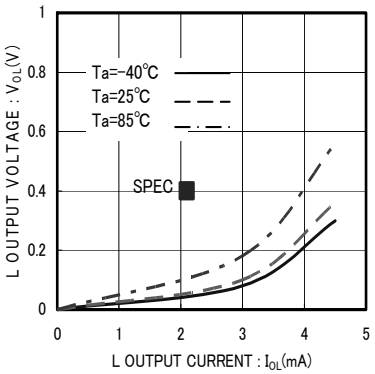


Fig.4 'L' output voltage
VOL-IOL(Vcc=3.0V)

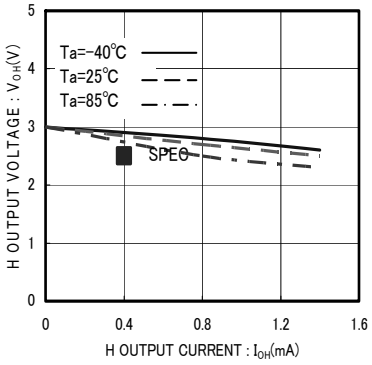


Fig.5 'H' output voltage
VOH-IOH(Vcc=3.0V)

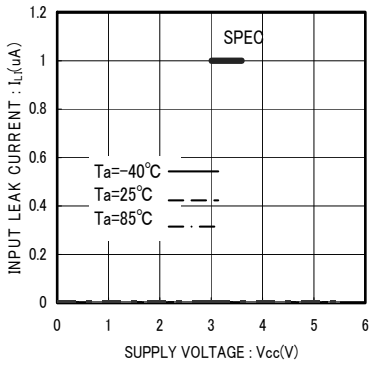


Fig.6 Input leak current
ILI(CS,SK,DI)

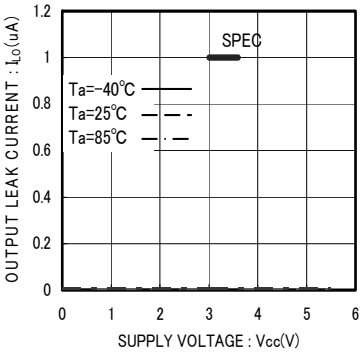


Fig.7 Output leak current
ILO(DO)

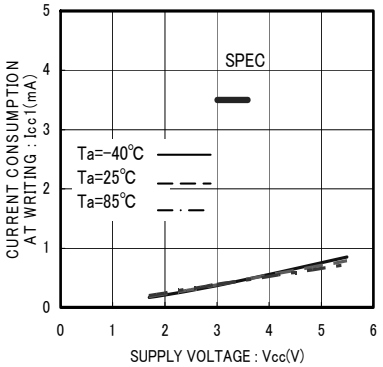


Fig.8 Current consumption at WRITE action ICC1(fSK=2MHz)

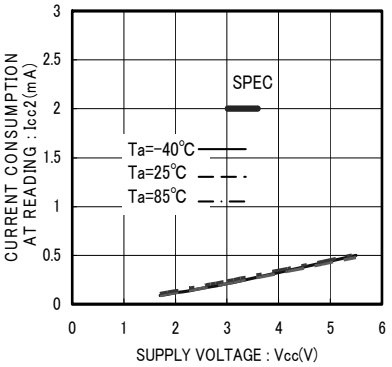


Fig.9 Consumption current at READ action ICC2(fSK=2MHz)

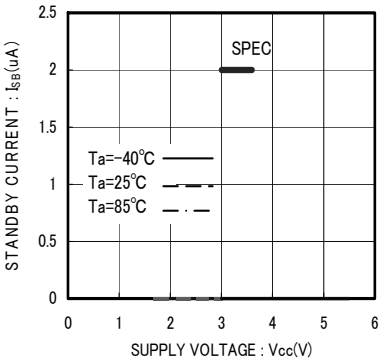


Fig.10 Consumption current at standby action ISB

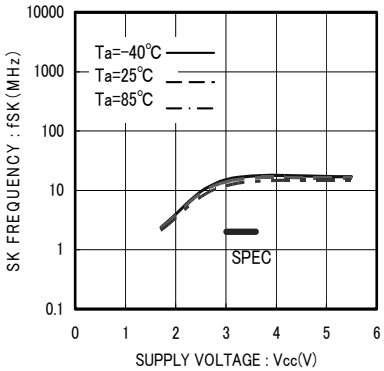


Fig.11 SK frequency fSK

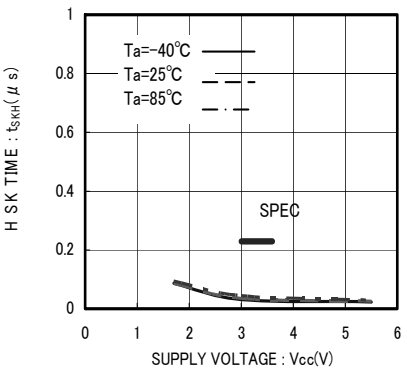


Fig.12 SK high time tSKH

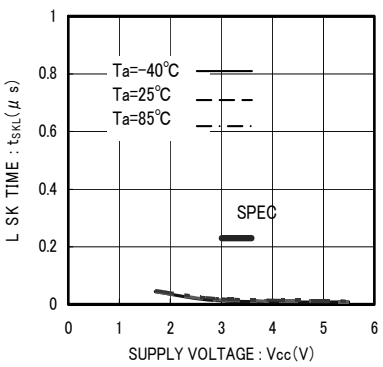


Fig.13 SK low time tSKL

●**Characteristic data** (The following characteristic data are Typ. Values.)

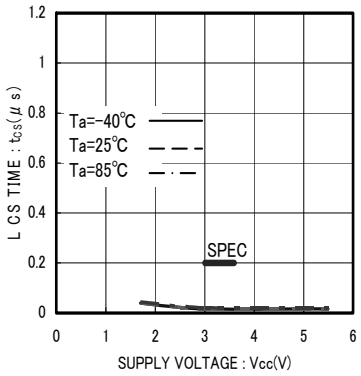


Fig.14 CS Low time t_{CS}

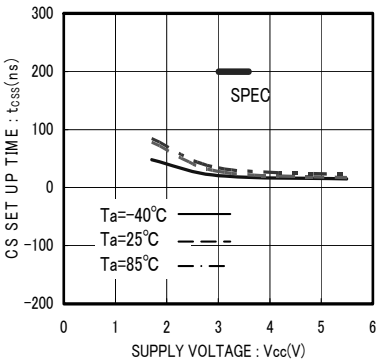


Fig.15 CS Setup time t_{CSS}

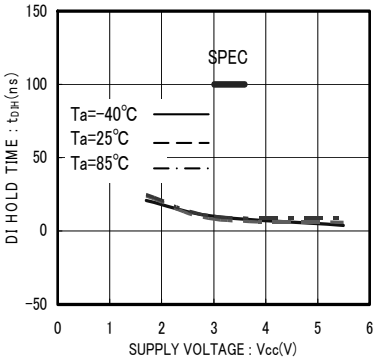


Fig.16 DI Hold time t_{DIH}

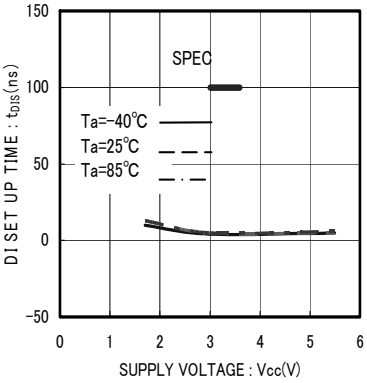


Fig.17 DI Setup time t_{DIS}

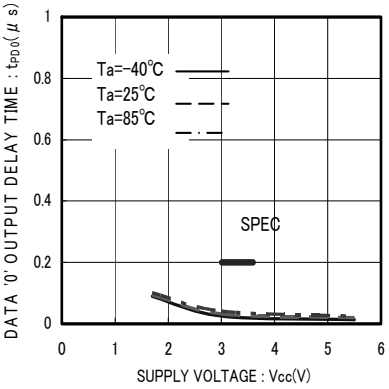


Fig.18 Data '0' output delay time t_{PD0}

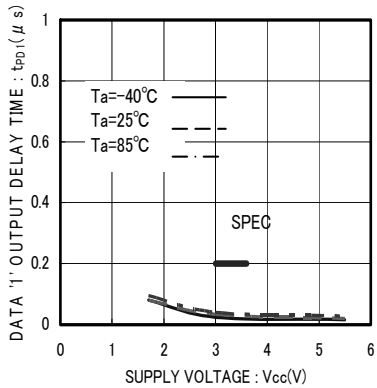


Fig.19 Data '1' output delay time t_{PD1}

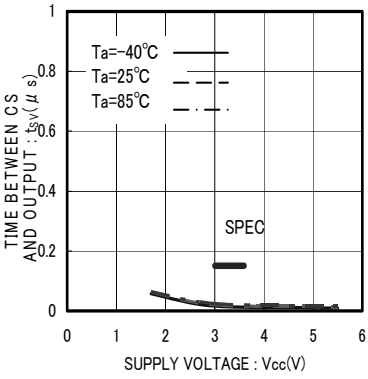


Fig.20 Time from CS to output establishment t_{SV}

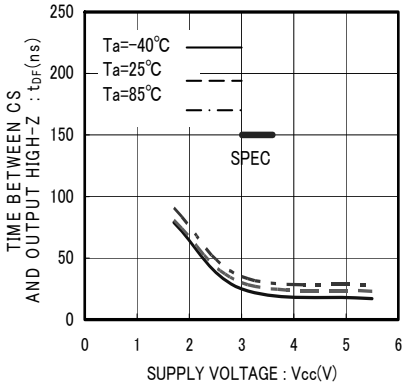


Fig.21 Time from CS to High-Z t_{DF}

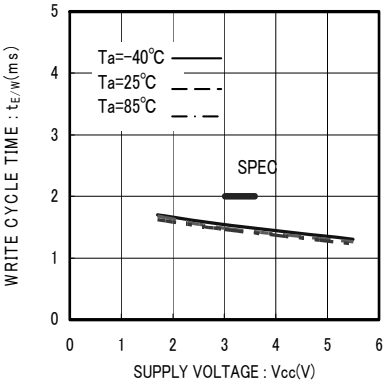


Fig.22 Write cycle time $t_{E/W}$

●Pin assignment

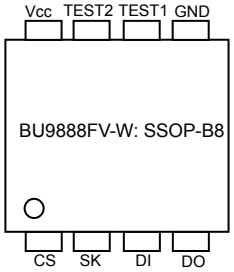


Fig.23 Pin assignment diagram

●Pin function

Pin name	I / O	Function
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Serial data input
DO	Output	Serial data output
TEST1	Input	Test pin. Please connect to power.
TEST2	-	Test pin. Please open at using.
Vcc	-	Power source
GND	-	All input / output reference voltage, 0V

●Block diagram

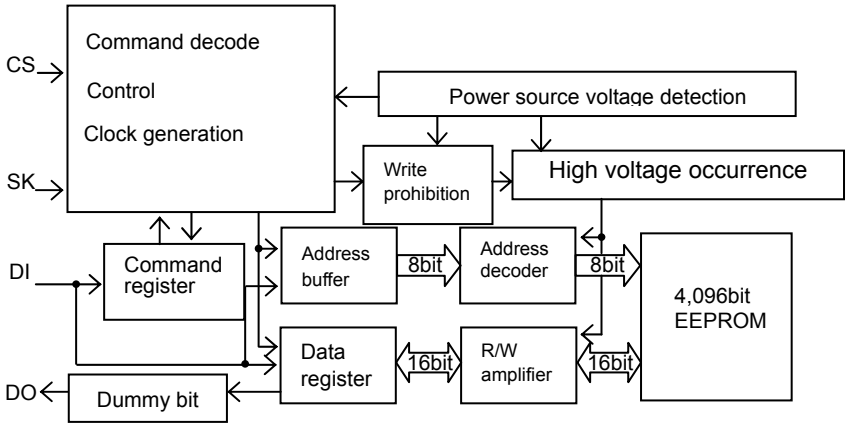


Fig.24 Block diagram

●Command mode

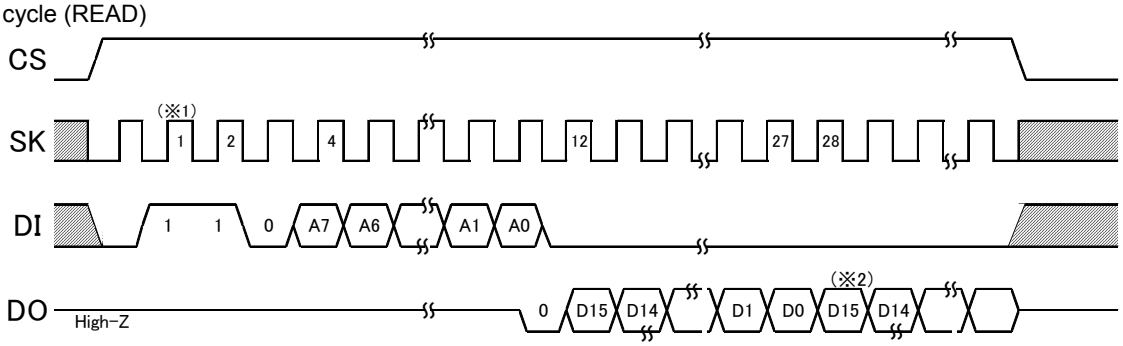
Command	Start bit	Ope code	Address	Data
Read (READ) (*1)	1	10	A7, A6, A5, A4, A3, A2,A1, A0	D15～D0(READ DATA)
Write enable (WEN)	1	00	1 1 * * * * * *	
Write (WRITE) (*2)	1	01	A7, A6, A5, A4, A3, A2, A1, A0	D15～D0(WRITE DATA)
Write disable (WDS)	1	00	0 0 * * * * * *	

・Input the address and the data in MSB first manners.
・As for ＊, input either VIH or VIL.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.
*1As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)
*2When the read and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.

●Timing chart

1. Read cycle (READ)



(※2) Next address data(Auto increment function)

Fig.25 Read cycle

(※1) Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, "0" (dummy bit) is output. And, the following data is output in sync with the rise of SK. This IC has an address auto increment function valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at "H".

2. Write cycle (WRITE)

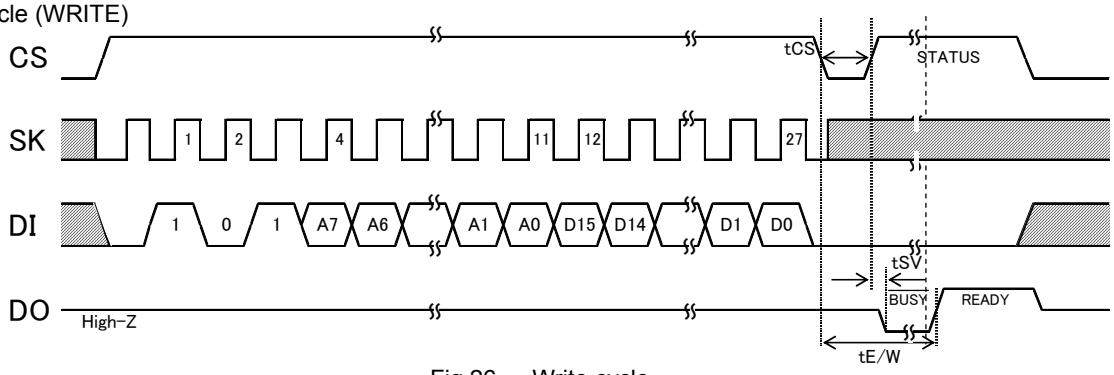


Fig.26 Write cycle

○In this command, input 16bit data (D15～D0) are written to designated addresses (A7~A0). The actual write starts by the fall of CS of D0 taken SK clock. When STATUS is not detected, (CS="L" fixed) Max. 2ms in conformity with tE/W, and when STATUS is detected (CS="H"), all commands are not accepted for areas where "L" ($\overline{BUSY}$) is output from D0, therefore, do not input any command.

3. Write enable (WEN)

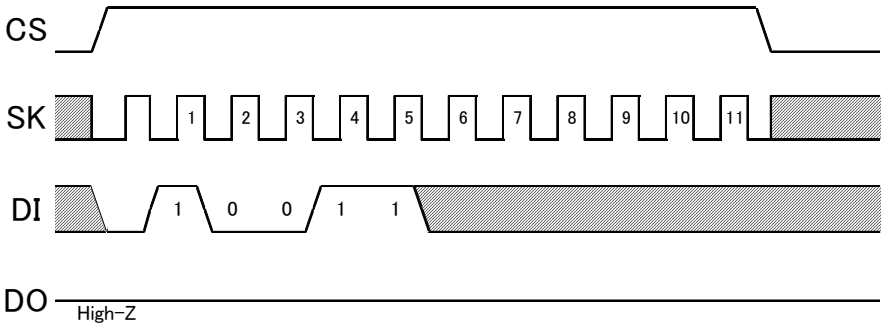


Fig.27 Write enable (WEN) cycle

○At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 8 clocks of this command is available by either “H” or “L”, but be sure to input it.

4. Write disable (WDS) cycle

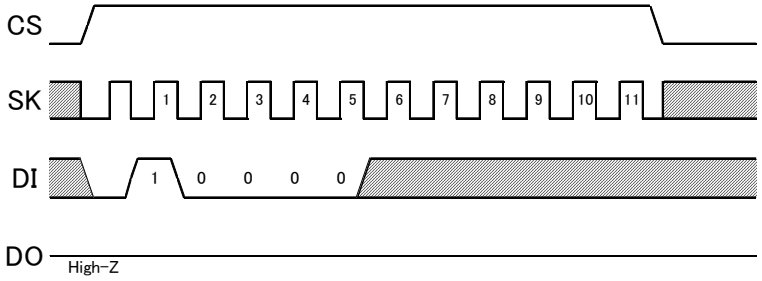


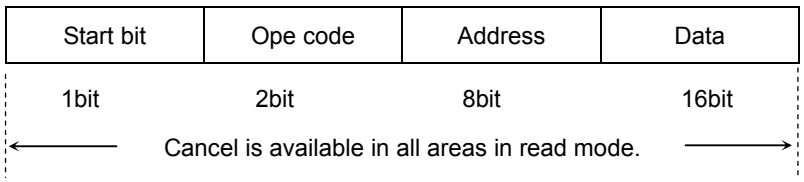
Fig.28 Write disable (WDS) cycle

○When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write. Input to SK after 8 clocks of this command is available by either “H” or “L”, but be sure to input it.

●Application

1) Method to cancel each command

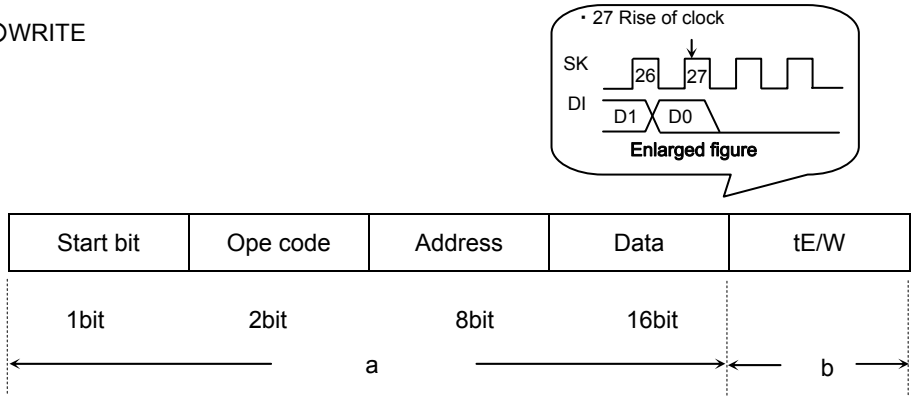
○READ



・Method to cancel:cancel by CS="L"

Fig.29 READ cancel available timing

○WRITE



a:From start bit to 27 clock rise
Cancel by CS="L"

b:27 clock rise and after
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

Fig.30 Write cancel available timing

2) At standby

○Standby current

When CS is "L", SK input is "L", DI input is "H", and even with middle electric potential, current does not increase.

○Timing

As shown in Fig.31, when SK at standby is "H", if CS is started, DI status may be read at the rise edge.
At standby and at power ON/OFF, when to start CS, set SK input or DI input to "L" status. (Refer to Fig.32)

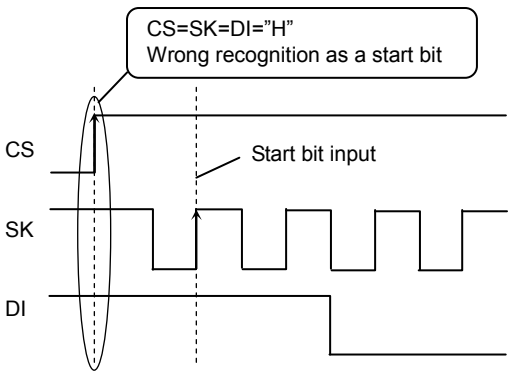


Fig.31 Wrong action timing

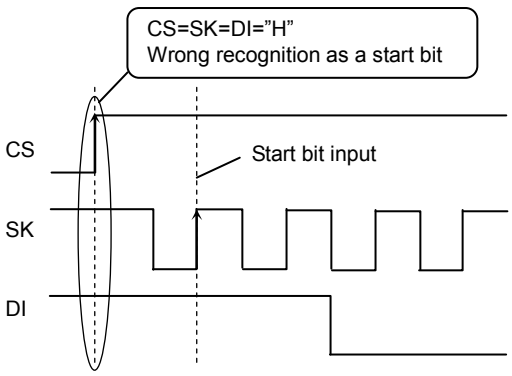


Fig.32 Normal action timing

3) Equivalent circuit

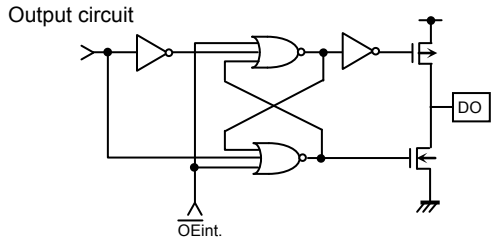


Fig.33 Output circuit (DO)

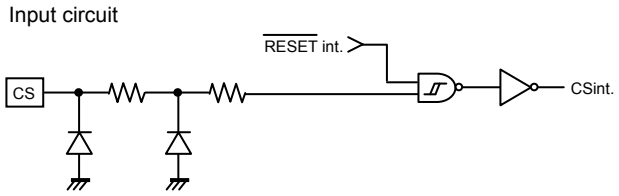


Fig.34 Input circuit (CS)

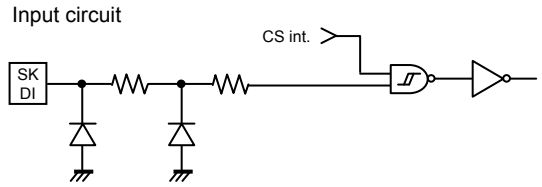


Fig.35 Input circuit (SK,DI)

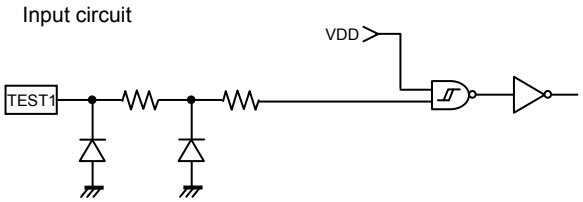


Fig.36 Input circuit (TEST1)

4) I/O peripheral circuit

4-1) Pull down CS.

By making CS="L" at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull down resistance Rpd of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary.
Select an appropriate value to this resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

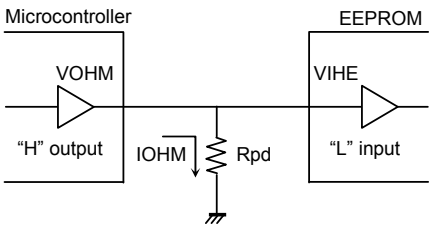


Fig.37 CS pull down resistance

$$Rpd \geqq \frac{VOHM}{IOHM} \quad \cdots ①$$

$$VOHM \geqq VIHE \quad \cdots ②$$

Example) When V_{CC} =5V, VIHE=2V, VOHM=2.4V, IOHM=2mA, from the equation ①,

$$Rpd \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and VIHE (=2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

4-2) DO is available in both pull up and pull down.
Do output become “High-Z” in other READY / $\overline{\text{BUSY}}$ output timing than after data output at read command and write command. When malfunction occurs at “High-Z” input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller actions, DO may be OPEN.
If DO is OPEN, and at timing to output status READY, at timing of CS=“H”, SK=“H”, DI=“H”, EEPROM recognizes this as a start bit, resets READY output, and DO=”High-Z”, therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

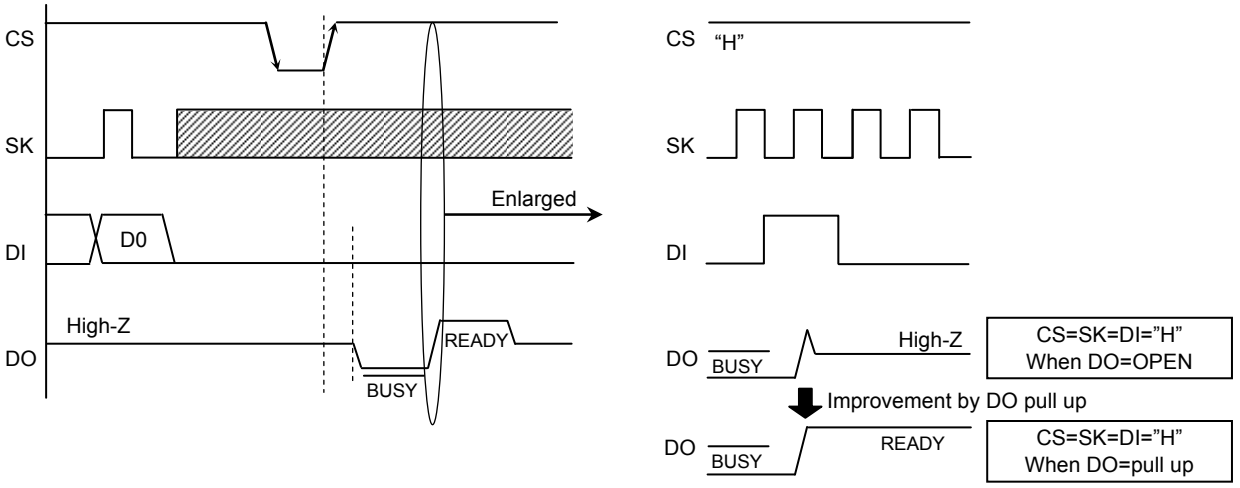


Fig.38 READY output timing at DO=OPEN

○Pull up resistance Rpu and pull down resistance Rpd of DO pin
As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.

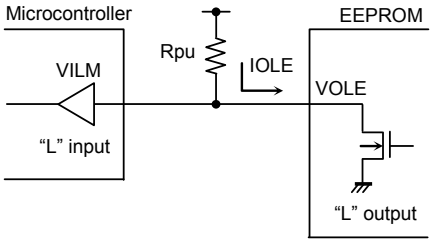


Fig.39 DO pull up resistance

$$Rpu \geqq \quad \cdots ③$$

$$VOLE \leqq VILM \quad \cdots ④$$

Example) When V_{CC} =5V, VOLE=0.4V, IOLE=2.1mA, VILM=0.8V, from the equation ③,

$$Rpu \geqq$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM(=0.8V), the equation ④ is also satisfied.

- VOLE : EEPROM VOL specifications
- IOLE : EEPROM IOL specifications
- VILM : Microcontroller VIL specifications

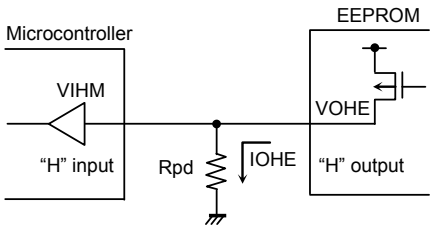


Fig.40 DO pull down resistance

$$Rpd \geqq \frac{VOHE}{IOHE} \quad \cdots ⑤$$

$$VOHE \geqq VIHM \quad \cdots ⑥$$

Example) When V_{CC} =5V, VOHE=Vcc−0.2V, IOHE=0.1mA, VIHM=Vcc×0.7V from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or below, and with VIHM (=3.5V), the equation ⑥ is also satisfied.

- VOHE : EEPROM VOH specifications
- IOHE : EEPROM IOH specifications
- VIHM : Microcontroller VIH specifications

5) READY / $\overline{BUSY}$ status display (DO terminal)
(common to BR93L46-W / A46-WM,BR93L56-W / A56-WM, BR93L66-W / A66-WM, BR93L76-W / A76-WM, BR93L86-W / A86-WM)
This display outputs the internal status signal. When CS is started after tCS (Min.200ns) from CS fall after write command input, “H” or “L” is output.

$R/\overline{B}$ display=“L” ($\overline{BUSY}$) = write under execution
(DO status)

After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically.
And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

$R/\overline{B}$ display = “H” (READY) = command wait status
(DO status)

Even after tE/W (max.5ms) from write of the memory cell, the following command is accepted.
Therefore, CS=“H” in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore, DI=“L” in the area
CS=“H”. (Especially, in the case of shared input port, attention is required.)

* Do not input any command while status signal is output.
Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted.
Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

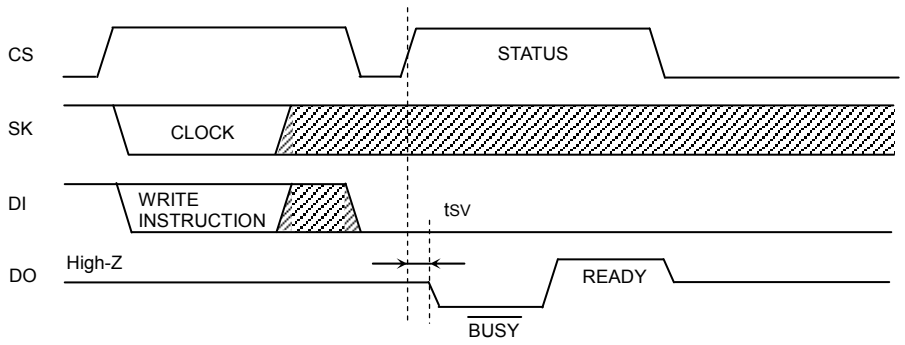


Fig.41 $R/\overline{B}$ status output timing chart

6) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

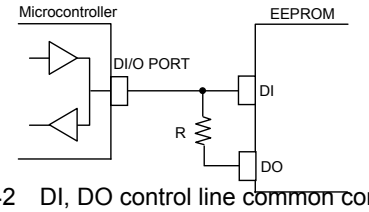


Fig.42 DI, DO control line common connection

○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

(1) 1 clock cycle to take in A0 address data at read command

Dummy bit “0” is output to DO terminal.

→When address data A0 = “1” input, through current route occurs.

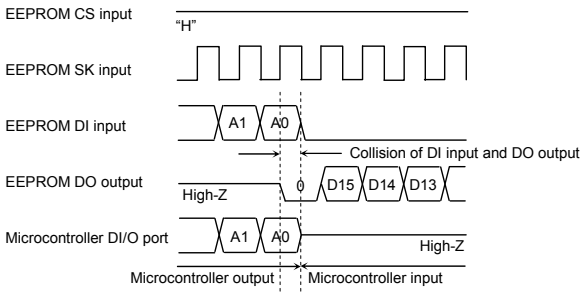


Fig.43 Collision timing at read data output at DI, DO direct connection

(2) Timing of CS = “H” after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.

When the next start bit input is recognized, “HIGH-Z” gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output “L”, READY output “H” is output from DO terminal, and through current route occurs.

Feedback input at timing of these (1) and (2) does not cause disorder in basic operations, if resistance R is inserted.

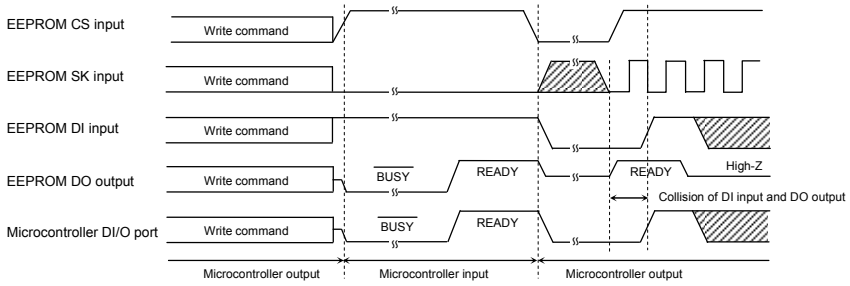


Fig.44 Collision timing at DI, DO direct connection

Note) As for the case (2), attention must be paid to the following.

When status READY is output, DO and DI are shared, DI=”H” and the microcontroller DI/O=”High-Z” or the microcontroller DI/O=”H”,if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at status READY output, set SK=“L”, or start CS within 4 clocks after “H” of READY signal is output.

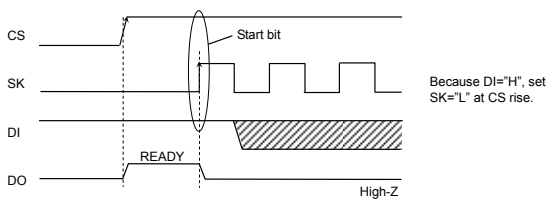


Fig.45 Start bit input timing at DI, DO direct connection

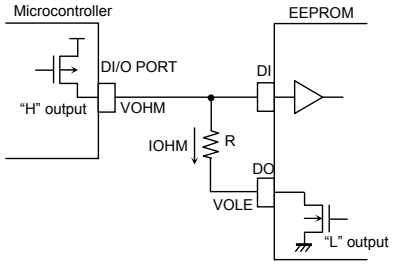
○Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

(1) Address data A0 = "1" input, dummy bit "0" output timing
(When microcontroller DI/O output is "H", EEPROM DO outputs "L", and "H" is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the level VIH of EEPROM should satisfy the following.



Conditions

$$VOHM \leqq VIHE$$

$$VOHM \leqq IOHM \times R + VOLE$$

At this moment, if VOLE=0V,

$$VOHM \leqq IOHM \times R$$

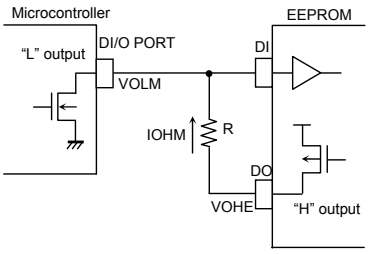
$$\therefore \quad R \geqq \frac{VOHM}{IOHM} \quad \cdots ⑦$$

・VIHE : EEPROM VIH specifications
・VOLE : EEPROM VOL specifications
・VOHM : Microcontroller VOH specifications
・IOHM : Microcontroller IOH specifications

Fig.46 Circuit at DI, DO direct connection (Microcontroller DI/O "H" output, EEPROM "L" output)

(2) DO status READY output timing
(When the microcontroller DI/O is "L", EEPROM DO output "H", and "L" is input to DI)

・Set the EEPROM input level VIL so as to satisfy the following.



Conditions

$$VOLM \geqq VILE$$

$$VOLM \geqq VOHE - IOLM \times R$$

As this moment, VOHE=Vcc

$$VOLM \geqq Vcc - IOLM \times R$$

$$\therefore \quad \frac{Vcc - VOLM}{IOLM} \quad \cdots ⑧$$

・VILE : EEPROM VIL specifications
・VOHE : EEPROM VOH specifications
・VOLM : Microcontroller VOL specifications
・IOLM : Microcontroller IOL specifications

Fig.47 Circuit at DI, DO direct connection (Microcontroller DI/O "L" output, EEPROM "H" output)

Example) When Vcc=5V, VOHM=5V, IOHM=0.4mA, VOLM=5V, IOLM=0.4mA,

From the equation ⑦,

$$R \geqq \frac{VOHM}{IOHM}$$

$$R \geqq \frac{5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 12.5\ [k\Omega] \quad \cdots ⑨$$

From the equation⑧,

$$R \geqq \frac{Vcc - VOLM}{IOLM}$$

$$R \geqq \frac{5 - 0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 2.2\ [k\Omega] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 12.5\ [k\Omega]$$

7) Notes on power ON/OFF

・At power ON/OFF, set CS “L”.

When CS is “H”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS “L”. (When CS is in “L” status, all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS “L”.

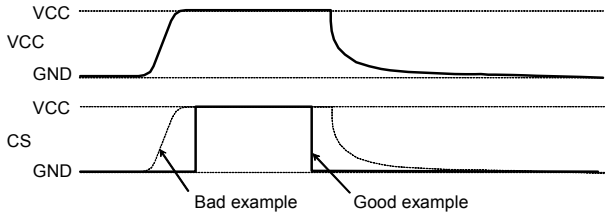


Fig.48 Timing at power ON/OFF

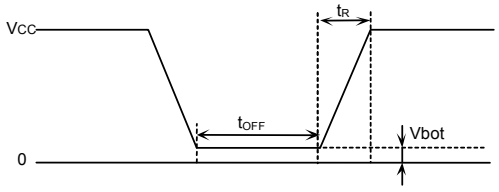
(Bad example) CS pin is pulled up to Vcc.
In this case, CS becomes “H” (active status), and EEPROM may have malfunction, mistake write owing to noise and the likes.
Even when CS input is High-Z, the status becomes like this case, which please note.

(Good example) It is “L” at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is “H” at power ON/OFF, it may become write enable status owing to noises and the likes. For secure actions, observe the follwing conditions.

1. Set CS=”L”
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit action.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Fig.49 Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ.=1.2V) or below, it prevent data rewrite.

8) Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1 μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time (tR) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

●Notes for use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short-circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short-circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficient.

●Ordering part number

B	U	9	8	8	8	F	V	-	W	E	2

Part No. (B U)

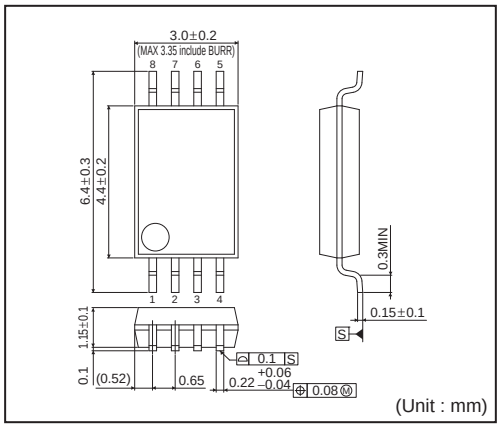
Part No. (9 8 8 8)

Package
FV: SSOP-B8

(W)

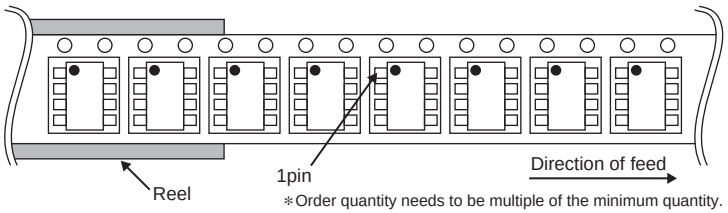
Packaging and forming specification
E2: Embossed tape and reel

SSOP-B8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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