20-Bit, 500ksps, Low Power SAR ADC with 0.5ppm INL

FEATURES

- **500ksps Throughput Rate**
- **±0.5ppm INL (Typ)**
- **Guaranteed 20-Bit No Missing Codes**
- **Low Power: 10.5mW at 500ksps, 10.5µW at 500sps**
- **104dB SNR (Typ) at f_{IN} = 2kHz**
- **–125dB THD (Typ) at f_{IN} = 2kHz**
- **Digital Gain Compression (DGC)**
- Guaranteed Operation to 85°C
- 2.5V Supply
- Fully Differential Input Range ±V_{REF}
- V_{REF} Input Range from 2.5V to 5.1V
- No Pipeline Delay, No Cycle Latency
- 1.8V to 5V I/O Voltages
- SPI-Compatible Serial I/O with Daisy-Chain Mode
- Internal Conversion Clock
- 16-Lead MSOP and 4mm × 3mm DFN Packages

APPLICATIONS

- Medical Imaging
- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Industrial Process Control
- Low Power Battery-Operated Instrumentation
- ATE

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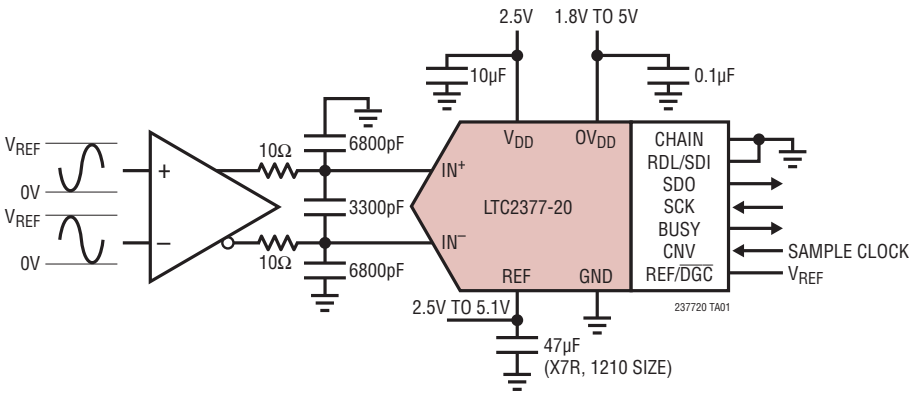
DESCRIPTION

The LTC®2377-20 is a low noise, low power, high speed 20-bit successive approximation register (SAR) ADC. Operating from a 2.5V supply, the LTC2377-20 has a ±V_{REF} fully differential input range with V_{REF} ranging from 2.5V to 5.1V. The LTC2377-20 consumes only 10.5mW and achieves ±2ppm INL maximum, no missing codes at 20 bits with 104dB SNR.

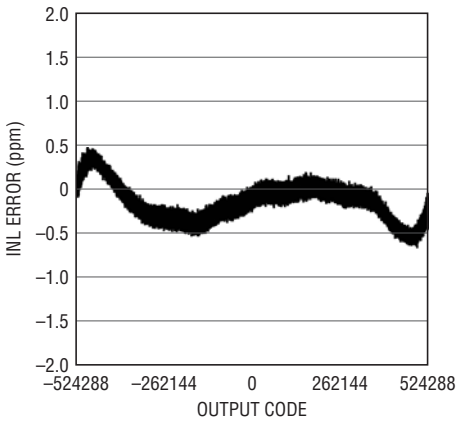
The LTC2377-20 has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The fast 500ksps throughput with no cycle latency makes the LTC2377-20 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2377-20 automatically powers down between conversions, leading to reduced power dissipation that scales with the sampling rate.

The LTC2377-20 features a unique digital gain compression (DGC) function, which eliminates the driver amplifier's negative supply while preserving the full resolution of the ADC. When enabled, the ADC performs a digital scaling function that maps zero-scale code from 0V to 0.1 • V_{REF} and full-scale code from V_{REF} to 0.9 • V_{REF}. For a typical reference voltage of 5V, the full-scale input range is now 0.5V to 4.5V, which provides adequate headroom for powering the driving amplifier from a single 5.5V supply.

TYPICAL APPLICATION



Integral Nonlinearity vs Output Code

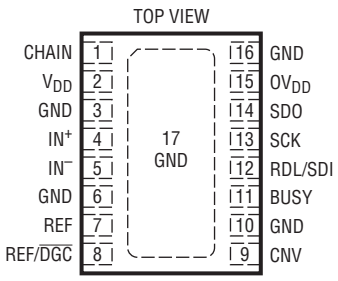


ABSOLUTE MAXIMUM RATINGS

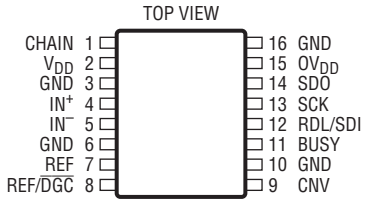
(Notes 1, 2)

Supply Voltage (V_{DD}) 2.8V
Supply Voltage (OV_{DD}) 6V
Reference Input (REF) 6V
Analog Input Voltage (Note 3)
  IN^+, IN^- ..... (GND – 0.3V) to (REF + 0.3V)
REF/$\overline{DGC}$ Input (Note 3) .... (GND – 0.3V) to (REF + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2377C ..... 0°C to 70°C
  LTC2377I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC2377-20#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2377CMS-20#PBF	LTC2377CMS-20#TRPBF	237720	16-Lead Plastic MSOP	0°C to 70°C
LTC2377IMS-20#PBF	LTC2377IMS-20#TRPBF	237720	16-Lead Plastic MSOP	–40°C to 85°C
LTC2377CDE-20#PBF	LTC2377CDE-20#TRPBF	23770	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2377IDE-20#PBF	LTC2377IDE-20#TRPBF	23770	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/ . Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}+$	Absolute Input Range (IN^+)	(Note 5)	●	–0.1		V_{REF} + 0.1	V
$V_{IN}–$	Absolute Input Range ($IN^–$)	(Note 5)	●	–0.1		V_{REF} + 0.1	V
$V_{IN}+ – V_{IN}–$	Input Differential Voltage Range	$V_{IN} = V_{IN}+ – V_{IN}–$	●	$–V_{REF}$		$+V_{REF}$	V
V_{CM}	Common-Mode Input Range		●	$V_{REF}/2–$ 0.1	$V_{REF}/2$	$V_{REF}/2+$ 0.1	V
I_{IN}	Analog Input Leakage Current				0.01		µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 250kHz			86		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	20			Bits
	No Missing Codes		●	20			Bits
	Transition Noise				2.3		ppm_{RMS}
INL	Integral Linearity Error	(Note 6) REF/$\overline{DGC}$ = GND, (Note 6)	● ●	–2 –2	±0.5 ±0.5	2 2	ppm ppm
DNL	Differential Linearity Error	(Note 10)	●	–0.5	±0.2	0.5	ppm
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–13	0	13	ppm
	Bipolar Zero-Scale Error Drift				±7		ppb/°C
FSE	Bipolar Full-Scale Error	(Note 7)	●	–100	±10	100	ppm
	Bipolar Full-Scale Error Drift				±0.05		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 2kHz, V_{REF} = 5V	●	101	104		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 2kHz, V_{REF} = 5V f_{IN} = 2kHz, V_{REF} = 5V, REF/$\overline{DGC}$ = GND f_{IN} = 2kHz, V_{REF} = 2.5V	● ● ●	101 99 95.5	104 102 98		dB dB dB
THD	Total Harmonic Distortion	f_{IN} = 2kHz, V_{REF} = 5V f_{IN} = 2kHz, V_{REF} = 5V, REF/$\overline{DGC}$ = GND f_{IN} = 2kHz, V_{REF} = 2.5V	● ● ●		–125 –125 –123	–115 –114 –113	dB dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 2kHz, V_{REF} = 5V	●	115	128		dB
	–3dB Input Bandwidth				34		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps
	Transient Response	Full-Scale Step			0.5		µs

REFERENCE INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	(Note 5)	●	2.5		5.1	V
I_{REF}	Reference Input Current	(Note 9)	●		0.47	0.53	mA
$V_{IH\overline{DGC}}$	High Level Input Voltage REF/$\overline{DGC}$ Pin		●	$0.8V_{REF}$			V
$V_{IL\overline{DGC}}$	Low Level Input Voltage REF/$\overline{DGC}$ Pin		●			$0.2V_{REF}$	V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.8 \cdot OV_{DD}$			V
V_{IL}	Low Level Input Voltage		●			$0.2 \cdot OV_{DD}$	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.375	2.5	2.625	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	500ksps Sample Rate	●		4.2	4.9	mA
I_{OVDD}	Supply Current	500ksps Sample Rate (C_L = 20pF)			0.1		mA
I_{PD}	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})	●		1	90	µA
P_D	Power Dissipation	500ksps Sample Rate			10.5	12.25	mW
	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})			2.5	225	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			500	ksps
t_{CONV}	Conversion Time		●	1		1.5	µs
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{HOLD} (Note 10)	●	1.312			µs
t_{HOLD}	Maximum Time Between Acquisitions		●			688	ns
t_{CYC}	Time Between Conversions		●	2			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{BUSYLH}	CNV↑ to BUSY Delay	C_L = 20pF	●			13	ns
t_{CNVL}	Minimum Low Time for CNV	(Note 11)	●	20			ns
t_{QUIET}	SCK Quiet Time from CNV↑	(Note 10)	●	20			ns
t_{SCK}	SCK Period	(Notes 11, 12)	●	10			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SCKH}	SCK High Time		●	4			ns
t_{SCKL}	SCK Low Time		●	4			ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	(Note 11)	●	4			ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	(Note 11)	●	1			ns
t_{SCKCH}	SCK Period in Chain Mode	$t_{SCKCH} = t_{SSDISCK} + t_{DSDO}$ (Note 11)	●	13.5			ns
t_{DSDO}	SDO Data Valid Delay from SCK↑	C_L = 20pF, OV_{DD} = 5.25V C_L = 20pF, OV_{DD} = 2.5V C_L = 20pF, OV_{DD} = 1.71V	● ● ●			7.5 8 9.5	ns ns ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↑	C_L = 20pF (Note 10)	●	1			ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 20pF (Note 10)	●			5	ns
t_{EN}	Bus Enable Time After RDL↓	(Note 11)	●			16	ns
t_{DIS}	Bus Relinquish Time After RDL↑	(Note 11)	●			13	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may effect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latch-up.

Note 4: V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 5V, V_{CM} = 2.5V, f_{SMPL} = 500kHz, REF/$\overline{DGC}$ = V_{REF}.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 0000 and 1111 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±5V input with a 5V reference voltage.

Note 9: f_{SMPL} = 500kHz, I_{REF} varies proportionately with sample rate.

Note 10: Guaranteed by design, not subject to test.

Note 11: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 12: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising capture.

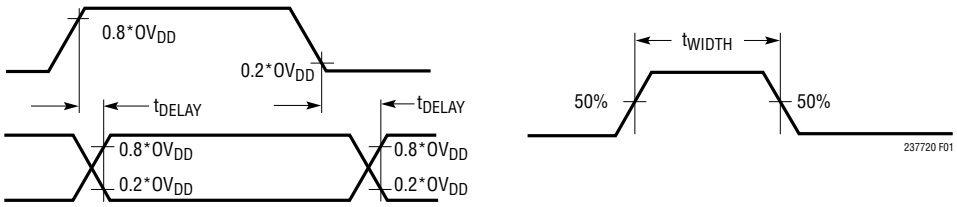
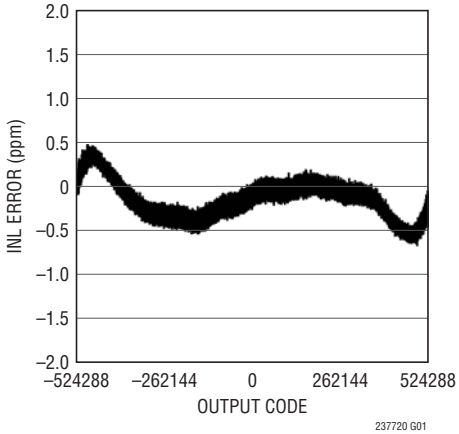


Figure 1. Voltage Levels for Timing Specifications

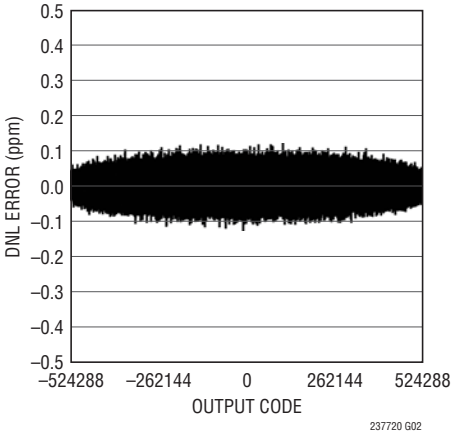
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 500ksps, unless otherwise noted.

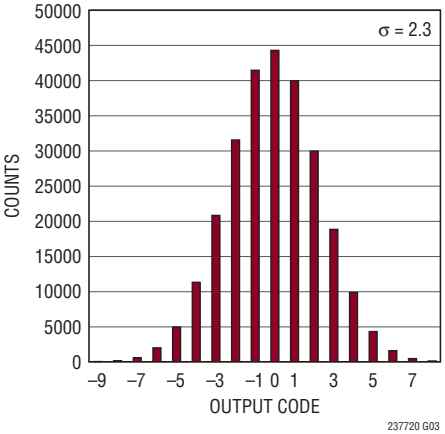
Integral Nonlinearity vs Output Code



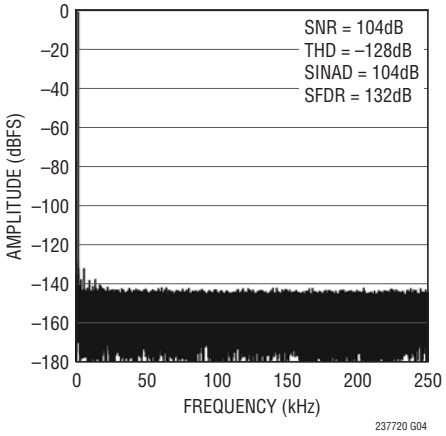
Differential Nonlinearity vs Output Code



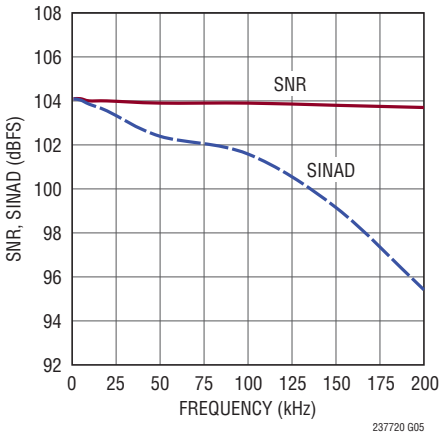
DC Histogram



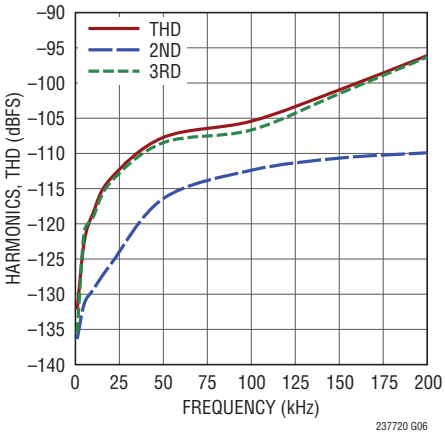
128k Point FFT f_S = 500ksps, f_{IN} = 2kHz



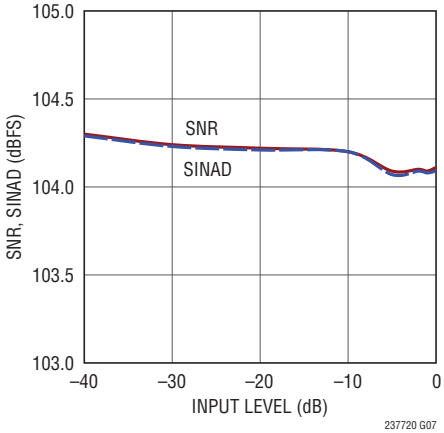
SNR, SINAD vs Input Frequency



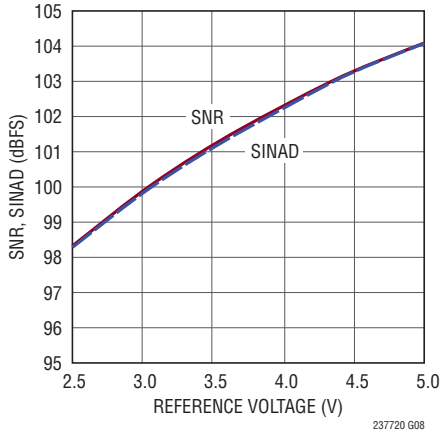
THD, Harmonics vs Input Frequency



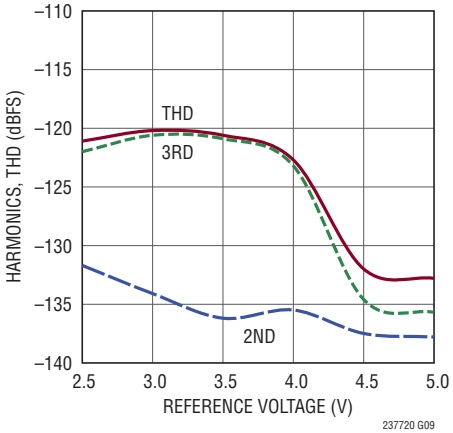
SNR, SINAD vs Input Level, f_{IN} = 2kHz



SNR, SINAD vs Reference Voltage, f_{IN} = 2kHz



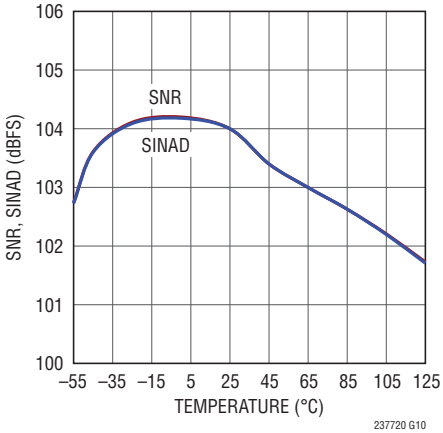
THD, Harmonics vs Reference Voltage, f_{IN} = 2kHz



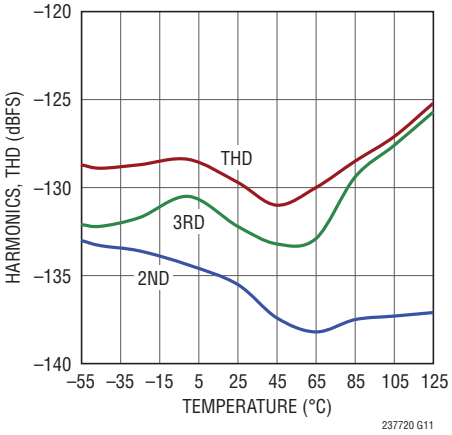
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 500ksps, unless otherwise noted.

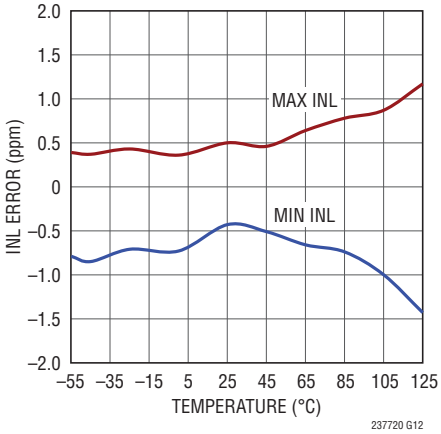
SNR, SINAD vs Temperature, f_{IN} = 2kHz



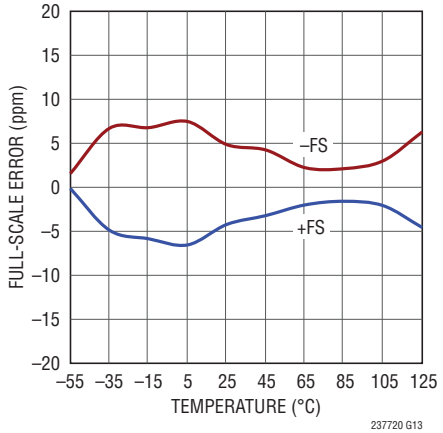
THD, Harmonics vs Temperature, f_{IN} = 2kHz



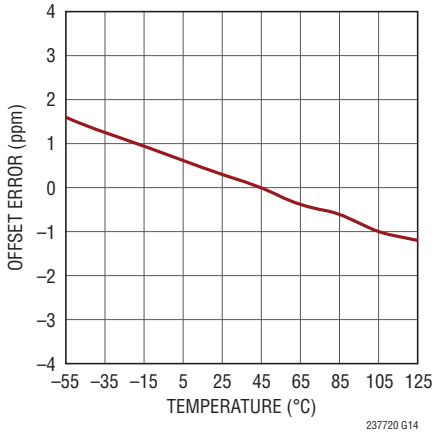
INL vs Temperature



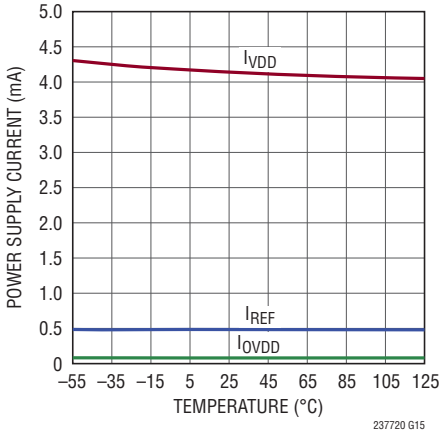
Full-Scale Error vs Temperature



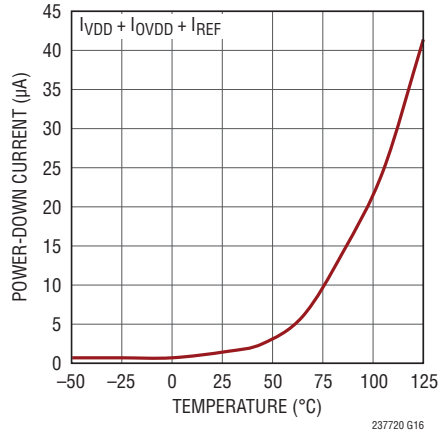
Offset Error vs Temperature



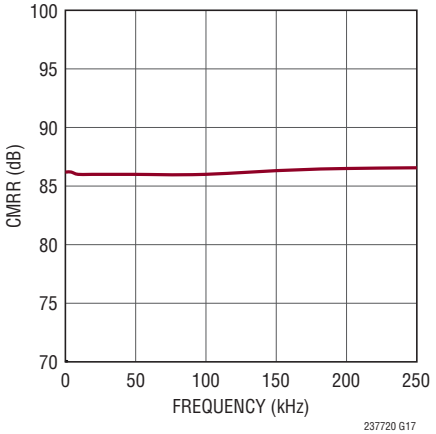
Supply Current vs Temperature



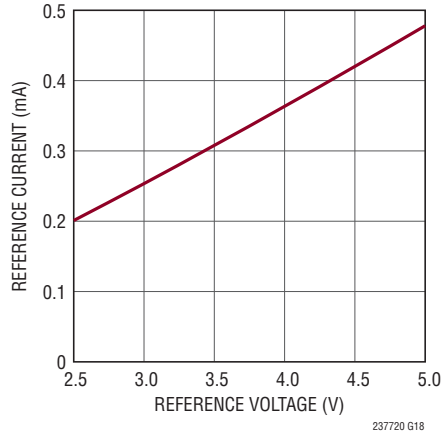
Shutdown Current vs Temperature



CMRR vs Input Frequency



Reference Current vs Reference Voltage



PIN FUNCTIONS

CHAIN (Pin 1): Chain Mode Selector Pin. When low, the LTC2377-20 operates in normal mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2377-20 operates in chain mode and the RDL/SDI pin functions as SDI, the daisy-chain serial data input. Logic levels are determined by OV_{DD}.

V_{DD} (Pin 2): 2.5V Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 3, 6, 10 and 16): Ground.

IN^+, IN^- (Pins 4, 5): Positive and Negative Differential Analog Inputs.

REF (Pin 7): Reference Input. The range of REF is 2.5V to 5.1V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating).

REF/$\overline{DGC}$ (Pin 8): When tied to REF, digital gain compression is disabled and the LTC2377-20 defines full-scale according to the $\pm V_{REF}$ analog input range. When tied to GND, digital gain compression is enabled and the LTC2377-20 defines full-scale with inputs that swing between 10% and 90% of the $\pm V_{REF}$ analog input range.

CNV (Pin 9): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

BUSY (Pin 11): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

RDL/SDI (Pin 12): When CHAIN is low, the part is in normal mode and the pin is treated as a bus enabling input. When CHAIN is high, the part is in chain mode and the pin is treated as a serial data input pin where data from another ADC in the daisy chain is input. Logic levels are determined by OV_{DD}.

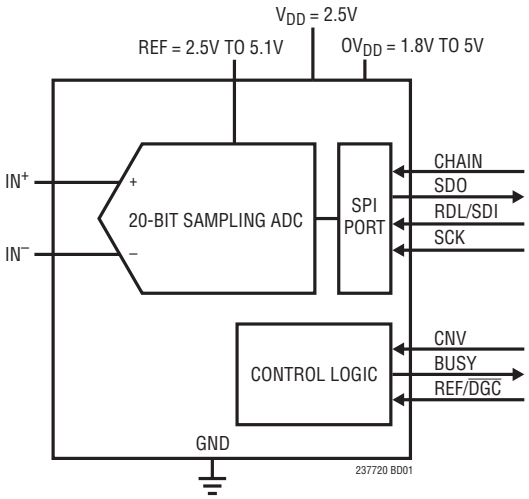
SCK (Pin 13): Serial Data Clock Input. When SDO is enabled, the conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSB first. Logic levels are determined by OV_{DD}.

SDO (Pin 14): Serial Data Output. The conversion result or daisy-chain data is output on this pin on each rising edge of SCK MSB first. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

OV_{DD} (Pin 15): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.

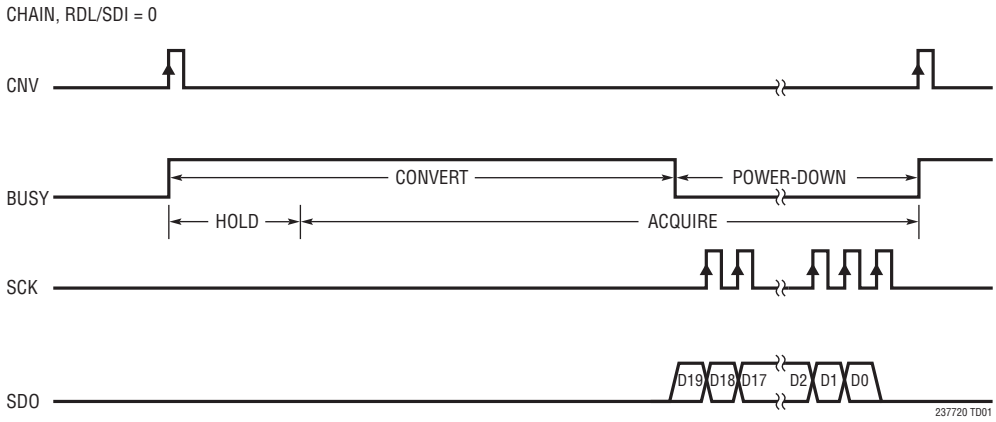
GND (Exposed Pad Pin 17 – DFN Package Only): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Conversion Timing Using the Serial Interface



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OVERVIEW

The LTC2377-20 is a low noise, low power, high speed 20-bit successive approximation register (SAR) ADC. Operating from a single 2.5V supply, the LTC2377-20 supports a large and flexible $\pm V_{REF}$ fully differential input range with V_{REF} ranging from 2.5V to 5.1V, making it ideal for high performance applications which require a wide dynamic range. The LTC2377-20 achieves ±2ppm INL maximum, no missing codes at 20 bits and 104dB SNR.

Fast 500ksps throughput with no cycle latency makes the LTC2377-20 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2377-20 dissipates only 10.5mW at 500ksps, while an auto power-down feature is provided to further reduce power dissipation during inactive periods.

The LTC2377-20 features a unique digital gain compression (DGC) function, which eliminates the driver amplifier's negative supply while preserving the full resolution of the ADC. When enabled, the ADC performs a digital scaling function that maps zero-scale code from 0V to $0.1 \cdot V_{REF}$ and full-scale code from V_{REF} to $0.9 \cdot V_{REF}$. For a typical reference voltage of 5V, the full-scale input range is now 0.5V to 4.5V, which provides adequate headroom for powering the driving amplifier from a single 5.5V supply.

CONVERTER OPERATION

The LTC2377-20 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the differential analog input voltage. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 20-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/1048576$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 20-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2377-20 digitizes the full-scale voltage of $2 \times$ REF into 2^{20} levels, resulting in an LSB size of 9.5µV with REF = 5V. Note that 1 LSB at 20 bits is approximately 1ppm. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

ANALOG INPUT

The analog inputs of the LTC2377-20 are fully differential in order to maximize the signal swing that can be digitized. The analog inputs can be modeled by the equivalent circuit

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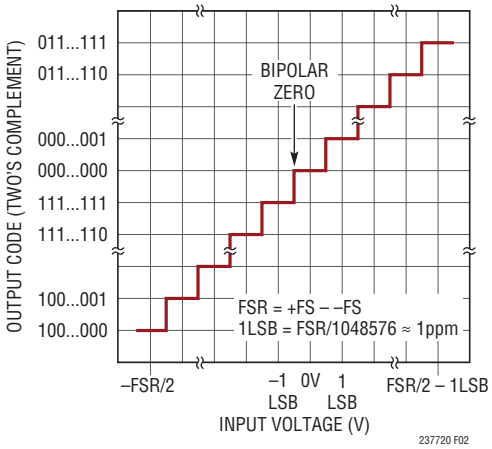

Figure 2. LTC2377-20 Transfer Function

shown in Figure 3. The diodes at the input provide ESD protection. In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC. The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2377-20 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2377-20. The amplifier provides low output impedance, which produces fast settling of the analog

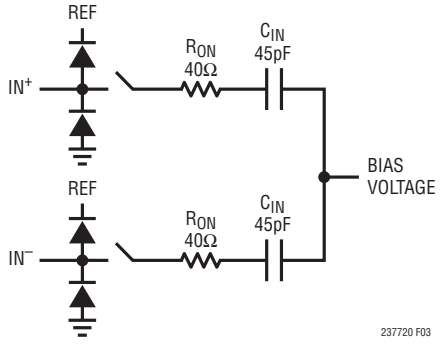

Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2377-20

signal during the acquisition phase. It also provides isolation between the signal source and the ADC input currents.

Noise and Distortion

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.

A coupling filter network (LPF2) should be used between

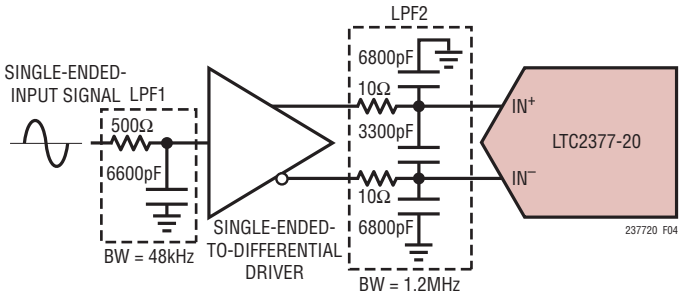

Figure 4. Input Signal Chain

the buffer and ADC input to minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer. A buffer amplifier with a low noise density must be selected to minimize degradation of the SNR.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2377-20 is in dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase. The ADC inputs may be modeled as a switched capacitor

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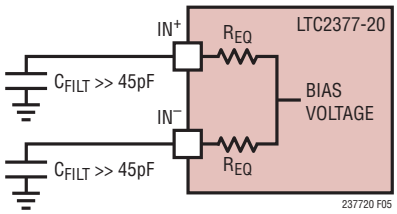
load of the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors (C_{FILT}) placed directly at the ADC inputs, and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled – This case is characterized by filter time constants and an overall settling time that is considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2377-20), the disturbance will not contribute any error.

Partially Settled – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high-frequency energy before it reaches the amplifier.

Fully Averaged – If the coupling filter capacitors (C_{FILT}) at the ADC inputs are much larger than the ADC's sample capacitors (45pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 500ksps, the equivalent input resistance is approximately 44k (as shown in Figure 5), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and the ADC's equivalent (switched-capacitor) input resistance, thus producing a gain error.

The input leakage currents of the LTC2377-20 should also be considered when designing the input drive circuit, because source impedances will convert input leakage currents to an added input voltage error. The input leakage currents, both common mode and differential, are typically extremely small over the entire operating temperature range. Figure 6 shows input leakage currents over temperature for a typical part.



$$R_{EQ} = \frac{1}{f_{SMPL} \bullet 45pF}$$

Figure 5. Equivalent Circuit for the Differential Analog Input of the LTC2377-20 at 500ksps.

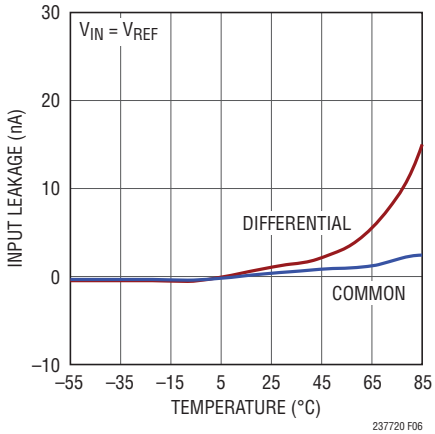


Figure 6. Common Mode and Differential Input Leakage Current Over Temperature

Let R_{S1} and R_{S2} be the source impedances of the differential input drive circuit shown in Figure 7, and let I_{L1} and I_{L2} be the leakage currents flowing out of the ADC's analog inputs. The voltage error, V_E, due to the leakage currents can be expressed as:

$$V_E = \frac{R_{S1}+R_{S2}}{2} \bullet (I_{L1}-I_{L2}) + (R_{S1}-R_{S2}) \bullet \frac{I_{L1}+I_{L2}}{2}$$

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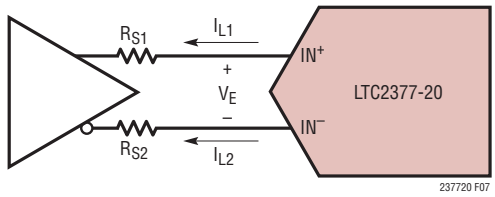

Figure 7. Source Impedances of a Driver and Input Leakage Currents of the LTC2377-20

The common mode input leakage current, $(I_{L1} + I_{L2})/2$, is typically extremely small (Figure 6) over the entire operating temperature range and common mode input voltage range. Thus, any reasonable mismatch (below 5%) of the source impedances R_{S1} and R_{S2} will cause only a negligible error. The differential input leakage current, $(I_{L1} – I_{L2})$, depends on temperature and is maximum when $V_{IN} = V_{REF}$, as shown in Figure 6. The differential leakage current is also typically very small, and its nonlinear component is even smaller. Only the nonlinear component will impact the ADC's linearity.

For optimal performance, it is recommended that the source impedances, R_{S1} and R_{S2}, be between 10Ω and 50Ω and with 1% tolerance. For source impedances in this range, the voltage and temperature coefficients of R_{S1} and R_{S2} are usually not critical. The guaranteed AC and DC specifications are tested with 10Ω source impedances, and the specifications will gradually degrade with increased source impedances due to incomplete settling of the inputs.

Fully Differential Inputs

A low distortion fully differential signal source driven through the LT6203 configured as two unity gain buffers as shown in Figure 8 can be used to get the full data sheet distortion performance of –125dB.

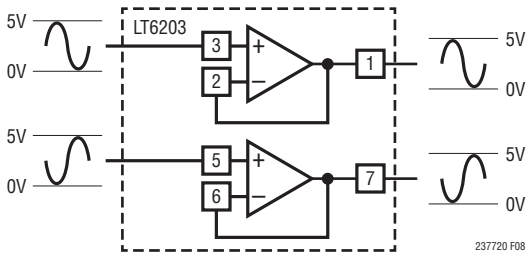

Figure 8. LT6203 Buffering a Fully Differential Signal Source

Single-Ended-to-Differential Conversion

For single-ended input signals, a single-ended-to-differential conversion circuit must be used to produce a differential signal at the inputs of the LTC2377-20. The LT6203 ADC driver is recommended for performing single-ended-to-differential conversions. The LT6203 is flexible and may be configured to convert single-ended signals of various amplitudes to the ±5V differential input range of the LTC2377-20.

Figure 9a shows the LT6203 being used to convert a 0V to 5V single-ended input signal. In this case, the first amplifier is configured as a unity gain buffer and the single-ended

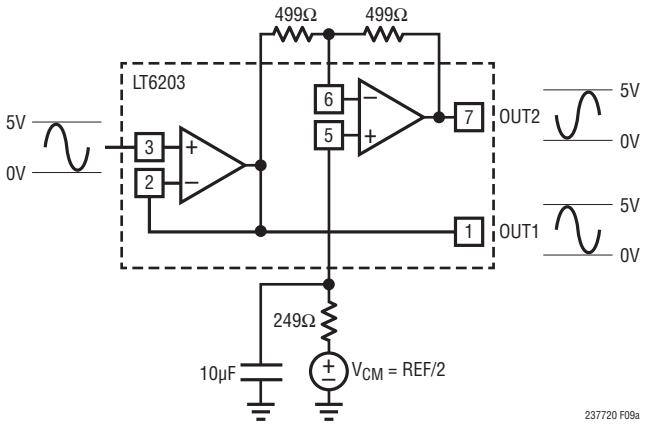

Figure 9a. LT6203 Converting a 0V to 5V Single-Ended Signal to a ±5V Differential Input Signal

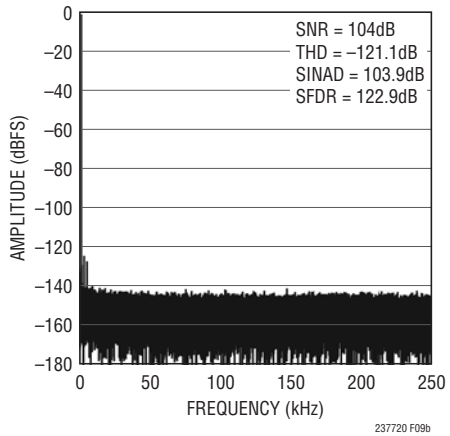

Figure 9b. 128k Point FFT Plot with f_{IN} = 2kHz for Circuit Shown in Figure 9a

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input signal directly drives the high-impedance input of the amplifier. As shown in the FFT of Figure 9b, the LT6203 drives the LTC2377-20 to near full data sheet performance.

Digital Gain Compression

The LTC2377-20 offers a digital gain compression ($\overline{DGC}$) feature which defines the full-scale input swing to be between 10% and 90% of the $\pm V_{REF}$ analog input range. To enable digital gain compression, bring the REF/$\overline{DGC}$ pin low. This feature allows the SAR ADC driver to be powered off of a single positive supply since each input swings between 0.5V and 4.5V as shown in Figure 10. Needing only one positive supply to power the SAR ADC driver results in additional power savings for the entire system.

With $\overline{DGC}$ enabled, the LTC2377-20 can be driven by the low power LTC6362 differential driver which is powered from a single 5V supply. Figure 11a shows how to configure the LTC6362 to accept a ±3.28V true bipolar single-ended input signal and level shift the signal to the reduced input range of the LTC2377-20 when digital gain compression is enabled. When paired with the LTC6655-4.096 for the reference, the entire signal chain solution can be powered from a single 5V supply, minimizing power consumption and reducing complexity. As shown in the FFT of Figure 11b, the single 5V supply solution can achieve up to 100dB of SNR.

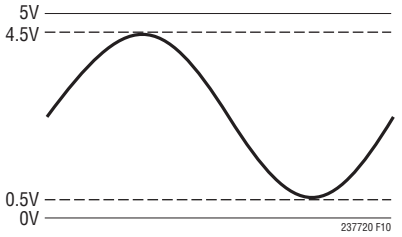

Figure 10. Input Swing of the LTC2377 with Gain Compression Enabled

DC Accuracy

Many driver circuits presented in this data sheet emphasize AC performance (distortion and signal-to-noise ratio), and the amplifiers are chosen accordingly. The very low level of distortion is a direct consequence of the excellent INL of the LTC2377-20, and this property can be exploited in DC applications as well. Note that while the LTC6362 and LT6203 are characterized by excellent AC specifications, their DC specifications do not match those of the LTC2377-20. The offset of these amplifiers, for example, is more than 500µV under certain conditions. In contrast, the LTC2377-20 has a guaranteed maximum offset error of 130µV (typical drift ±0.007ppm/°C), and a guaranteed maximum full-scale error of 100ppm (typical drift ±0.05ppm/°C). Low drift is important to maintain accuracy over wide temperature ranges in a calibrated system.

Amplifiers have to be selected very carefully to provide a 20-bit accurate DC signal chain. A large-signal open-loop gain of at least 126dB may be required to ensure 1ppm linearity for amplifiers configured for a gain of negative 1. However, less gain is sufficient if the amplifier's gain

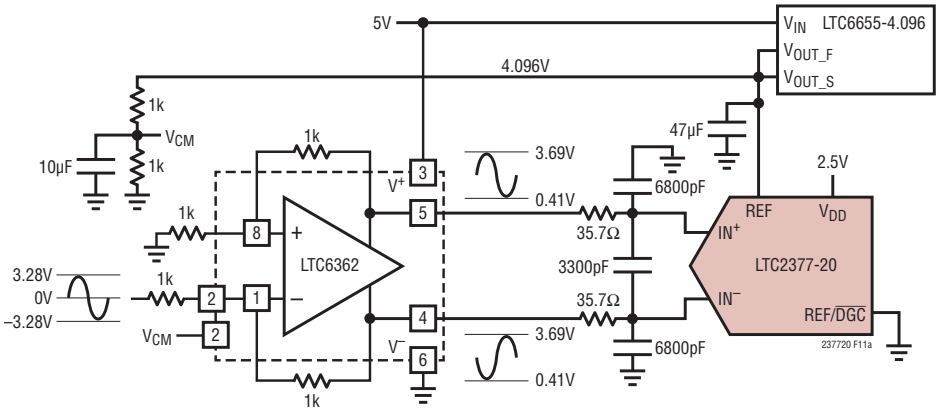

Figure 11a. LTC6362 Configured to Accept a ±3.28V Input Signal While Running from a Single 5V Supply When Digital Gain Compression Is Enabled in the LTC2377-20

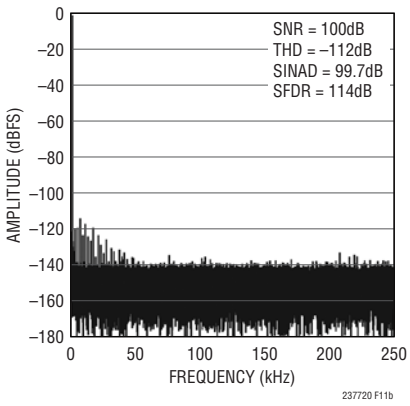

Figure 11b. 64k Point FFT Plot with f_{IN} = 2kHz for Circuit Shown in Figure 11a

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characteristic is known to be (mostly) linear. An amplifier's offset versus signal level must be considered for amplifiers configured as unity gain buffers. For example, 1ppm linearity may require that the offset is known to vary less than 5µV for a 5V swing. However, greater offset variations may be acceptable if the relationship is known to be (mostly) linear. Unity-gain buffer amplifiers typically require substantial headroom to the power supply rails for best performance. Inverting amplifier circuits configured to minimize swing at the amplifier input terminals may perform better with only little headroom than unity-gain buffer amplifiers. The linearity and thermal properties of an inverting amplifier's feedback network should be considered carefully to ensure DC accuracy.

ADC REFERENCE

The LTC2377-20 requires an external reference to define its input range. A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2377-20. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications.

When choosing a bypass capacitor for the LTC6655-5, the capacitor's voltage rating, temperature rating, and package size should be carefully considered. Physically larger capacitors with higher voltage and temperature ratings tend to provide a larger effective capacitance, better filtering the noise of the LTC6655-5, and consequently producing a higher SNR. Therefore, we recommend bypassing the LTC6655-5 with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating) close to the REF pin.

The REF pin of the LTC2377-20 draws charge (Q_{CONV}) from the 47µF bypass capacitor during each conversion cycle. The reference replenishes this charge with a DC current, $I_{REF} = Q_{CONV}/t_{CYC}$. The DC current draw of the REF pin, I_{REF}, depends on the sampling rate and output code. If the LTC2377-20 is used to continuously sample a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5LSBs.

When idling, the REF pin on the LTC2377-20 draws only a small leakage current (< 1µA). In applications where a burst of samples is taken after idling for long periods as shown in Figure 12, I_{REF} quickly goes from approximately 0µA to a maximum of 0.53mA at 500ksps. This step in DC current draw triggers a transient response in the reference that must be considered since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-5 reference is also recommended.

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2377-20 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling

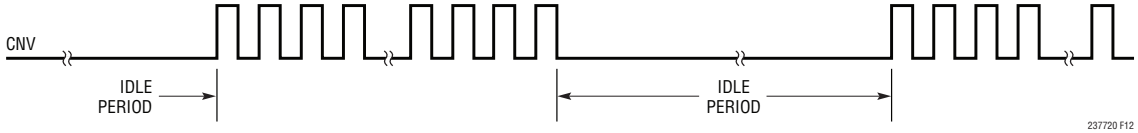

Figure 12. CNV Waveform Showing Burst Sampling

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frequency. Figure 13 shows that the LTC2377-20 achieves a typical SINAD of 104dB at a 500kHz sampling rate with a 2kHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and

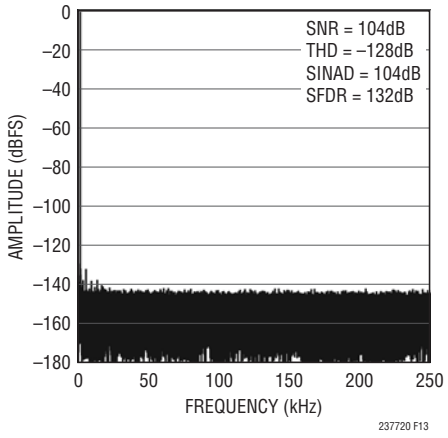

Figure 13. 128k Point FFT Plot with f_{IN} = 2kHz of the LTC2377-20

the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 13 shows that the LTC2377-20 achieves a typical SNR of 104dB at a 500kHz sampling rate with a 2kHz input.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2377-20 provides two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2377-20 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2377-20 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2377-20 has a power-on-reset (POR) circuit that will reset the LTC2377-20 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 200µs after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

CNV Timing

The LTC2377-20 conversion is controlled by CNV. A rising edge on CNV will start a conversion and power up the LTC2377-20. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed.

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Acquisition

A proprietary sampling architecture allows the LTC2377-20 to begin acquiring the input signal for the next conversion 675ns after the start of the current conversion. This extends the acquisition time to 1.312µs, easing settling requirements and allowing the use of extremely low power ADC drivers. (Refer to the Timing Diagram.)

Internal Conversion Clock

The LTC2377-20 has an internal clock that is trimmed to achieve a maximum conversion time of 1.5µs.

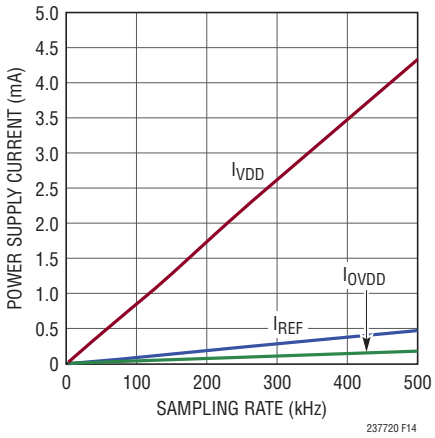


Figure 14. Power Supply Current of the LTC2377-20 Versus Sampling Rate

Auto Power-Down

The LTC2377-20 automatically powers down after a conversion has been completed and powers up once a new conversion is initiated on the rising edge of CNV. During power down, data from the last conversion can be clocked out. To minimize power dissipation during power down, disable SDO and turn off SCK. The auto power-down feature will reduce the power dissipation of the LTC2377-20 as the sampling frequency is reduced. Since power is consumed only during a conversion, the LTC2377-20 remains powered-down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 14.

DIGITAL INTERFACE

The LTC2377-20 has a serial digital interface. The flexible OV_{DD} supply allows the LTC2377-20 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

The serial output data is clocked out on the SDO pin when an external clock is applied to the SCK pin if SDO is enabled. Clocking out the data after the conversion will yield the best performance. With a shift clock frequency of at least 40MHz, a 500ksps throughput is still achieved. The serial output data changes state on the rising edge of SCK and can be captured on the falling edge or next rising edge of SCK. D19 remains valid until the first rising edge of SCK.

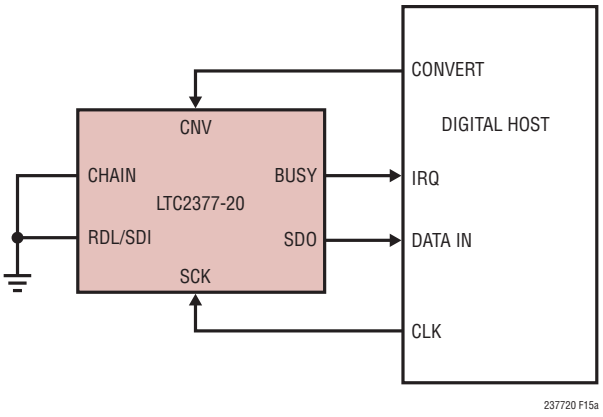
The serial interface on the LTC2377-20 is simple and straightforward to use. The following sections describe the operation of the LTC2377-20. Several modes are provided depending on whether a single or multiple ADCs share the SPI bus or are daisy chained.

APPLICATIONS INFORMATION

Normal Mode, Single Device

When CHAIN = 0, the LTC2377-20 operates in normal mode. In normal mode, RDL/SDI enables or disables the serial data output pin SDO. If RDL/SDI is high, SDO is in high impedance. If RDL/SDI is low, SDO is driven.

Figure 15 shows a single LTC2377-20 operated in normal mode with CHAIN and RDL/SDI tied to ground. With RDL/SDI grounded, SDO is enabled and the MSB(D19) of the new conversion data is available at the falling edge of BUSY. This is the simplest way to operate the LTC2377-20.



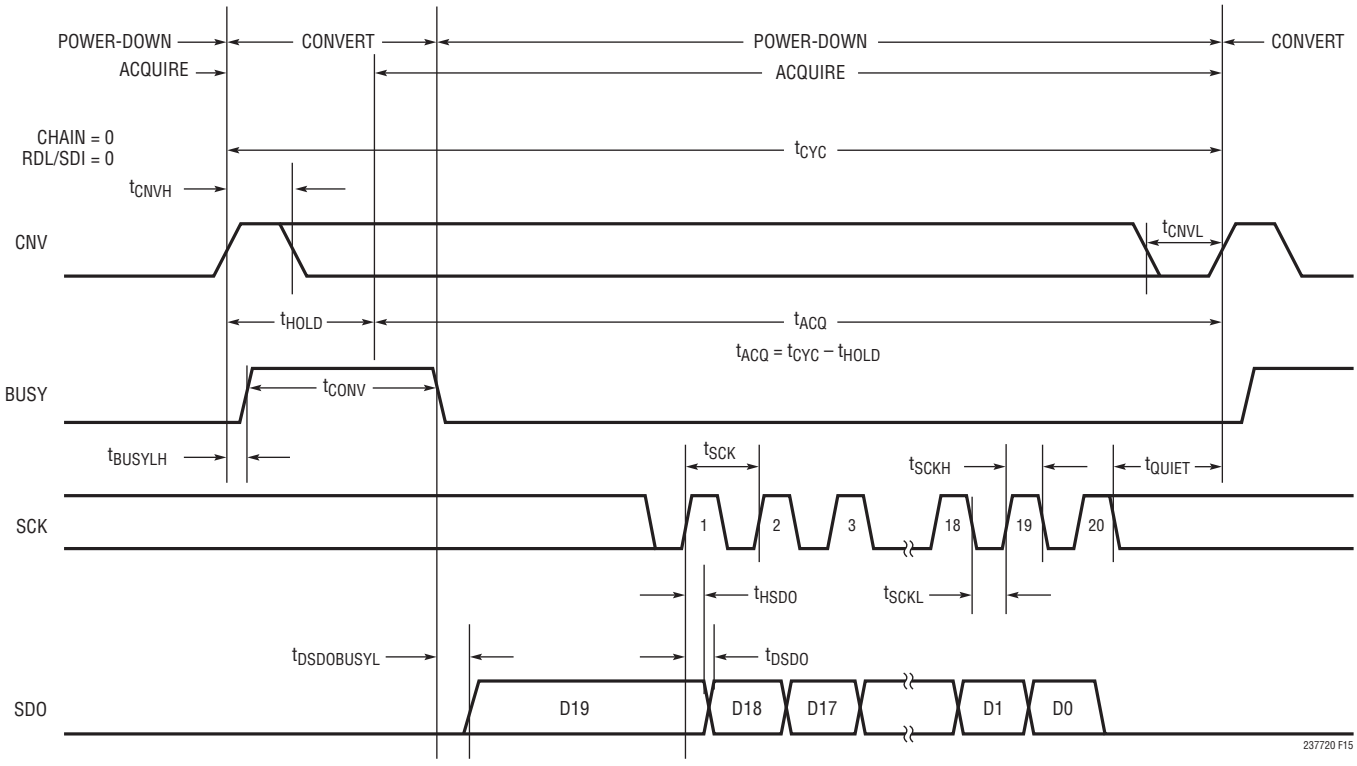


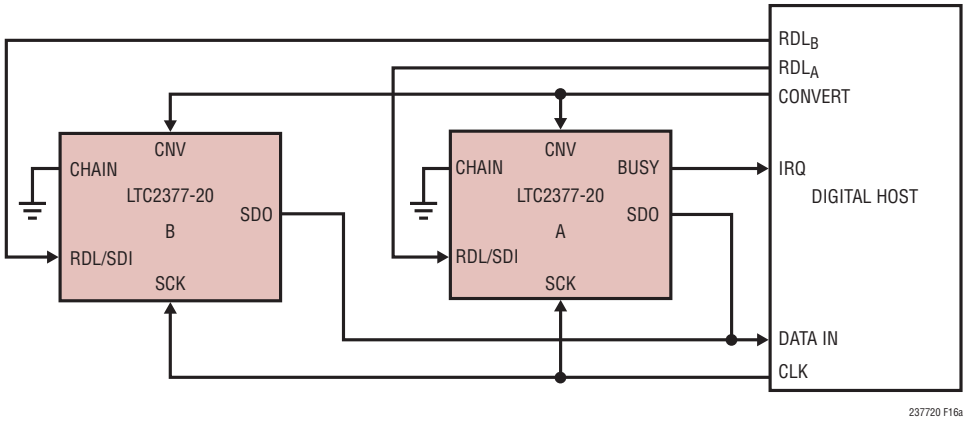
Figure 15. Using a Single LTC2377-20 in Normal Mode

APPLICATIONS INFORMATION

Normal Mode, Multiple Devices

Figure 16 shows multiple LTC2377-20 devices operating in normal mode (CHAIN = 0) sharing CNV, SCK and SDO. By sharing CNV, SCK and SDO, the number of required signals to operate multiple ADCs in parallel is reduced.

Since SDO is shared, the RDL/SDI input of each ADC must be used to allow only one LTC2377-20 to drive SDO at a time in order to avoid bus conflicts. As shown in Figure 16, the RDL/SDI inputs idle high and are individually brought low to read data out of each device between conversions. When RDL/SDI is brought low, the MSB of the selected device is output onto SDO.



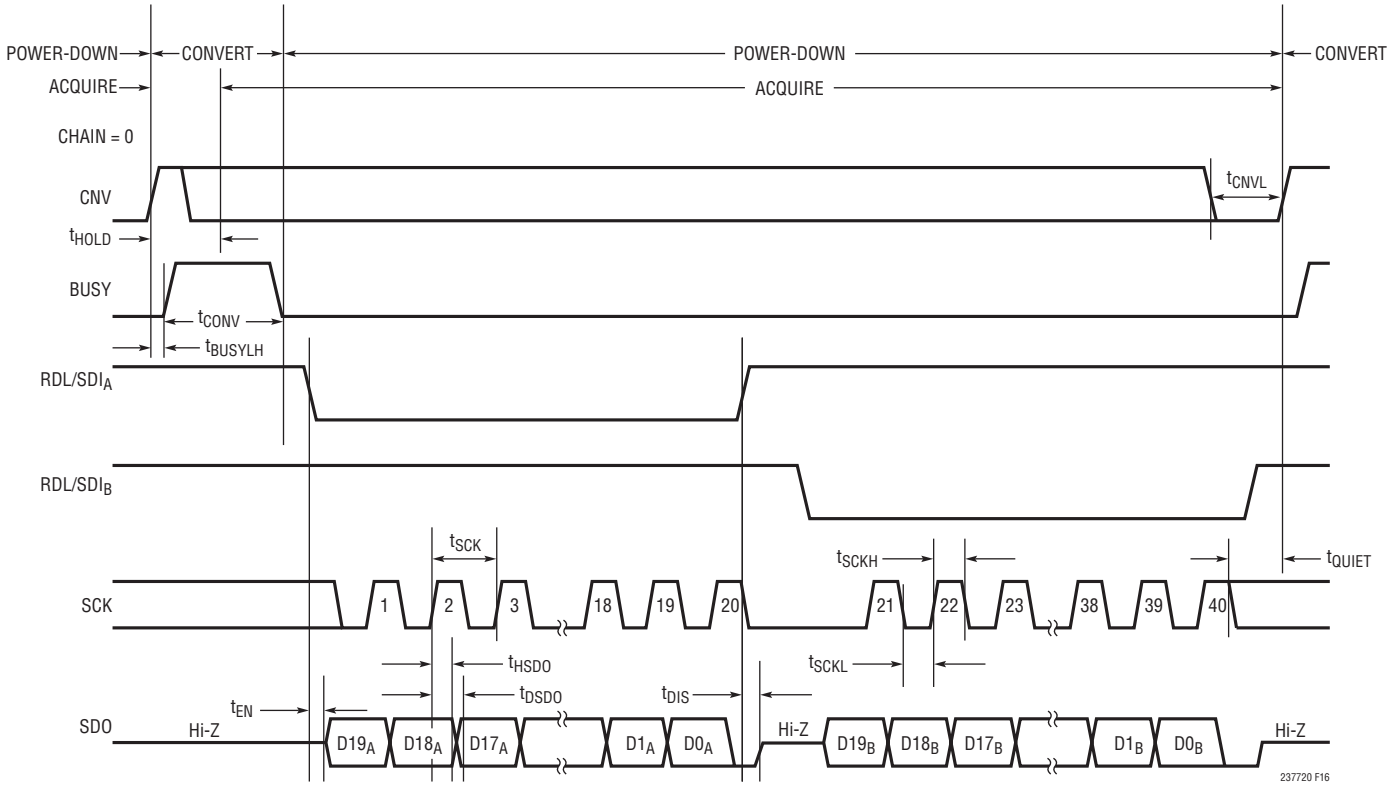


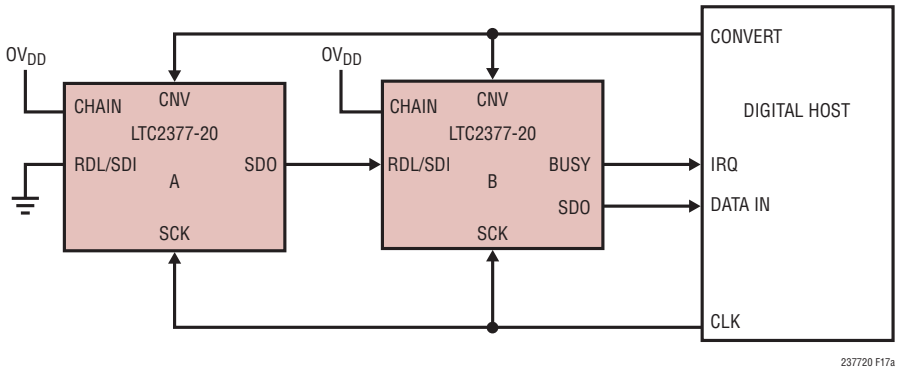
Figure 16. Normal Mode With Multiple Devices Sharing CNV, SCK and SDO

APPLICATIONS INFORMATION

Chain Mode, Multiple Devices

When CHAIN = OV_{DD}, the LTC2377-20 operates in chain mode. In chain mode, SDO is always enabled and RDL/SDI serves as the serial data input pin (SDI) where daisy-chain data output from another ADC can be input.

This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. Figure 17 shows an example with two daisy-chained devices. The MSB of converter A will appear at SDO of converter B after 20 SCK cycles. The MSB of converter A is clocked in at the SDI/RDL pin of converter B on the rising edge of the first SCK.



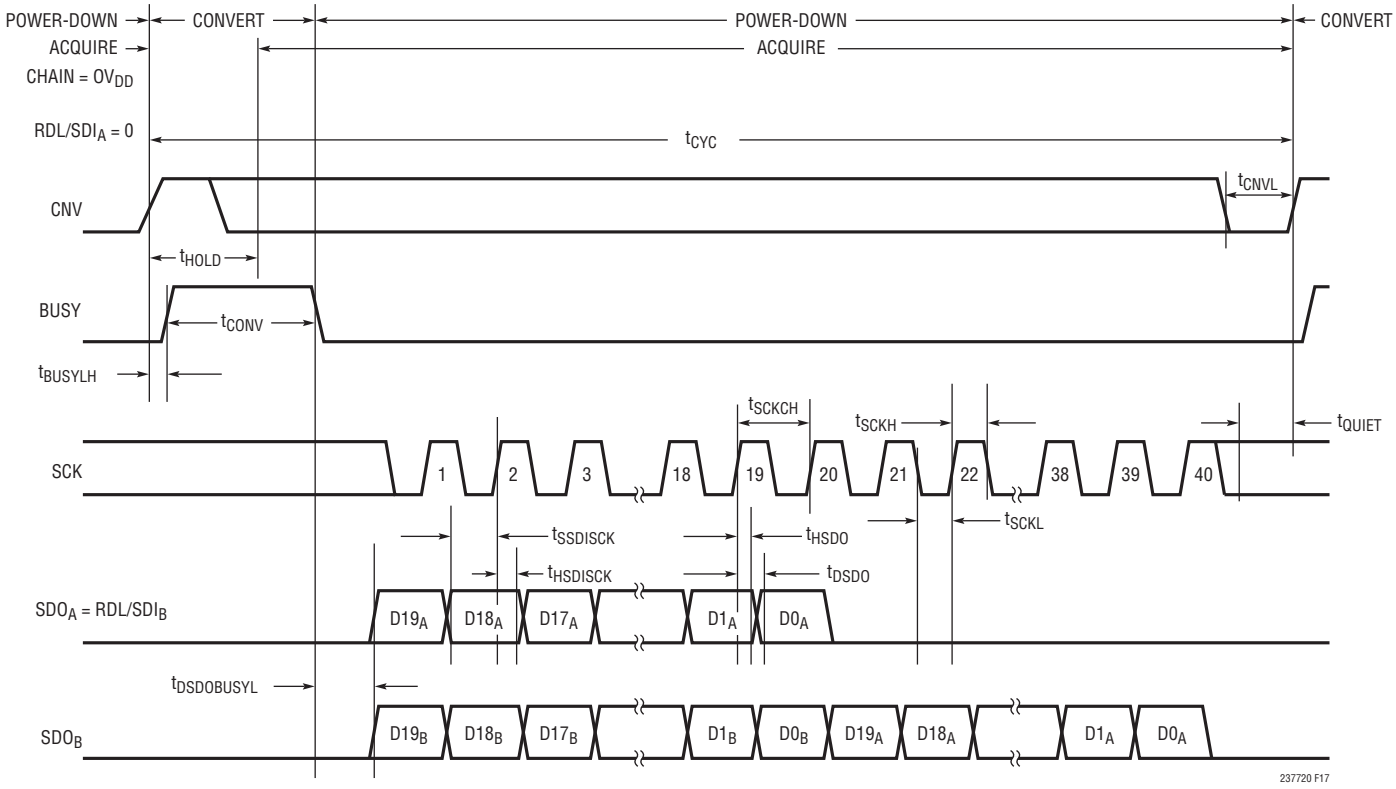


Figure 17. Chain Mode Timing Diagram

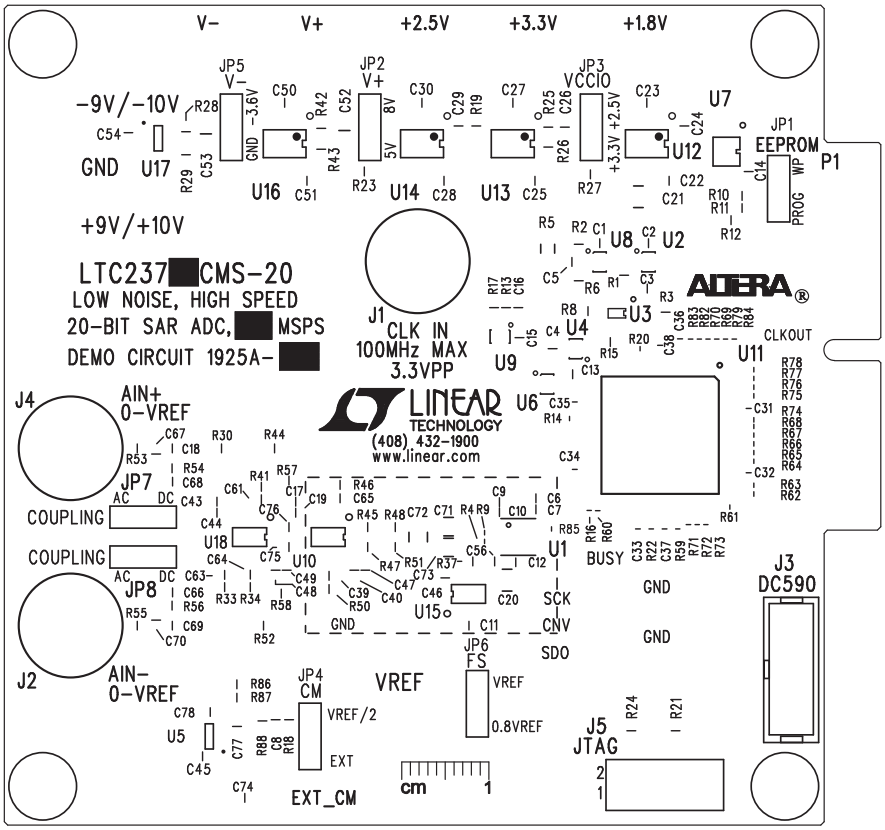
BOARD LAYOUT

To obtain the best performance from the LTC2377-20 a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Recommended Layout

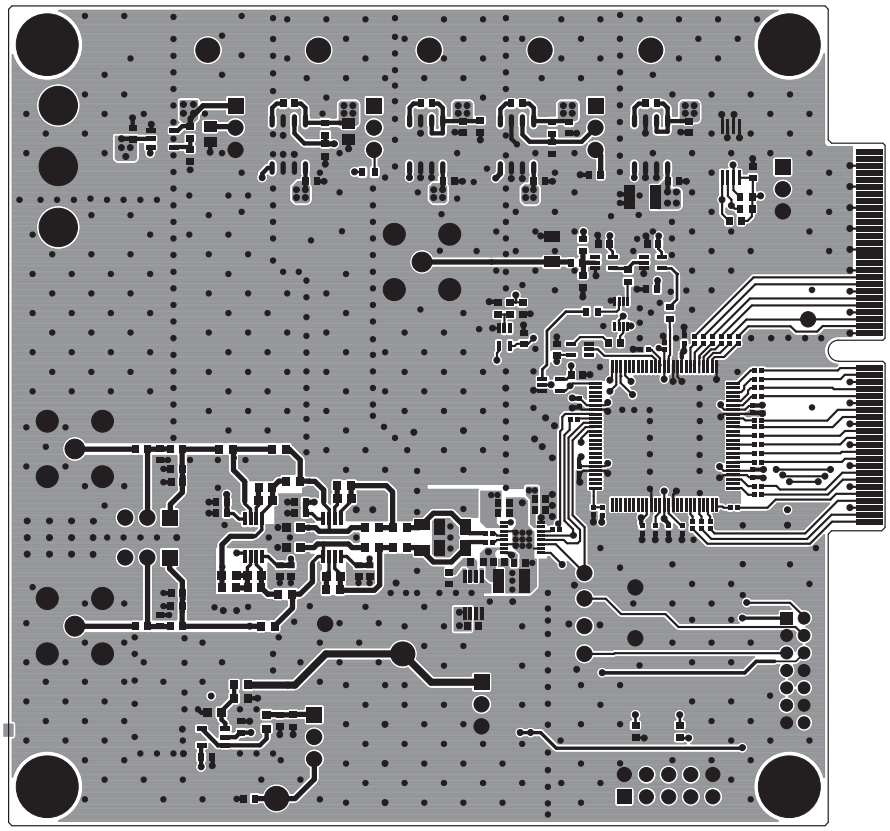
The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1925A, the evaluation kit for the LTC2377-20.

Top Silkscreen



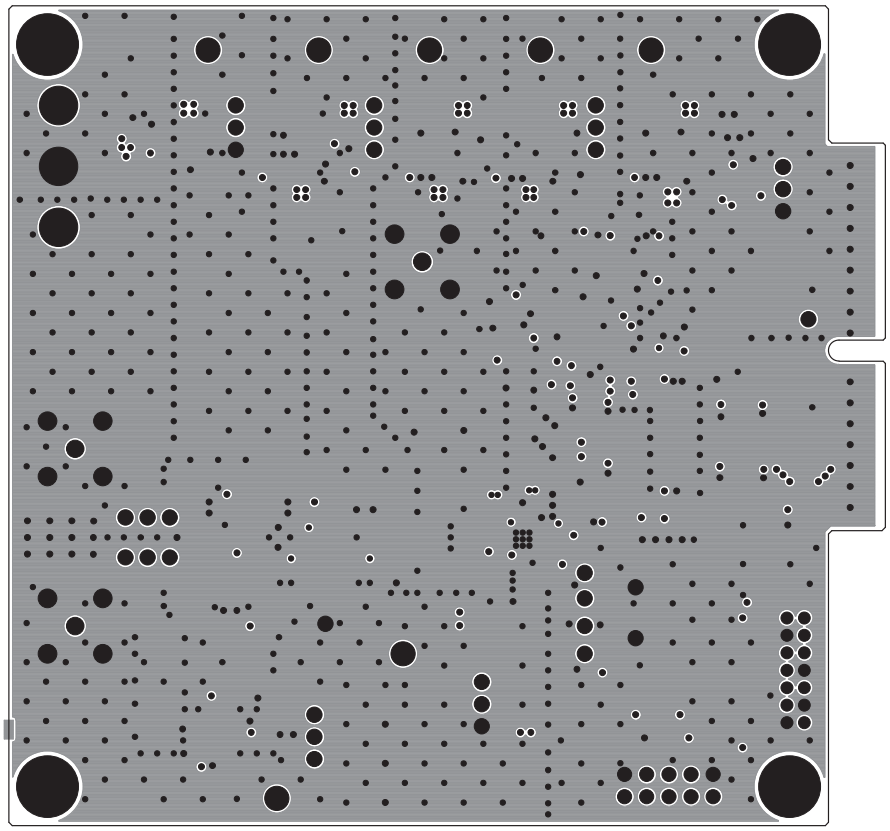
BOARD LAYOUT

Layer 1 Component Side



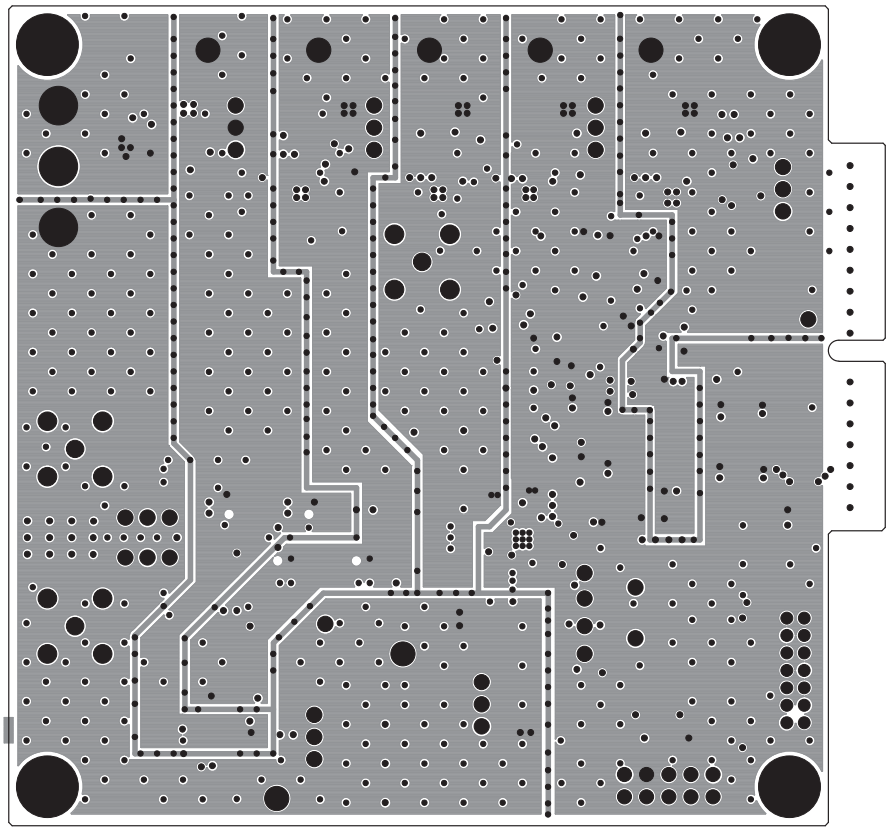
BOARD LAYOUT

Layer 2 Ground Plane



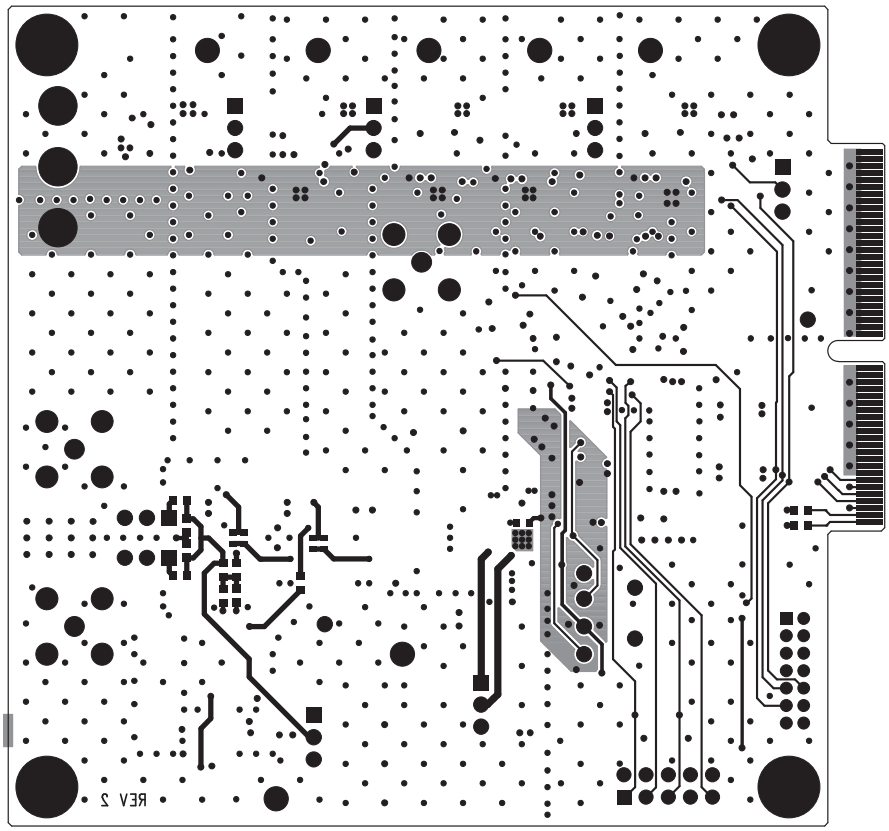
BOARD LAYOUT

Layer 3 PWR Plane



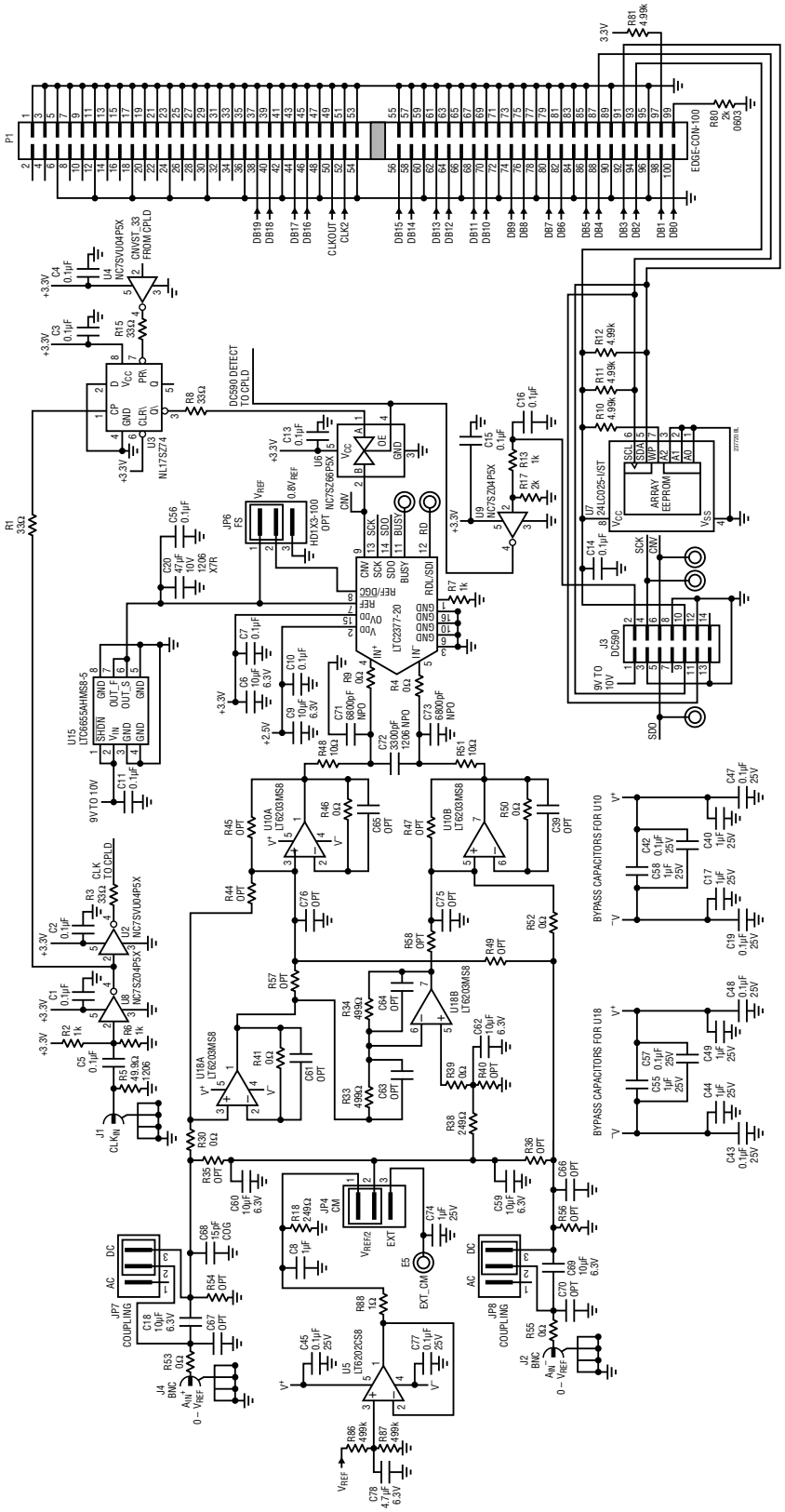
BOARD LAYOUT

Layer 4 Bottom Layer



BOARD LAYOUT

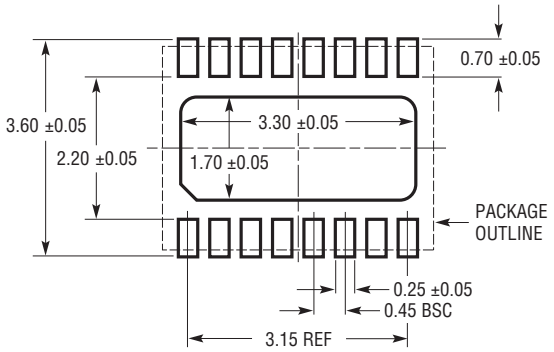
Partial Schematic of Demoboard



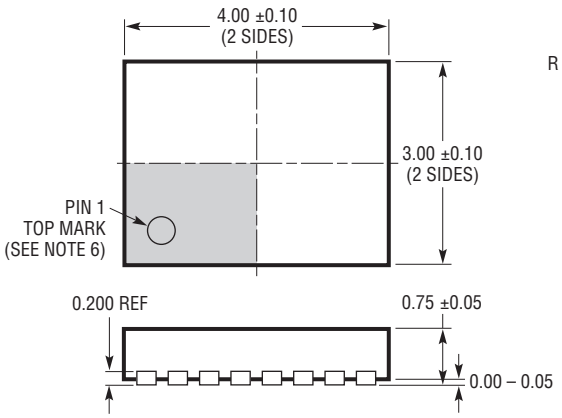
PACKAGE DESCRIPTION

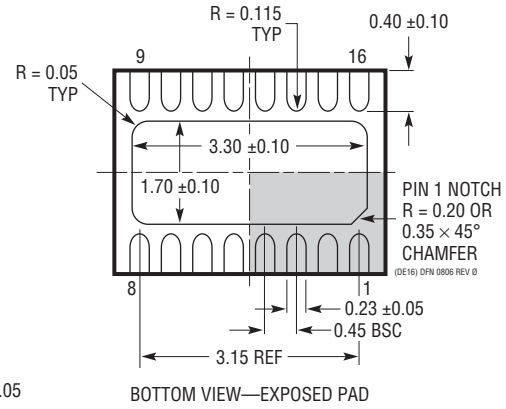
Please refer to http://www.linear.com/product/LTC2377-20#packaging for the most recent package drawings.

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





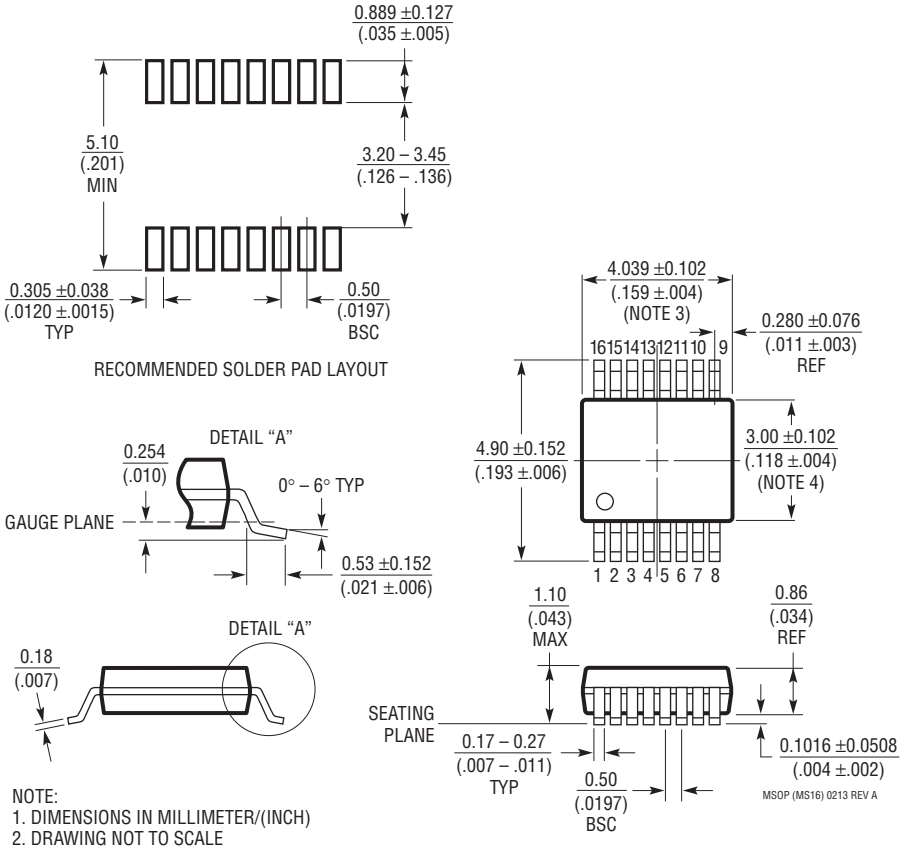
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2377-20#packaging for the most recent package drawings.

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/15	Corrected a typo in the schematic of Figure 11a and Typical Application	14 and 30
B	09/16	Updated graphs G01, G02 and G03.	6

LINEAR TECHNOLOGY

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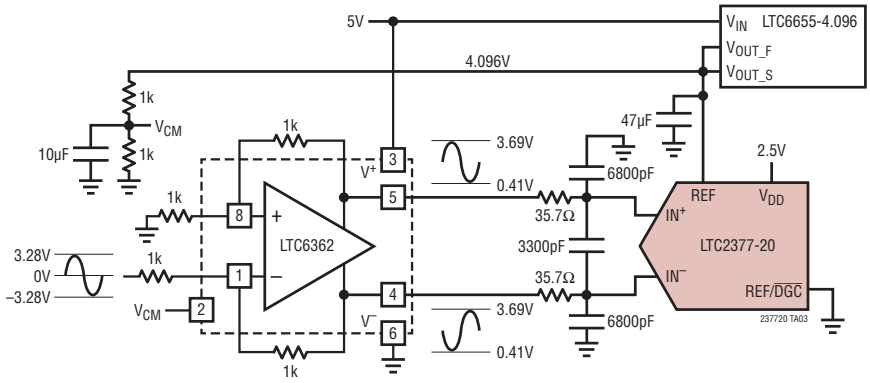
TYPICAL APPLICATION

LTC6362 Configured to Accept a ±3.28V Input Signal While Running from a Single 5V Supply with Digital Gain Compression Enabled in the LTC2377-20



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2378-20	20-Bit, 1Msps, ±0.5ppm INL Serial, Low Power ADC	2.5V Supply, ±5V Fully Differential Input, 104dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2379-18/LTC2378-18 LTC2377-18/LTC2376-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16 LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2369-18/LTC2368-18/ LTC2367-18/LTC2364-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 96.5dB SNR, 0V to 5V Input Range, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2370-16/LTC2368-16 LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 0V to 5V Input Range, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2389-18/LTC2389-16	18-/16-Bit, 2.5Msps Parallel/Serial, ADC	5V Supply, Pin Configurable Input Range, 99.8dB SNR, Pin Compatible Parts in 7mm × 7mm LQFP-48 and QFN-48 Packages
LTC2383-16/LTC2382-16/ LTC2381-16	16-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 92dB SNR, ±2.5V Input Range, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
DACS		
LTC2756/LTC2757	18-Bit, Single Serial/Parallel I_{OUT} SoftSpan™ DAC	±1LSB INL/DNL, SSOP-28 and 7mm × 7mm LQFP-48 Packages
LTC2641	16-/14-/12-Bit Single Serial V_{OUT} DAC	±1LSB INL/DNL, MSOP-8 Package, 0V to 5V Output
LTC2630	12-/10-/8-Bit Single V_{OUT} DACs	SC70 6-Pin Package, Internal Reference, ±1LSB INL (12 Bits)
REFERENCES		
LTC6655	Precision Low Drift Low Noise Buffered Reference	5V/2.5V, 5ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift Low Noise Buffered Reference	5V/2.5V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
AMPLIFIERS		
LTC6362	Low Power Rail-to-Rail Input/Output Differential Output Amplifier/ADC Driver	Single 2.8V to 5.25V Supply, 1mA Supply Current, MSOP-8 and 3mm × 3mm DFN-8 Packages
LT6200/LT6200-5/ LT6200-10	165MHz/800MHz/1.6GHz Op Amp with Unity Gain/AV = 5/AV = 10	Low Noise Voltage: 0.95nV/√Hz (100kHz), Low Distortion: –80dB at 1MHz, TSOT23-6 Package
LT6202/LT6203	Single/Dual 100MHz Rail-to-Rail Input/Output Noise Low Power Amplifiers	1.9nV√Hz, 3mA Maximum, 100MHz Gain Bandwidth, TSOT23-5, SO-8 , MSOP-8 and 3mm × 3mm DFN-8 Packages

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