IRS2890DS

Half-Bridge Driver with Overcurrent Protection

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Integrated bootstrap functionality
- Suitable for both trapezoidal and sinusoidal motor control
- Overcurrent protection and fault reporting
- Advanced input filter
- Integrated deadtime protection
- Shoot-through (cross-conduction) protection
- Adjustable fault clear timing

Product Summary

V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{O+} & I_{O-} (typ.)	220 mA & 480 mA
t_{ON} & t_{OFF} (typ.)	500 ns & 500 ns
Deadtime (typ.)	300 ns

Description

The IRS2890D is a high voltage, high speed power MOSFET and IGBT half bridge gate driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or TTL outputs, down to 3.3 V logic. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction.The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.

Package Options

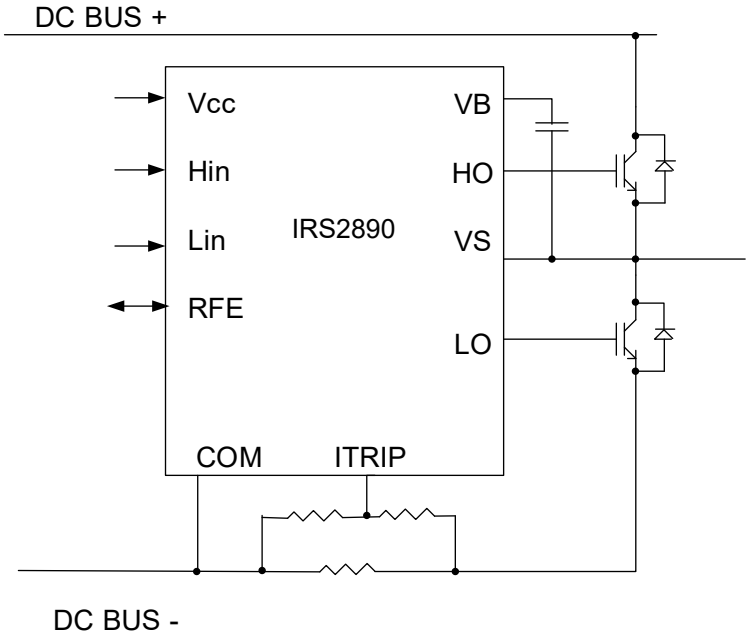
14-Lead SOIC

Typical Applications

- Motor Control
- Air Conditioners/Washing Machines
- Micro/Mini inverter drives
- General Purpose Inverters

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRS2890DSPBF	14-Lead SOIC N	Tube/Bulk	55	IRS2890DSPBF
		Tape and Reel	2500	IRS2890DSTRPBF

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to Application Notes & Design Tips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low side supply voltage	-0.3	25†	V
V_{IN}	Logic input voltage (LIN, HIN, RFE, ITRIP)	COM - 0.3	V_{CC} + 0.3	
V_B	High-side floating well supply voltage	-0.3	625	
V_S	High-side floating well supply return voltage	V_B - 25	V_B + 0.3	
V_{HO}	Floating gate drive output voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	Low-side output voltage	COM - 0.3	V_{CC} + 0.3	
COM	Power ground	V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable V_S offset supply transient relative to COM	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$+25ºC	—	1	W
Rth_{JA}	Thermal resistance, junction to ambient	—	120	ºC/W
T_J	Junction temperature	—	150	ºC
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are tested at 25V

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Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15 V.

Symbol	Definition	Min	Max	Units
V_{CC}	Low-side supply voltage	10	20	V
V_{IN}	Logic input voltage	0	V_{CC}	
V_B	High-side floating well supply voltage	V_S + 10	V_S + 20	
V_S	High-side floating well supply offset voltage†	COM - 8†	600	
V_{St}	Transient High-side floating well supply offset voltage	- 50††	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{LO}	Low-side output voltage	COM	V_{CC}	
T_A	Ambient temperature	-40	125	ºC

† Logic operation for VS of –8 V to 200 V. Logic state held for V_S of –8 V to –V_{BS}. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative VS of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Static Electrical Characteristics

(V_{CC} - COM) = (V_B - V_S) = 15 V. T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply under voltage positive threshold	8.0	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply under voltage negative threshold	6.9	7.7	8.5		
V_{BSUVHY}	V_{BS} supply under voltage hysteresis	—	1.2	—		
V_{CCUV+}	V_{CC} supply under voltage positive threshold	8.0	8.9	9.8		
V_{CCUV-}	V_{CC} supply under voltage negative threshold	6.9	7.7	8.5		
V_{CCUVHY}	V_{CC} supply under voltage hysteresis	—	1.2	—		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	0.65	—		I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	0.13	—		
V_{IH}	Logic “1” input voltage	2.2	—	—		
V_{IL}	Logic “0” input voltage	—	—	0.8		
V_{RFE+}	RFE positive going threshold	—	1.9	2.2		
V_{RFE-}	RFE negative going threshold	0.8	1.1	—		
V_{ITRIP+}	ITRIP positive going threshold	0.475	0.500	0.525		
V_{ITRIP-}	ITRIP negative going threshold	—	0.43	—		
$V_{ITRIP\ HYS}$	ITRIP hysteresis	—	0.07	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		V_{IN} = 0 V or 4 V
I_{QCC}	Quiescent V_{CC} supply current	—	—	3000		
I_{O+}	Output high short circuit pulsed current	—	220	—	mA	V_O = 0 V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	—	480	—		V_O = 15 V PW ≤ 10 µs
I_{RFE+}	Logic “1” Input bias current (RFE)	—	0	1	µA	
I_{RFE-}	Logic “0” Input bias current (RFE)	1	0	—		
I_{IN+}	Logic “1” Input bias current (LIN, HIN)	—	5	10		V_{IN} = 4 V
I_{IN-}	Logic “0” Input bias current (LIN, HIN)	—	—	1		V_{IN} = 0 V
I_{ITRIP+}	Logic “1” Input bias current (ITRIP)	—	5	10		V_{IN} = 4 V
I_{ITRIP-}	Logic “0” Input bias current (ITRIP)	—	—	1		V_{IN} = 0 V
R_{BS}	Bootstrap resistance	—	200	—	Ω	
$R_{ON,\ RFE}$	RFE mos resistance	—	40	100	Ω	Io = 1.5mA

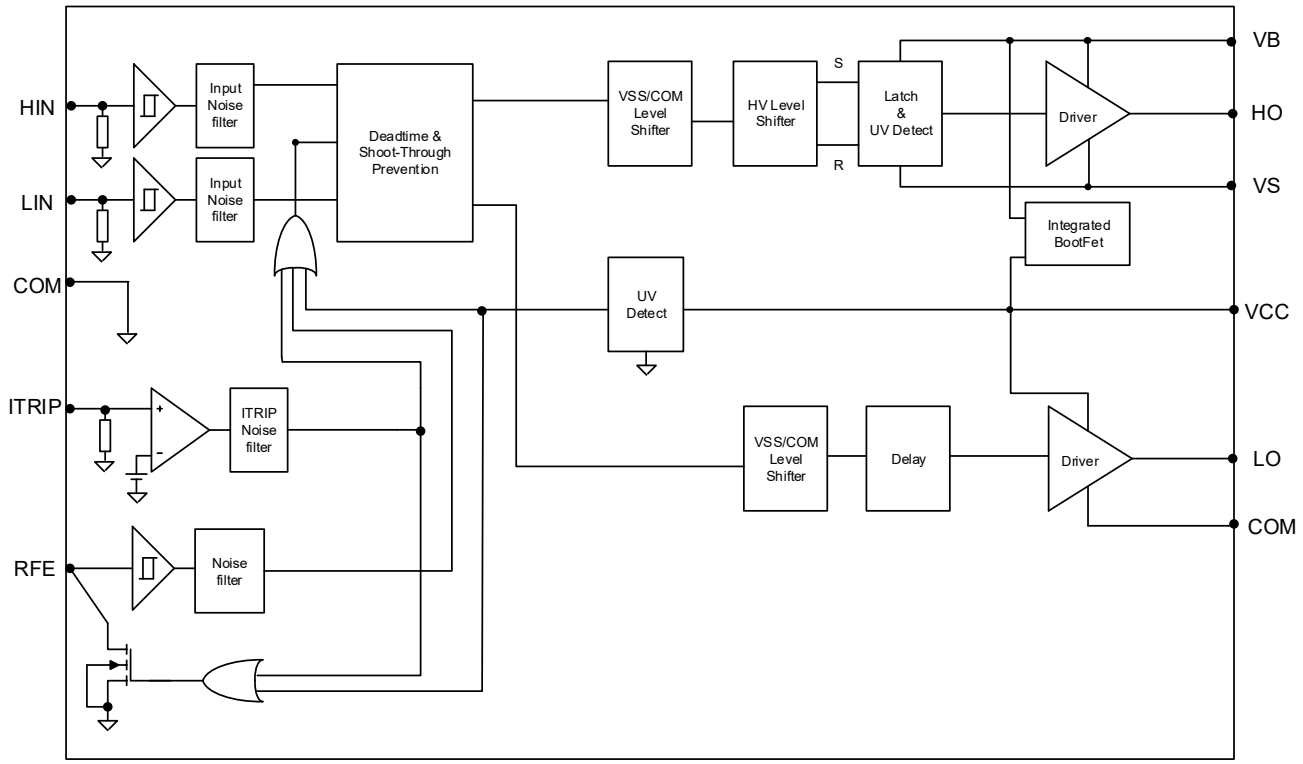
Please refer to Application Section for integrated bootstrap description.

Dynamic Electrical Characteristics

V_{CC} = V_B = 15 V, V_S = COM, T_A = 25 °C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	350	500	650	ns	V_S =0 V or 600 V
t_{OFF}	Turn-off propagation delay	350	500	650		
t_R	Turn-on rise time	—	85	—		V_S = 0 V
t_F	Turn-off fall time	—	30	—		
DT	Dead time, LO turn-off to HO turn-on & HO turn-off to LO turn-on	200	300	430		
MT	Delay matching time (t_{ON}, t_{OFF})	—	—	50		
t_{EN}	Enable low to output shutdown propagation delay	270	400	530		
$T_{FIL,EN}$	Enable input filter time	100	200	300		
T_{FLTCLR}	FAULT clear time (R = 2 MΩ, C = 1 nF)	1.35	1.75	2.1	ms	VDD = 3.3 V
T_{ITRIP}	ITRIP to output shutdown propagation delay	500	720	950	ns	
T_{BL}	ITRIP blanking time	300	500	700		
T_{FLT}	ITRIP to FAULT propagation delay	450	680	900		

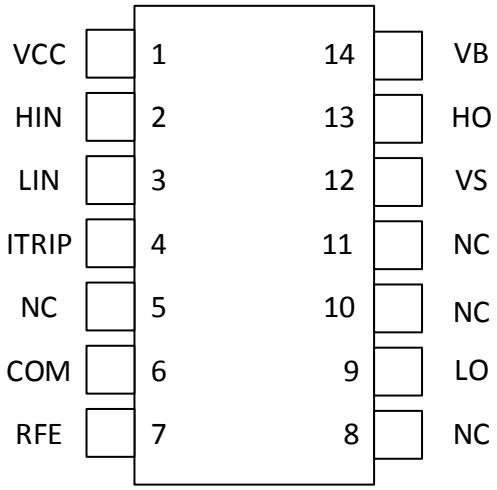
Functional Block Diagram



Lead Definitions

Pin	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	LIN	Logic input for low side gate driver output (LO), in phase
4	ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates RFE low. When ITRIP becomes inactive, RFE stays active low for an externally set time tFLTCLR, then automatically becomes inactive (open-drain high impedance).
5	NC	No connection
6	COM	Low side return
7	RFE	Integrated fault reporting function like over-current (ITRIP), or low-side undervoltage lockout and the fault clear timer. This pin has negative logic and an open-drain output. The use of over-current protection requires the use of external components.
8	NC	No connection
9	LO	Low side gate drive output
10	NC	No connection
11	NC	No connection
12	V_S	High side floating supply return
13	HO	High side gate drive output
14	V_B	High side floating supply

Lead Assignments



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Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Daisy Chain Multiple Devices
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Negative V_S Transient SOA
- PCB Layout Tips
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS2890D HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

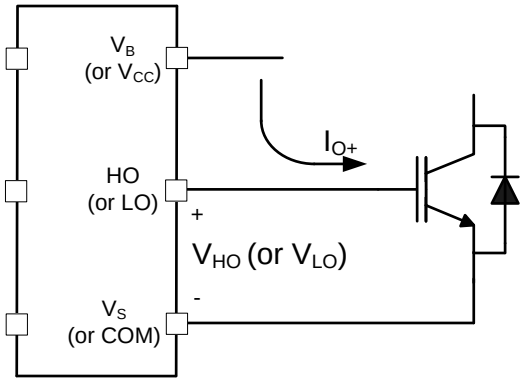


Figure 1: HVIC sourcing current

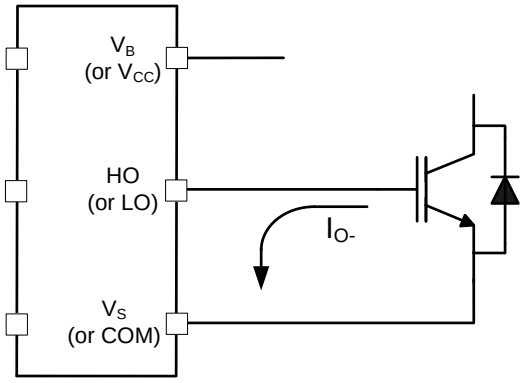


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationships between the input and output signals of the IRS2890D are illustrated below in Figures 3. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

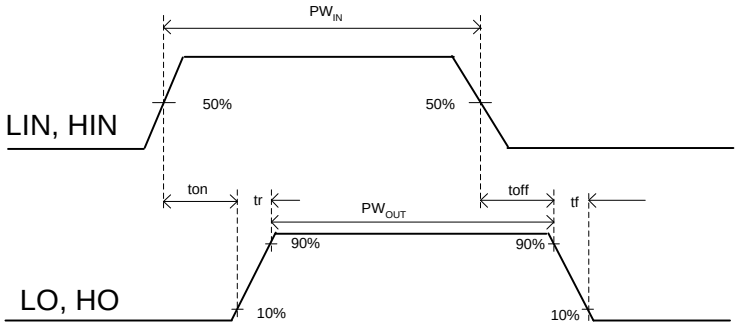


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the IRS2890D; this functionality is described in further detail later in this document.

During interval A of Figure 4, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 4 and 5 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold (see interval C in Figure 4); the charging characteristics are dictated by the RC network attached to the RFE pin.

During interval E of Figure 4 and 6, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high.

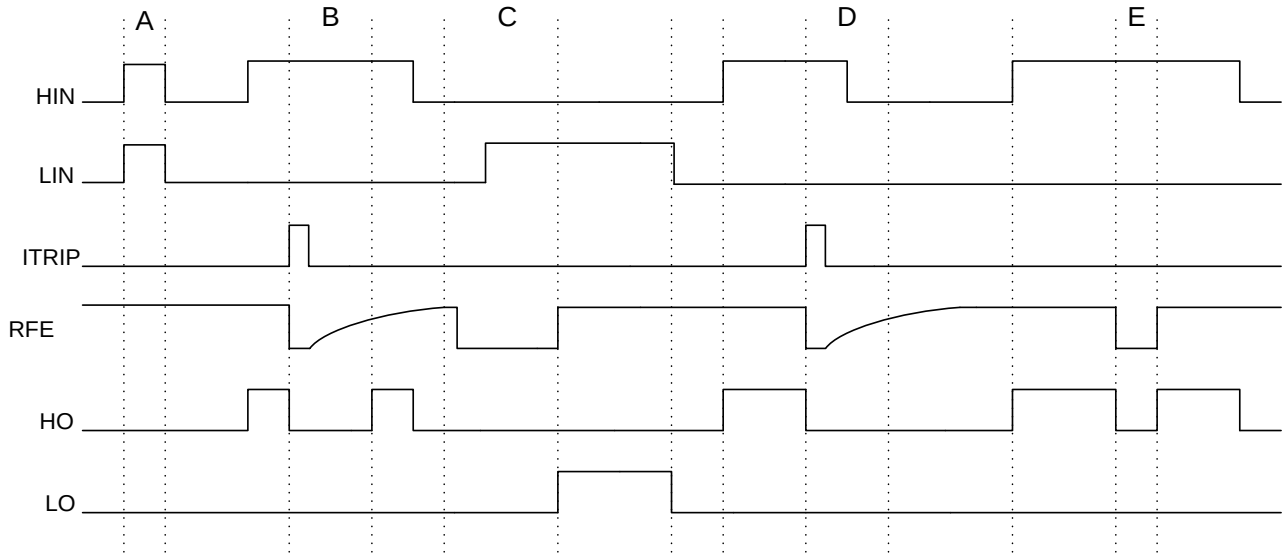


Figure 4: Input/output timing diagram

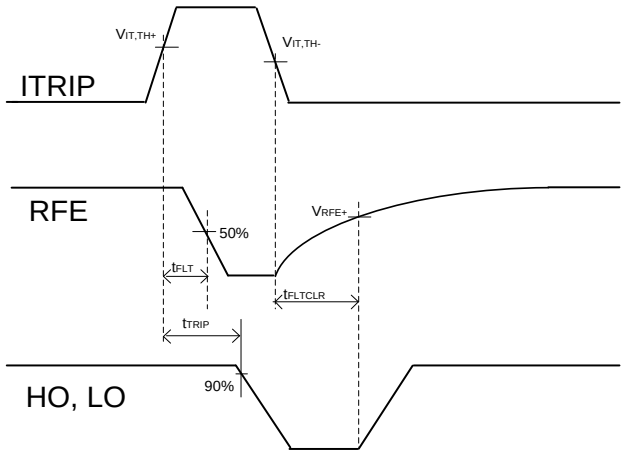


Figure 5: Detailed view of B interval

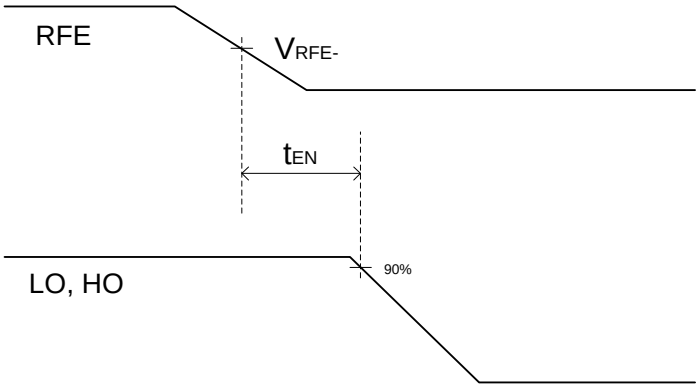


Figure 6: Detailed view of E interval

Deadtime

This HVIC features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver.

Matched Propagation Delays

The IRS2890D HVIC is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the IRS2890D is matched to the propagation turn-on delay (t_{OFF}).

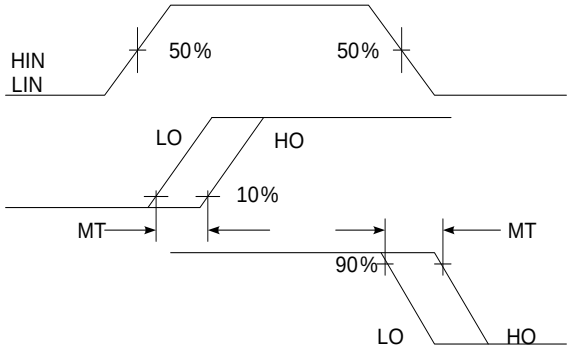


Figure 7: Delay Matching Waveform Definition

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS2890D has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the IRS2890D, its input threshold values, and the logic state of the IC as a result of the input signal.

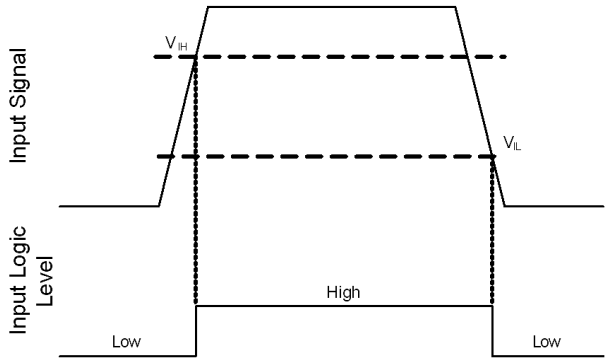


Figure 8: HIN & LIN input thresholds

Undervoltage Lockout Protection

This HVIC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 9 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this

could result in very high conduction losses within the power device and could lead to power device failure.

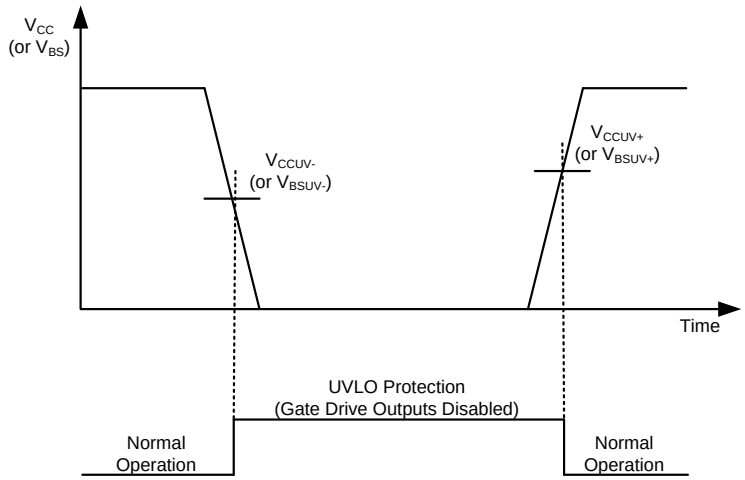


Figure 9: UVLO protection

Shoot-Through Protection

The IRS2890D is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table.

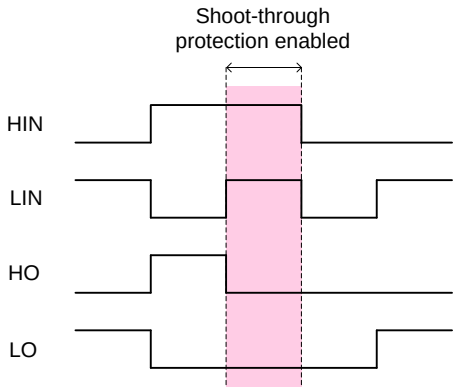


Figure 10: Illustration of shoot-through protection circuitry

IRS2890D			
HIN	**LIN**	**HO**	**LO**
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

Table 1: Input/output truth table for IRS2890D

Enable Input

The IRS2890D provides an enable functionality that allows it to shutdown or enable the HVIC. When the RFE pin is in the high state the HVIC is able to operate normally (assuming no other under voltage fault conditions on Vcc). When the RFE pin is in a low state, the gate drive outputs are pulled low until the enable condition is restored. The enable circuitry of the IRS2890D features an input filter; the minimum input duration is specified by $t_{FIL,EN}$. Please refer to the RFE pin parameters V_{RFE+}, V_{RFE-}, and I_{RFE} for the details of its use. Table 2 gives a summary of this pin's functionality.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table
(*assumes no undervoltage fault on Vcc)

Fault Reporting and Programmable Fault Clear Timer

The IRS2890D provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the RFE pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the RFE pin is internally pulled to COM and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. Figure 11 shows that R_{RFE} is connected between the external supply (V_{DD}) and the RFE pin, while C_{RFE} is placed between the RFE and COM pins.

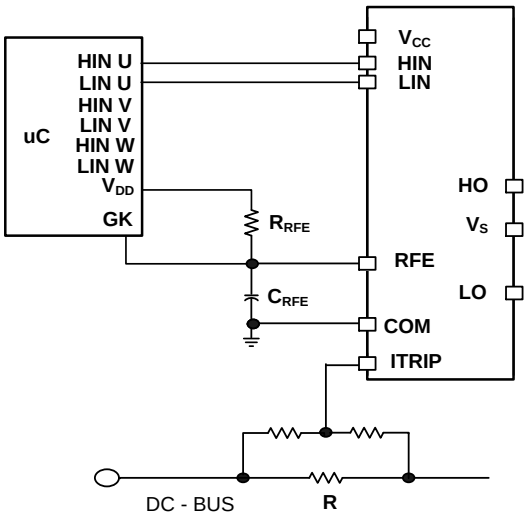


Figure 11 Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RFE}	≤1 nF
	Ceramic
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f*(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RFE}*C_{RFE})*\ln(1-V_{RFE+}/V_{DD}) + 100ns$$

The voltage on the RFE pin should not exceed the VDD of the uC power supply.

Over-Current Protection

The IRS2890D HVICs are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, and RFE is pulled to COM.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 12, and the ITRIP threshold (V_{ITRIP+}). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold (V_{ITRIP+}) at that current level.

$$V_{ITRIP+} = R_0*I_{DC-}(R_1/(R_1+R_2))$$

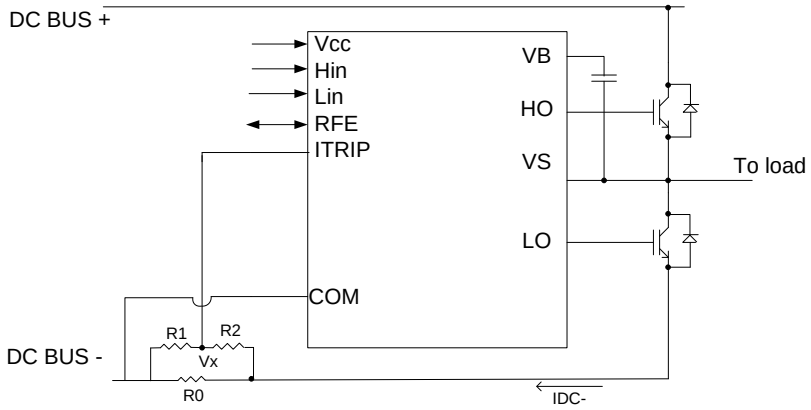


Figure 12 Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

Truth Table: Undervoltage lockout, ITRIP, and ENABLE

Table 4 provides the truth table for the IRS2890D. The first line shows that the UVLO for V_{CC} has been tripped; the RFE output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns the driver is functional.

The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time. The last case shows when the HVIC has received an enable command through the RFE input to shutdown; as a result, the gate drive outputs have been disabled.

	VCC	VBS	ITRIP	RFE	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	—	—	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	HIGH	LIN	0
Normal operation	15 V	15 V	0 V	HIGH	LIN	HIN
ITRIP fault	15 V	15 V	$>V_{ITRIP+}$	0	0	0
Enable command	15 V	15 V	0 V	0	0	0

Table 4: IRS2890D UVLO, ITRIP, FLT/EN/RCIN

Daisy Chain Multiple Devices

The IRS2890D can be daisy chained together for applications which require more than one device, such as in the three phase circuit shown below. In Figure 13, the three IRS2890D RFE pins are connected together. The ITRIP sensing is only used on the first HVIC; the other two ITRIP pins are disabled by tying them to COM. The programmable fault clear timing components, RRFE and CRFE, are populated only once for the RFE pin. When a fault occurs, either from ITRIP or UVLO, or an external command, all three HVICs are disabled simultaneously via the daisy chained RFE pin being pulled low to COM.

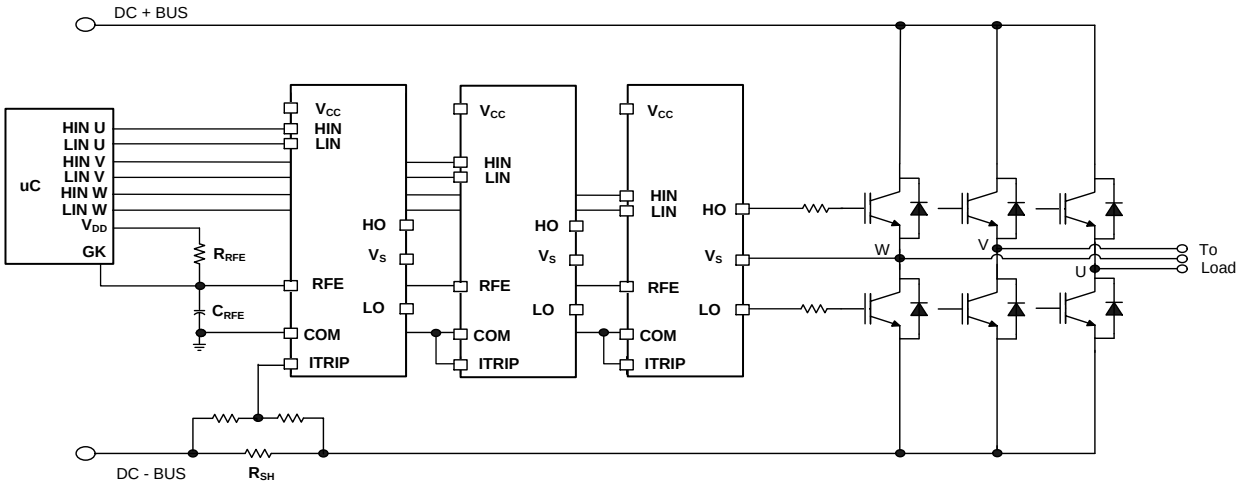


Figure 13: Daisy Chain Circuit with Single Shunt

In Figure 14 we want to be able to measure two of the individual leg currents. The RFE pins are connected together with the components for the pin only populated for the first HVIC. Two of the ITRIP pins are used, one for each leg, with the third ITRIP tied to COM. A fault can occur by the ITRIP sensing network for either of the two legs, shutting down all three IRS2890D HVICs simultaneously.

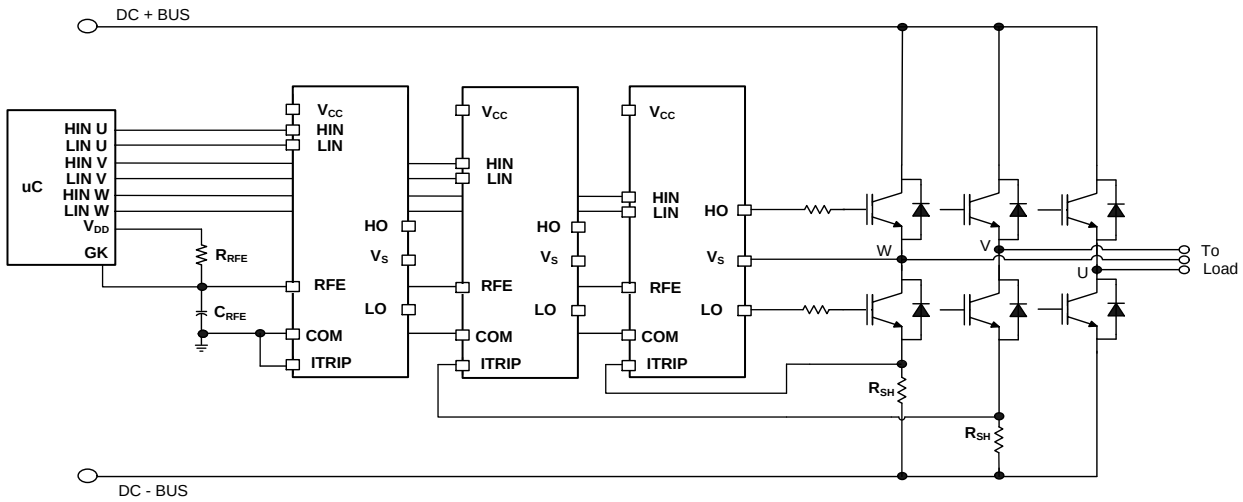


Figure 14: Daisy Chain circuit with Multiple Shunt

Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN ans LIN inputs. The working principle of the new filter is shown in Figures 15 and 16.

Figure 15 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 16 shows the advanced input filter of the IRS2890D and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

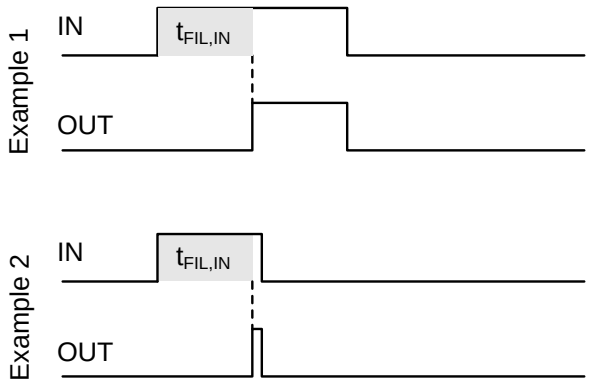


Figure 15: Typical input filter

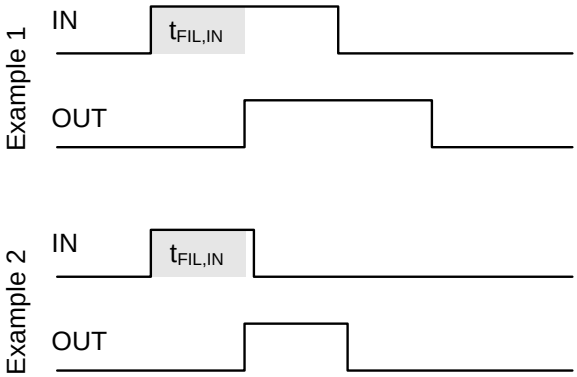


Figure 16: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 17 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 17 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

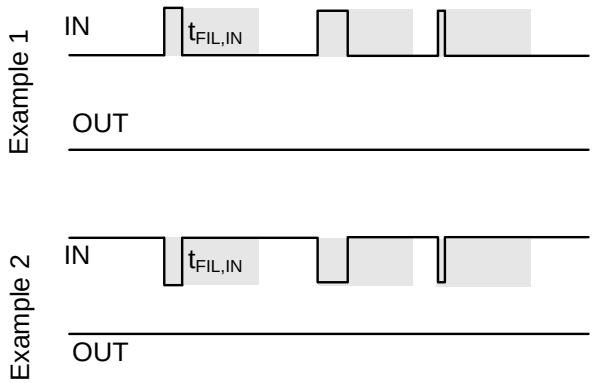


Figure 17: Noise rejecting input filters

Figures 18 and 19 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 18; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the right shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 18 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PW_{IN} duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PW_{IN} duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PW_{OUT} and PW_{IN} signals of both the narrow ON and narrow OFF cases is shown in Figure 19; the careful reader will note the scale of the y-axis. The x-axis of Figure 19 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

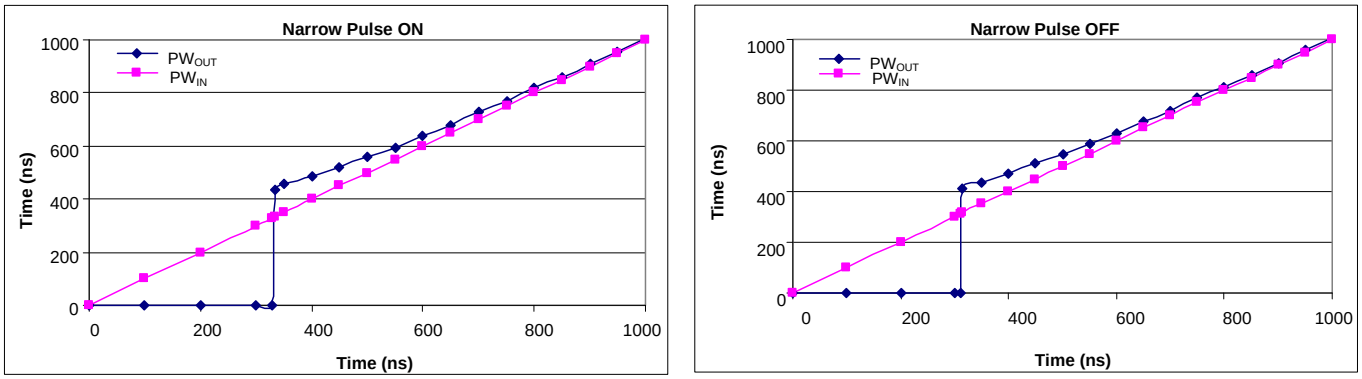


Figure 18: Input filter characteristic

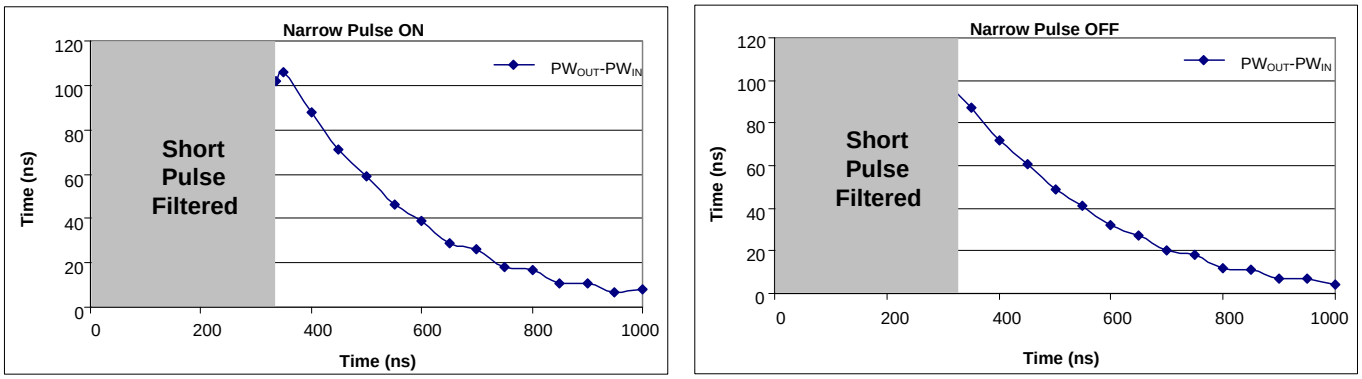


Figure 19: Difference between the input pulse and the output pulse

Integrated Bootstrap Functionality

The IRS2890D embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.

A bootstrap FET is connected between the floating supply V_B and V_{CC} (see Fig. 20).

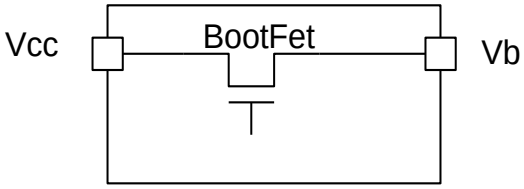


Figure 20: Simplified BootFET connection

The bootstrap FET is suitable for most PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode+ resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations at very high PWM duty cycle due to bootstrap FET equivalent resistance (R_{BS}, see page 3).

The integrated bootstrap FET is turned on during the time when LO is 'high', and it has a limited source current due to R_{BS}. The VBS voltage will be charged each cycle depending on the on-time of LO and the value of the CBS capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap FET follows the state of low-side output stage (i.e., the bootstrap FET is ON when LO is high, unless the VB voltage is higher than approximately VCC. In that case, the bootstrap FET is designed to remain off until VB returns below that threshold; this concept is illustrated in Figure 21.

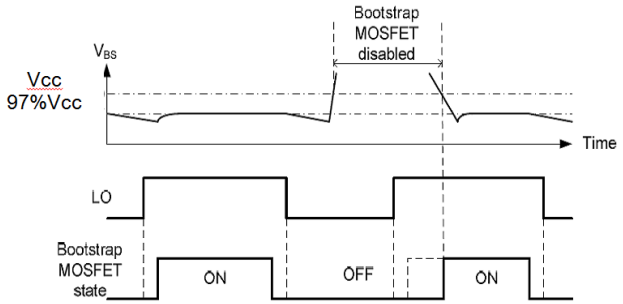


Figure 21: BootFET timing diagram

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical three phase inverter circuit is shown in Figure 22; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 23 and 24) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

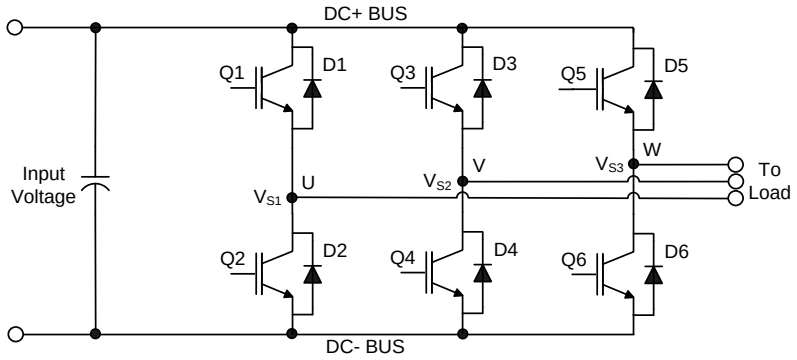


Figure 22: Three phase inverter

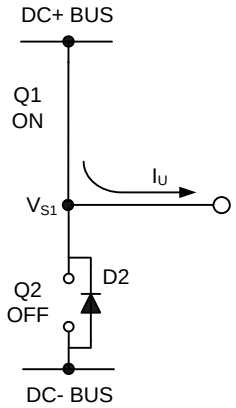


Figure 23: Q1 conducting

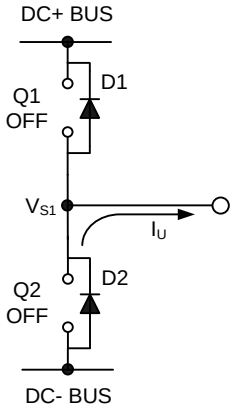


Figure 24: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 25 and 26), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

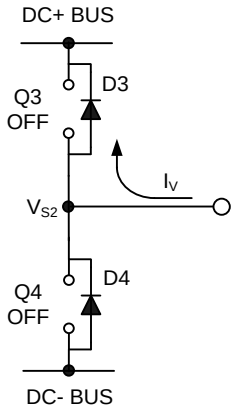


Figure 25: D3 conducting

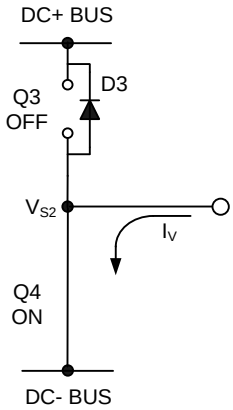


Figure 26: Q4 conducting

However, in a real inverter circuit the V_S voltage swing does not stop at the level of the negative DC bus but instead swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”.

The circuit shown in Figure 27 depicts one leg of the three phase inverter; Figures 28 and 29 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

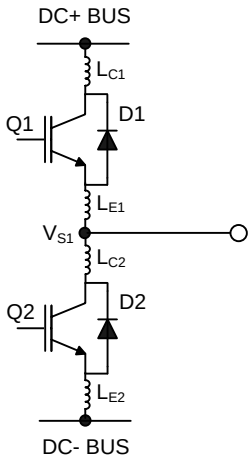


Figure 27: Parasitic Elements

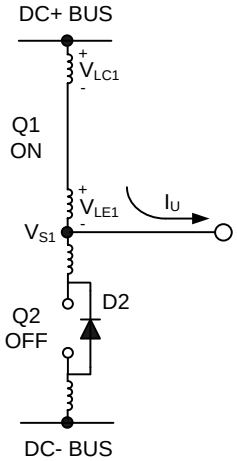


Figure 28: V_S positive

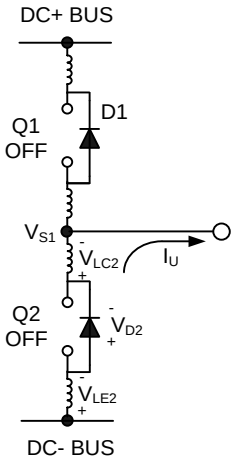


Figure 29: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon’s HVICs have been designed for the robustness required in many of today’s demanding applications. An

indication of the IRS2890D's robustness can be seen in Figure 30, where the IRS2890D Safe Operating Area is shown at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

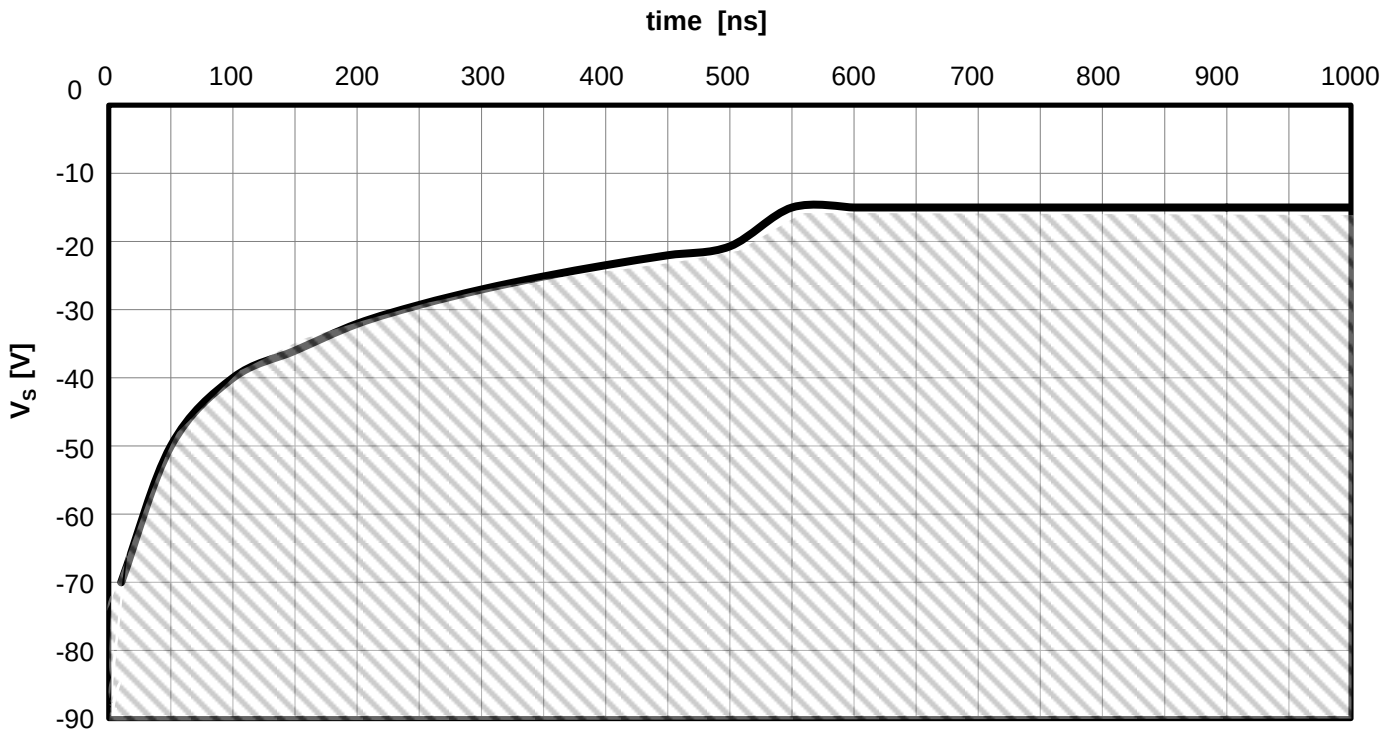


Figure 30: Negative V_S transient SOA for IRS2890D @ VBS=15 V

Even though the IRS2890D has been shown to be able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

- Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.
- Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.
- Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 31). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

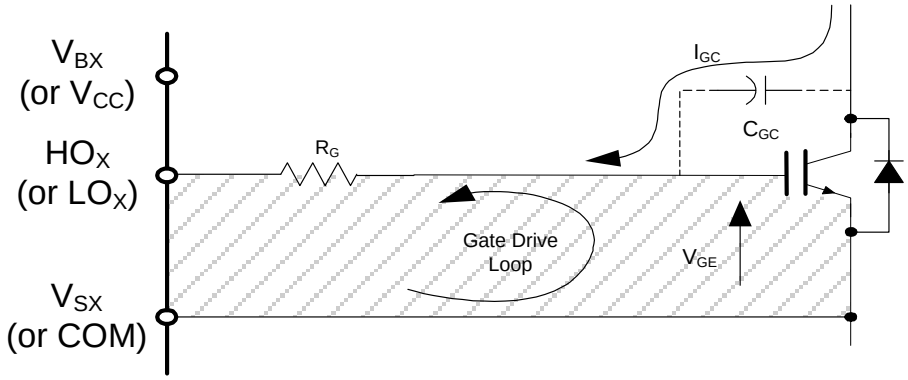


Figure 31: Antenna Loops

- Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.
- Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 32), and in some cases using a clamping diode between COM and V_S (see Figure 33). See DT04-4 at www.infineon.com for more detailed information.

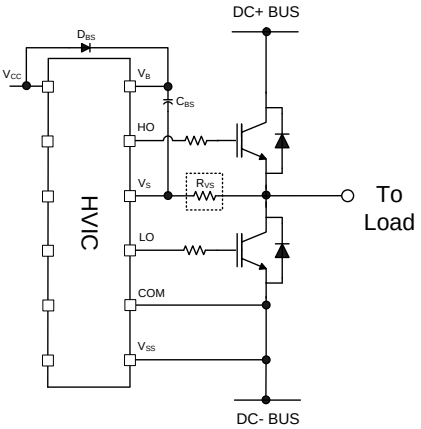


Figure 32: V_S resistor

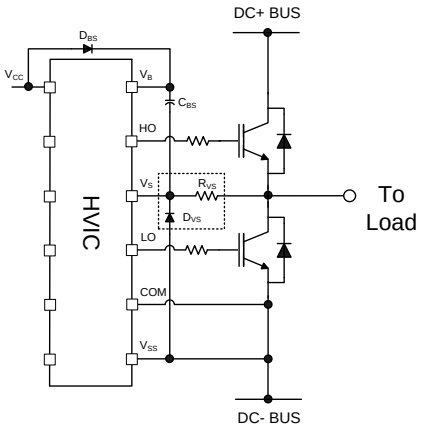


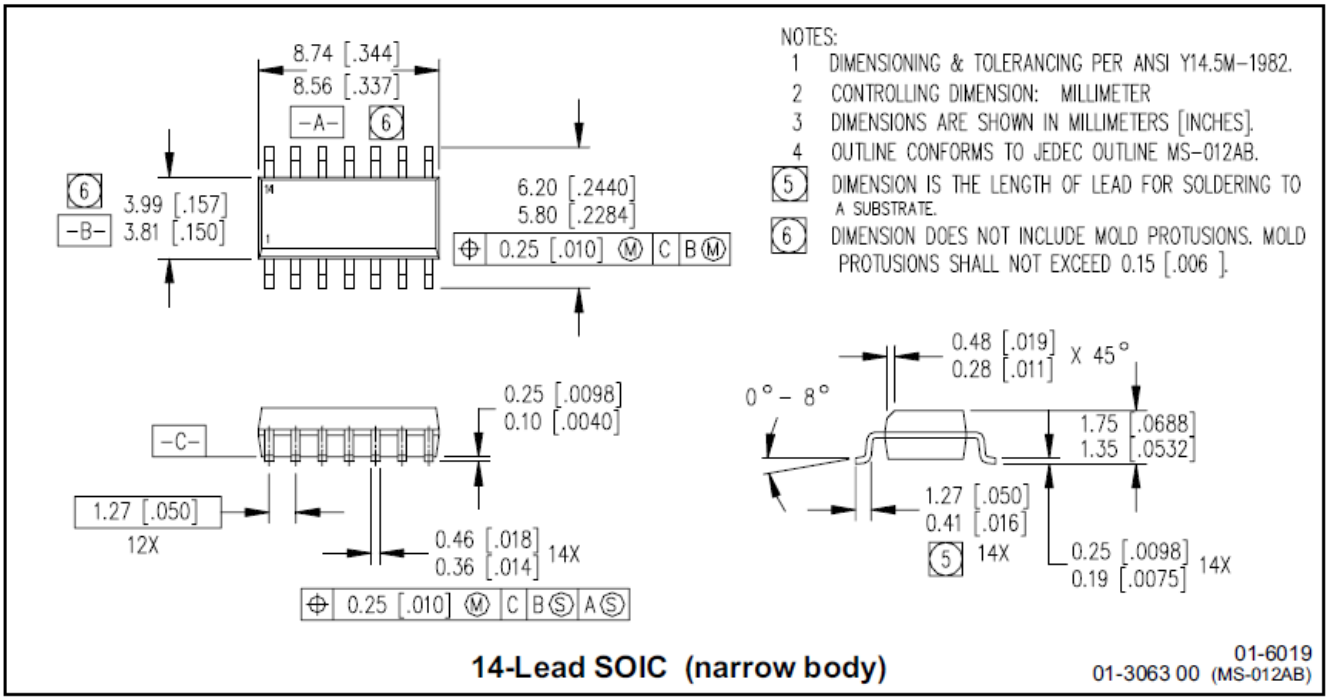
Figure 33: V_S clamping diode

Additional Documentation

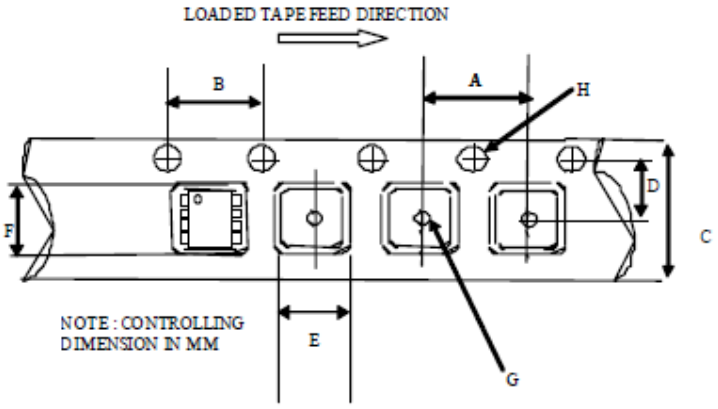
Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Package Details: 14-Lead SOIC

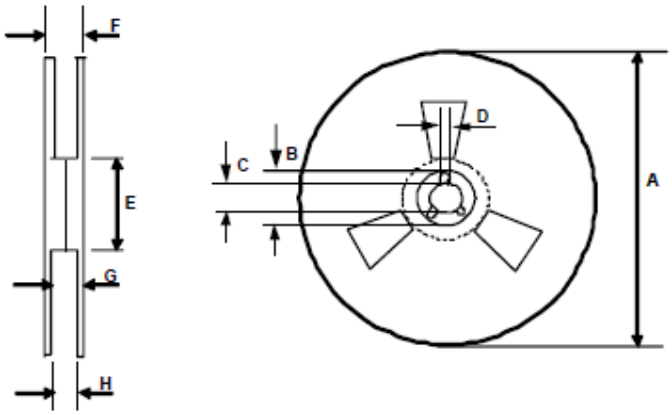


Tape and Reel Details: 14-Lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

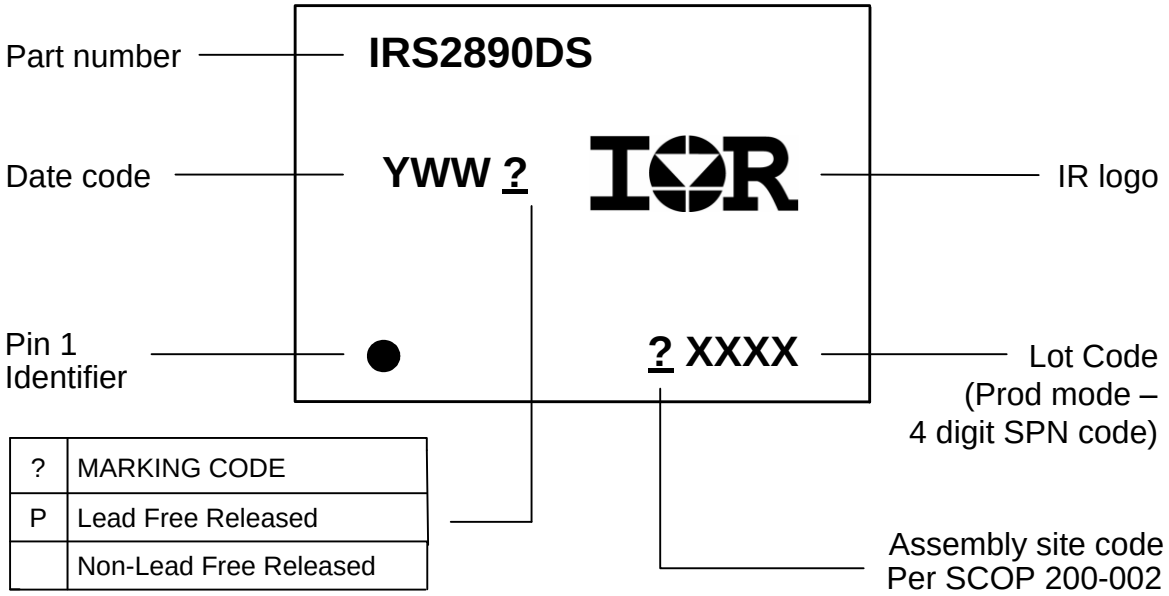
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B 3	.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

14-Lead SOIC8
IRS2890DSPBF

Qualification Information

Qualification Level		Industrial†	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		14 Lead SOIC	MSL2††, 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1C (per JEDEC standard JESD22-A114)	
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
	Charged Device Model	C3 (per JEDEC standard JS-002-2014)	
IC Latch-Up Test		Class II, Level A (per JESD78)	
RoHS Compliant		Yes	

† Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

†† Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

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