## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

#### 2. Features and benefits

- Fully automotive qualified to AEC-Q101:
  - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
  - Reduced cell pitch enables enhanced power density and efficiency with lower  $R_{\mbox{\scriptsize DSon}}$  in same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight V<sub>GS(th)</sub> limits enable easy paralleling of MOSFETs
- · LFPAK Gull Wing leads:
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - · Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
  - Improved reliability, with reduced R<sub>th</sub> and R<sub>DSon</sub>
  - · Increases maximum current capability and improved current spreading

# 3. Applications

- 12 V automotive systems
- · Motors, lamps and solenoid control
- · Start-Stop micro-hybrid applications
- · Transmission control
- Ultra high performance power switching



## 4. Quick reference data

#### Table 1. Quick reference data

	CK reference data	0		-		11.04
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	-	190	W
Static chara	acteristics			'	•	
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10	1.5	2.13	2.5	mΩ
Dynamic ch	aracteristics			'		
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <u>Fig. 12</u> ; <u>Fig. 13</u>	-	8.9	22	nC
Source-drai	in diode			<u>'</u>		
Q <sub>r</sub>	recovered charge	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C	-	22.7	-	nC
S	softness factor	$I_S$ = 25 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 16	-	0.79	-	

# 5. Pinning information

### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	a	G (F)
4	G	gate		mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package						
	Name	Description	Version				
BUK7Y2R5-40H	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669				

# 7. Marking

### Table 4. Marking codes

Type number	Marking code
BUK7Y2R5-40H	72H540

# 8. Limiting values

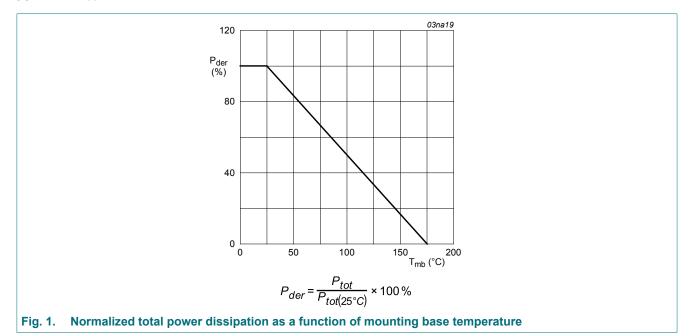
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	190	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C		-	120	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 2		-	600	Α
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	n diode					
Is	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	600	Α
Avalanche r	uggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 120 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[2] [3]	-	82.1	mJ

<sup>[1] 120</sup>A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175  $^{\circ}$ C.
- [3] Refer to application note AN10273 for further information.



### N-channel 40 V, 2.5 m $\Omega$ standard level MOSFET in LFPAK56

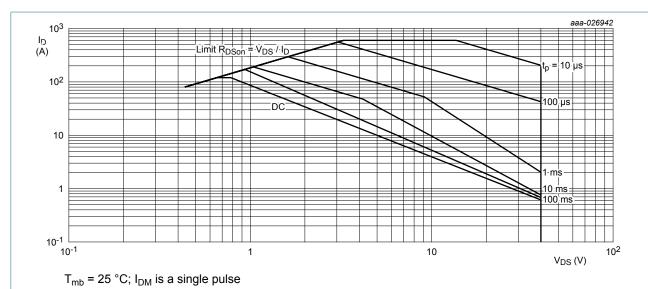
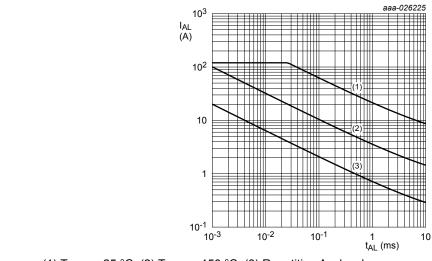


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



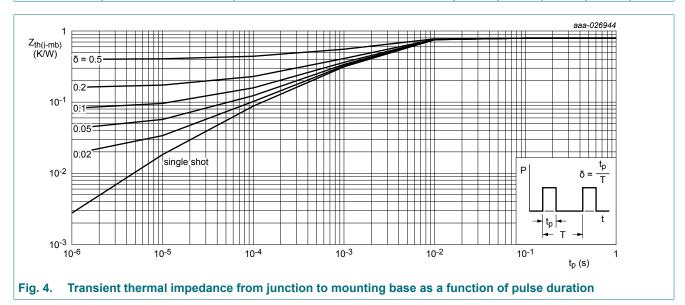
(1)  $T_{j \text{ (init)}}$  = 25 °C; (2)  $T_{j \text{ (init)}}$  = 150 °C; (3) Repetitive Avalanche

Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 4	-	0.63	0.79	K/W



## 10. Characteristics

#### Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	43	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -40 °C	-	40.7	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <u>Fig. 8</u> ; <u>Fig. 9</u>	2.4	3	3.6	V
		$I_D = 1 \text{ mA; } V_{DS} = V_{GS}; T_j = -55 \text{ °C; } Fig. 8$	-	-	4.3	V
		$I_D = 1 \text{ mA; } V_{DS} = V_{GS}; T_j = 175 \text{ °C; } Fig. 8$	1	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 16 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	1.2	10	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	113	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
	V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA	
R <sub>DSon</sub> drain-source on-state resistance		$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10	1.5	2.13	2.5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 105 °C; Fig. 11	2.12	2.82	3.98	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 125 °C; Fig. 11	2.34	3.18	4.38	mΩ
	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11	2.94	4.07	5.45	mΩ	
$R_G$	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.3	0.74	1.85	Ω
Dynamic ch	naracteristics		,			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V;	-	45.8	79	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 12</u> ; <u>Fig. 13</u>	-	12.7	19	nC
Q <sub>GD</sub>	gate-drain charge	1	-	8.9	22	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	3193	4790	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 14</u>	-	831	1163	pF
C <sub>rss</sub>	reverse transfer capacitance		-	150	330	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V;	-	12.3	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	10.3	-	ns
t <sub>d(off)</sub>	turn-off delay time	1	-	27.5	-	ns
t <sub>f</sub>	fall time	1	-	13	-	ns
Source-dra	in diode	1			1	1
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 25 °C; <u>Fig. 15</u>	-	0.8	1.2	V
		,				

#### N-channel 40 V, 2.5 m $\Omega$ standard level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}$ ; $dI_S/dt = -100 \text{ A/µs}$ ; $V_{GS} = 0 \text{ V}$ ;	-	29.3	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	22.7	-	nC
S	softness factor	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	0.79	-	
		$I_S$ = 25 A; $dI_S/dt$ = -500 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 16	-	0.65	-	

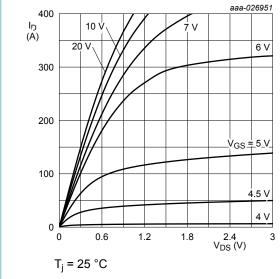


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

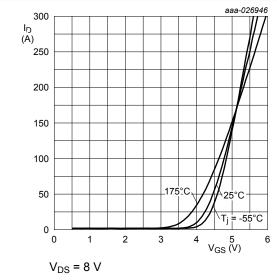


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

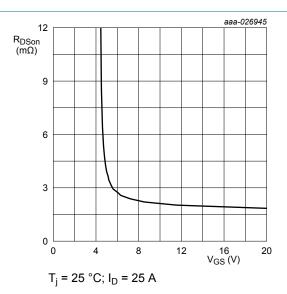
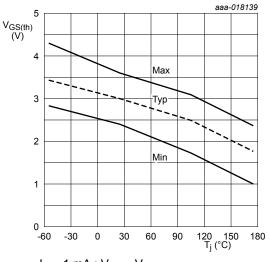


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS}$ 

Fig. 8. Gate-source threshold voltage as a function of junction temperature

### N-channel 40 V, 2.5 m $\Omega$ standard level MOSFET in LFPAK56

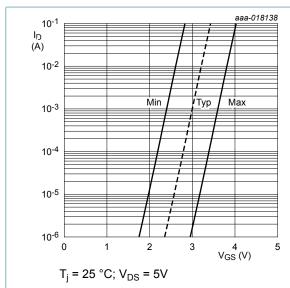


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

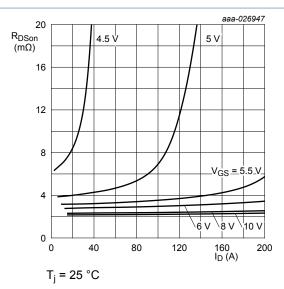


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

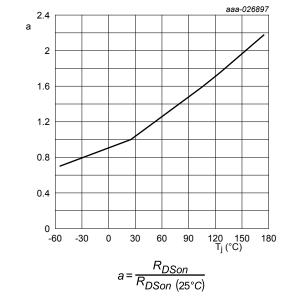


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

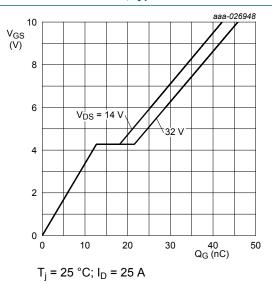


Fig. 12. Gate-source voltage as a function of gate charge; typical values

### N-channel 40 V, 2.5 m $\Omega$ standard level MOSFET in LFPAK56

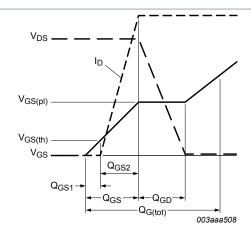
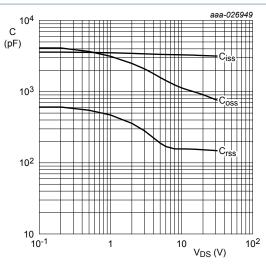


Fig. 13. Gate charge waveform definitions



 $V_{GS} = 0 V$ ; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

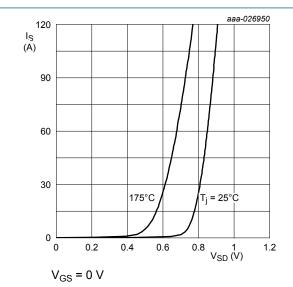
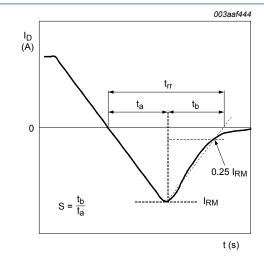


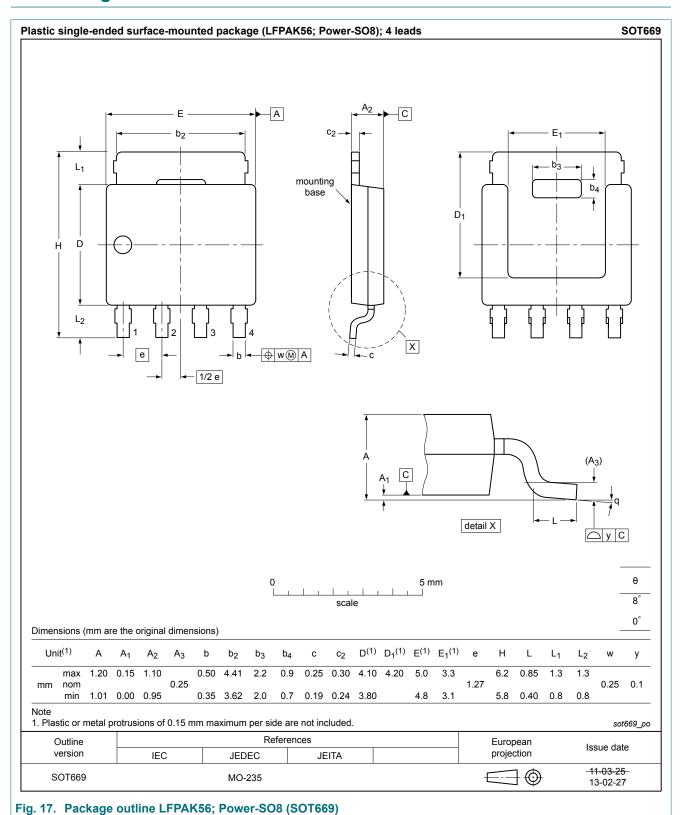
Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values



 $t_{rr} = t_a + t_b$ 

Fig. 16. Reverse recovery waveform definitions

# 11. Package outline



# 12. Legal information

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# **BUK7Y2R5-40H**

### N-channel 40 V, 2.5 m $\Omega$ standard level MOSFET in LFPAK56

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