

Low Voltage Detectors ($V_{DF} = 0.8V \sim 1.5V$)
 Standard Voltage Detectors ($V_{DF} = 1.6V \sim 6.0V$)

■ GENERAL DESCRIPTION

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies.

Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N-ch open drain output configurations are available.

■ APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

■ FEATURES

- Highly Accurate** : $\pm 2\%$
: $\pm 1\%$ (Standard Voltage VD: 2.6V~5.1V)
- Low Power Consumption** : $0.7 \mu A$ (TYP.) [$V_{IN} = 1.5V$]
- Detect Voltage Range** : $0.8V \sim 6.0V$ in $0.1V$ increments
- Operating Voltage Range** : $0.7V \sim 6.0V$ (Low Voltage)
 $0.7V \sim 10.0V$ (Standard Voltage)
- Detect Voltage Temperature Characteristics**
: $\pm 100ppm/^{\circ}C$ (TYP.)
- Output Configuration** : N-ch open drain or CMOS
- Packages** : SSOT-24
SOT-23
SOT-89
- Environmentally Friendly** : EU RoHS Compliant, Pb Free

■ TYPICAL APPLICATION CIRCUITS

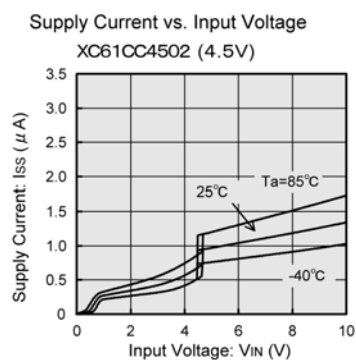


CMOS Output



N-ch Open Drain Output

■ TYPICAL PERFORMANCE CHARACTERISTICS



PIN CONFIGURATION



PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
SSOT-24	SOT-23	SOT-89		
2	3	2	V _{IN}	Supply Voltage Input
4	2	3	V _{SS}	Ground
1	1	1	V _{OUT}	Output
3	-	-	NC	No Connection

PRODUCT CLASSIFICATION

Ordering Information

XC61C①②③④⑤⑥⑦-⑧^(*)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	08 ~ 60	e.g.0.9V → ②0, ③9
			e.g.1.5V → ②1, ③5
④	Output Delay	0	No delay
⑤	Detect Accuracy	1	Within ±1% (V _{DF(T)} =2.6V~5.1V)
		2	Within ±2%
⑥⑦-⑧ ^(*)	Packages (Order Unit)	NR	SSOT-24 (3,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)
		MR	SOT-23 (3,000pcs/Reel)
		MR-G	SOT-23 (3,000pcs/Reel)
		PR	SOT-89 (1,000pcs/Reel)
		PR-G	SOT-89 (1,000pcs/Reel)

^(*) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■ BLOCK DIAGRAMS

(1) CMOS Output



(2) N-ch Open Drain Output



■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage	*1	V _{IN}	V _{SS} -0.3 ~ 9.0	V
	*2		V _{SS} -0.3 ~ 12.0	
Output Current		I _{OUT}	50	mA
Output Voltage	CMOS	V _{OUT}	V _{SS} -0.3 ~ V _{IN} +0.3	V
	N-ch Open Drain Output *1		V _{SS} -0.3 ~ 9.0	
	N-ch Open Drain Output *2		V _{SS} -0.3 ~ 12.0	
Power Dissipation	SSOT-24	P _d	150	mW
	SOT-23		150	
	SOT-89		500	
Operating Ambient Temperature		T _{opr}	-40 ~ +85	°C
Storage Temperature		T _{stg}	-55 ~ +125	°C

*1: Low voltage: V_{DF(T)}=0.8V~1.5V

*2: Standard voltage: V_{DF(T)}=1.6V~6.0V

ELECTRICAL CHARACTERISTICS

$V_{DF(T)} = 0.8V \text{ to } 6.0V \pm 2\%$

$V_{DF(T)} = 2.6V \text{ to } 5.1V \pm 1\%$

$T_a = 25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS	
Detect Voltage	V_{DF}	$V_{DF(T)} = 0.8V \sim 1.5V$ *1 $V_{DF(T)} = 1.6V \sim 6.0V$ *2	$V_{DF(T)}$ $\times 0.98$	$V_{DF(T)}$	$V_{DF(T)}$ $\times 1.02$	V	1	
		$V_{DF(T)} = 2.6V \sim 5.1V$ *2	$V_{DF(T)}$ $\times 0.99$	$V_{DF(T)}$	$V_{DF(T)}$ $\times 1.01$	V	1	
Hysteresis Range	V_{HYS}		V_{DF} $\times 0.02$	V_{DF} $\times 0.05$	V_{DF} $\times 0.08$	V	1	
Supply Current	I_{SS}	$V_{IN} = 1.5V$	-	0.7	2.3	μA	2	
		$V_{IN} = 2.0V$	-	0.8	2.7			
		$V_{IN} = 3.0V$	-	0.9	3.0			
		$V_{IN} = 4.0V$	-	1.0	3.2			
		$V_{IN} = 5.0V$	-	1.1	3.6			
Operating Voltage *1	V_{IN}	$V_{DF(T)} = 0.8V \text{ to } 1.5V$	0.7	-	6.0	V	1	
Operating Voltage *2		$V_{DF(T)} = 1.6V \text{ to } 6.0V$	0.7	-	10.0			
Output Current *1	I_{OUT}	N-ch $V_{DS} = 0.5V$	$V_{IN} = 0.7V$	0.10	0.80	-	mA	3
			$V_{IN} = 1.0V$	0.85	2.70	-		
CMOS, P-ch $V_{DS} = 2.1V$		$V_{IN} = 6.0V$	-	-7.5	-1.5	3		
		$V_{IN} = 1.0V$	1.0	2.2	-			
Output Current *2		N-ch $V_{DS} = 0.5V$	$V_{IN} = 2.0V$	3.0	7.7	-		
			$V_{IN} = 3.0V$	5.0	10.1	-		
	$V_{IN} = 4.0V$		6.0	11.5	-			
	$V_{IN} = 5.0V$		7.0	13.0	-			
CMOS, P-ch $V_{DS} = 2.1V$	$V_{IN} = 8.0V$	-	-10.0	-2.0	4			
Leakage Current	CMOS Output (Pch)	I_{LEAK}	$V_{IN} = V_{DF} \times 0.9, V_{OUT} = 0V$	-	-10	-	nA	3
	N-ch Open Drain		$V_{IN} = 6.0V, V_{OUT} = 6.0V$ *1 $V_{IN} = 10.0V, V_{OUT} = 10.0V$ *2	-	10	100		
Temperature Characteristics	$\Delta V_{DF} / (\Delta T_{opr} \cdot V_{DF})$	$-40^\circ\text{C} \leq T_{opr} \leq 85^\circ\text{C}$	-	± 100	-	ppm/ $^\circ\text{C}$	1	
Delay Time (VDR \rightarrow VOUT inversion)	t_{DLY}	Inverts from VDR to VOUT	-	0.03	0.20	ms	5	

NOTE:

*1: Low Voltage: $V_{DF(T)} = 0.8V \sim 1.5V$

*2: Standard Voltage: $V_{DF(T)} = 1.6V \sim 6.0V$

$V_{DF(T)}$: Nominal detect voltage

Release Voltage: $V_{DR} = V_{DF} + V_{HYS}$

OPERATIONAL EXPLANATION

(Especially prepared for CMOS output products)

- ① When input voltage (V_{IN}) is higher than detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.
- ③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. (As for the N-ch open drain product of XC61CN, the pull-up voltage goes out at the output voltage.)
- ④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.
- ⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN} .
(A condition of high impedance exists with N-ch open drain output configurations.)
- ⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

Timing Chart



NOTES ON USE

1. Please use this IC within the stated absolute maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. When a resistor is connected between the V_{IN} pin and the power supply with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the V_{IN} pin and the power supply with CMOS output configurations, irrespective of N-ch open-drain output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to the Oscillation Description (2) below)
4. Please use N-ch open drain output configuration, when a resistor R_{IN} is connected between the V_{IN} pin and power source. In such cases, please ensure that R_{IN} is less than $10k\Omega$ and that C is more than $0.1\mu F$, please test with the actual device. (refer to the Oscillation Description (1) below)
5. With a resistor R_{IN} connected between the V_{IN} pin and the power supply, the V_{IN} pin voltage will be getting lower than the power supply voltage as a result of the IC's supply current flowing through the V_{IN} pin.
6. In order to stabilize the IC's operations, please ensure that V_{IN} pin input frequency's rise and fall times are more than $2\mu s/V$.
7. Torex places an importance on improving our products and its reliability.
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.



Figure 1: Circuit using an input resistor

Oscillation Description

(1) Load current oscillation with the CMOS output configuration

When the voltage applied at power supply, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow at R_L . Because a voltage drop ($R_{IN} \times I_{OUT}$) is produced at the R_{IN} resistor, located between the power supply and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again. Oscillation may occur with this " release - detect - release " repetition. Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to Figure 3)
Since hysteresis exists during detect operations, oscillation is unlikely to occur.



Figure 2: Oscillation in relation to output current



Figure 3: Oscillation in relation to through current

■ TEST CIRCUITS

Circuit 1



Circuit 2



Circuit 3



Circuit 4



Circuit 5



* : A resistor is not necessary with CMOS output products.

TYPICAL PERFORMANCE CHARACTERISTICS

Low Voltage

(1) Supply Current vs. Input Voltage



(2) Detect, Release Voltage vs. Ambient Temperature



(3) Output Voltage vs. Input Voltage



Note : Unless otherwise stated, the N-ch open drain pull-up resistance value is 100kΩ.

■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Low Voltage (Continued)

(4) N-ch Driver Output Current vs. V_{DS}



(5) N-ch Driver Output Current vs. Input Voltage



(6) P-ch Driver Output Current vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Standard Voltage

(1) Supply Current vs. Input Voltage



(2) Detect, Release Voltage vs. Ambient Temperature



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Standard Voltage (Continued)

(3) Output Voltage vs. Input Voltage



Note : The N-ch open drain pull up resistance value is 100kΩ.

(4) N-ch Driver Output Current vs. Vds



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Standard Voltage (Continued)

(4) N-ch Driver Output Current vs. V_{DS}



(5) N-ch Driver Output Current vs. Input Voltage



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

● Standard Voltage (Continued)

(6) P-ch Driver Output Current vs. Input Voltage



PACKAGING INFORMATION

●SSOT-24



●SOT-23



●SOT-89



MARKING RULE

- SSOT-24, SOT-23, SOT-89



- ① represents integer of detect voltage and CMOS Output (XC61CC series)

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.X
B	CMOS	1.X
C	CMOS	2.X
D	CMOS	3.X
E	CMOS	4.X
F	CMOS	5.X
H	CMOS	6.X

- N-Channel Open Drain Output (XC61CN series)

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.X
L	N-ch	1.X
M	N-ch	2.X
N	N-ch	3.X
P	N-ch	4.X
R	N-ch	5.X
S	N-ch	6.X

- ② represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	X.0	5	X.5
1	X.1	6	X.6
2	X.2	7	X.7
3	X.3	8	X.8
4	X.4	9	X.9

- ③ represents delay time
(Except for SSOT-24)

MARK	DELAY TIME	PRODUCT SERIES
3	No Delay Time	XC61Cxxx0xxx

- ④ represents production lot number

Based on the internal standard. (G, I, J, O, Q, W excluded)

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