74AHC1G4210

**10-stage divider and oscillator** Rev. 4 — 27 June 2019

### 1. General description

74AHC1G4210 is a 10-stage divider and oscillator. It consists of a chain of 10 flip-flops. Each flipflop divides the frequency of the previous flip-flop by two, consequently the 74AHC1G4210 counts up to  $2^{10} = 1024$ . The single inverting stage (X1 to X2) functions as a crystal oscillator or an input buffer for an external oscillator. When used as a buffer the output X2 should be left floating. The frequency of the output (Q) is the frequency applied to X1 divided by 1024. The divider advances on the negative-going transition of X1.

The X1 input is overvoltage tolerant. This feature allows the use of this device as a voltage level translator in mixed voltage environments.

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ESD protection:
  - HBM JESD22-A114F: exceeds 2000 V
  - CDM JESD22-C101E: exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

#### Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74AHC1G4210GW	-40 °C to +125 °C		plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1				

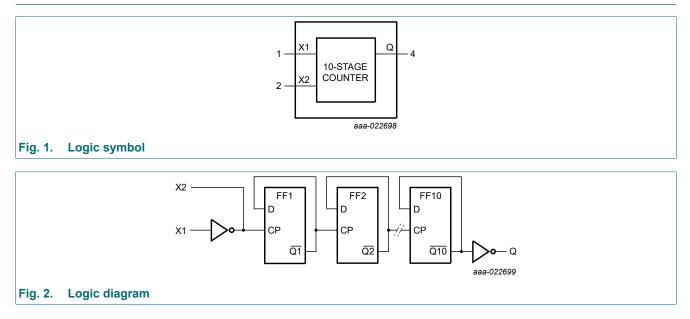
### 4. Marking

Table 2. Marking codes	
Type number	Marking[1]
74AHC1G4210GW	C1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

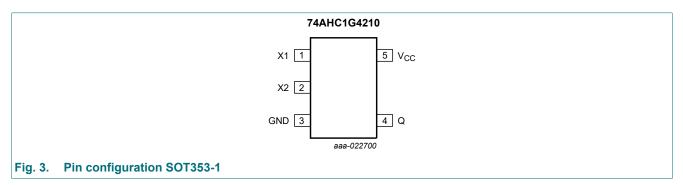
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# 5. Functional diagram



# 6. Pinning information

### 6.1. Pinning



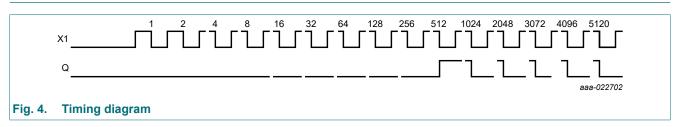
### 6.2. Pin description

#### Table 3. Pin description

Symbol	Pin	Description
X1	1	clock input/oscillator pin
X2	2	oscillator pin
GND	3	ground (0 V)
Q	4	divider output
V <sub>CC</sub>	5	supply voltage

74AHC1G4210

# 7. Functional description



# 8. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V		-20	-	mA
I <sub>OK</sub>	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I <sub>O</sub>	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$		-	±25	mA
I <sub>CC</sub>	supply current			-	75	mA
I <sub>GND</sub>	ground current			-75	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: above 74 °C the value of Ptot derates linearly with 3.3 mW/K.

# 9. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	ns/V
	rate	V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	ns/V

# **10. Static characteristics**

#### **Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Мах	1
VIH	HIGH-level	X1								
	input voltage	V <sub>CC</sub> = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
	V <sub>CC</sub> = 3.0 V	2.4	-	-	2.4	-	2.4	-	V	
		V <sub>CC</sub> = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V <sub>IL</sub>	LOW-level	X1								
	input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V <sub>CC</sub> = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V <sub>CC</sub> = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V <sub>OH</sub>	HIGH-level	Q; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
		X2; $V_I = V_{IH}$ or $V_{IL}$								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μΑ; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -2.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -3.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level	Q; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
		X2; $V_I = V_{IH}$ or $V_{IL}$								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 3.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
lı	input leakage current	X1; V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	μA
CI	input capacitance	X1	-	3	8	-	8	-	8	pF

# 11. Dynamic characteristics

#### Table 7. Dynamic characteristics

GND = 0 V;  $t_r = t_f = \le 3.0 \text{ ns.}$  For test circuit see Fig. 7. For waveforms see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
				Min	Тур	Мах	Min	Мах	Min	Мах	1
t <sub>pd</sub>	propagation	X1 to X2	[1]								
	delay	V <sub>CC</sub> = 3.0 V to 3.6 V	[2]								
		C <sub>L</sub> = 15 pF		-	3	7	1	11	1	13	ns
		C <sub>L</sub> = 50 pF		-	7	13	1	16	1	18	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	[3]								
		C <sub>L</sub> = 15 pF		-	2	5	1	7	1	9	ns
		C <sub>L</sub> = 50 pF		-	6	10	1	11	1	12	ns
		X1 to Q	[1]								
		V <sub>CC</sub> = 3.0 V to 3.6 V	[2]								
		C <sub>L</sub> = 15 pF		-	24	41	1	50	1	59	ns
		C <sub>L</sub> = 50 pF		-	26	45	1	53	1	63	ns
		$V_{CC}$ = 4.5 V to 5.5 V	[3]								
		C <sub>L</sub> = 15 pF		-	17	27	1	33	1	39	ns
		C <sub>L</sub> = 50 pF		-	19	30	1	38	1	44	ns
t <sub>W</sub>	pulse width	X1 HIGH or LOW									
		V <sub>CC</sub> = 3.0 V to 3.6 V		4	-	-	5	-	7	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		3	-	-	4	-	5	-	ns
f <sub>max</sub>	maximum	X1									
	frequency	V <sub>CC</sub> = 3.3 V		125	-	-	100	-	70	-	MHz
		V <sub>CC</sub> = 5 V		165	-	-	125	-	100	-	MHz
C <sub>PD</sub>	power dissipation	$C_L$ = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	[4]								
	capacitance	V <sub>CC</sub> = 3.3 V		-	4	-	-	-	-	-	pF
		V <sub>CC</sub> = 5 V		-	5	-	-	-	-	-	pF

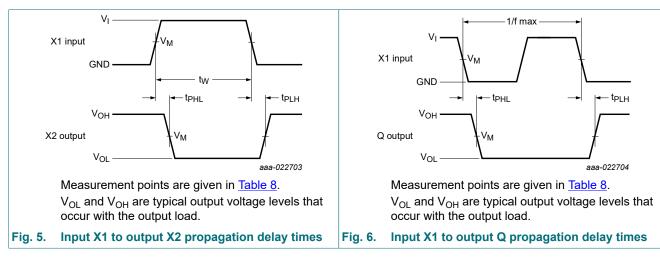
[1]

 $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}.$  Typical values are measured at V\_{CC} = 3.3 V. Typical values are measured at V\_{CC} = 5.0 V. [2]

[3]

 $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  (µW).  $P_D = C_{PD} x V_{CC}^2 x f_i + C_L x V_{CC}^2 x f_i/1024$  where: [4]

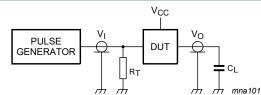
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  $V_{CC}$  = supply voltage in Volt.



### 11.1. Waveforms and test circuit

 Table 8. Measurement points

Inputs		Output
VI	V <sub>M</sub>	V <sub>M</sub>
GND to V <sub>CC</sub>	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in Table 7. Definitions for test circuit:

 $C_L$  = Load capacitance including jig and probe capacitance.

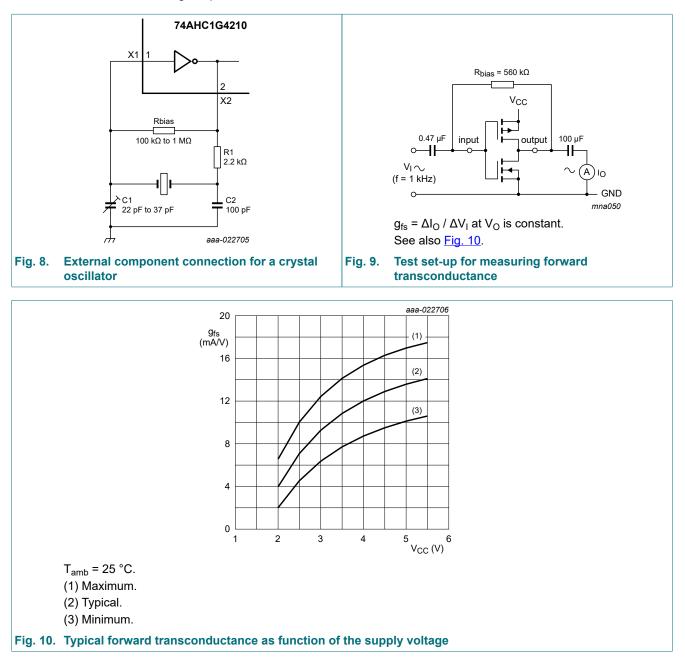
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig. 7. Test circuit for measuring switching times

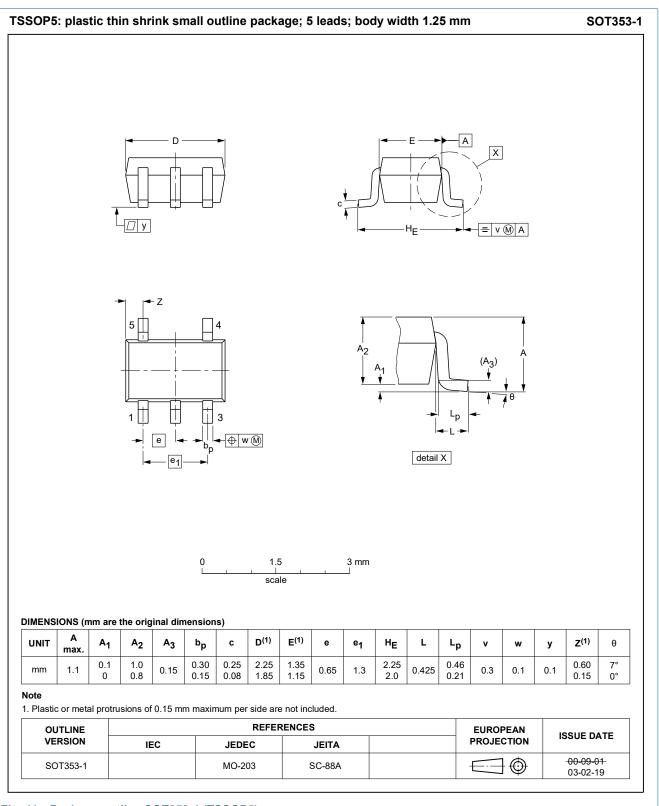
## 12. Crystal oscillator

### 12.1. Typical crystal oscillator circuit

A typical crystal oscillator schematic is shown in Fig. 8. R1 is the power limiting resistor, its value depends on the frequency and required stability against changes in V<sub>CC</sub> or average I<sub>CC</sub>. For starting and maintaining oscillation a minimum transconductance is necessary, so R1 should not be too large. A practical value for R1 is 2.2 k $\Omega$ .



# 13. Package outline



# 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 15. Revision history

Table 10. Revision his	tory								
Document ID	Release date	Data sheet status	Change notice	Supersedes					
74AHC1G4210 v.4	20190627	Product data sheet	-	74AHC1G4210 v.3					
Modifications:	Typo correct	• Typo corrected in Fig. 4.							
74AHC1G4210 v.3	20180425	Product data sheet	-	74AHC1G4210 v.2					
Modifications:	Nexperia.	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>							
74AHC1G4210 v.2	20161026	Product data sheet	-	74AHC1G4210 v.1					
Modifications:	Type numbe	Type number 74AHC1G4210GM removed.							
74AHC1G4210 v.1	20160415	Product data sheet	-	-					

# 16. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# Contents

1. General description	. 1
2. Features and benefits	. 1
3. Ordering information	1
4. Marking	. 1
5. Functional diagram	2
6. Pinning information	2
6.1. Pinning	2
6.2. Pin description	.2
7. Functional description	. 3
8. Limiting values	. 3
9. Recommended operating conditions	3
10. Static characteristics	4
11. Dynamic characteristics	5
11.1. Waveforms and test circuit	. 6
12. Crystal oscillator	. 7
12.1. Typical crystal oscillator circuit	. 7
13. Package outline	. 8
14. Abbreviations	
15. Revision history	9
16. Legal information	10
-	

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74AHC1G4210





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