Datasheet

DS000504

AS7341

11-Channel Spectral Sensor Frontend

v1-00 • 2018-Oct-17

Content Guide

1 General Description

AS7341 is an 11-channel spectrometer for spectral identification and color matching applications used in mobile devices. The spectral response is defined in the wavelengths from approximately 350nm to 1000nm. 6 channels can be processed in parallel by independent ADCs while the other channels are accessible via a multiplexer. 8 optical channels cover the visible spectrum, one channel can be used to measure near infra-red light and one channel is a photo diode without filter (“clear”). The device also integrates a dedicated channel to detect 50Hz or 60Hz ambient light flicker. The flicker detection engine can also buffer data for calculating other flicker frequencies externally. The NIR channel in combination with the other VIS channel may provide information of surrounding ambient light conditions (light source detection).The device can also be synchronized to external signals via pin GPIO.

AS7341 integrates filters into standard CMOS silicon via Nano-optic deposited interference filter technology and its package provides a built in aperture to control the light entering the sensor array. Control and Spectral data access is implemented through a serial I²C interface. The device is available in an ultra-low profile package with dimensions of 3.1mm x 2mm x 1mm.

1.1 Key Benefits & Features

The benefits and features of AS7341, 11-Channel Spectral Sensor Frontend, are listed below:

Figure 1: Added Value of Using AS7341

Benefits	Features
Color matching and skin tone measurement in mobile phones	8 optical channels distributed over the visible spectral range + clear and NIR channel to accurately measure and match colors in mobile phones
Low power consumption and minimum I²C traffic	● 1.8VDD operation ● Configurable sleep mode ● Interrupt-driven device
Integrated ambient light flicker detection on chip and light source detection through NIR channel	● Dedicated channel ● Independently configurable timing and gain ● Automatic gain adjustment ● 50Hz and 60Hz flicker detection flags
Electronic shutter/external trigger functionality	GPIO can be used as external trigger input
External photodiodes to expand detection range	GPIO can be used as input for external InGaAs PDs for MIR range.

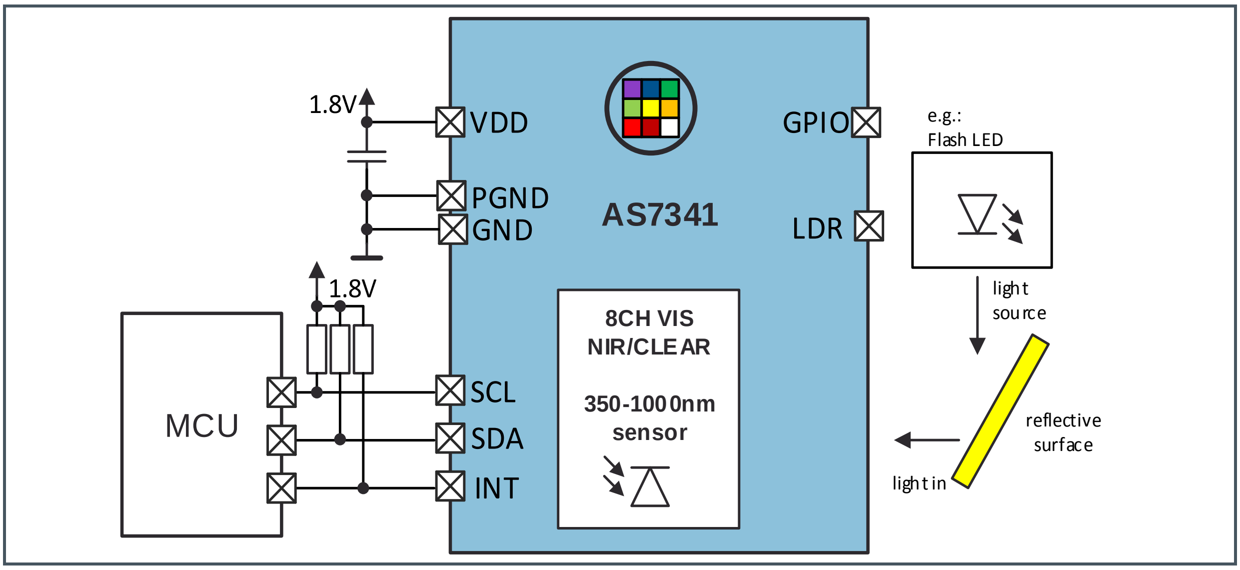
1.2 Applications

- Reflective object color sensor in mobile phones
- Color management for displays
- Ambient light flicker detection for camera assist (flicker detection)

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 : Functional Blocks of AS7341



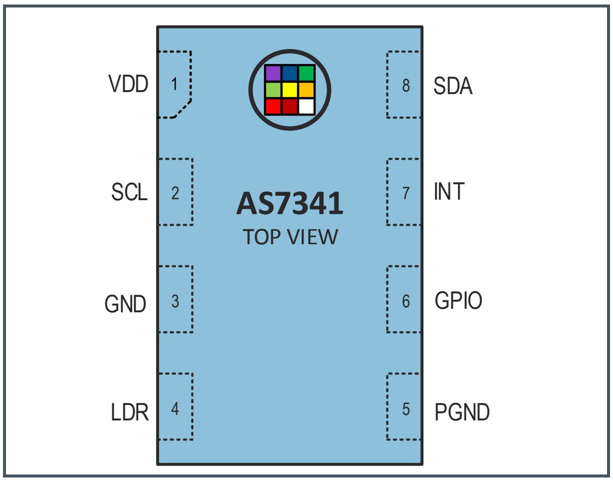
2 Ordering Information

Ordering Code	Package	Delivery Form	Delivery Quantity
AS7341-DLGT	OLGA-8	Tape & Reel 13-inch	5000 pcs/reel
AS7341-DLGM	OLGA-8	Tape & Reel 7-inch	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3: Pin Assignment of AS7341 (TOP VIEW)



3.2 Pin Description

Figure 4: Pin Description of AS7341

Pin Number	Pin Name	Pin Type(1)	Description
1	VDD	P	Positive supply terminal
2	SCL	DI	Serial interface clock signal line for I^{2}C interface
3	GND	P	Ground. All voltages referenced to GND
4	LDR	A_I/O	LED current sink input
5	PGND	P	Ground. All voltages referenced to GND
6	GPIO	DI	General purpose input/output
7	INT	DO_OD	Interrupt. Open drain output. Connect pull up resistor to 1.8V.
8	SDA	D_I/O	Serial interface data signal line for I^{2}C interface

(1) Explanation of abbreviations:

DI	Digital Input
D_I/O	Digital Input/Output
DO_OD	Digital Output, open drain
P	Power pin
A_I/O	Analog pin

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages with respect to GND/PGND. Device parameters are guaranteed at V_{DD}=1.8V and T_A=25°C unless otherwise noted.

Figure 5
Absolute Maximum Ratings of AS7341

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD} / V_{GND}	Supply Voltage to Ground	-0.3	2.2	V	Applicable for pin VDD
V_{ANA_MAX}	Analog Pins	-0.3	3.6	V	Applicable for pin LDR
V_{DIG_MAX}	Digital Pins	-0.3	3.6	V	Applicable for pins SCL,SDA and INT
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78D Nov 2011
I_O	Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JS-001-2014
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-30	85	°C	
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8V and T_A=25°C unless otherwise noted.

Figure 6:
Electrical Characteristics of AS7341

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.7	1.8	2.0	V
T_A	Operating free-air temperature(1)		-30	25	70	°C
Power Consumption						
I_{DD}	Supply Current(2)	V_{DD}=1.8V; T_A=25°C Active mode(3)		210	300	µA
		V_{DD}=1.8V; T_A=25°C Idle mode(4)		35	60	µA
		V_{DD}=1.8V; T_A=25°C Sleep mode(5)		0.7	5	µA
Digital pins						
V_{IH}	SCL,SDA input high voltage		1.26			V
V_{IL}	SCL,SDA input low voltage				0.54	V
V_{OL}	INT, SDA output low voltage	6mA sink current			0.4	V
C_I	Input pin capacitance				10	pF
I_{leak}	Leakage current into SCL,SDA,INT pins		-5		5	µA
GPIO						
C_{LOAD}	Maximum capacitive load GPIO				20	pF

(1) While the device is operational across the temperature range, functionality will vary with temperature.

(2) Supply current values are shown at the VDD pin and do not include current through pin LDR.

(3) Active state occurs during active integration. (PON = “1” ; SP_EN = “1”) If wait is enabled (WEN = “1”), supply current is lower during the wait period

(4) Idle state occurs when PON = “1” and all functions are disabled

(5) Sleep state occurs when PON = “0” and I^2C bus is idle. If I^2C traffic is active device automatically enters idle mode.

6 Optical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8V and T_A=25°C unless otherwise noted.

Figure 7:
Optical Characteristics of Channel F1, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F1}	Irradiance responsivity channel F1(2)	LED: warm white 2700K (3) Ee = 107.67µW/cm^2		48		counts
		LED: 420nm (3) Ee = 57 µW/cm^2 AGAIN = 512x tint = 100ms		2330		counts
λ_p	Center wavelength(1)		400	410	420	nm
FWHM	Full width half maximum(1)			29		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 8:
Optical Characteristics of Channel F2, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F2}	Irradiance responsivity channel F2(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		92		counts
λ_p	Center wavelength(1)		430	440	450	nm
FWHM	Full width half maximum(1)			33		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 9:
Optical Characteristics of Channel F3, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F3}	Irradiance responsivity channel F3(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		180		counts
λ_p	Center wavelength(1)		460	470	480	nm
FWHM	Full width half maximum(1)			36		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 10:
Optical Characteristics of Channel F4, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F4}	Irradiance responsivity channel F4(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		345		counts
λ_p	Center wavelength(1)		500	510	520	nm
FWHM	Full width half maximum(1)			40		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 11:
Optical Characteristics of Channel F5, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F5}	Irradiance Responsivity channel F5(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		560		counts
λ_p	Center wavelength(1)		540	550	560	nm
FWHM	Full width half maximum(1)			42		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 12:
Optical Characteristics of Channel F6, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F6}	Irradiance responsivity channel F6(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		825		counts
λ_p	Center wavelength(1)		573	583	593	nm
FWHM	Full width half maximum(1)			44		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 13:
Optical Characteristics of Channel F7, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F7}	Irradiance responsivity channel F7(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm^2		1290		counts
λ_p	Center wavelength(1)		610	620	630	nm
FWHM	Full width half maximum(1)			53		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 14:
Optical Characteristics of Channel F8, AGAIN: 64x, Integration Time: 27.8ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_F8}	Irradiance responsivity channel F8(2)	LED: warm white 2700K(3) Ee = 107.67µW/cm²		1054		counts
λ_p	Center wavelength(1)		660	670	680	nm
FWHM	Full width half maximum(1)			60		nm

(1) Parameter measured on a production ongoing sample bases on glass using diffused light
(2) The following diffuser is used in final test on top of AS7341: ED1-C50
(3) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

Figure 15:
Typical LED Spectra Used in Final Test of AS7341

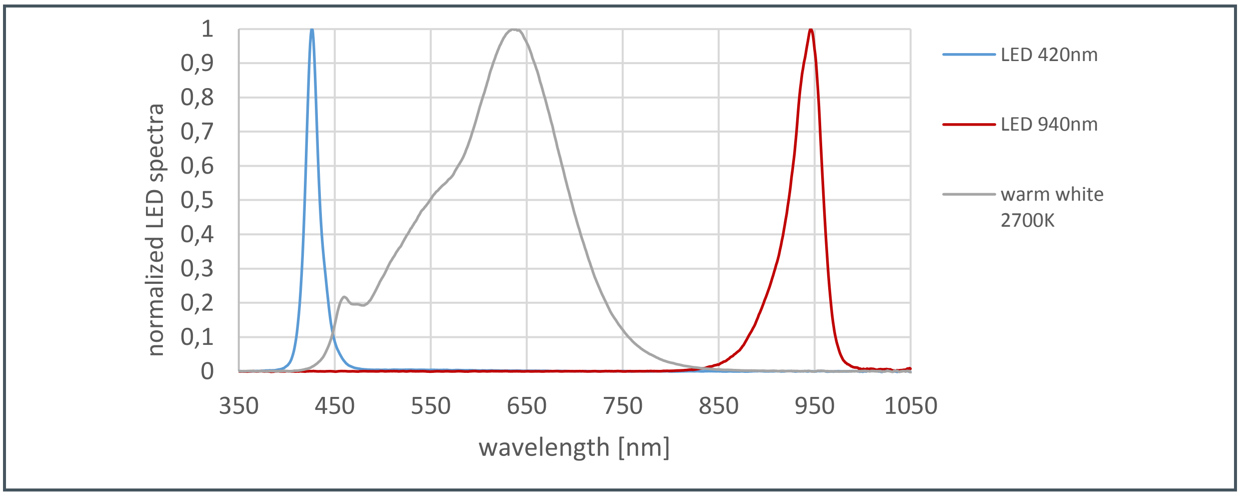


Figure 16:
Optical Characteristics of AS7341, AGAIN: 64x, Integration Time: 27.8ms (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{e_CLEAR}	Irradiance responsivity channel CLEAR	LED: warm white 2700K(5) Ee = 107.67μW/cm^2		1690		counts
$R_{e\_FLICKER}$	Irradiance responsivity channel FLICKER	LED: warm white 2700K(5) Ee = 52.32μW/cm^2		6810		counts
R_{e_NIR}	Irradiance responsivity channel NIR	LED: warm white 2700K(5) Ee = 107.67μW/cm^2		112		counts
		LED: 940nm(5) Ee = 98 μW/cm^2 AGAIN = 128x tint = 100ms		5135		
Dark_$_1$(1)(6)	Dark ADC 0-4 count value	Ee = 0μW/cm^2 AGAIN: 512x Integration time: 98ms		0	3	counts
Dark_$_2$(6)	Dark ADC 5 count value	Ee = 0μW/cm^2 AGAIN: 512x Integration time: 98ms		0	5	counts
Gain(2) ratio	Optical gain ratios, relative to 64x gain setting	AGAIN: 0.5x	0.007	0.008	0.009	
		AGAIN: 1x	0.0145	0.016	0.0175	
		AGAIN: 2x	0.03	0.032	0.034	
		AGAIN: 4x	0.062	0.065	0.068	
		AGAIN: 8x	0.119	0.125	0.131	
		AGAIN: 16x	0.237	0.25	0.263	
		AGAIN: 32x	0.47	0.5	0.53	
		AGAIN: 64x		1		
		AGAIN: 128x	1.8	2	2.1	
		AGAIN: 256x	3.75	3.95	4.25	
		AGAIN: 512x	7.25	7.75	8.25	
ADC noise(3)		AGAIN: 16x Integration time: 10ms		0.005		% full scale
t_{int}	Typical integration time(4)	ASTEP = 599 ATIME = 29		50		ms
t_{ASTEP}	Integration time step size	ASTEP = 999		2.78		ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
h_{ca}	Half cone angle	On the sensor		40		deg

(1) The typical 3-sigma distribution is between 0 and 1 counts for AGAIN setting of 16x.

(2) The gain ratios are calculated relative to the response with integration time: 27.8ms and AGAIN: 64x.

(3) ADC noise is calculated as the standard deviation of 1000 data samples divided by full scale.

(4) Integration time, in milliseconds, is equal to: (ATIME + 1) x (ASTEP + 1) x 2.78µs

(5) Refer to Figure 15:
Typical LED Spectra Used in Final Test of AS7341

(6) Register 0xD6 / AZ_CONFIG is set to “1” – auto zero done before every integration cycle

7 Typical Operating Characteristics

Figure 17:
Normalized Spectral Responsivity

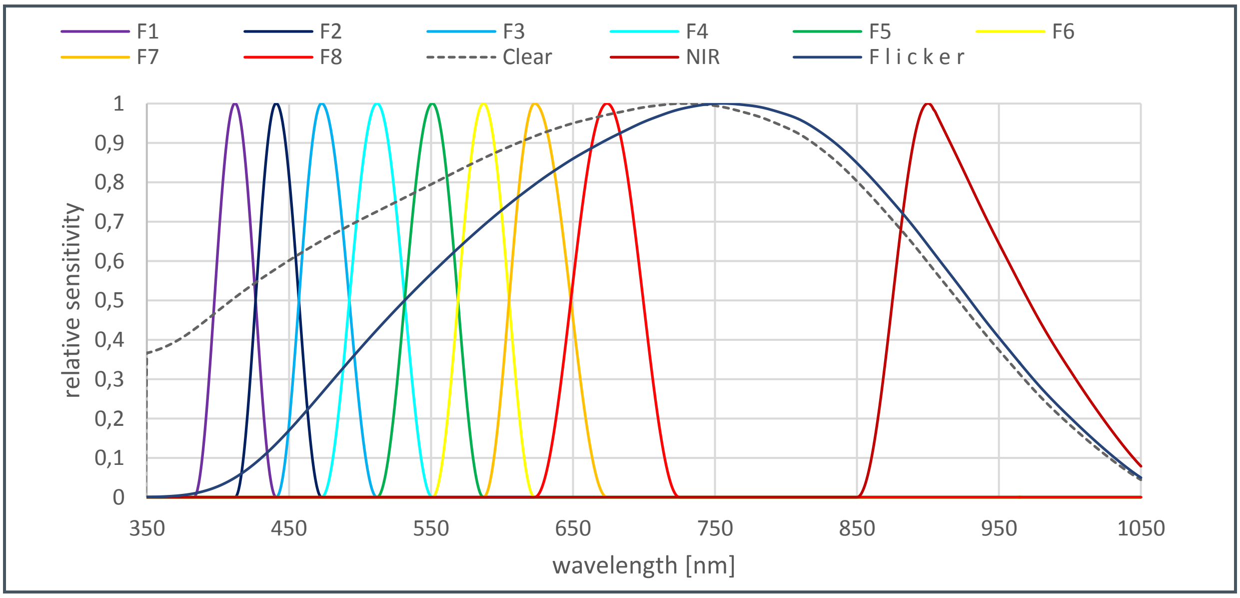
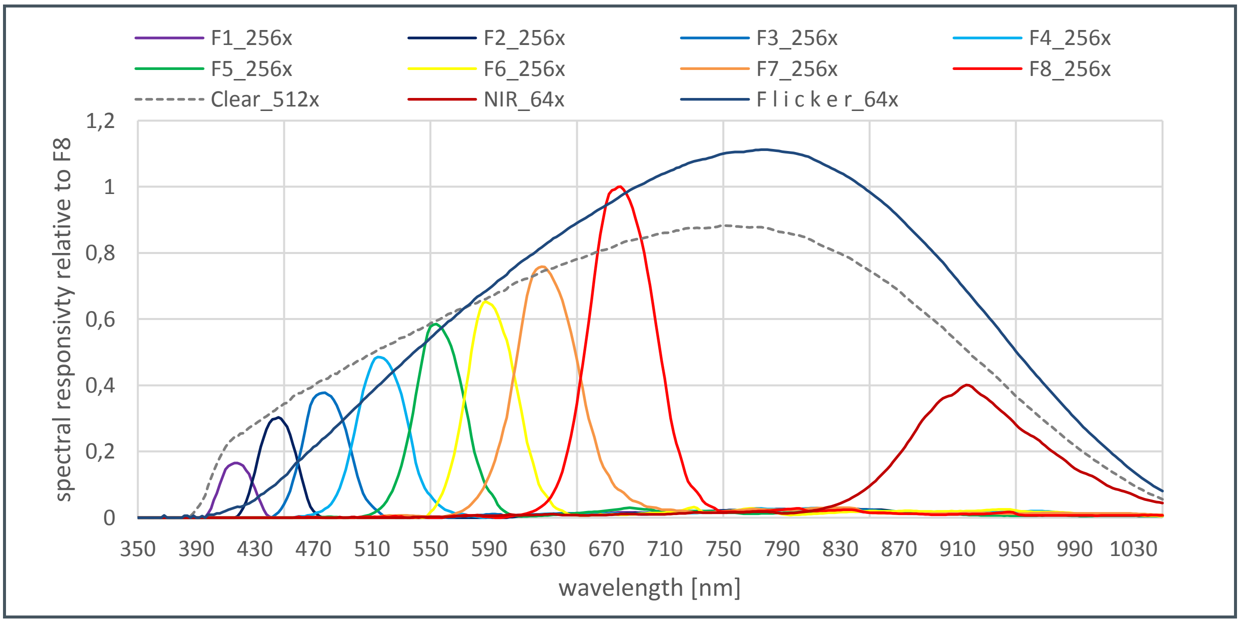


Figure 18:
Measured Spectral Responsivity Relative to F8(1)



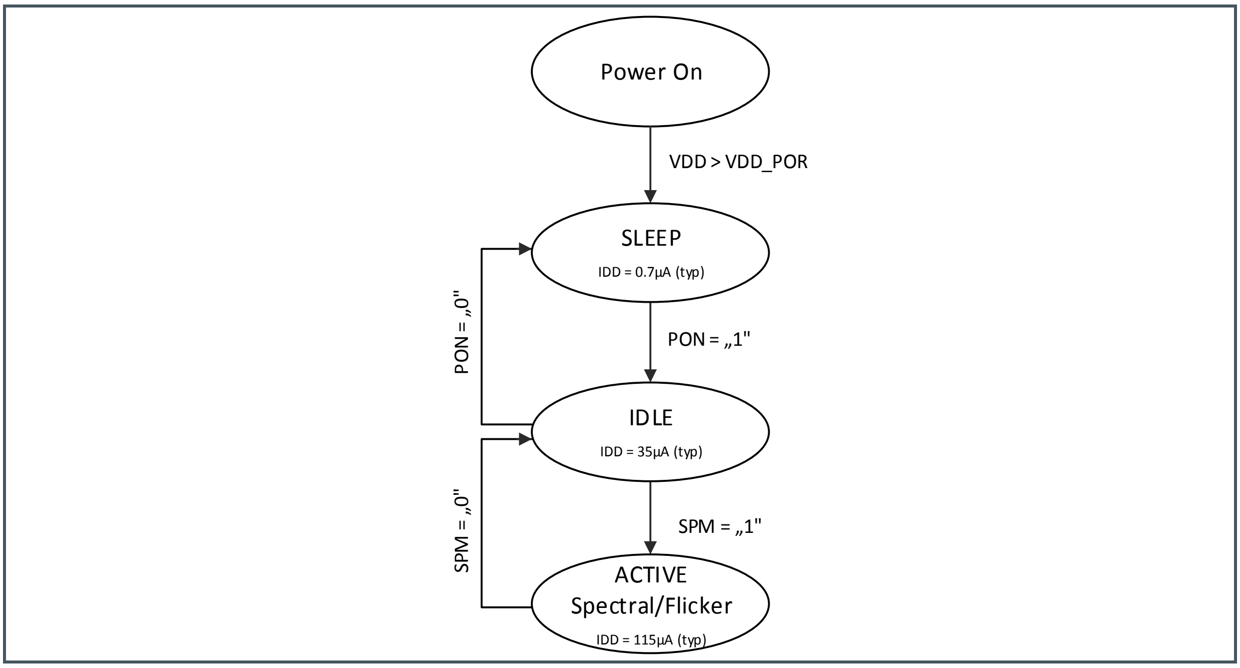
(1) Fx_256x…AGAIN = 256x, diffuser mounted on top of package surface

8 Functional Description

Upon power-up (POR), the device initializes. During initialization (typically 200µs), the device will deterministically send NAK on I²C and cannot accept I²C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during this state, the I²C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the spectral measurement is enabled (SP_EN = "1") the device enters the ACTIVE state. If the spectral measurement is disabled (SP_EN = "0") the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state.

If Sleep after Interrupt is enabled (SAI = "1" in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

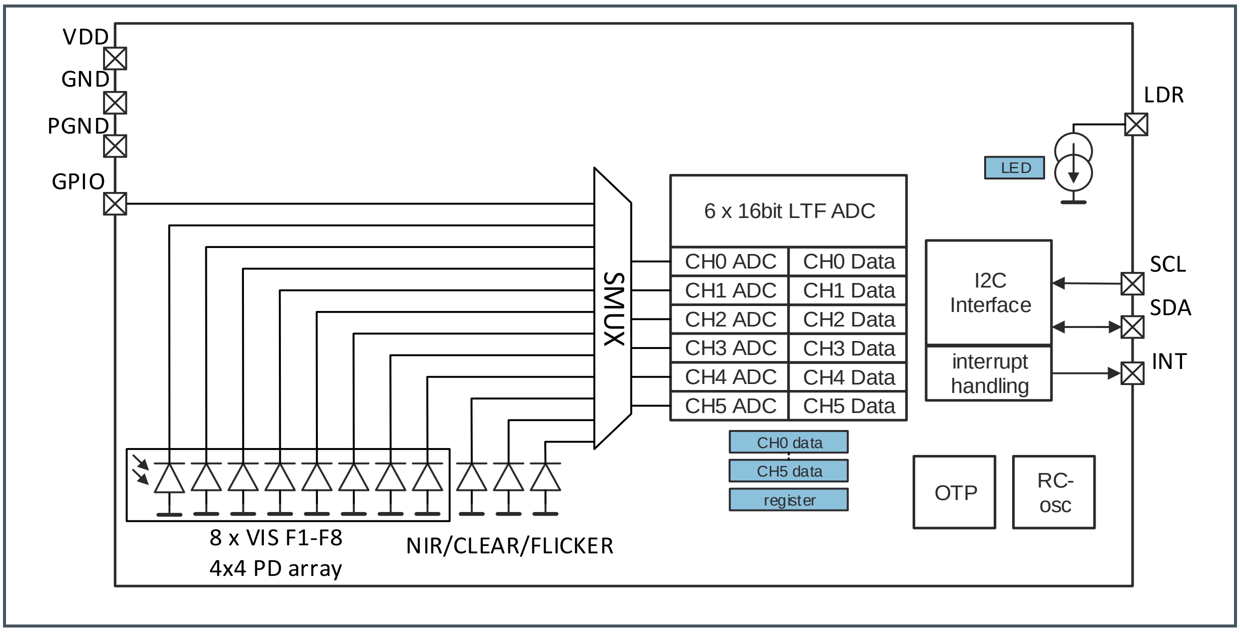
Figure 19: Simplified State Diagram



8.1 Channel Architecture

The device features 6 independent optical channels with a dedicated 16-bit light-to-frequency converter. Gain and integration time of the 6 channels can be adjusted with the serial interface. A wait time can be programed to automatically set a delay between two consecutive spectral measurements and to reduce overall power consumption. The other available channels can be accessed by a multiplexer (SMUX) connecting them to one of the internal ADCs.

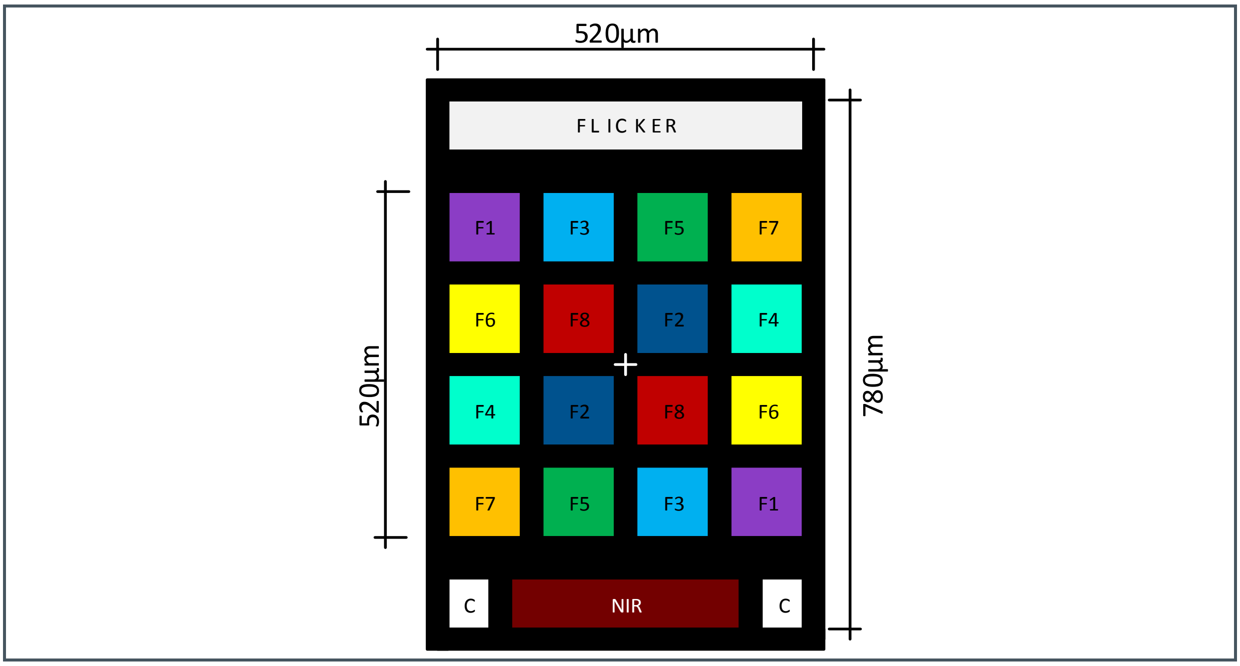
Figure 20: Simplified Block Diagram



8.2 Sensor Array

The device features a 4x4-photodiode array. On top and below the photodiode array there are two photodiodes with dedicated functions such as flicker detection (“FLICKER”) and near- infrared response (“NIR”). A clear channel (“C”) – photodiode without filter – is provided at the left and right bottom corner. Each of the filter pairs can be mapped to one of the six internal ADCs (CH0 – CH5).

Figure 21:
Sensor Array



8.3 GPIO/INT

The GPIO can be either used as input for external photodiodes (e.g. InGaAs) or as synchronization input to start/stop the spectral measurement. (SYNS/SYND mode)

The interrupt output pin INT can also be used to indicate the status (READY/BUSY) of the spectral measurement in mode SYNS and SYND.

8.4 SMUX

The device integrates a multiplexer (SMUX). With the SMUX, it is possible to map all available photo diodes to one of the six available light-to-frequency converter (ADC0 to ADC5). After power up of the device the SMUX needs to be configured before a spectral measurement is started. **ams** provides reference codes and an application note on how to configure the SMUX.

8.5 Integration Mode

The device features three modes to perform a spectral measurement. The integration mode (INT_MODE) can be configured in register 0x70 (CONFIG). For auto zero configuration refer to register 0xD6.

Figure 22:
Integration Mode Description

Mode	Description	Synchronization	Integration Time	Registers
SPM (spectral measurement, no sync) INT_MODE = 0x0	**Default setting:** Integration is started with bit SP_EN = "1". Integration Time is set by register ATIME and ASTEP.	No	ATIME [7:0] ASTEP [15:0]	SP_EN = "1" INT_MODE = 0x0 ATIME [7:0] ASTEP [15:0] WTIME [7:0]
SYNS (spectral measurement, start sync) INT_MODE = 0x1	**Integration with external start:** Integration is started with rising/falling edge on pin GPIO. Integration Time is set by register ATIME and ASTEP.	Yes (start)	ATIME [7:0] ASTEP [15:0]	SP_EN = "1" INT_MODE = 0x1 ATIME [7:0] ASTEP [15:0] WTIME [7:0]
SYND (spectral measurement, start/stop sync) INT_MODE = 0x3	**Integration with external start and stop:** Integration is controlled via rising/falling edge on pin GPIO and register EDGE. If the number of edges on pin GPIO is reached, integration time is stopped. Actual integration time can be read out in register "ITIME".	Yes (start/stop)	Rising/falling edge on pin GPIO and register EDGE[7:0]	SP_EN = "1" INT_MODE = 0x3 EDGE[7:0] ITIME[23:0]

Figure 23 :
SPM Mode

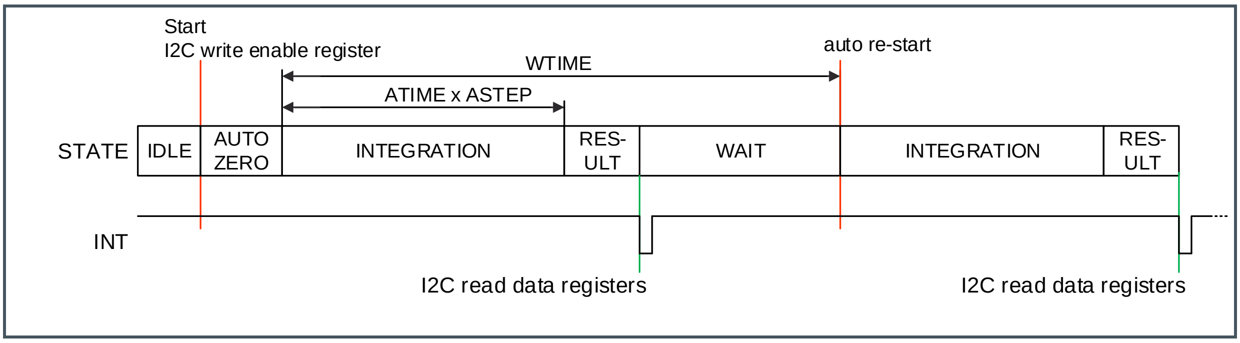


Figure 24 :
SYNS Mode

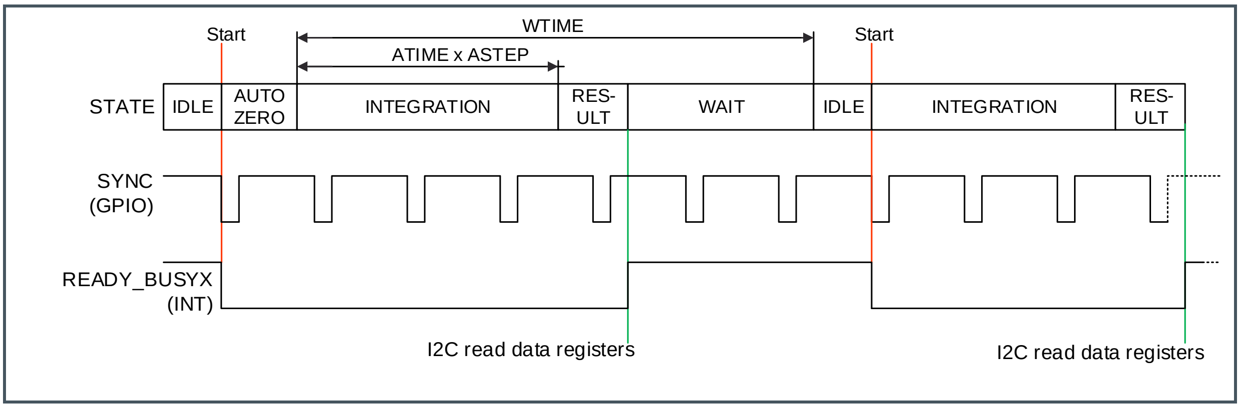
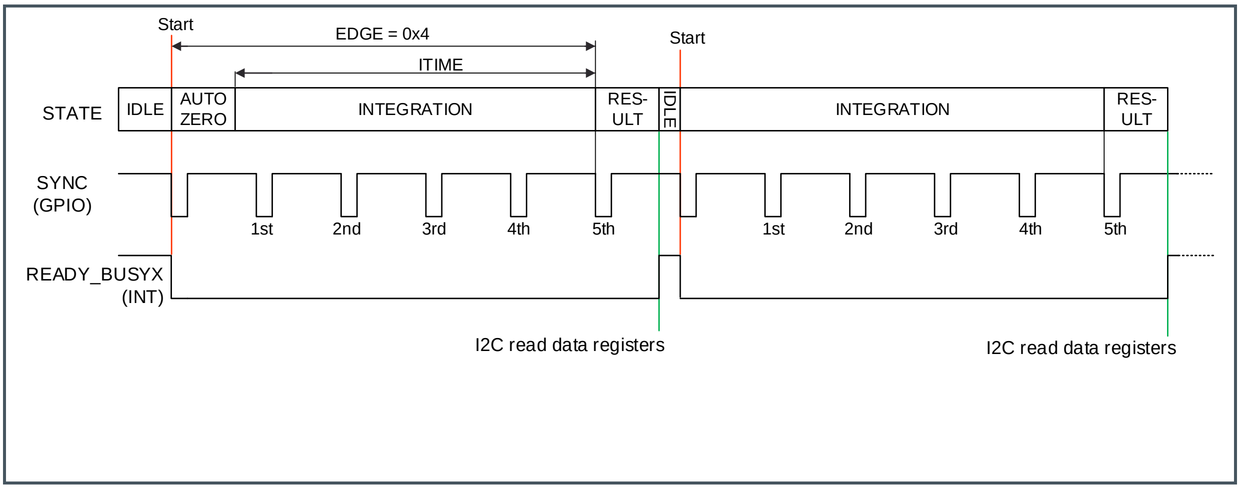


Figure 25 :
SYND Mode



9 I²C Interface

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

9.1 I²C Address

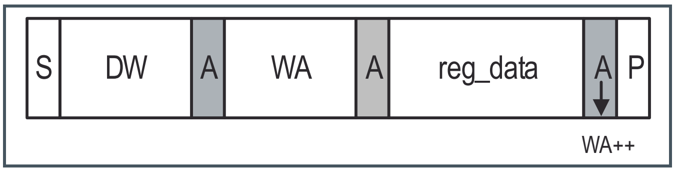
Figure 26:
AS7341 I²C Slave Address

Device	I²C Address
AS7341	0x39

9.2 I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

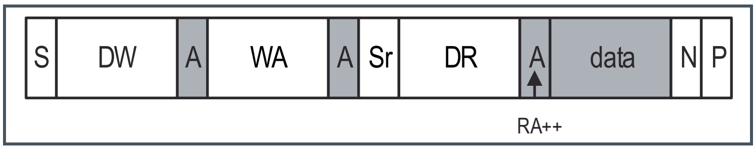
Figure 27:
I²C Byte Write



9.3 I^{2}C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Figure 28:
I^{2}C Read



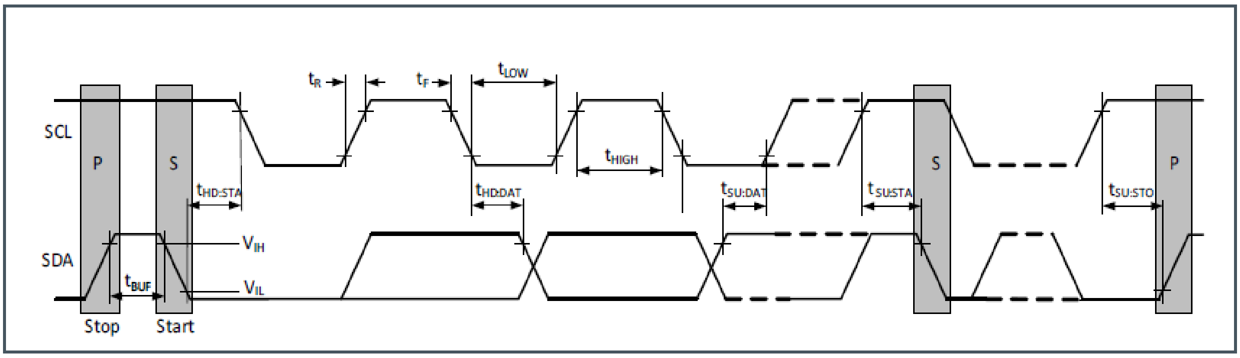
9.4 Timing Characteristics

Figure 29:
I^{2}C Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I^{2}C clock frequency			400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HS;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{SU;STA}$	Repeated start condition setup time	0.6			µs
$t_{SU;STO}$	Stop condition setup time	0.6			µs
t_{LOW}	SCL clock low period	1.3			µs
t_{HIGH}	SCL clock high period	0.6			µs
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			ns
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns

9.5 Timing Diagrams

Figure 30:
I²C Slave Timing Diagram



10 Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0). GRAY fields are reserved and their values must not be changed at any time.

In order to access registers from 0x60 to 0x74 bit REG_BANK in register CFG0 (0xA9) needs to be set to “1”.

10.1 Register Overview

Figure 31:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x60	ASTATUS	ASAT_ STATUS				AGAIN_STATUS [3:0]			
0x61	CH0_DATA	CH0_DATA_L [7:0]							
0x62		CH0_DATA_H [7:0]							
0x63	ITIME	ITIME_L [7:0]							
0x64		ITIME_M [7:0]							
0x65		ITIME_H [7:0]							
0x66	CH1_DATA	CH1_DATA_L [7:0]							
0x67		CH1_DATA_H [7:0]							
0x68	CH2_DATA	CH2_DATA_L [7:0]							
0x69		CH2_DATA_H [7:0]							
0x6A	CH3_DATA	CH3_DATA_L [7:0]							
0x6B		CH3_DATA_H [7:0]							
0x6C	CH4_DATA	CH4_DATA_L [7:0]							
0x6D		CH4_DATA_H [7:0]							
0x6E	CH5_DATA	CH5_DATA_L [7:0]							
0x6F		CH5_DATA_H [7:0]							
0x70	CONFIG					LED_SEL	INT_SEL	INT_MODE[1:0]	
0x71	STAT							WAIT_SYNC	READY
0x72	EDGE	SYNC_EDGE [7:0]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x73	GPIO							PD_GPIO	PD_INT
0x74	LED	LED_ACT	LED_DRIVE [6:0]						
0x80	ENABLE		FDEN		SMUXEN	WEN		SP_EN	PON
0x81	ATIME	ATIME [7:0]							
0x83	WTIME	WTIME [7:0]							
0x84	SP_TH_L	SP_TH_L_LSB [7:0]							
0x85		SP_TH_L_MSB [7:0]							
0x86	SP_TH_H	SP_TH_H_LSB [7:0]							
0x87		SP_TH_H_MSB [7:0]							
0x90	AUXID	AUXID [7:0]							
0x91	REVID	REVID [7:0]							
0x92	ID	ID [7:0]							
0x93	STATUS	ASAT				AINT	FINT	CINT	SINT
0x94	ASTATUS	ASAT_STATUS				AGAIN_STATUS [3:0]			
0x95	CH0_DATA	CH0_DATA_L [7:0]							
0x96		CH0_DATA_H [7:0]							
0x97	CH1_DATA	CH1_DATA_L [7:0]							
0x98		CH1_DATA_H [7:0]							
0x99	CH2_DATA	CH2_DATA_L [7:0]							
0x9A		CH2_DATA_H [7:0]							
0x9B	CH3_DATA	CH3_DATA_L [7:0]							
0x9C		CH3_DATA_H [7:0]							
0x9D	CH4_DATA	CH4_DATA_L [7:0]							
0x9E		CH4_DATA_H [7:0]							
0x9F	CH5_DATA	CH5_DATA_L [7:0]							
0xA0		CH5_DATA_H [7:0]							
0xA3	STATUS 2		AVALID		ASAT_DIG	ASAT_ANA		FDSAT_ANA	FDSAT_DIG
0xA4	STATUS 3			INT_SP_H	INT_SP_L				
0xA6	STATUS 5					SINT_FD			
0xA7	STATUS 6	FIFO_OV		OVTEMP	FD_TRIG		SP_TRIG	SAI_ACT	INT_BUSY
0xA9	CFG 0			LOW_POWER		REG_BANK	WLONG		
0xAA	CFG 1				AGAIN[4:0]				
0xAC	CFG 3				SAI				
0xAF	CFG 6				SMUX_CMD[4:3]				
0xB1	CFG 8	FIFO_TH [7:6]				FD_AGC	SP_AGC		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xB2	CFG 9		SIEN_FD		SIEN_SMUX				
0xB3	CFG 10	AGC_H [7:6]		AGC_L[7:6]			FD_PERS [2:0]		
0xB5	CFG 12						SP_TH_CH [2:0]		
0xBD	PERS					APERS [3:0]			
0xBE	GPIO 2					GPIO_INV	GPIO_IN	GPIO_OUT	GPIO_IN
0xCA	ASTEP	ASTEP [7:0]							
0xCB		ASTEP [15:8]							
0xCF	AGC_GAIN_MAX	AGC_FD_GAIN_MAX [7:4]				AGC_AGAIN_MAX [3:0]			
0xD6	AZ_CONFIG	AT_NTH_ITERATION [7:0]							
0xD8	FD_TIME 1	FD_TIME [7:0]							
0xDA	FD_TIME 2	FD_GAIN [7:3]					FD_TIME [10:8]		
0xD7	FD_CFG0	FD_FIFO							
0xDB	FD_STATUS			FD_VALID	FD_SAT	FD_120HZ_VALID	FD_100Hz_VALID	FD_120Hz	FD_100Hz
0xF9	INTENAB	ASIEN				SP_IEN	FIEN	CIEN	SIEN
0xFA	CONTROL						AZ_SP_MAN	FIFO_CLR	CLEAR_SAI_ACT
0xFC	FIFO_MAP		FIFO_WRITE_CH5_DATA – FIFO_WRITE_CH0_DATA [6:1]						ASTATUS
0xFD	FIFO_LVL	FIFO_LVL [7:0]							
0xFE	FDATA	FDATA [7:0]							
0xFF		FDATA [15:8]							

10.2 Detailed Register Description

For easier readability, the detailed register description is done in groups of registers related to dedicated device functions. This is not necessarily related to its register address.

Explanation of register access abbreviations:
RW = read or write
R = read only
W = write only
SC = self-clearing after access

10.2.1 Enable and Configuration Register

The following registers are needed to power up and configure the device. To operate the device set bit PON = “1” first (register 0x80) after that configure the device and enable interrupts before setting SP_EN = “1”. Changing configuration while SP_EN = “1” may result in invalid results. Register CONFIG (0x70) is used to set the INT_MODE (SYNS,SYND).

ENABLE Register (Address 0x80)

Figure 32:
ENABLE Register

Addr: 0x80		**ENABLE**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	reserved	0	RW	reserved
6	FDEN	0	RW	**Flicker Detection Enable.** 0: Flicker Detection disabled 1: Flicker Detection enabled
5	reserved	0	RW	reserved
4	SMUXEN	0	RW	**SMUX Enable.** 1: Starts SMUX command Note: this bit gets cleared automatically as soon as SMUX operation is finished
3	WEN	0	RW	**Wait Enable.** 0: Wait time between two consecutive spectral measurements disabled 1: Wait time between two consecutive spectral measurements enabled
2	reserved	0	RW	reserved
1	SP_EN	0	RW	**Spectral Measurement Enable.** 0: Spectral Measurement Enabled 1: Spectral Measurement Disabled
0	PON	0	RW	**Power ON.** 0: AS7341 disabled 1: AS7341 enabled Note: When bit is set, internal oscillator is activated, allowing timers and ADC channels to operate.

CONFIG Register (Address 0x70)

Figure 33:
CONFIG Register

Addr: 0x70		CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reserved	0	RW	reserved
3	LED_SEL	0	RW	**LED control.** 0: External LED not controlled by AS7341 1: Register LED controls LED connected to pin LDR Note: register 0x74
2	INT_SEL	0	RW	1: Sync signal applied on output pin INT
1:0	INT_MODE	0	RW	**Ambient light sensing mode:** 0: SPM mode (spectral measurement, normal mode) 1: SYNS mode 2: reserved 3: SYND mode Note: in SYND mode it is recommended to use register 0x60 to 0x6F to read out spectral data.

GPIO Register (Address 0x73)

Figure 34:
GPIO Register

Addr: 0x73		GPIO		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	reserved	0	RW	reserved
1	PD_GPIO	0	RW	1: Photo diode connected to pin GPIO
0	PD_INT	0	RW	1: Photo diode connected to pin INT

GPIO 2 Register (Address 0xBE)

Figure 35:
GPIO2 Register

Addr: 0xBE		GPIO 2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reserved	0		reserved
3	GPIO_INV	0	RW	**GPIO Invert.** If set, the GPIO output is inverted.
2	GPIO_IN_EN	0	RW	**GPIO Input Enable.** If set, the GPIO pin accepts a non-floating input.
1	GPIO_OUT	1	RW	**GPIO Output.** If set, the output state of the GPIO is active directly.
0	GPIO_IN	0	R	**GPIO Input.** Indicates the status of the GPIO input if GPIO_IN_EN is set.

LED Register (Address 0x74)

Figure 36:
LED Register

Addr: 0x74		LED		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LED_ACT	0	RW	**LED control.** 0: External LED connected to pin LDR off 1: External LED connected to pin LDR on
6:0	LED_DRIVE	000 0100	RW	**LED driving strength.** 000 0000: 4mA 000 0001: 6mA 000 0010: 8mA 000 0011: 10mA **000 0100:** 12mA …… 111 1110: 256mA 111 1111: 258mA Note: Bit LED_SEL (register 0x70) needs to be set to “1” to control LED connected to pin LDR.

INTENAB Register (Address 0xF9)

Figure 37:
INTENAB Register

Addr: 0xF9		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	**Spectral and Flicker Detect Saturation Interrupt Enable.** When asserted permits saturation interrupts to be generated.
6:4	reserved			reserved
3	SP_IEN	0	RW	**Spectral Interrupt Enable.** When asserted permits interrupts to be generated, subject to the spectral thresholds and persistence filter. Bit is mirrored in the ENABLE register.
2	F_IEN	0	RW	**FIFO Buffer Interrupt Enable.** When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition.
1	reserved	0		reserved
0	SIEN		RW	**System Interrupt Enable.** When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed or SMUX operation has finished.

CONTROL Register (Address 0xFA)

Figure 38:
CONTROL Register

Addr: 0xFA		CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	reserved	0		reserved
2	SP_MAN_AZ	0	RW	**Spectral Engine Manual Autozero.** Starts a manual autozero of the spectral engines. Set SP_EN = 0 before starting a manual autozero for it to work.
1	FIFO_CLR	0	RW	**FIFO Buffer Clear.** Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL.
0	CLEAR_SAI_ACT	0	RW	**Clear Sleep-After-Interrupt Active.** Clears SAI_ACTIVE, ends sleep, and restarts device operation.

10.2.2 ADC Timing Configuration / Integration Time

The integration time in INT_MODE = “00” and “01” (SPM/SYNS) is set using the ATIME (0x81) and ASTEP (0xCA, 0xCB) registers. The integration time, in milliseconds, is equal to:

Equation 1: Setting the integration time

$$t_{int} = (ATIME + 1) \times (ASTEP + 1) \times 2.78\mu s$$

The reset value for ASTEP is 999 (2.78ms) and the recommended configuration for these two registers is ASTEP = 599 and ATIME = 29, which results in an integration time of 50ms. It is not allowed that both settings –ATIME and ASTEP – are set to “0”.

The integration time also defines the full-scale ADC value, which is equal to:

Equation 2: ADC full scale value

$$ADC_{fullscale} = (ATIME + 1) \times (ASTEP + 1)$$

ATIME Register (Address 0x81)

Figure 39:
ATIME Register

<table>
<tr><th colspan="2">Addr: 0x81</th><th colspan="4">ATIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">ATIME</td><td rowspan="5">0x00</td><td rowspan="5">RW</td><td colspan="2">Integration time.
Sets the number of integration steps from 1 to 256.</td></tr>
<tr><td>Value</td><td>Integration Time</td></tr>
<tr><td>0</td><td>ASTEP</td></tr>
<tr><td>n</td><td>ASTEP x (n+1)</td></tr>
<tr><td>255</td><td>256 x ASTEP</td></tr>
</table>

ASTEP Register (Address 0xCA, 0xCB)

Figure 40:
ASTEP Register

<table>
<tr><th>Addr: 0xCA, 0xCB</th><th></th><th>ASTEP</th><th></th><th colspan="2"></th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="4">7:0</td><td rowspan="4">ASTEP 0xCA</td><td rowspan="9">999</td><td rowspan="9">RW</td><td colspan="2">Integration time step size.
Sets the integration time per step in increments of 2.78µs. The default value is 999.</td></tr>
<tr><td>VALUE</td><td>STEP SIZE</td></tr>
<tr><td>0</td><td>2.78µs</td></tr>
<tr><td>n</td><td>2.78µs x (n+1)</td></tr>
<tr><td rowspan="5">15:8</td><td rowspan="5">ASTEP 0xCB</td><td>599</td><td>1.67ms</td></tr>
<tr><td>999</td><td>2.78ms</td></tr>
<tr><td>17999</td><td>50ms</td></tr>
<tr><td>65534</td><td>182ms</td></tr>
<tr><td>65535</td><td>reserved, do not use</td></tr>
</table>

WTIME Register (Address 0x83)

If wait is enabled (WEN = “1” register 0x80), each new measurement is started based on WTIME. It is necessary for WTIME to be sufficiently long for spectral integration and any other functions to be completed within the period. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then SP_TRIG in register STATUS6 (ADDR: 0xA7) will be set to “1”.

Figure 41:
WTIME Register

<table>
<tr><th>Addr: 0x83</th><th></th><th>WTIME</th><th></th><th colspan="3"></th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td rowspan="6">7:0</td><td rowspan="6">WTIME</td><td rowspan="6">0x00</td><td rowspan="6">RW</td><td colspan="3">Spectral Measurement Wait time.
8-bit value to specify the delay between two consecutive spectral measurements.</td></tr>
<tr><td>Value</td><td>Wait Cycles</td><td>Wait Time</td></tr>
<tr><td>0x00</td><td>1</td><td>2.78ms</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56ms</td></tr>
<tr><td>n</td><td>n</td><td>2.78ms x (n+1)</td></tr>
<tr><td>0xff</td><td>256</td><td>711ms</td></tr>
</table>

ITIME Register (Address 0x63, 0x64, 0x65)

The register ITIME can be used to read-out the actual integration time in INT_MODE = “11” (SYND). In SYND mode the integration time is defined by the register “EDGE” and the device is running integration until the number of falling edges on pin GPIO is reached.

Equation 3: Calculating the integration time in SYND mode

$$t_{int} = ITIME \times 2.78\mu s$$

Figure 42:
ITIME_L Register

Addr: 0x63		ITIME_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ITIME_L	0	R	Integration time in integration mode SYND

Figure 43:
ITIME_M Register

Addr: 0x64		ITIME_M		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	ITIME_M	0	R	Integration time in integration mode SYND

Figure 44:
ITIME_H Register

Addr: 0x65		ITIME_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
23:16	ITIME_H	0	R	Integration time in integration mode SYND

EDGE Register (Address 0x72)

Figure 45:
EDGE Register

Addr: 0x72		EDGE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SYNC_EDGE	0	RW	Number of falling SYNC-edges between start and stop of integration in mode SYND Number of edges = SYNC_EDGE + 1

FD_TIME Register (Address 0xD8, 0xDA)

The register FD Time 1 and FD Time 2 can be used to configure the integration time and gain (ADC 5) of the flicker detection independently from the other ADCs. The FD_TIME register is an 11-bit register with the MSB in register 0xDA (bit 10:8) and the LSB in register 0xD8 (bit 7:0). The bit FDEN (register 0x80) must be set to “1” in order to use the FD_TIME registers. If the bit FDEN is not set, ADC5 runs automatically with the same gain and integration time as ADC0 to ADC4.

Equation 4: Calculating the flicker detection integration time

$$t_{int\_FD} = FD\_TIME \times 2.78\mu s$$

Figure 46:
FD Time Register

Addr: 0xD8		FD_TIME_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FD_TIME [7:0]	0	RW	LSB of flicker detection integration time Note: must not be changed during FDEN = 1 and PON = 1.

Figure 47:
FD Time Register

Addr: 0xDA		FD_TIME_2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:3	FD_GAIN	9	R/W	**Flicker Detection gain setting (ADC5)**	
				VALUE	**GAIN**
				0	0.5x
				1	1x
				2	2x
				3	4x
				4	8x
				5	16x
				6	32x
				7	64x
				8	128x
				9	256x
				10	512x
2:0	FD_TIME [10:8]	0	RW	MSB of flicker detection integration time Note: must not be changed during FDEN = 1 and PON = 1.	

10.2.3 ADC Configuration (gain, AGC…)

The following registers provide configuration for the 6 integrated ADCs (CH0 to CH5). It is possible to adjust the gain, configure and enable the automatic gain control (AGC) and setup the auto zero compensation for the engines.

CFG1 Register (Address 0xAA)

Figure 48:
CFG1 Register

Addr: 0xAA		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	reserved	0		reserved
4:0	AGAIN	9	RW	**Spectral engines gain setting.** Sets the spectral sensitivity. **VALUE** – **GAIN** 0 – 0.5x 1 – 1x 2 – 2x 3 – 4x 4 – 8x 5 – 16x 6 – 32x 7 – 64x 8 – 128x 9 – 256x 10 – 512x

CFG10 Register (Address 0xB3)

Figure 49:
CFG10 Register

Addr: 0xB3		CFG10		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	AGC_H	3	RW	**AGC High Hysteresis.** Sets the data threshold at which AGAIN is reduced when spectral AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) x (ASTEP + 1).

Addr: 0xB3		CFG10			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				VALUE	**SIGNAL**
				0	50%
				1	62.5%
				2	75%
				3	87.5%
5:4	AGC_L	3	RW	**AGC Low Hysteresis.** Sets the data threshold at which AGAIN is increased when spectral AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) x (ASTEP + 1).	
				VALUE	**SIGNAL**
				0	12.5%
				1	25%
				2	37.5%
				3	50%
3	reserved	0		reserved	
2:0	FD_PERS	2	RW	**Flicker Detect Persistence.** Sets the number of consecutive flicker detect results that must be different before the flicker detect status will be changed. Flicker detection interrupts on SINT are affected by this setting. Flicker detect persistence is equal to $2^{(FD_{PERS}-1)}$	

AZ_CONFIG Register (Address 0xD6)

The following register configures how often the spectral engine offsets are reset (auto zero) to compensate for changes of the device temperature. The typical time auto zero needs to be completed is 15ms.

Figure 50:
AZ_CONFIG Register

Addr: 0xD6		AZ_CONFIG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	AZ_NTH_ITERATION	255	RW	**AUTOZERO FREQUENCY.** Sets the frequency at which the device performs auto zero of the spectral engines. Note: If FDEN = “1” auto zero is also done for ADC 5. The flicker detection measurement will be interrupted and restarted in this case.	
				VALUE	**AUTOZERO FREQUENCY**
				0	Never (not recommended)
				1	Every integration cycle
				2	Every 2 cycles
				…	Every “AZ_NTH_ITERATION” cycle
				254	Every 254 cycles
				255	Only before first measurement cycle

AGC_GAIN_MAX Register (Address 0xCF)

Figure 51:
AGC_GAIN_MAX Register

Addr: 0xCF		AGC_GAIN_MAX		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	AGC_FD_GAIN_MAX	9	RW	**Flicker Detection AGC Gain Max.** Sets the maximum gain for flicker detection to $2^{AGC\_FD\_GIAN\_MAX}$ Default value is 9 (256x). The range can be set from 0 (0.5x) to 10 (512x).
3:0	AGC_AGAIN_MAX	9	RW	**AGC Gain Max.** Sets the maximum gain for AGC engine to $2^{AGC\_FD\_GIAN\_MAX}$ Default value is 9 (256x). The range can be set from 0 (0.5x) to 10 (512x).

CFG8 Register (Address 0xB1)

Figure 52:
CFG8 Register

<table>
<tr><th colspan="2">Addr: 0xB1</th><th colspan="4">CFG8</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">FIFO_TH</td><td rowspan="6">2</td><td rowspan="6">R/W</td><td colspan="2">FIFO Threshold.
Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT).</td></tr>
<tr><td>VALUE</td><td>FIFO_LVL</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>4</td></tr>
<tr><td>2</td><td>8</td></tr>
<tr><td>3</td><td>16</td></tr>
<tr><td>5:4</td><td>reserved</td><td>0</td><td></td><td colspan="2">reserved</td></tr>
<tr><td>3</td><td>FD_AGC</td><td>1</td><td>RW</td><td colspan="2">Flicker Detect AGC Enable.
If set, device uses automatic gain control for the flicker detect engine to maximize flicker signal and avoid saturation.</td></tr>
<tr><td>2</td><td>SP_AGC</td><td>0</td><td>RW</td><td colspan="2">Spectral AGC enable.
If asserted, device uses automatic gain control for the spectral engines to maximize signal while avoiding saturation.</td></tr>
<tr><td>1</td><td>reserved</td><td>0</td><td></td><td colspan="2">reserved</td></tr>
<tr><td>0</td><td>reserved</td><td>0</td><td></td><td colspan="2">reserved</td></tr>
</table>

10.2.4 Device Identification

The following registers provided device identification. Device ID, revision ID and auxiliary ID are read only.

AUXID Register (Address 0x90)

Figure 53:
AUXID Register

Addr: 0x90		AUXID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reserved			reserved
3:0	AUXID	000	R	**Auxiliary identification**

REVID Register (Address 0x91)

Figure 54:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	reserved			reserved
2:0	REV_ID	000	R	**Revision number identification**

ID Register (Address 0x92)

Figure 55:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	ID	001001	R	**Part number Identification** Value 001001
1:0	reserved			reserved

10.2.5 Spectral Interrupt Configuration

The spectral interrupt threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CH0_DATA values (ADC CH0). If SP_IEN (register 0xF9) is enabled and CH0_DATA is not between the two thresholds for the number of consecutive measurements specified in APERS (register 0xBD) an interrupt is set.

SP_TH_L_LSB Register (Address 0x84)

Figure 56:
SP_TH_L_LSB Register

Addr: 0x84		SP_TH_L_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_L_LSB	0x00	RW	**Spectral low threshold LSB** This register provides the low byte of the low interrupt threshold (CH0).

SP_TH_L_MSB Register (Address 0x85)

Figure 57:
SP_TH_L_MSB Register

Addr: 0x85		SP_TH_L_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_L_MSB	0x00	RW	**Spectral low threshold MSB** This register provides the high byte of the low interrupt threshold (CH0). Both SP_TH_L registers are combined to a 16-bit threshold. If the value captured by channel 0 is below the low threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated. There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied at the same time to avoid an invalid threshold. Note: The LSB register cannot be changed without writing to the MSB register. It is recommended to write to SP_TH_L_LSB and SP_TH_L_MSB within one I^{2}C command.

SP_TH_H_LSB Register (Address 0x86)

Figure 58:
SP_TH_H_LSB Register

Addr: 0x86		SP_TH_H_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_H_LSB	0x00	RW	**Spectral high threshold LSB** This register provides the low byte of the high interrupt threshold (CH0).

SP _TH_H_MSB Register (Address 0x87)

Figure 59:
SP _TH_H_MSB Register

Addr: 0x87		SP _TH_H_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SP_TH_H_MSB	0x00	RW	**Spectral high threshold MSB** This register provides the high byte of the high interrupt threshold (CH0).

Addr: 0x87		SP _TH_H_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				Both SP_TH_H registers are combined to a 16-bit threshold. If the value captured by channel 0 is above the high threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated.

CFG12 Register (Address 0xB5)

Figure 60:
CFG12 Register

Addr: 0xB5		CFG12			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:3	reserved	0		reserved	
2:0	SP_TH_CH	0	RW	**Spectral Threshold Channel.** Sets the channel used for interrupts, persistence and the AGC, if enabled, to determine device status and gain settings.	
				VALUE	**CHANNEL**
				0	CH0
				1	CH1
				2	CH2
				3	CH3
				4	CH4

10.2.6 Device Status Register

The following register provide status of the device and indicate details about saturation, interrupts, over temperature, device execution and ambient light flicker detection.

STAT Register (Address 0x71)

Figure 61:
STAT Register

Addr: 0x71		STAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	reserved	0	RW	reserved
1	WAIT_SYNC	0	R	1: Device waits for sync pulse on GPIO to start integration (SYNS / SYND INT_mode)
0	READY	0	R	0: Spectral measurement status is busy 1: Spectral measurement status is ready

STATUS Register (Address 0x93)

The primary status register for AS7341 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a "1" to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s) and then write the register value back to STATUS to clear the handled events. Writing "0" will not clear those bits if they have a value of "1", which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared.

Figure 62:
STATUS Register

Addr: 0x93		**STATUS**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT	0	R, SC	**Spectral and Flicker Detect saturation.** If ASIEN is set, indicates Spectral saturation. Check STATUS2 register to distinguish between analog or digital saturation.
6:4	reserved	0	R	reserved
3	AINT	0	R, SC	**Spectral Channel Interrupt.** If SP_IEN is set, indicates that a spectral event that met the programmed thresholds and persistence (APERS) occurred.
2	FINT	0	R, SC	**FIFO Buffer Interrupt.** If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer.
1	C_INT	0	R, SC	**Calibration Interrupt.**
0	SINT	0	R, SC	**System Interrupt.** If SIEN is set, indicates that system interrupt is set. Refer to Status5 register.

STATUS 2 Register (Address 0xA3)

Figure 63:
STATUS 2 Register

Addr: 0xA3		**STATUS 2**		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	reserved	0		reserved
6	AVALID	0	R	**Spectral Valid**. Indicates that the spectral measurement has been completed
5	reserved	0		reserved

Addr: 0xA3		STATUS 2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	ASAT_DIGITAL	0	R	**Digital saturation**. Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.
3	ASAT_ANALOG	0	R	**Analog saturation**. Indicates that the intensity of ambient light has exceeded the maximum integration level for the spectral analog circuit.
2	reserved	0	R	reserved
1	FDSAT_ANALOG	0	R	**Flicker detect analog saturation**. Indicates that the intensity of ambient light has exceeded the maximum integration level for the analog circuit for flicker detection.
0	FDSAT_DIGITAL	0	R	**Flicker detect digital saturation**. Indicates that the maximum counter value has been reached during flicker detection.

STATUS 3 Register (Address 0xA4)

Figure 64:
STATUS 3 Register

Addr: 0xA4		STATUS 3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	reserved	0		reserved
5	INT_SP_H	0	R	**Spectral interrupt high.** Indicates that a spectral interrupt occurred because the data exceeded the high threshold.
4	INT_SP_L	0	R	**Spectral interrupt low**. Indicates that a spectral interrupt occurred because the data is below the low threshold.
3:0	reserved	0		reserved

STATUS 5 Register (Address 0xA6)

Figure 65:
STATUS 5 Register

Addr: 0xA6		STATUS 5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reserved	0		reserved

Addr: 0xA6		STATUS 5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	SINT_FD	0	R	**Flicker Detect interrupt.** If SIEN_FD is set, indicates that the FD_STATUS register status has changed
2	SINT_SMUX	0	R	**SMUX operation interrupt.** Indicates that SMUX command execution has finished.
1:0	reserved	0		reserved

STATUS 6 Register (Address 0xA7)

Figure 66:
STATUS 6 Register

Addr: 0xA7		STATUS 6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FIFO_OV	0	R	**FIFO Buffer Overflow.** Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read
6	reserved	0	R	reserved
5	OVTEMP	0	R	**Over Temperature Detected.** Indicates the device temperature is too high. Write 1 to clear this bit.
4	FD_TRIG	0	R	**Flicker Detect Trigger Error.** Indicates that there is a timing error that prevents flicker detect from working correctly.
3	reserved	0		reserved
2	SP_TRIG	0	R	**Spectral Trigger Error.** Indicates that there is a timing error. The WTIME is too short for the selected ATIME.
1	SAI_ACTIVE	0	R	**Sleep after Interrupt Active.** Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.
0	INT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete.

FD_STATUS Register (Address 0xDB)

Figure 67:
FD STATUS Register

Addr: 0xDB		FD_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	reserved			reserved
5	FD_MEASUREMENT_VALID	0	R	**Flicker Detection Measurement Valid.** Indicates that flicker detection measurement is complete. Write 1 to this bit to clear this field.
4	FD_SATURATION_DETECTED	0	R	**Flicker Saturation Detected.** Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field.
3	FD_120HZ_FLICKER_VALID	0	R	**Flicker Detection 120Hz Flicker Valid.** Indicates that the 120Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
2	FD_100HZ_FLICKER_VALID	0	R	**Flicker Detection 100Hz Flicker Valid.** Indicates that the 100Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
1	FD_120HZ_FLICKER	0	R	**Flicker Detected at 120Hz.** Indicates if an ambient light source is flickering at 120Hz.
0	FD_100HZ_FLICKER	0	R	**Flicker Detected at 100Hz.** Indicates if an ambient light source is flickering at 100Hz.

10.2.7 Spectral Data and Status

The ASTATUS register is mapped to register address 0x60 and 0x94. It provides saturation and gain status associated to each set of spectral data. Reading the ASTATUS register (0x60 or 0x94) latches all 12 spectral data bytes to that status read. Reading these bytes consecutively (0x60 to 0x6F or 0x94 to 0xA0) ensures that the data is concurrent. All spectral data are stored as 16-bit values. If flicker detection is enabled, spectral channel five (CH5 ADC) is used for the flicker detection function and CH5_DATA will read “0”. The ASTATUS and spectral data registers are read only.

In SPM or SYNS mode, it is recommended to use the ASTATUS register 0x94 and spectral data register 0x94 to 0xA0. In SYND mode, it is possible to use register 0x60 to 0x6F for easier implementation.

ASTATUS Register (Address 0x60 or 0x94)

Figure 68:
ASTATUS Register

Addr: 0x60 and 0x94		ASTATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT_STATUS	0	R, SC	**Saturation Status.** Indicates if the latched data is affected by analog or digital saturation.
6:4	reserved	0	R	reserved
3:0	AGAIN_STATUS	0	R, SC	**Gain Status.** Indicates the gain applied for the spectral data latched to this ASTATUS read. The gain from this status read is required to calculate spectral results if AGC is enabled.

CH0_DATA Register (Address 0x95/0x96)

Figure 69:
CH0_DATA_L Register

Addr: 0x95		CH0_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH0_DATA_L	0	R	CH0 ADC data – low byte

Figure 70:
CH0_DATA_H Register

Addr: 0x96		CH0_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH0_DATA_H	0	R	CH0 ADC data – high byte

CH1_DATA Register (Address 0x97/0x98)

Figure 71:
CH1_DATA_L Register

Addr: 0x97		CH1_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH1_DATA_L	0	R	CH1 ADC data – low byte

Figure 72:
CH1_DATA_H Register

Addr: 0x98		CH1_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH1_DATA_H	0	R	CH1 ADC data – high byte

CH2_DATA Register (Address 0x99/0x9A)

Figure 73:
CH2_DATA_L Register

Addr: 0x99		CH2_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH2_DATA_L	0	R	CH2 ADC data – low byte

Figure 74:
CH2_DATA_H Register

Addr: 0x9A		CH2_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH2_DATA_H	0	R	CH2 ADC data – high byte

CH3_DATA Register (Address 0x9B/0x9C)

Figure 75:
CH3_DATA_L Register

Addr: 0x9B		CH3_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH3_DATA_L	0	R	CH3 ADC data – low byte

Figure 76:
CH3_DATA_H Register

Addr: 0x9C		CH3_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH3_DATA_H	0	R	CH3 ADC data – high byte

CH4_DATA Register (Address 0x9D/0x9E)

Figure 77:
CH4_DATA_L Register

Addr: 0x9D		CH4_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH4_DATA_L	0	R	CH4 ADC data – low byte

Figure 78:
CH4_DATA_H Register

Addr: 0x9E		CH4_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH4_DATA_H	0	R	CH4 ADC data – high byte

CH5_DATA Register (Address 0x9F/0xA0)

Figure 79:
CH5_DATA_L Register

Addr: 0x9F		CH5_DATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH5_DATA_L	0	R	CH5 ADC data – low byte

Figure 80:
CH5_DATA_H Register

Addr: 0xA0		CH5_DATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CH5_DATA_H	0	R	CH5 ADC data – high byte

10.2.8 Miscellaneous Configuration

CFG0 Register (Address 0xA9)

Figure 81:
CFG 0 Register

Addr: 0xA9		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	reserved	0		reserved
5	LOW_POWER	0	RW	**Low Power Idle.** When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.

Addr: 0xA9		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	REG_BANK	0	RW	**Register Bank Access** 0: Register access to register 0x80 and above 1: Register access to register 0x60 to 0x74 Note: Bit needs to be set to access registers 0x60 to 0x74. If registers 0x80 and above needs to be accessed bit needs to be set to "0".
3	reserved	0		reserved
2	WLONG	0	RW	**Trigger Long.** Increases the WTIME setting by a factor of 16.
1:0	reserved	0		reserved

CFG3 Register (Address 0xAC)

Figure 82:
CFG 3 Register

Addr: 0xAC		CFG3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	reserved	0		reserved
4	SAI	0	RW	**Sleep after interrupt.** If set, the oscillator is turned off whenever an interrupt is active. SAI_ACTIVE is set in this event. To activate the oscillator again, clear all interrupts and clear the SAI_ACTIVE bit.
3:0	reserved	0xC		reserved

CFG6 Register (Address 0xAF)

Figure 83:
CFG 6 Register

<table>
<tr><th>Addr: 0xAF</th><th></th><th>CFG6</th><th></th><th colspan="2"></th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">4:3</td><td rowspan="6">SMUX_CMD</td><td rowspan="6">2</td><td rowspan="6">RW</td><td colspan="2">SMUX command.
Selects the SMUX command to execute when setting SMUXEN gets set. Do not change during ongoing SMUX operation.</td></tr>
<tr><td>VALUE</td><td>SMUX_CMD</td></tr>
<tr><td>0</td><td>ROM code initialization of SMUX</td></tr>
<tr><td>1</td><td>Read SMUX configuration to RAM from SMUX chain</td></tr>
<tr><td>2</td><td>Write SMUX configuration from RAM to SMUX chain</td></tr>
<tr><td>3</td><td>Reserved, do not use</td></tr>
</table>

CFG9 Register (Address 0xB2)

Figure 84:
CFG 9 Register

Addr: 0xB2		CFG9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	reserved	0		reserved
6	SIEN_FD	0	RW	**System Interrupt Flicker Detection.** Enables system interrupt when flicker detection status change has occurred.
5	reserved			reserved
4	SIEN_SMUX	0	RW	**System Interrupt SMUX Operation.** Enables system interrupt when SMUX command has finished
3:0	reserved			reserved

PERS Register (Address 0xBD)

Figure 85:
PERS Register

<table>
<tr><th colspan="2">Addr: 0xBD</th><th colspan="4">PERS</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:4</td><td>reserved</td><td>0</td><td></td><td colspan="2">reserved</td></tr>
<tr><td rowspan="11">3:0</td><td rowspan="11">APERS</td><td rowspan="11">0</td><td rowspan="11">RW</td><td colspan="2">Spectral Interrupt Persistence.
Defines a filter for the number of consecutive occurrences that spectral data must remain outside the threshold range between SP_TH_L and SP_TH_H before an interrupt is generated. The spectral data channel used for the persistence filter is set by SP_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.</td></tr>
<tr><td>VALUE</td><td>CHANNEL</td></tr>
<tr><td>0</td><td>Every spectral cycle generates an interrupt</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>3</td><td>3</td></tr>
<tr><td>4</td><td>5</td></tr>
<tr><td>5</td><td>10</td></tr>
<tr><td>…</td><td>5 x (APERS – 3)</td></tr>
<tr><td>14</td><td>55</td></tr>
<tr><td>15</td><td>60</td></tr>
</table>

10.2.9 FIFO Buffer Data and Status

The FIFO buffer is used to poll spectral data with fewer I²C read and write transactions. The FIFO buffer is 256 bytes of RAM containing 128 two-byte datasets. If the FIFO overflows (i.e. 129 datasets before host reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. The Host acquires data by reading addresses: 0xFE – 0xFF. The register address pointer automatically wraps from 0xFF to 0xFE as data are read. Data can be read one byte at a time or in blocks, (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL update for each two-byte entry. If the FIFO continues to be accessed after FIFO_LVL = 0, the device will return 0 for all data. The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO_LVL.

FIFO_MAP Register (Address 0xFC)

Figure 86:
FIFO_MAP Register

Addr: 0xFC		FIFO_MAP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	reserved	0		reserved
6	FIFO_WRITE_CH5_DATA	0	RW	**FIFO write CH5 Data.** If set, CH5 data is written to the FIFO Buffer. (two bytes per sample) Note: If flicker detection is enabled, this bit is ignored. Refer to register 0xD7 for FDEN="1".
5	FIFO_WRITE_CH4_DATA	0	RW	**FIFO write CH4 Data.** If set, CH4 data is written to the FIFO Buffer. (two bytes per sample)
4	FIFO_WRITE_CH3_DATA	0	RW	**FIFO write CH3 Data.** If set, CH3 data is written to the FIFO Buffer. (two bytes per sample)
3	FIFO_WRITE_CH2_DATA	0	RW	**FIFO write CH2 Data.** If set, CH2 data is written to the FIFO Buffer. (two bytes per sample)
2	FIFO_WRITE_CH1_DATA	0	RW	**FIFO write CH1 Data.** If set, CH1 data is written to the FIFO Buffer. (two bytes per sample)
1	FIFO_WRITE_CH0_DATA	0	RW	**FIFO write CH0 Data.** If set, CH0 data is written to the FIFO Buffer. (two bytes per sample)
0	FIFO_WRITE_ASTATUS	0	RW	**FIFO write Status.** If set, ASTATUS (one byte per sample) is written to the FIFO Buffer. In case SP_AGC_ENABLE = 1, ASTATUS should be written to FIFO buffer.

FIFO_CFG0 Register (Address 0xD7)

Figure 87:
FIFO_CFG0 Register

Addr: 0xD7		FIFO_CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FIFO_WRITE_FD	0	R/W	**FIFO write Flicker Detection** If set flicker raw data is written into FIFO (two bytes per sample) Note: This bit is ignored if flicker detection is disabled. Refer to register 0xFC for FDEN=”0”.
6:0	reserved	0100001		Reserved, do not change

FIFO_LVL Register (Address 0xFD)

Figure 88:
FIFO_LVL Register

Addr: 0xFD		FIFO_LVL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_LVL	0	R	**FIFO Buffer Level.** Indicates the number of entries (each are 2 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256byte, the FIFO_LVL range is from 0 entries to 128 entries.

FDATA Register (Address 0xFE and 0xFF)

Figure 89:
FDATA Register

Addr: 0xFE		FDATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FDATA	0	R	FIFO Buffer Data

Figure 90:
FDATA Register

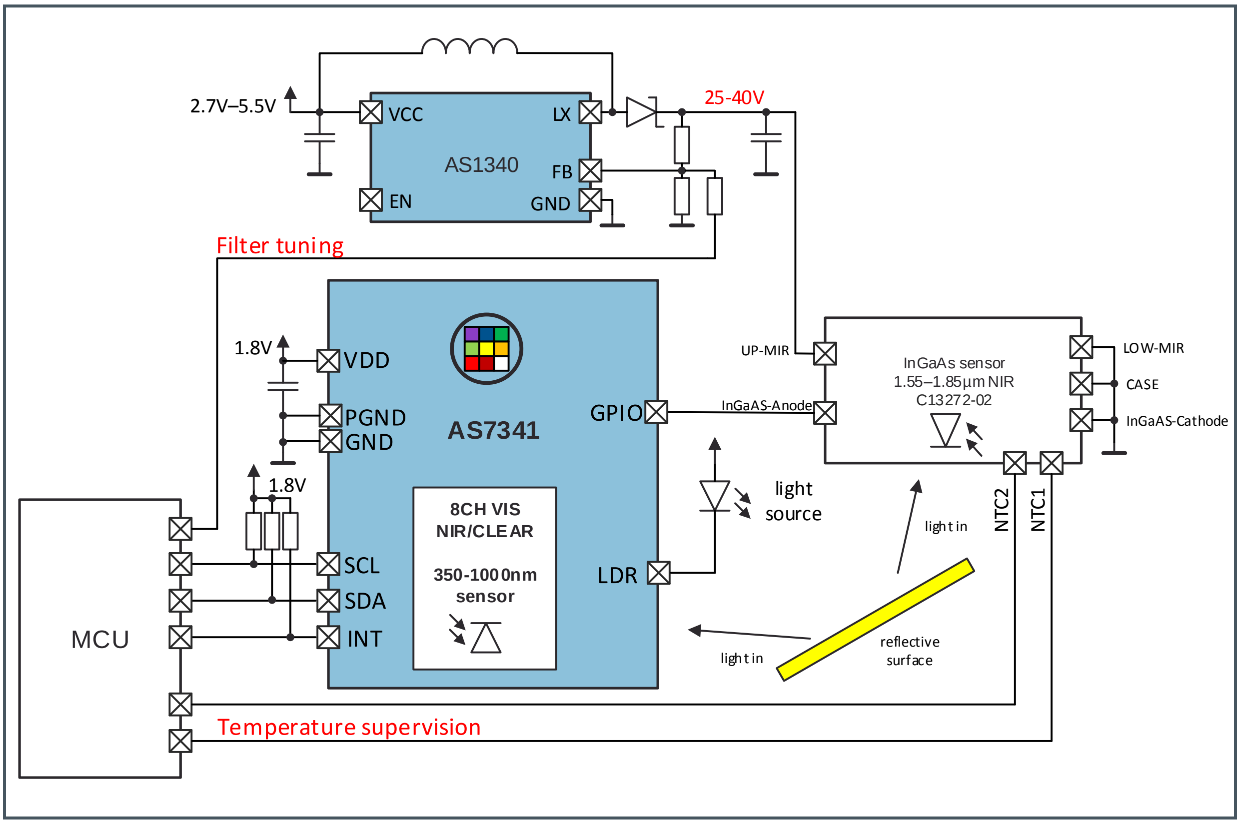
Addr: 0xFF		FDATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:8	FDATA	0	R	FIFO Buffer Data

11 Application Information

Figure 91 shows an example how AS7341 can be utilized to interface to an external InGaAs photodiode. GPIO2 is mapped to an internal ADC.

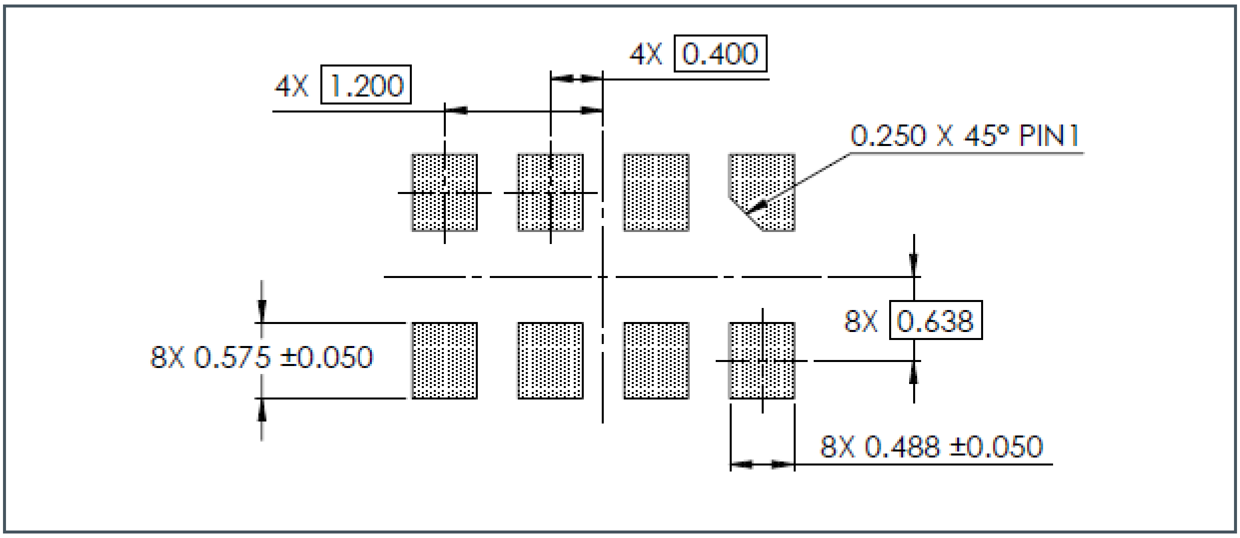
11.1 Schematic

Figure 91:
Application Example with External InGaAs Detector



11.2 PCB Pad Layout

Figure 92:
Recommended PCB Pad Layout

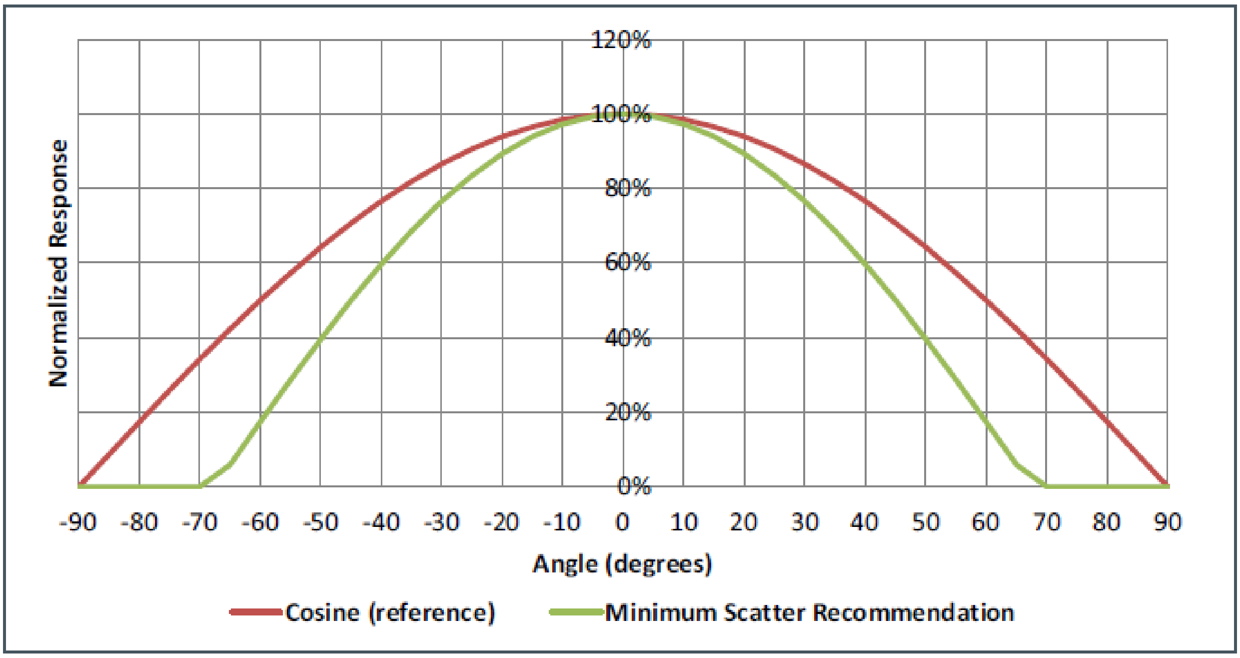


(1) All dimensions are in millimeters.
(2) Dimension tolerances are 0.05mm unless otherwise noted.
(3) This drawing is subject to change without notice.

11.3 Application Optical Requirements

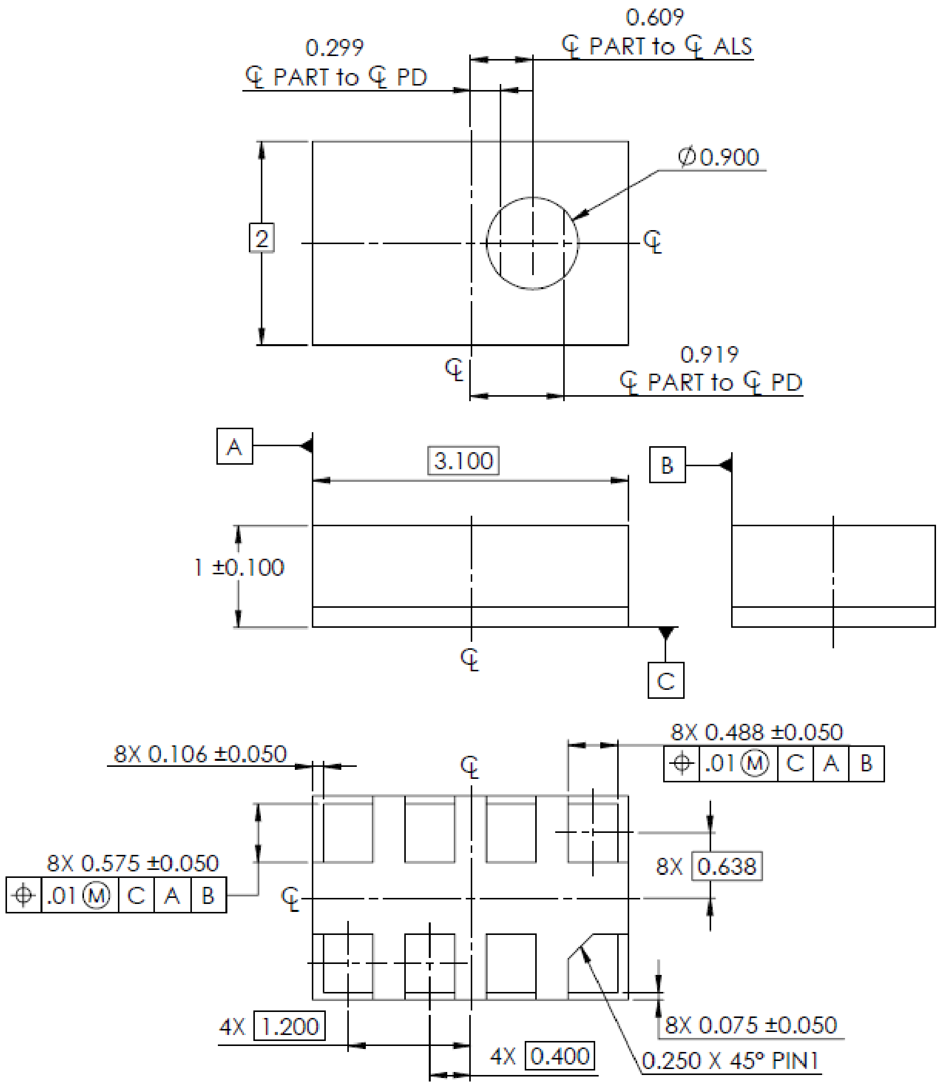
For optimal performance, an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the optical design guide or contact ams.

Figure 93:
Diffuser Characteristics



12 Package Drawings & Markings

Figure 94:
OLGA8 Package Outline Drawing



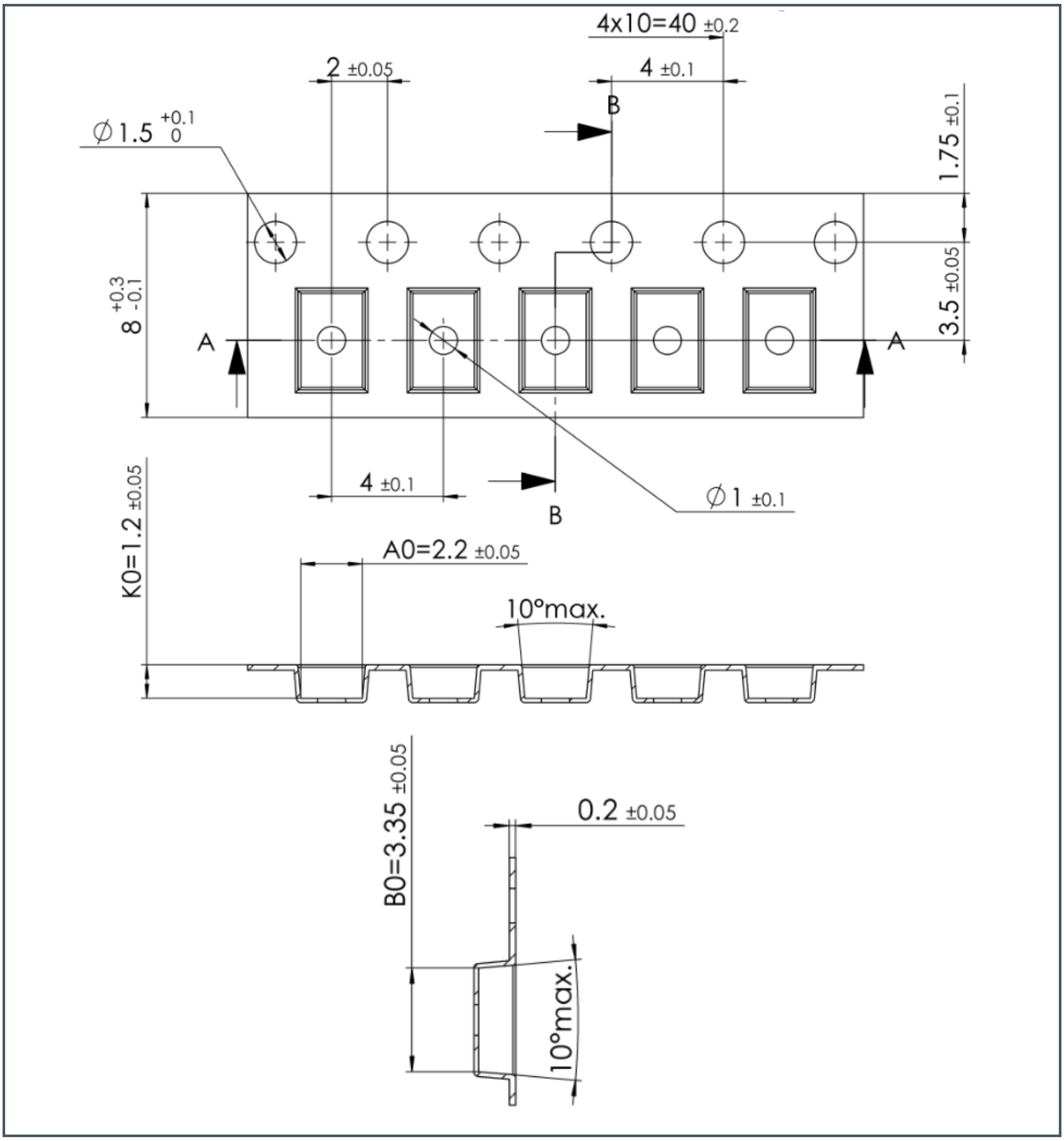
RoHS

Green

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13 Tape & Reel Information

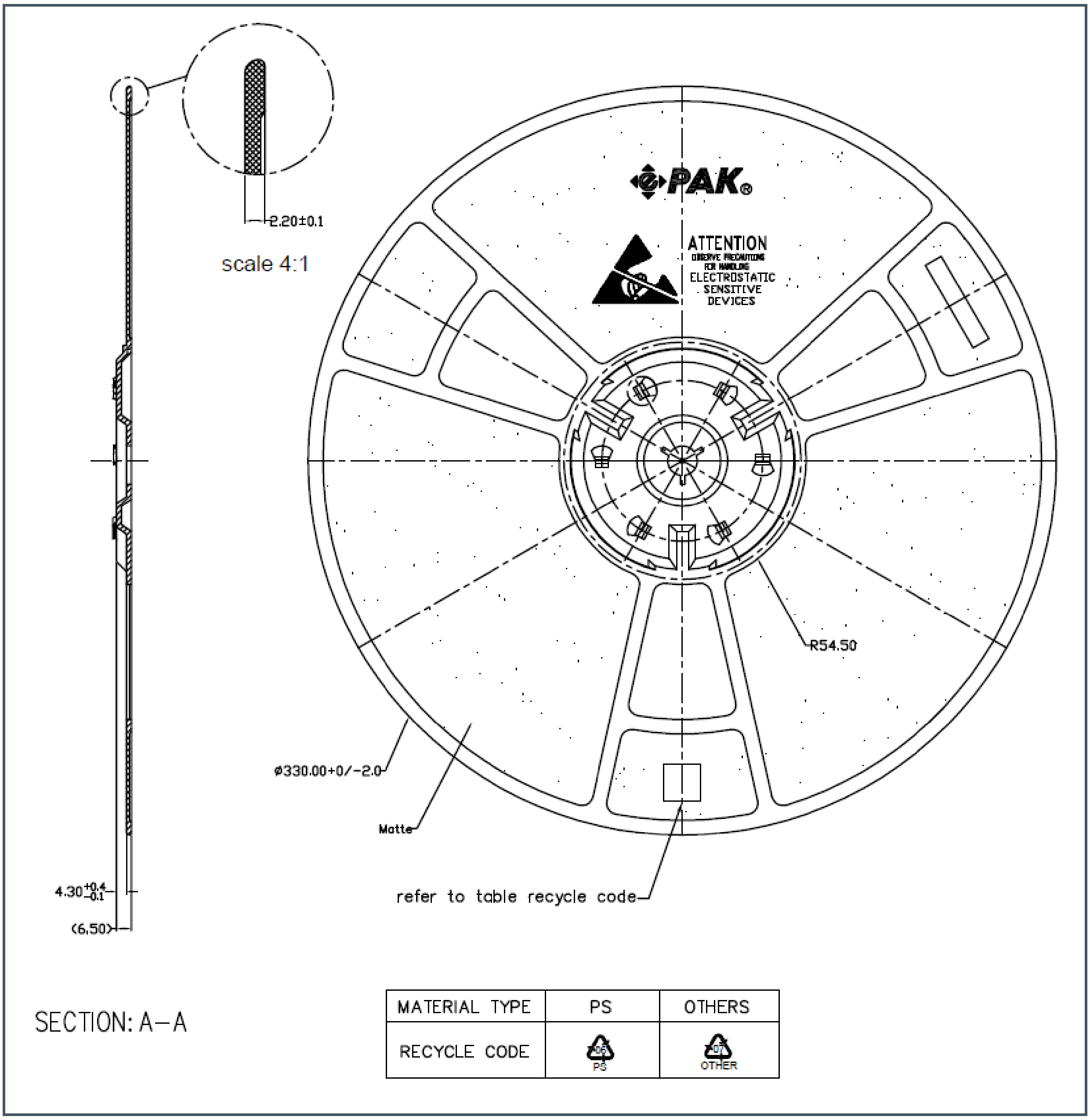
Figure 95:
AS7341 OLGA8 Tape Dimensions



(1) All dimensions are in millimeters. Angles in degrees.

(2) This drawing is subject to change without notice.

**Figure 96:
AS7341 OLGA8 Reel Dimensions**



MATERIAL TYPE	PS	OTHERS
RECYCLE CODE	♳ 06 PS	♳ 07 OTHER

(1) All dimensions are in millimeters. Angles in degrees.

(2) This drawing is subject to change without notice.

14 Soldering & Storage Information

Figure 97:
Solder Reflow Profile Graph

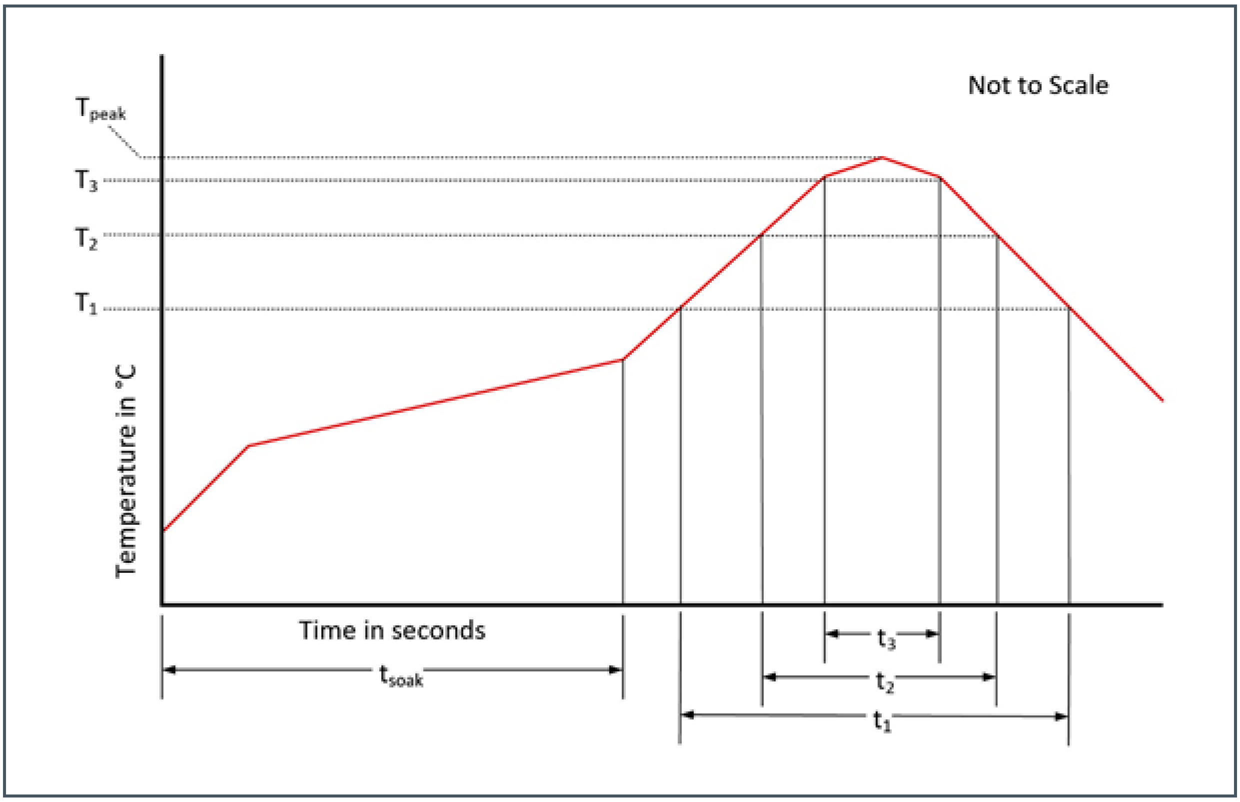


Figure 98:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

14.1 Storage Information

14.1.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

14.1.2 Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

14.1.3 Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

14.1.4 Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

15 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v1-00	Page

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

16 Legal Information

RoHS Compliant & ams Green Statement

RoHS Compliant: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams AG knowledge and belief as of the date that it is provided. ams AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams AG and ams AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Headquarters
ams AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

Please visit our website at www.ams.com
Buy our products or get free samples online at www.ams.com/Products
Technical Support is available at www.ams.com/Technical-Support
Provide feedback about this document at www.ams.com/Document-Feedback
For sales offices, distributors and representatives go to www.ams.com/Contact
For further information and requests, e-mail us at ams_sales@ams.com

MOSCHIP.RU
ВМЕСТЕ МЫ СОЗДАЕМ БУДУЩЕЕ

ПОСТАВКА
ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный
+7 495 668 12 70
info@moschip.ru

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9