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FDS3992

Dual N-Channel PowerTrench® MOSFET 100V, 4.5A, 62m Ω

Features

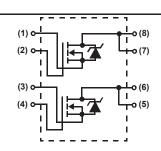
- $r_{DS(ON)} = 54m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 4.5A$
- $Q_q(tot) = 11nC (Typ.), V_{GS} = 10V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)

Formerly developmental type 82745

Applications

- DC/DC converters and Off-Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42V Automotive Load Control
- Electronic Valve Train Systems





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain to Source Voltage	100	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current		
	Continuous ($T_A = 25^{\circ}C$, $V_{GS} = 10V$, $R_{\theta JA} = 50^{\circ}C/W$)	4.5	Α
	Continuous ($T_A = 100$ °C, $V_{GS} = 10V$, $R_{\theta JA} = 50$ °C/W)	2.8	Α
	Pulsed	Figure 4	Α
E _{AS}	Single Pulse Avalanche Energy (Note 1)	167	mJ
	Total Package Power Dissipation	2.5	W
P_{D}	Derate above 25°C	20	mW/°C
T _J , T _{STG}	Operating and Storage Temperature -55 to 150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 10 seconds (Note 3)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	85	°C/W
$R_{\theta,JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W

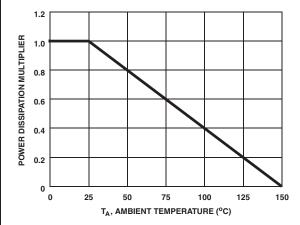
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS3992	FDS3992	SO-8	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100	-	-	V
_		V _{DS} = 80V	-	-	1	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V$ $T_C = 150^{\circ}C$	-	-	250	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20V	-	-	±100	nA
On Chara	cteristics					
V _{GS(TH)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	-	4	V
G3(111)	Ŭ	$I_D = 4.5A, V_{GS} = 10V$	-	0.054	0.062	
		$I_D = 2A$, $V_{GS} = 6V$	-	0.072	0.108	
r _{DS(ON)}	Drain to Source On Resistance	$I_D = 4.5A, V_{GS} = 10V,$		0.407	0.400	Ω
		$T_{\rm C} = 150^{\rm o}{\rm C}$	-	0.107	0.123	
Dynamic	Characteristics					
C _{ISS}	Input Capacitance		_	750	_	pF
C _{OSS}	Output Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$,	_	118	-	pF
C _{RSS}	Reverse Transfer Capacitance	f = 1MHz	_	27	-	pF
Q _{g(TOT)}	Total Gate Charge at 10V	V _{GS} = 0V to 10V	_	11	15	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$ $V_{DD} = 50V$	_	1.4	1.9	nC
Q _{gs}	Gate to Source Gate Charge	$I_{D} = 4.5A$	_	3.5	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau	$I_q = 1.0 \text{mA}$	_	2.1	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		_	2.8	-	nC
-	Characteristics (V _{GS} = 10V)					
t _{ON}	Turn-On Time		_	_	47	ns
t _{d(ON)}	Turn-On Delay Time	\dashv	_	8	-	ns
t _r	Rise Time	$V_{DD} = 50V, I_D = 4.5A$	-	23	_	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 27\Omega$	_	28	_	ns
t _f	Fall Time		-	26	_	ns
t _{OFF}	Turn-Off Time	\neg	-	-	81	ns
					-	
Drain-Sol	urce Diode Characteristics	1 - 454			1.05	17
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 4.5A$	-	-	1.25	V
+	Poverse Pecevery Time	I _{SD} = 2A	-	-	1.0	-
t _{rr}	Reverse Recovery Time	I _{SD} = 4.5A, dI _{SD} /dt= 100A/μs	-	-	48	ns
Q _{RR}	Reverse Recovery Charge	I_{SD} = 4.5A, dI_{SD} / dt = 100A/ μ s	-	-	65	nC

<sup>Notes:
1: E_{AS} of 167mJ is based on starting T_J = 25°C, L = 37mH, I_{AS} = 3A. 100% test at L = 1mH, I_{AS} = 10.3A.
2: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design while R_{0,CA} is determined by the user's board design.
3: R_{0,JA} is measured with 1.0 in² copper on FR-4 board</sup>





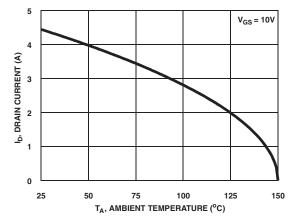


Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs
Ambient Temperature

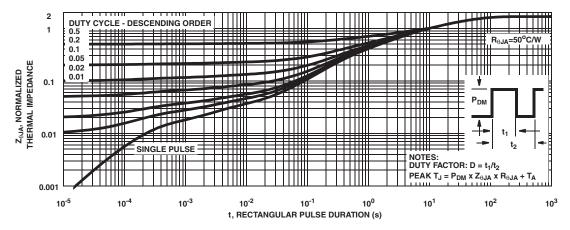


Figure 3. Normalized Maximum Transient Thermal Impedance

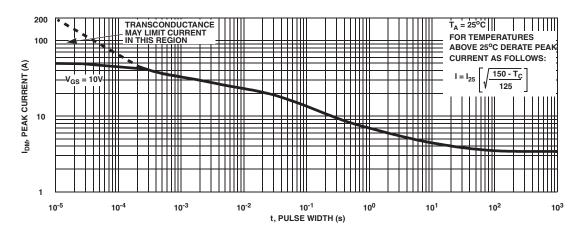
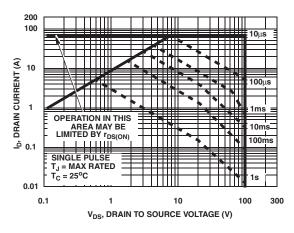


Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted



The standing $T_J = 25^{\circ}C$ STARTING $T_J = 25^{\circ}C$ STARTING $T_J = 150^{\circ}C$ If R = 0 $t_{AV} = (L)(t_{AS})/(1.3^{\circ}RATED\ BV_{DSS} - V_{DD})$ 1

0.01

0.1

1 10

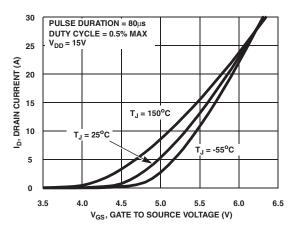
100 t_{AV} Time in Avalanche (ms)

Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability



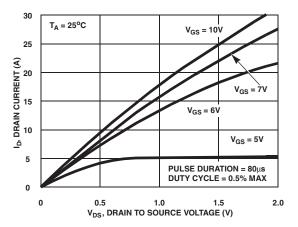
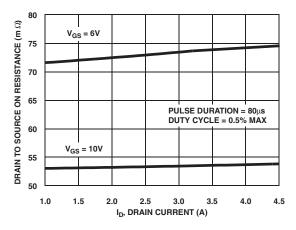


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



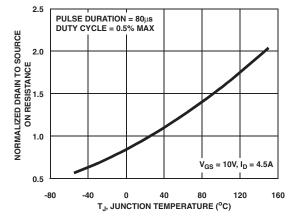


Figure 9. Drain to Source On Resistance vs Drain Current

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

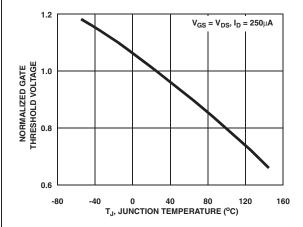


Figure 11. Normalized Gate Threshold Voltage vs
Junction Temperature

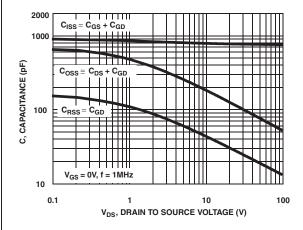


Figure 13. Capacitance vs Drain to Source Voltage

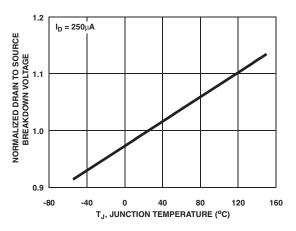


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

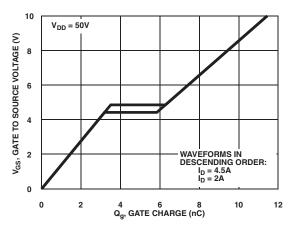
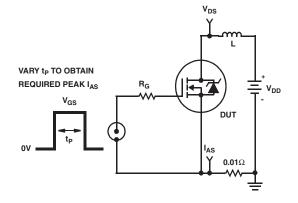


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms



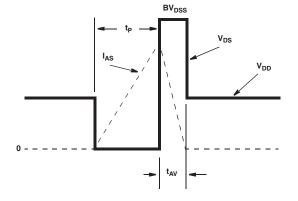


Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

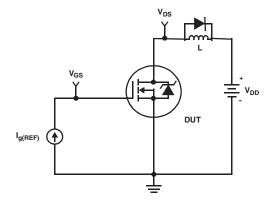


Figure 17. Gate Charge Test Circuit

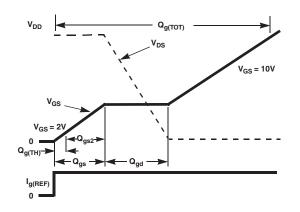


Figure 18. Gate Charge Waveforms

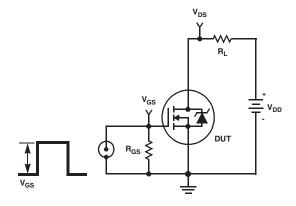


Figure 19. Switching Time Test Circuit

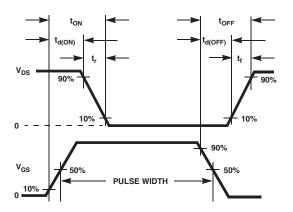


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- The number of copper layers and the thickness of the hoard
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized

maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + Area}$$
 (EQ. 2)

The transient thermal impedance $(Z_{\theta JA})$ is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

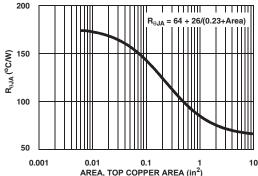


Figure 21. Thermal Resistance vs Mounting Pad Area

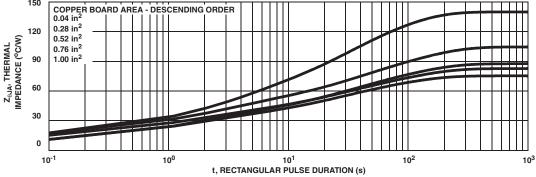
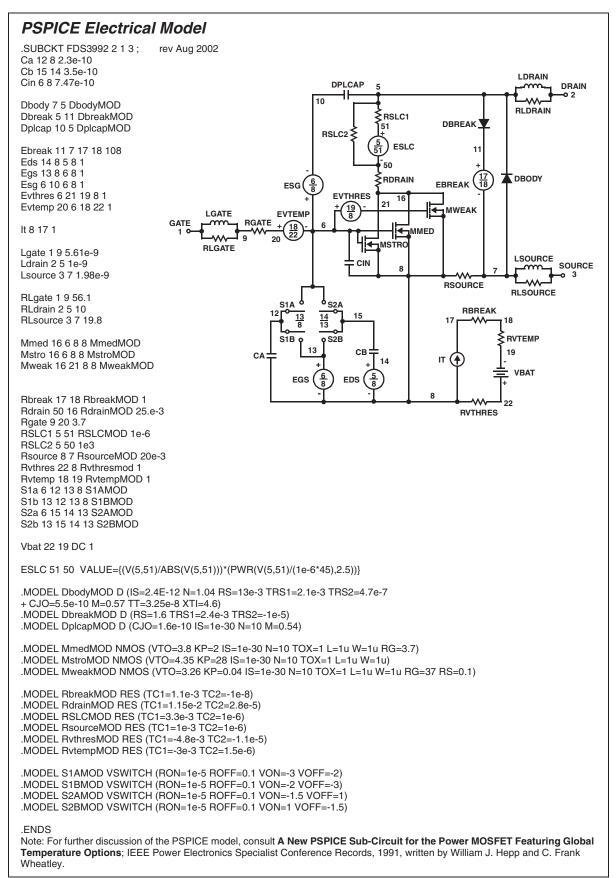


Figure 22. Thermal Impedance vs Mounting Pad Area



SABER Electrical Model REV Aug 2002 template FDS3992 n2,n1,n3 electrical n2,n1,n3 var i iscl dp..model dbodymod = (isl=2.4e-12,nl=1.04,rs=13e-3,trs1=2.1e-3,trs2=4.7e-7,cjo=5.5e-10,m=0.57,tt=3.25e-8,xti=4.6) dp..model dbreakmod = (rs=1.6,trs1=2.4e-3,trs2=-1.0e-5) dp..model dplcapmod = (cjo=1.6e-10,isl=10e-30,nl=10,m=0.54) $m..model mmedmod = (type=_n,vto=3.8,kp=2.0,is=1e-30, tox=1)$ m..model mstrongmod = (type=_n,vto=4.35,kp=28,is=1e-30, tox=1) m..model mweakmod = (type=_n,vto=3.26,kp=0.04,is=1e-30, tox=1,rs=0.1) sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-3.0,voff=-2.0) LDRAIN sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2.0,voff=-3.0) DPLCAP DRAIN sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1.5,voff=1.0) 10 sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=1.0,voff=-1.5) **BLDBAIN** c.ca n12 n8 = 2.3e-10ERSLC1 c.cb n15 n14 = 3.5e-10 51 RSLC2 ₹ c.cin n6 n8 = 7.47e-10ISCL dp.dbody n7 n5 = model=dbodymod DBREAK 50 dp.dbreak n5 n11 = model=dbreakmod RDRAIN <u>6</u> 8 dp.dplcap n10 n5 = model=dplcapmod ESG (11 DBODY **EVTHRES** spe.ebreak n11 n7 n17 n18 = 108 19 8 MWEAK LGATE EVTEMP spe.eds n14 n8 n5 n8 = 1 **RGATE** ММЕD 18 22 EBREAK spe.egs n13 n8 n6 n8 = 1 20 MSTRO spe.esg n6 n10 n6 n8 = 1 RLGATE spe.evthres n6 n21 n19 n8 = 1 LSOURCE spe.evtemp n20 n6 n18 n22 = 1 CIN SOURCE 8 RSOURCE i.it n8 n17 = 1RLSOURCE I.lgate n1 n9 = 5.61e-9RBREAK <u>13</u> 8 <u>14</u> 13 I.ldrain n2 n5 = 1e-917 18 I.Isource n3 n7 = 1.98e-9**₹**RVTEMP o S2B 13 CB 19 res.rlgate n1 n9 = 56.1 CA IT res.rldrain n2 n5 = 10 VBAT res.rlsource n3 n7 = 19.8 EGS **EDS** m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u 22 m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u **RVTHRES** m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=1.1e-3,tc2=-1e-8 res.rdrain n50 n16 = 25e-3, tc1=1.15e-2,tc2=2.8e-5 res.rgate n9 n20 = 3.7res.rslc1 n5 n51 = 1e-6, tc1=3.3e-3,tc2=1e-6 res.rslc2 n5 n50 = 1e3res.rsource n8 n7 = 20e-3, tc1=1e-3,tc2=1e-6 res.rvthres n22 n8 = 1, tc1=-4.8e-3,tc2=-1.1e-5 res.rvtemp n18 n19 = 1. tc1=-3e-3.tc2=1.5e-6

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/45))** 2.5))

}
```

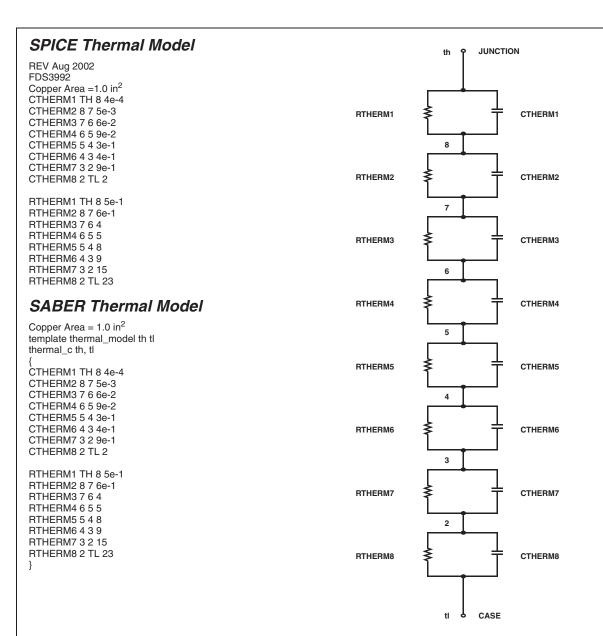


TABLE 1. THERMAL MODELS

COMPONANT	0.04 in ²	0.28 in ²	0.52 in ²	0.76 in ²	1.0 in ²
CTHERM6	3.2e-1	3.5e-1	4.0e-1	4.0e-1	4.0e-1
CTHERM7	8.5e-1	9.0e-1	9.0e-1	9.0e-1	9.0e-1
CTHERM8	0.3	1.8	2.0	2.0	2.0
RTHERM6	24	18	12	10	9
RTHERM7	36	21	18	16	15
RTHERM8	53	37	30	28	23





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