

74LV4053

Triple single-pole double-throw analog switch

Rev. 6 — 17 March 2016

Product data sheet

1. General description

The 74LV4053 is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. It is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC4053 and 74HCT4053. Each switch has a digital select input (S_n), two independent inputs/outputs ($nY0$ and $nY1$) and a common input/output (nZ). All three switches share an enable input ($\overline{E}$). A HIGH on $\overline{E}$ causes all switches into the high-impedance OFF-state, independent of S_n .

V_{CC} and GND are the supply voltage connections for the digital control inputs (S_n and $\overline{E}$). The V_{CC} to GND range is 1 V to 6 V. The analog inputs/outputs ($nY0$, $nY1$ and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2. Features and benefits

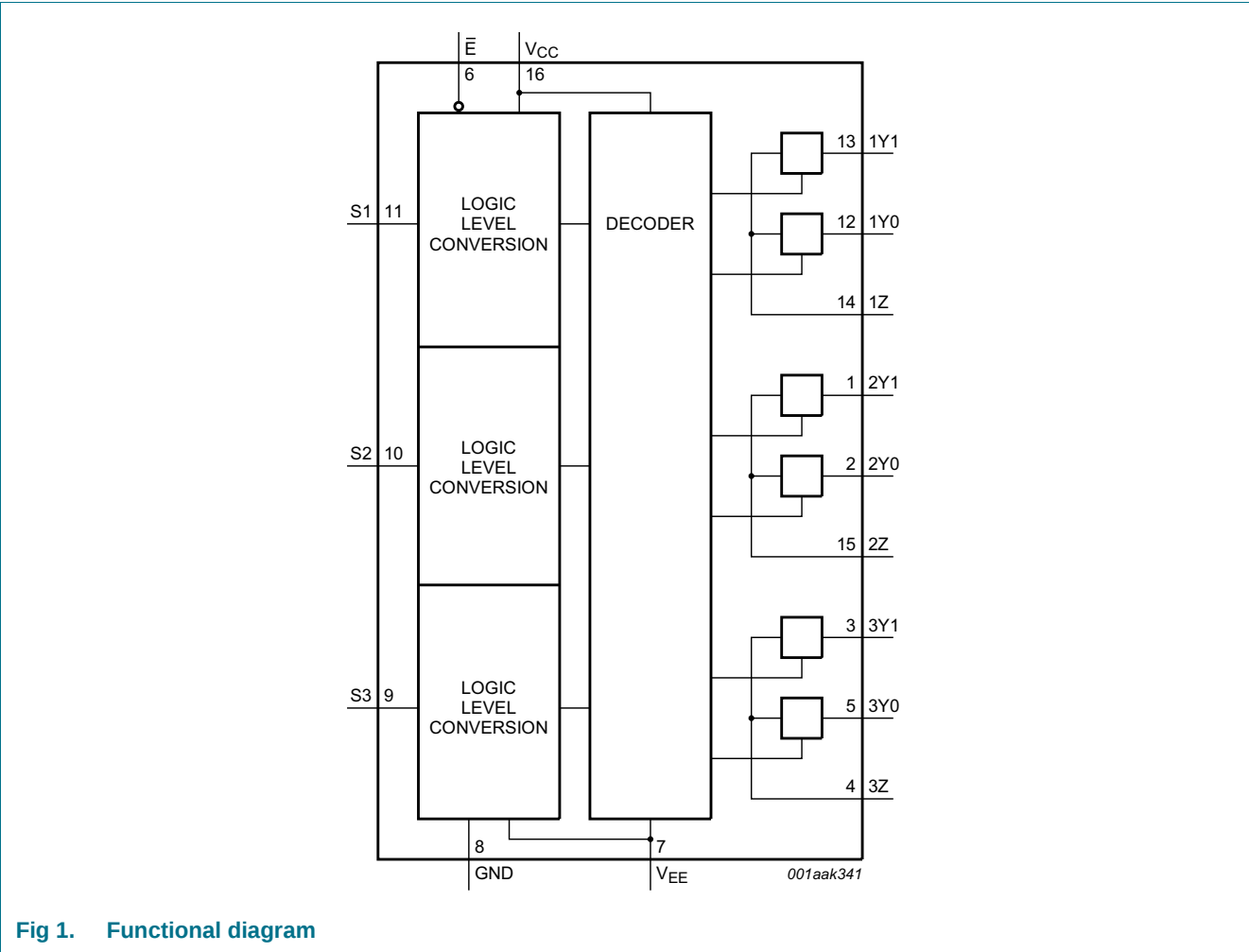
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low ON resistance:
 - ◆ 180 Ω (typical) at $V_{CC} - V_{EE} = 2.0$ V
 - ◆ 100 Ω (typical) at $V_{CC} - V_{EE} = 3.0$ V
 - ◆ 75 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
- Logic level translation:
 - ◆ To enable 3 V logic to communicate with ± 3 V analog signals
- Typical 'break before make' built in
- ESD protection:
 - ◆ HBM JESD22-A114-C exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

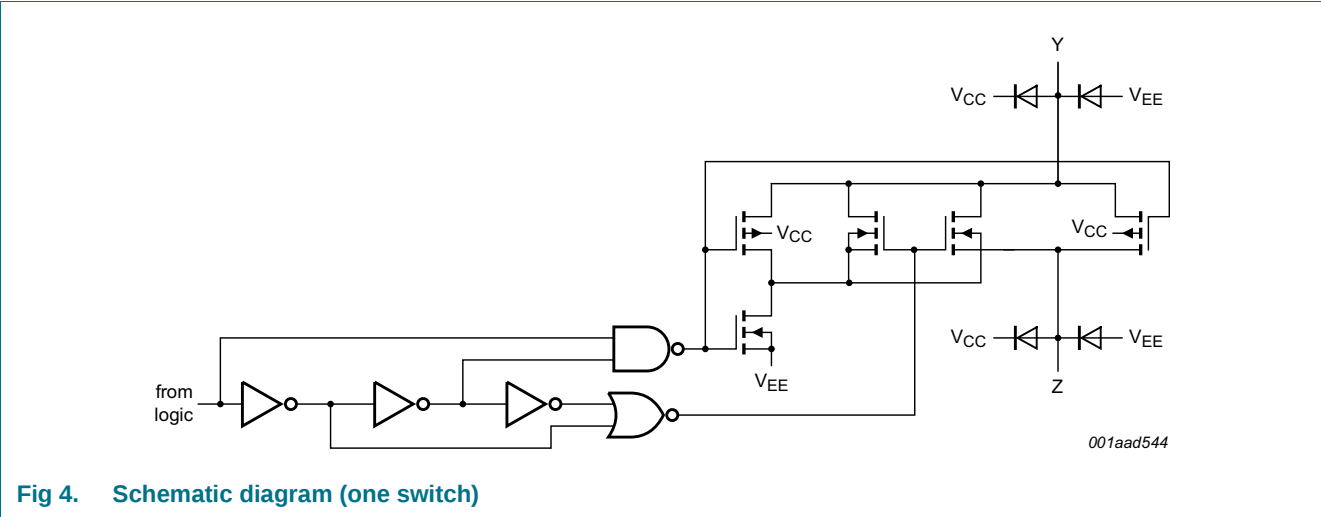
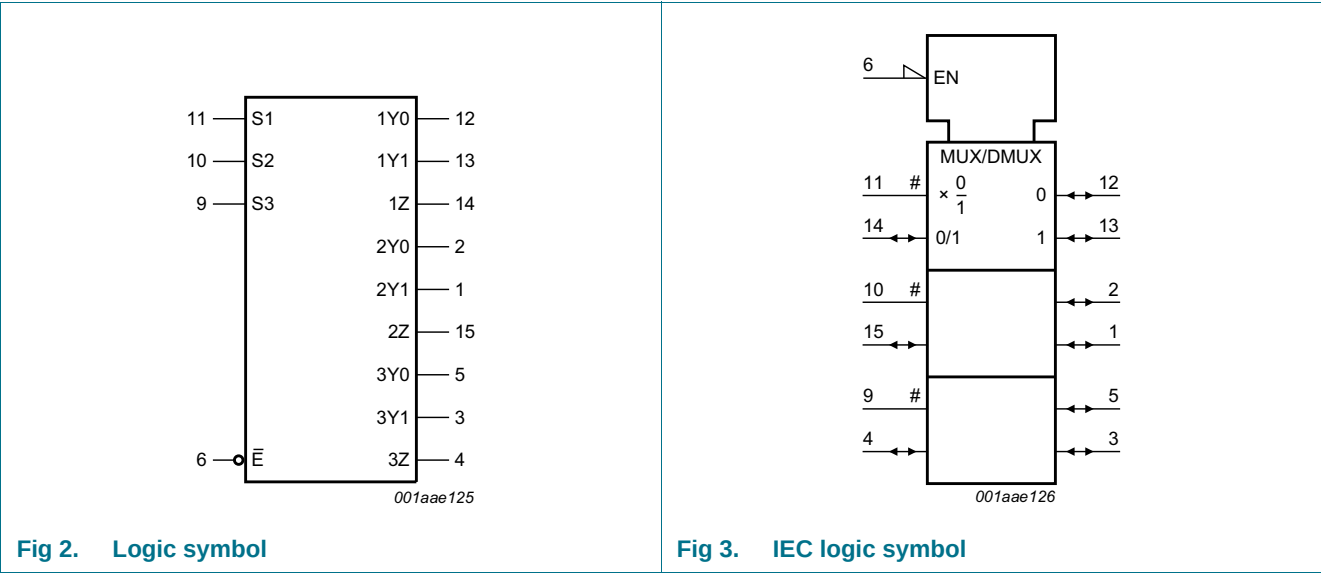
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4053D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4053DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4053PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV4053BQ	–40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

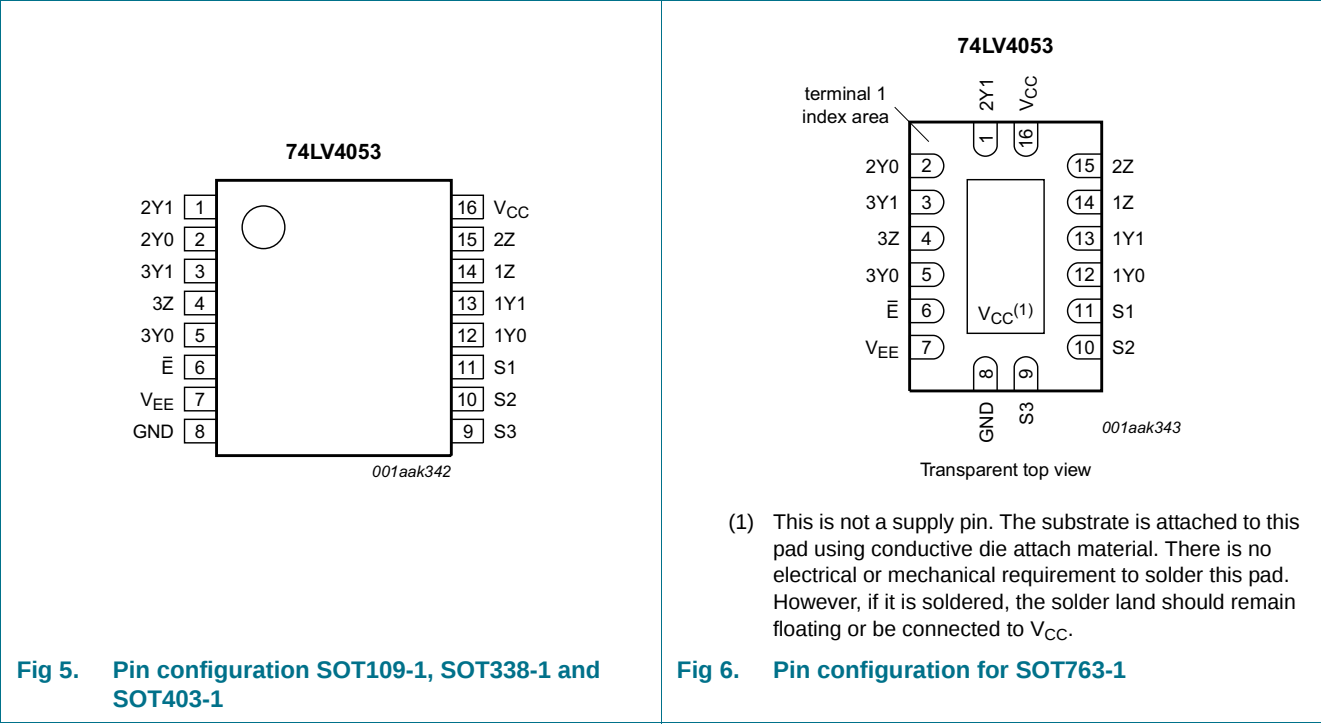
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\bar{E}$	6	enable input (active LOW)
V_{EE}	7	supply voltage
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
1Y0, 2Y0, 3Y0	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	14, 15, 4	common output or input
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table [\[1\]](#)

Inputs		Channel on
$\overline{E}$	Sn	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [2]	-	± 20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5$ V or $V_{SW} > V_{CC} + 0.5$ V [2]	-	± 20	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current [2]	-	± 25	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]			
		DIP16 package	-	750	mW
		SO16 package	-	500	mW
		TSSOP16 package	-	500	mW
		DHVQFN16 package	-	500	mW

- [1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE} .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
 For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage	see Figure 7	1	3.3	6	V
V _I	input voltage		0	-	V _{CC}	V
V _{SW}	switch voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	−40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to 6.0 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

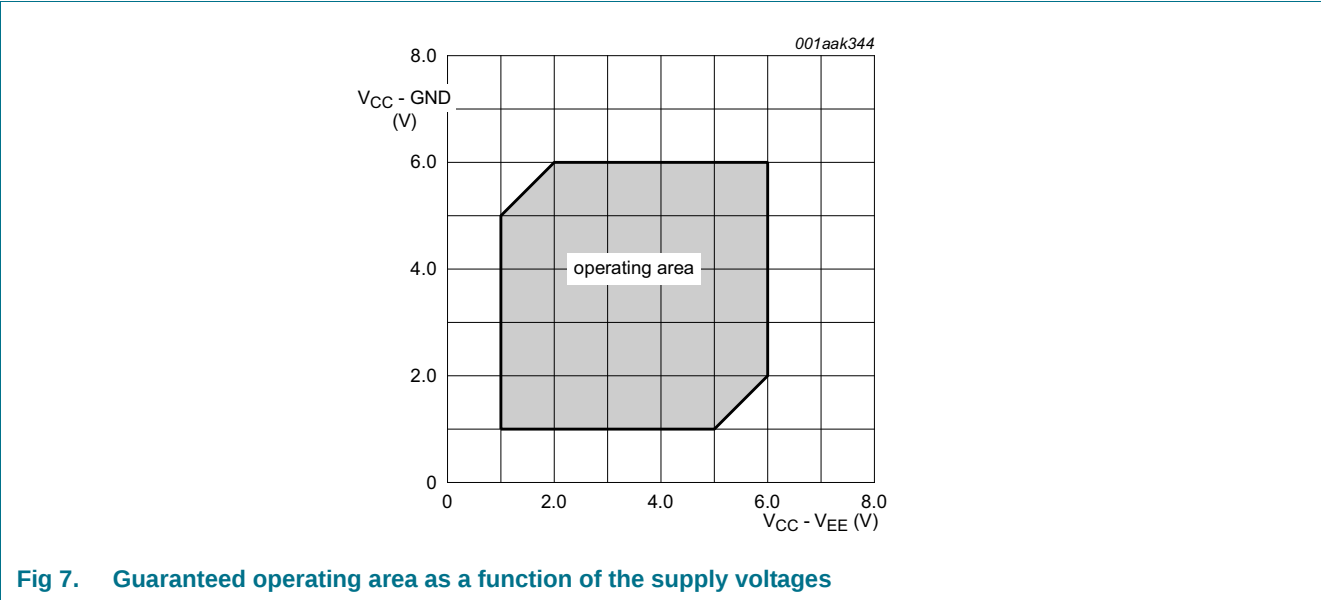


Fig 7. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V	3.15	-	-	3.15	-	V
		V _{CC} = 6.0 V	4.20	-	-	4.20	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V	-	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.80	-	1.80	V
I _I	input leakage current	V _I = V _{CC} or GND						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(OFF)}	OFF-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 8						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; see Figure 9						
		V _{CC} = 3.6 V	-	-	1.0	-	1.0	μA
		V _{CC} = 6.0 V	-	-	2.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A						
		V _{CC} = 3.6 V	-	-	20	-	40	μA
		V _{CC} = 6.0 V	-	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} – 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{SW}	switch capacitance	independent pins nYn	-	5	-	-	-	pF
		common pins nZ	-	8	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

9.1 Test circuits

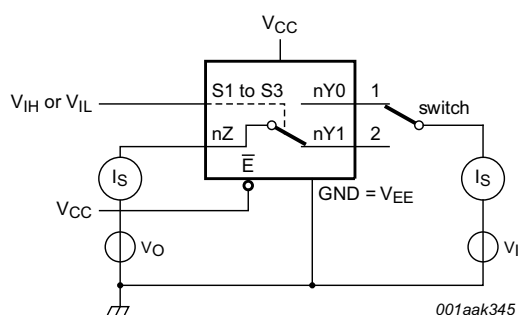

$$V_I = V_{CC} \text{ or } V_{EE} \text{ and } V_O = V_{EE} \text{ or } V_{CC}.$$

Fig 8. Test circuit for measuring OFF-state leakage current

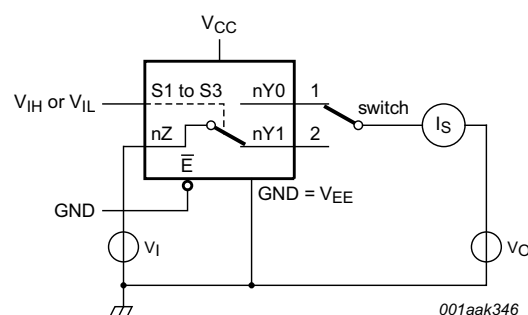

$$V_I = V_{CC} \text{ or } V_{EE} \text{ and } V_O = \text{open circuit.}$$

Fig 9. Test circuit for measuring ON-state leakage current

9.2 ON resistance

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 10](#) and [Figure 11](#).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = 0 V to V _{CC} − V _{EE}						
		V _{CC} = 1.2 V; I _{SW} = 100 μA ^[2]	-	-	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 μA	-	180	365	-	435	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 μA	-	115	225	-	270	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA	-	100	200	-	245	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 μA	-	75	150	-	180	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 μA	-	70	140	-	165	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = 0 V to V _{CC} − V _{EE}						
		V _{CC} = 1.2 V; I _{SW} = 100 μA ^[2]	-	-	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 μA	-	5	-	-	-	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 μA	-	4	-	-	-	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA	-	4	-	-	-	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 μA	-	3	-	-	-	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 μA	-	2	-	-	-	Ω

Table 7. ON resistance ...continued

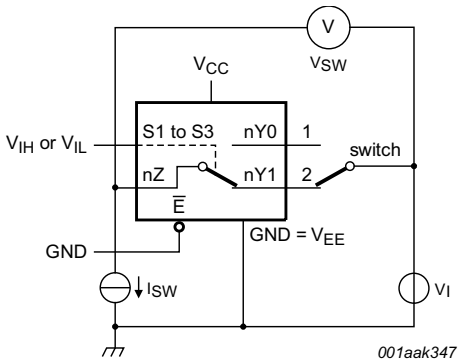
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 10](#) and [Figure 11](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(rail)}	ON resistance (rail)	V _I = GND						
		V _{CC} = 1.2 V; I _{SW} = 100 µA ^[2]	-	250	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA	-	120	280	-	325	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA	-	75	170	-	195	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA	-	70	155	-	180	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA	-	50	120	-	135	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA	-	45	105	-	120	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = V _{CC} – V _{EE}						
		V _{CC} = 1.2 V; I _{SW} = 100 µA ^[2]	-	350	-	-	-	Ω
		V _{CC} = 2.0 V; I _{SW} = 1000 µA	-	170	340	-	400	Ω
		V _{CC} = 2.7 V; I _{SW} = 1000 µA	-	105	210	-	250	Ω
		V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 µA	-	95	190	-	225	Ω
		V _{CC} = 4.5 V; I _{SW} = 1000 µA	-	70	140	-	165	Ω
		V _{CC} = 6.0 V; I _{SW} = 1000 µA	-	65	125	-	150	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

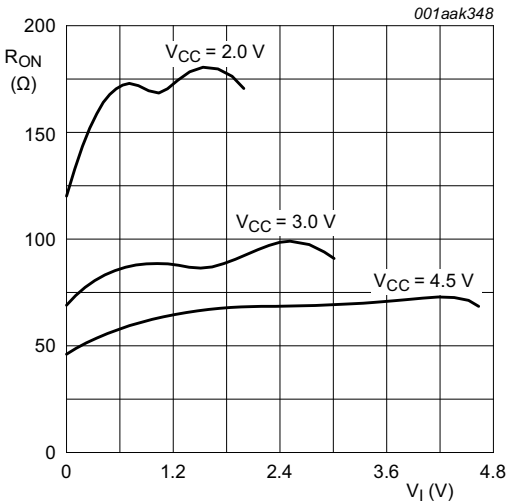
[2] When supply voltages (V_{CC} – V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3 On resistance waveform and test circuit



$R_{ON} = V_{SW} / I_{SW}$

Fig 10. Test circuit for measuring R_{ON}



$V_i = 0\text{ V to }V_{CC} - V_{EE}$

Fig 11. Typical R_{ON} as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nYn, nZ to nZ, nYn; see Figure 12 ^[2]						
		V _{CC} = 1.2 V	-	25	-	-	-	ns
		V _{CC} = 2.0 V	-	9	17	-	20	ns
		V _{CC} = 2.7 V	-	6	13	-	15	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	5	10	-	12	ns
		V _{CC} = 4.5 V	-	4	9	-	10	ns
		V _{CC} = 6.0 V	-	3	7	-	8	ns
t _{en}	enable time	$\overline{E}$ to nYn, nZ; see Figure 13 ^[2]						
		V _{CC} = 1.2 V	-	100	-	-	-	ns
		V _{CC} = 2.0 V	-	34	65	-	77	ns
		V _{CC} = 2.7 V	-	25	48	-	56	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	16	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	19	38	-	45	ns
		V _{CC} = 4.5 V	-	17	32	-	38	ns
		V _{CC} = 6.0 V	-	13	25	-	29	ns
		Sn to nYn, nZ; see Figure 13 ^[2]						
		V _{CC} = 1.2 V	-	125	-	-	-	ns
		V _{CC} = 2.0 V	-	43	82	-	97	ns
		V _{CC} = 2.7 V	-	31	60	-	71	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	20	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	24	48	-	57	ns
		V _{CC} = 4.5 V	-	21	41	-	48	ns
		V _{CC} = 6.0 V	-	16	31	-	37	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{dis}	disable time	$\overline{E}$ to nYn, nZ; see Figure 13 ^[2]						
		V _{CC} = 1.2 V	-	95	-	-	-	ns
		V _{CC} = 2.0 V	-	34	61	-	73	ns
		V _{CC} = 2.7 V	-	26	46	-	54	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	17	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	20	37	-	44	ns
		V _{CC} = 4.5 V	-	18	32	-	38	ns
		V _{CC} = 6.0 V	-	15	25	-	30	ns
		Sn to nYn, nZ; see Figure 13 ^[2]						
		V _{CC} = 1.2 V	-	90	-	-	-	ns
		V _{CC} = 2.0 V	-	32	59	-	70	ns
		V _{CC} = 2.7 V	-	24	44	-	52	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF ^[3]	-	16	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	-	19	36	-	42	ns
		V _{CC} = 4.5 V	-	17	31	-	36	ns
		V _{CC} = 6.0 V	-	14	24	-	28	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; ^[4] V _I = GND to V _{CC}	-	36	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

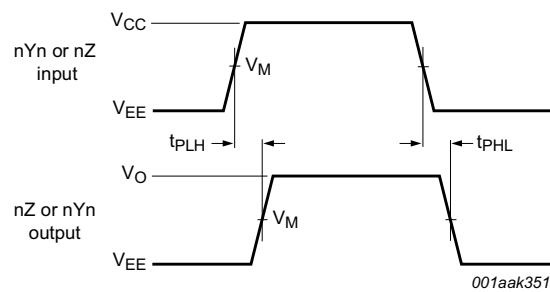
C_{SW} = maximum switch capacitance in pF;

V_{CC} = supply voltage in Volts

N = number of inputs switching

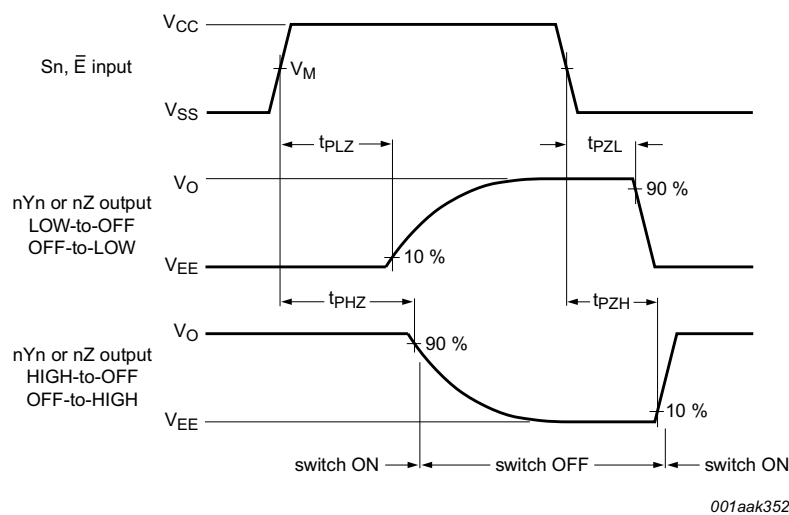
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1 Waveforms



Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 12. Propagation delay input (nYn, nZ) to output (nZ, nYn)

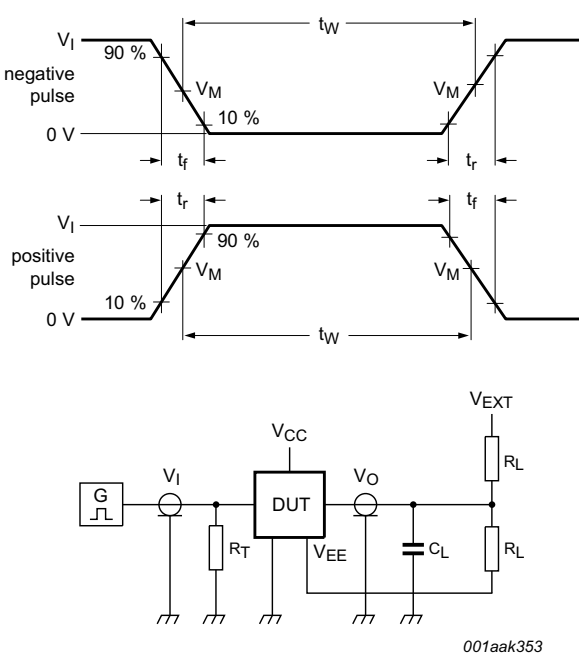


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 13. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
> 3.6 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 14. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$
> 3.6 V	V_{CC}	≤ 6 ns	50 pF	1 k Ω	open	V_{EE}	$2V_{CC}$

10.2 Additional dynamic parameters

Table 11. Additional dynamic characteristics

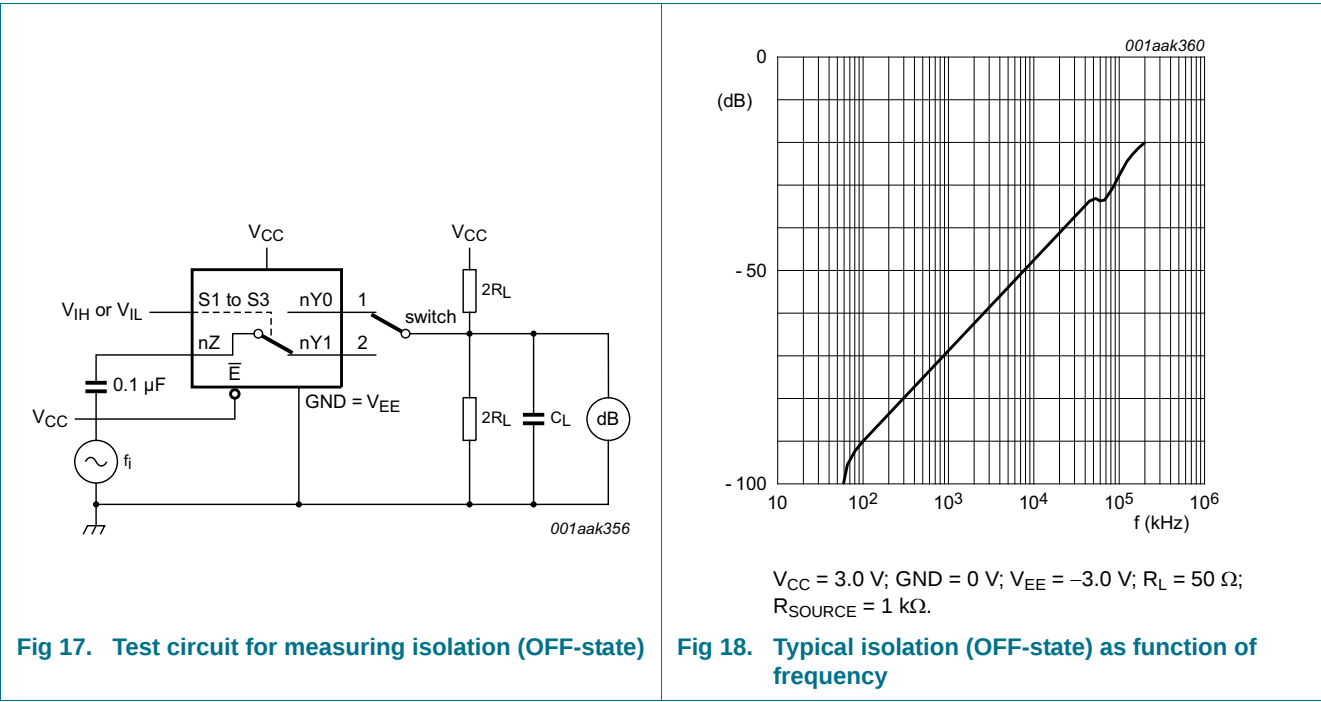
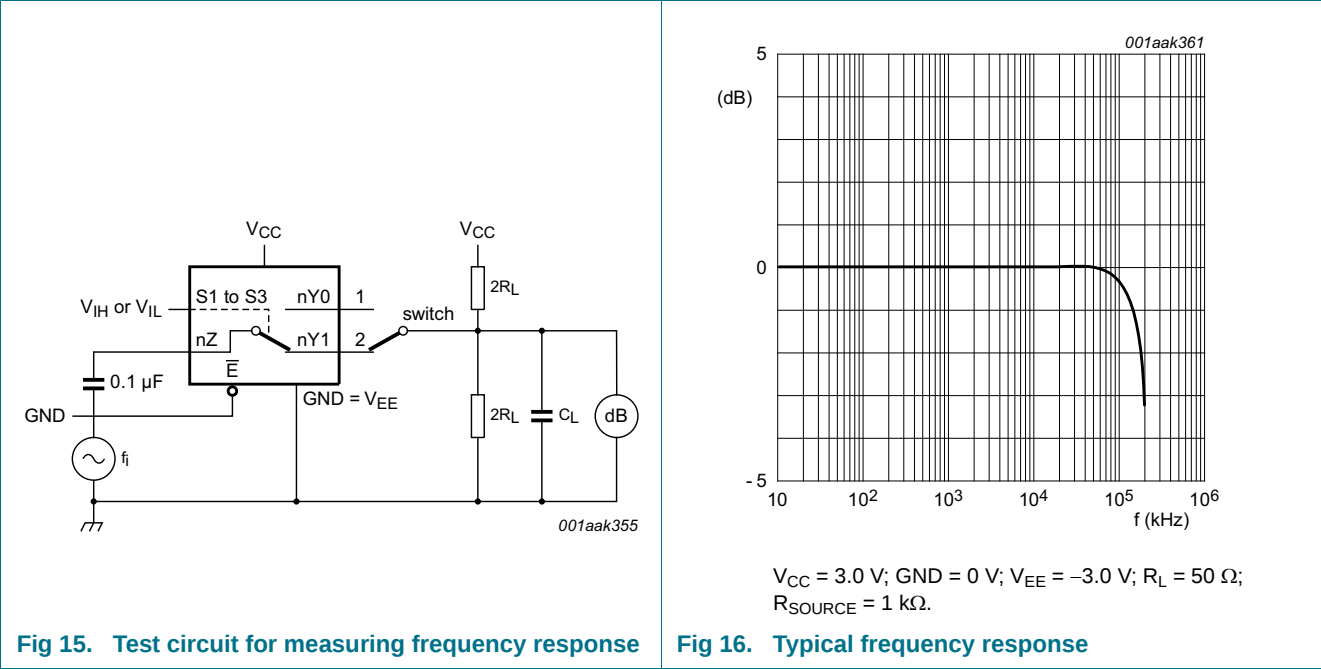
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1$ kHz; $C_L = 50$ pF; $R_L = 10$ k Ω ; see Figure 19				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	0.8	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	0.4	-	%
		$f_i = 10$ kHz; $C_L = 50$ pF; $R_L = 10$ k Ω ; see Figure 19				
		$V_{CC} = 3.0$ V; $V_I = 2.75$ V (p-p)	-	2.4	-	%
		$V_{CC} = 6.0$ V; $V_I = 5.5$ V (p-p)	-	1.2	-	%
$f_{(-3dB)}$	–3 dB frequency response	$C_L = 50$ pF; $R_L = 50$ Ω ; see Figure 15 ^[1]				
		$V_{CC} = 3.0$ V	-	180	-	MHz
		$V_{CC} = 6.0$ V	-	200	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ Ω ; see Figure 17 ^[2]				
		$V_{CC} = 3.0$ V	-	–50	-	dB
		$V_{CC} = 6.0$ V	-	–50	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; ^[2] $f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ Ω ; see Figure 20				
		$V_{CC} = 3.0$ V	-	0.11	-	V
		$V_{CC} = 6.0$ V	-	0.12	-	V
Xtalk	crosstalk	between switches; $f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 600$ Ω ; see Figure 21				
		$V_{CC} = 3.0$ V	-	–60	-	dB
		$V_{CC} = 6.0$ V	-	–60	-	dB

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).

[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.2.1 Test circuits



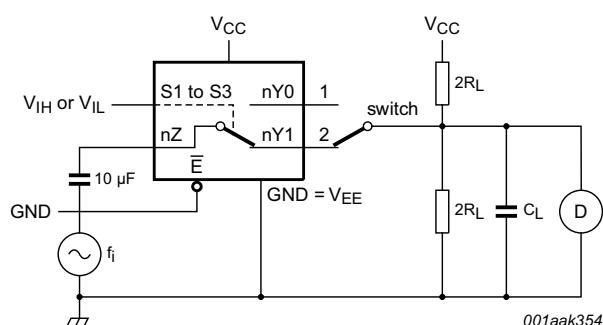
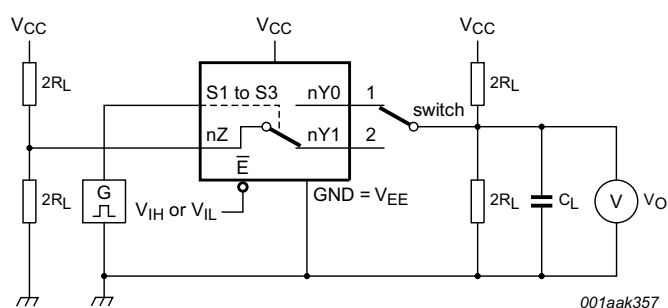
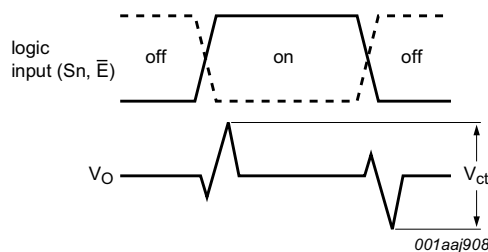


Fig 19. Test circuit for measuring total harmonic distortion



a. Test circuit



b. Input and output pulse definitions

V_i may be connected to S_n or $\bar{E}$.

Fig 20. Test circuit for measuring crosstalk voltage between digital inputs and switch

The circuit diagram shows a chain of three CMOS inverters. The first inverter has its input connected to a signal source \$V_{IH}\$ or \$V_{IL}\$ through a resistor \$2R_L\$. Its output is connected to the input of the second inverter through a series combination of a resistor \$2R_L\$, a voltage source \$V_O\$, a capacitor \$C_L\$, and a delay element \$dB\$. The second inverter's output is connected to the input of the third inverter through a resistor \$R_L\$ and a voltage source \$V_I\$. All inverters have their non-inverting inputs connected to ground (\$GND = V_{EE}\$). Each inverter's supply voltage is \$V_{CC}\$. Parasitic capacitors \$nZ\$ are shown at the input of the second inverter, and parasitic capacitances \$nY0\$ and \$nY1\$ are indicated near the internal nodes of the second inverter. The output of the third inverter is connected to ground through a resistor \$2R_L\$. The identifier '001aak359' is present in the bottom right corner.

Fig 21. Test circuit for measuring crosstalk between switches

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

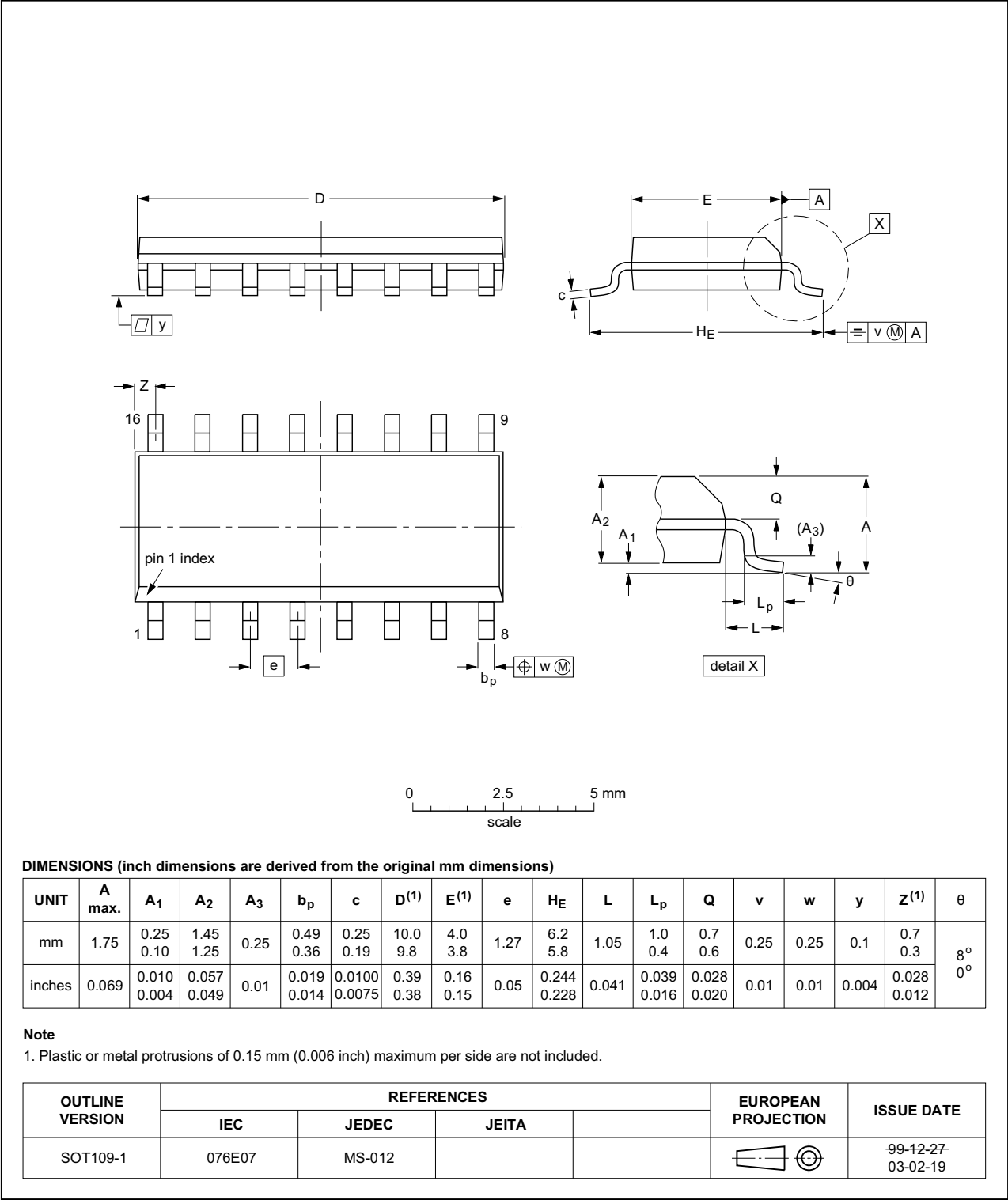


Fig 22. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

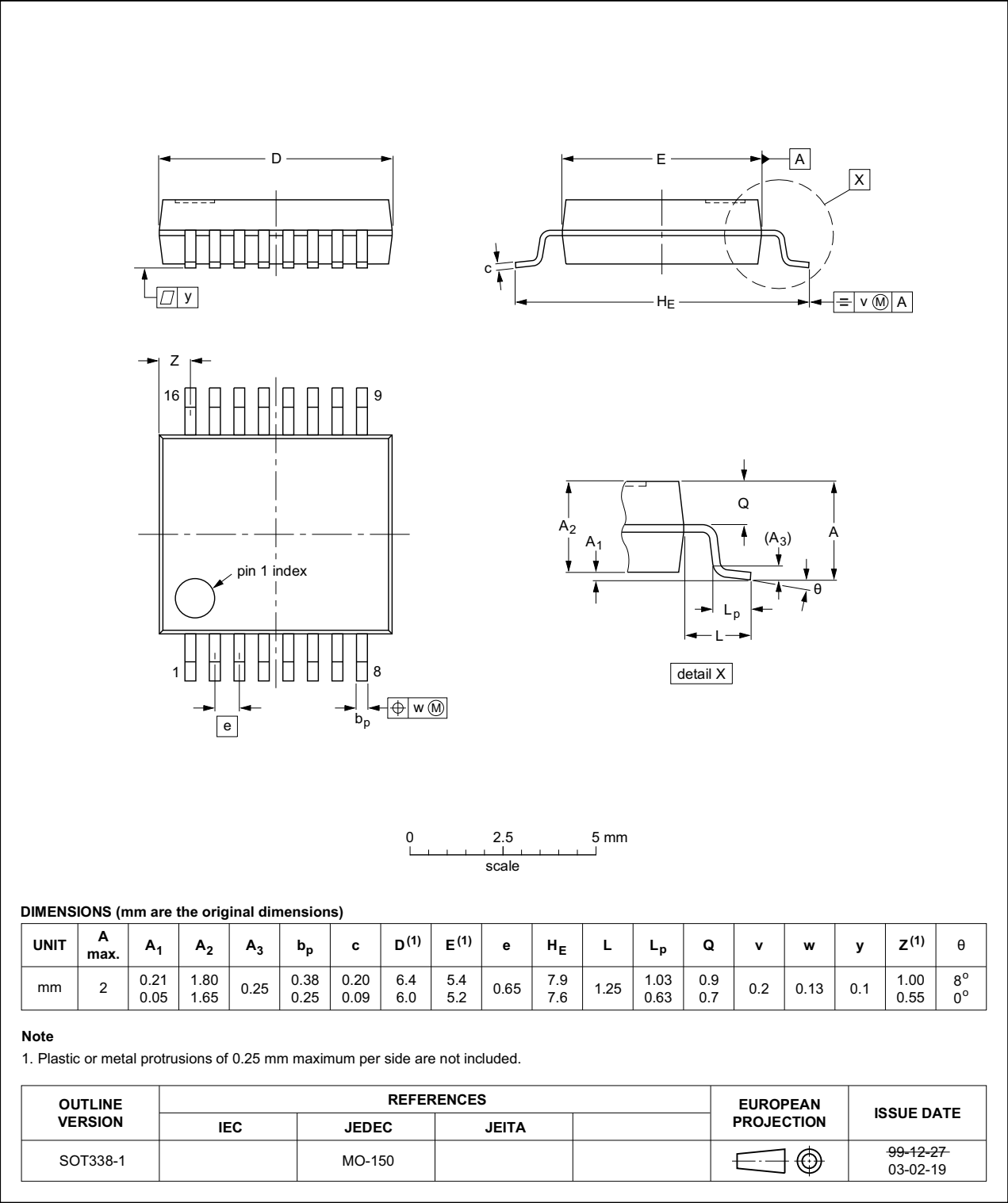


Fig 23. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

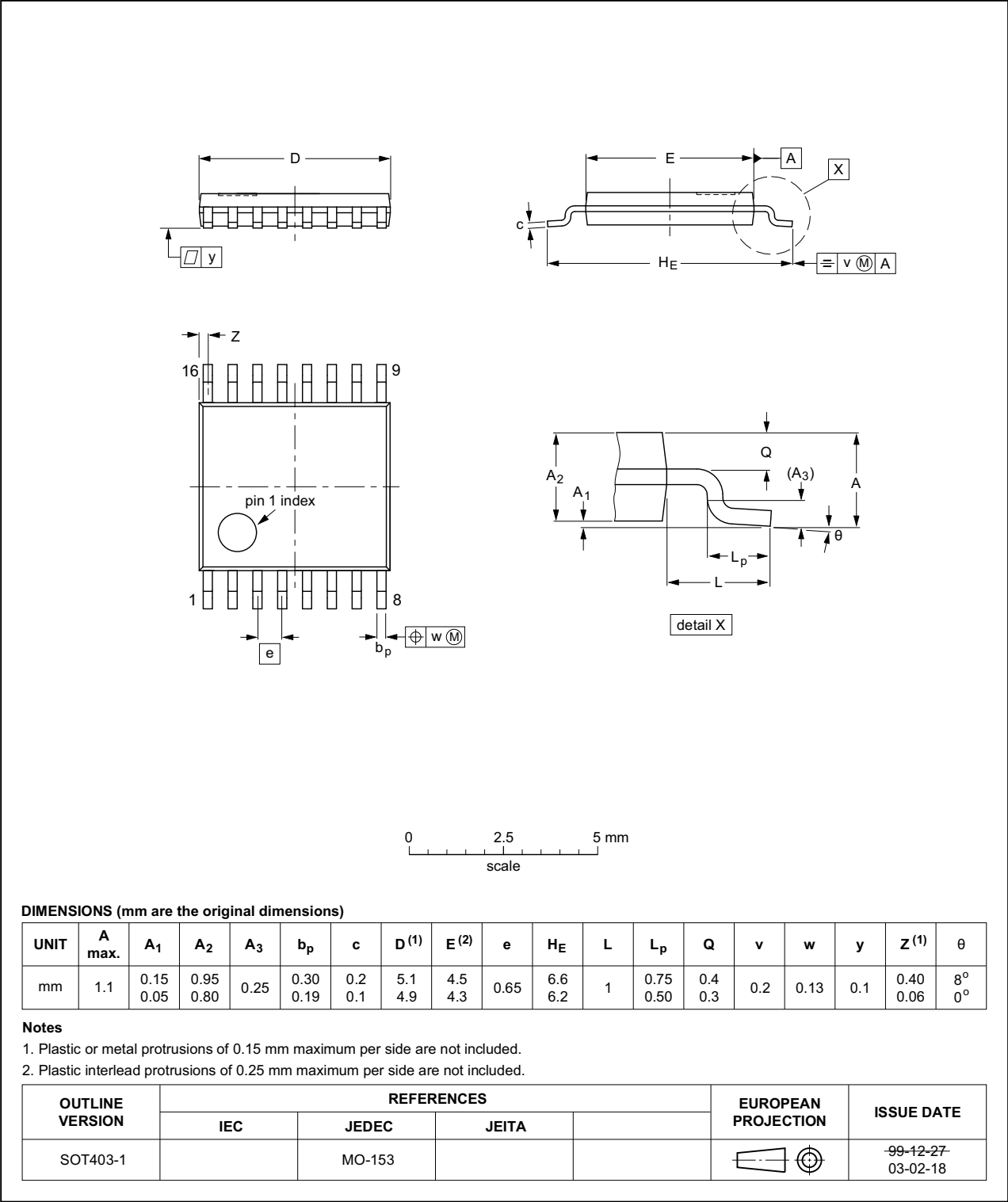


Fig 24. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

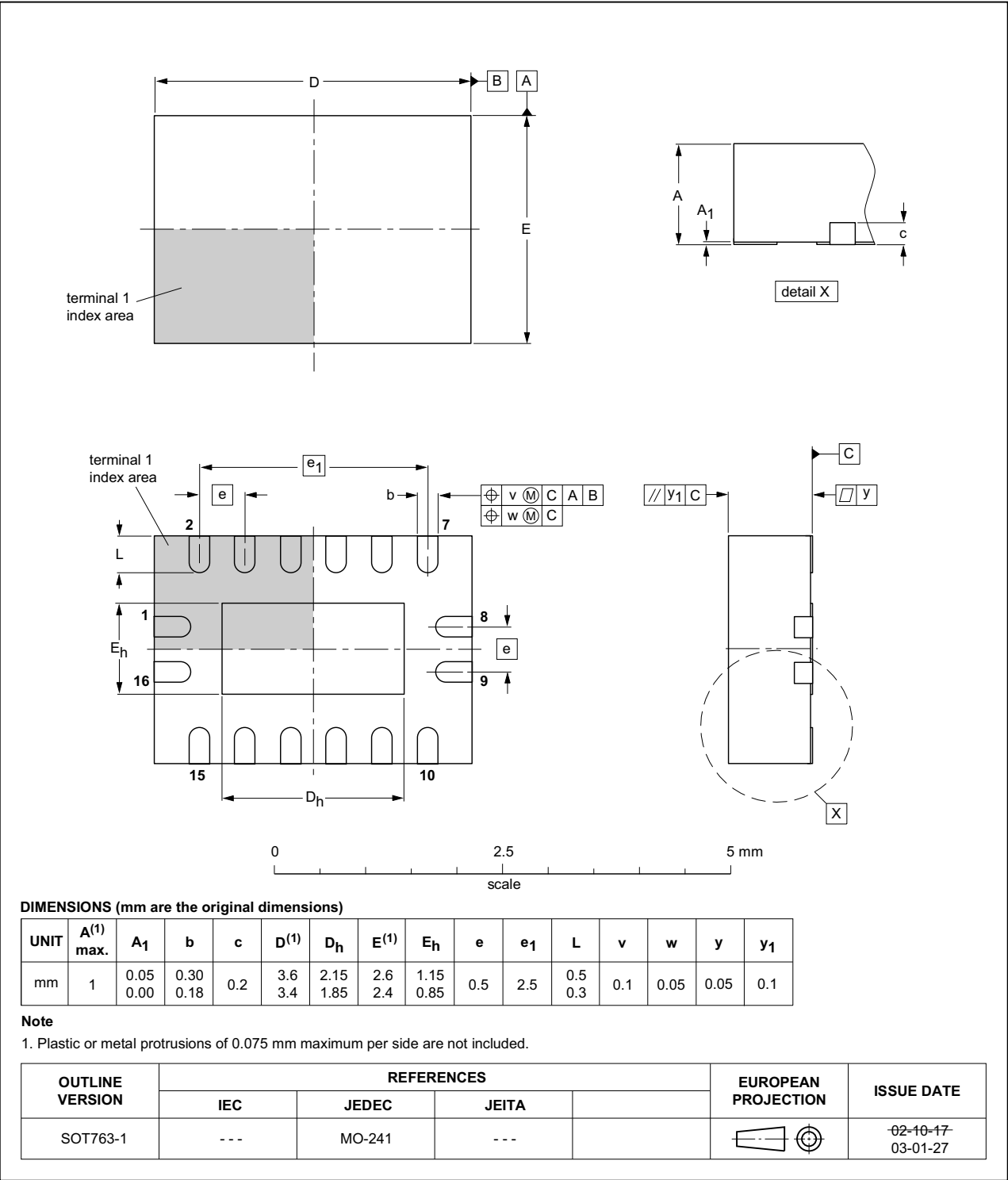


Fig 25. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4053 v.6	20160317	Product data sheet	-	74LV4053 v.5
Modifications:	Type number 74LV4053N (SOT38-4) removed.			
74LV4053 v.5	20140918	Product data sheet	-	74LV4053 v.4
Modifications:	Figure 6: Figure note added for DHVQFN16 package.			
74LV4053 v.4	20090810	Product data sheet	-	74LV4053 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors - Legal texts have been adapted to the new company name where appropriate. - Added type number 74LV4053BQ (DHVQFN16 package) - R_{ON} values changed in Section 2. - Package version SOT38-1 changed to SOT38-4 in Section 3, and Figure 23.			
74LV4053 v.3	19980623	Product specification	-	74LV4053 v.2
74LV4053 v.2	19970715	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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