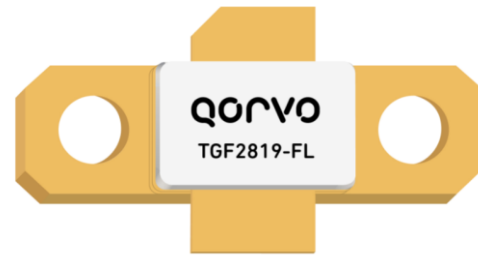


### Product Overview

The Qorvo TGF2819-FL is a greater-than 200 W ( $P_{3dB}$ ) discrete GaN on SiC HEMT which operates from DC to 4 GHz. The device is in an industry standard air cavity package and is ideally suited for IFF, avionics, military and civilian radar, and test instrumentation. The device can support pulsed and linear operations.

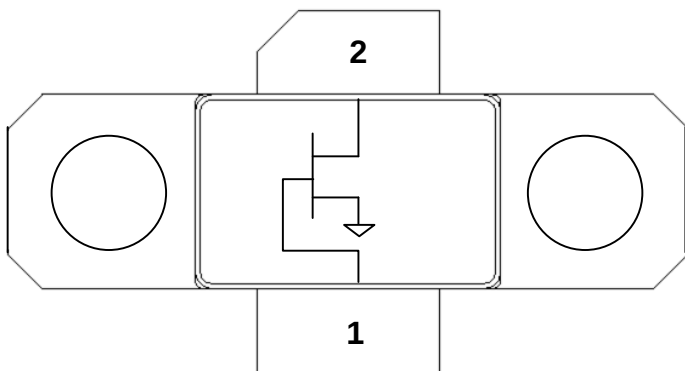
Lead-free and ROHS compliant

Evaluation boards are available upon request.



NI-360 Package

### Functional Block Diagram



### Key Features

- Frequency: DC to 4 GHz
  - Output Power ( $P_{3dB}$ )<sup>1</sup>: 257 W
  - Linear Gain<sup>1</sup>: 18 dB
  - Typical PAE<sub>3dB</sub><sup>1</sup>: 67.5%
  - Operating Voltage: 50 V
  - CW and Pulse capable
- Note 1: @ 3 GHz Load Pull

### Applications

- Military and civilian radar
- Professional and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers

### Ordering info

| Part No.          | ECCN        | Description                             |
|-------------------|-------------|-----------------------------------------|
| TGF2819-FL        | 3A001.b.3.a | DC–4 GHz, 50 V, 200 W GaN RF Transistor |
| TGF2819-FLPCB4B01 | EAR99       | 3.1 – 3.5 GHz EVB                       |
| TGF2819-FLEVB03   | EAR99       | 1.35 – 1.75 GHz EVB                     |

### Absolute Maximum Ratings<sup>1</sup>

| Parameter                         | Rating           | Units      |
|-----------------------------------|------------------|------------|
| Breakdown Voltage, $BV_{DG}$      | +145             | V          |
| Gate Voltage Range, $V_G$         | -7 to +2.0       | V          |
| Drain Current, $I_{D_{MAX}}$      | 12               | A          |
| Gate Current Range, $I_G$         | See page 20.     | mA         |
| Power Dissipation, $P_{DISS}$     | 207 <sup>2</sup> | W          |
| RF Input Power, $T = 25^\circ C$  | +39.8            | dBm        |
| Channel Temperature, $T_{CH}$     | 275              | $^\circ C$ |
| Mounting Temperature (30 Seconds) | 320              | $^\circ C$ |
| Storage Temperature               | -65 to +150      | $^\circ C$ |

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed 100uS PW, 20% DC

### Recommended Operating Conditions<sup>1</sup>

| Parameter                                      | Min | Typ  | Max | Units      |
|------------------------------------------------|-----|------|-----|------------|
| Operating Temp. Range                          | -40 | +25  | +85 | $^\circ C$ |
| Drain Voltage Range, $V_D$                     | +32 | +50  | +55 | V          |
| Drain Bias Current, $I_{DQ}$                   |     | 250  |     | mA         |
| Drain Current, $I_D$ <sup>4</sup>              | –   | 7.2  | –   | A          |
| Gate Voltage, $V_G$ <sup>3</sup>               | –   | -2.8 | –   | V          |
| Channel Temperature ( $T_{CH}$ )               | –   | –    | 250 | $^\circ C$ |
| Power Dissipation ( $P_D$ ) <sup>2,4</sup>     | –   | –    | 184 | W          |
| Power Dissipation ( $P_D$ ), $CW$ <sup>2</sup> | –   | –    | 98  | W          |

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85  $^\circ C$
3. To be adjusted to desired  $I_{DQ}$
4. Pulsed, 100uS PW, 20% DC

### Measured Load Pull Performance – Power Tuned<sup>1</sup>

| Parameter                                              | Typical Values |      |      |      |     |      | Units |
|--------------------------------------------------------|----------------|------|------|------|-----|------|-------|
| Frequency, F                                           | 2.7            | 2.9  | 3.1  | 3.3  | 3.5 | 3.7  | GHz   |
| Drain Voltage, $V_D$                                   | 50             | 50   | 50   | 50   | 50  | 50   | V     |
| Drain Bias Current, $I_{DQ}$                           | 200            | 200  | 200  | 200  | 200 | 200  | mA    |
| Output Power at 3dB compression, $P_{3dB}$             | 54             | 53.5 | 53.2 | 53   | 53  | 52.7 | dBm   |
| Power Added Efficiency at 3dB compression, $PAE_{3dB}$ | 60.0           | 53.7 | 46.0 | 48.8 | 43  | 51.4 | %     |
| Gain at 3dB compression, $G_{3dB}$                     | 13.9           | 14.3 | 13.3 | 16.5 | 14  | 15.5 | dB    |

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance,  $Z_0 = 7 \Omega$ .

### Measured Load Pull Performance – Efficiency Tuned<sup>1</sup>

| Parameter                                              | Typical Values |      |      |      |      |      | Units |
|--------------------------------------------------------|----------------|------|------|------|------|------|-------|
| Frequency, F                                           | 2.7            | 2.9  | 3.1  | 3.3  | 3.5  | 3.7  | GHz   |
| Drain Voltage, $V_D$                                   | 50             | 50   | 50   | 50   | 50   | 50   | V     |
| Drain Bias Current, $I_{DQ}$                           | 200            | 200  | 200  | 200  | 200  | 200  | mA    |
| Output Power at 3dB compression, $P_{3dB}$             | 52.5           | 53.2 | 52.6 | 52.1 | 52.3 | 51.9 | dBm   |
| Power Added Efficiency at 3dB compression, $PAE_{3dB}$ | 65.5           | 64.3 | 54.4 | 52.2 | 53.7 | 53.9 | %     |
| Gain at 3dB compression, $G_{3dB}$                     | 15.8           | 15.5 | 15.5 | 17.8 | 16.1 | 15.9 | dB    |

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance,  $Z_0 = 7 \Omega$ .

### 3.1 – 3.5 GHz EVB – 3.5 GHz Performance<sup>1</sup>

| Parameter                                          | Min   | Typ  | Max | Units |
|----------------------------------------------------|-------|------|-----|-------|
| Linear Gain, $G_{LIN}$                             | –     | 15.1 | –   | dB    |
| Output Power at 3dB compression point, P3dB        | –     | 126  | –   | W     |
| Drain Efficiency at 3dB compression point, DEFF3dB | –     | 52.4 | –   | %     |
| Gain at 3dB compression point, G3dB                | –     | 12.1 | –   | dB    |
| Gate Leakage <sup>2</sup>                          | -31.7 | –    | –   | mA    |

Notes:

1.  $V_D = +32$  V,  $I_{DQ} = 250$  mA, Temp = +25 °C, Pulse Width = 100  $\mu$ S, Duty Cycle = 20%
2.  $V_D = +10$  V,  $V_G = -3.8$  V

### RF Characterization – Mismatch Ruggedness at 3.5 GHz

| Symbol | Parameter                     | dB Compression | Typical |
|--------|-------------------------------|----------------|---------|
| VSWR   | Impedance Mismatch Ruggedness | 3              | 10:1    |

Test conditions unless otherwise noted:  $T_A = 25$  °C,  $V_D = 32$  V,  $I_{DQ} = 250$  mA

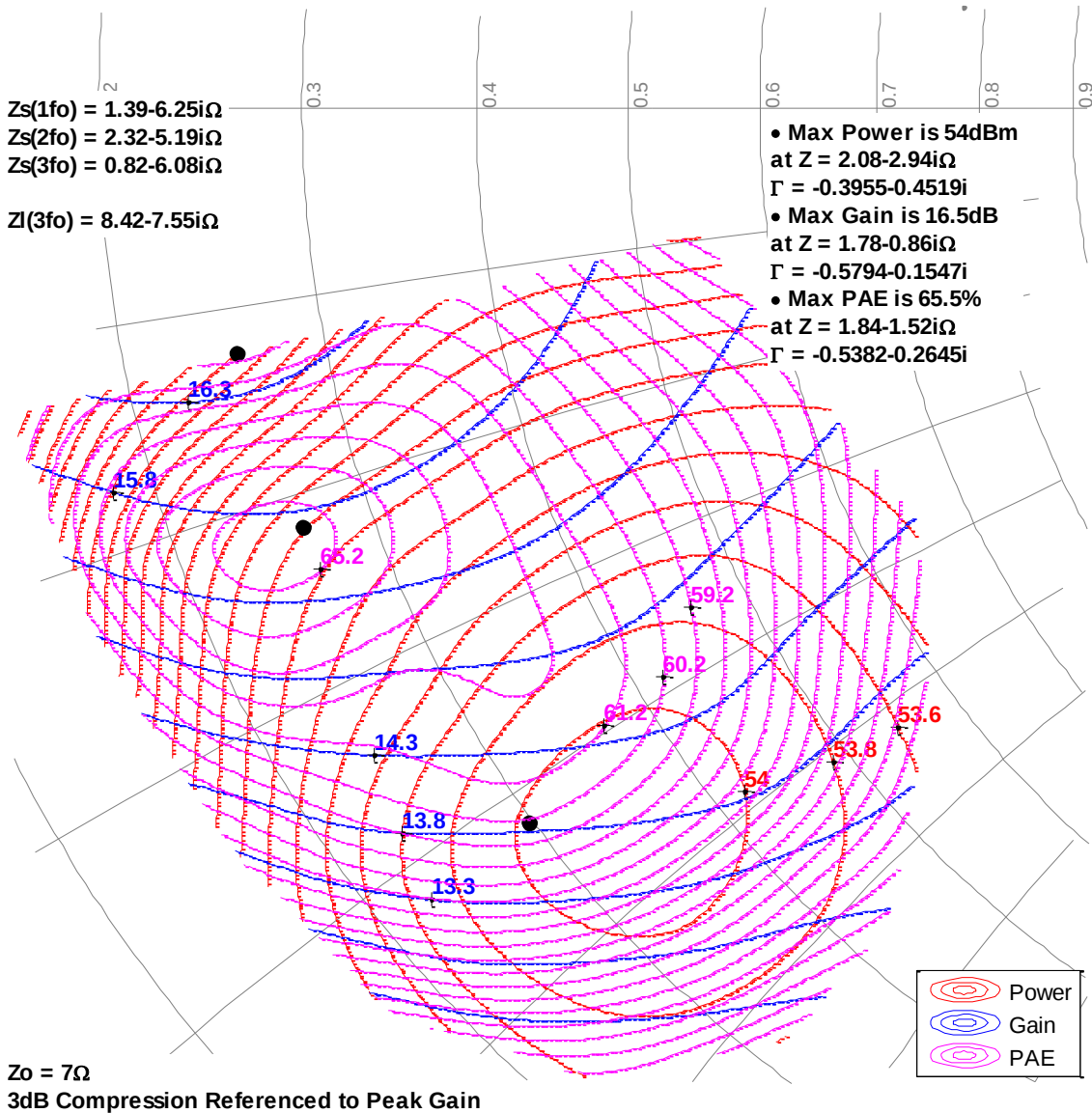
Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.

## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

### 2.7GHz, Load-pull

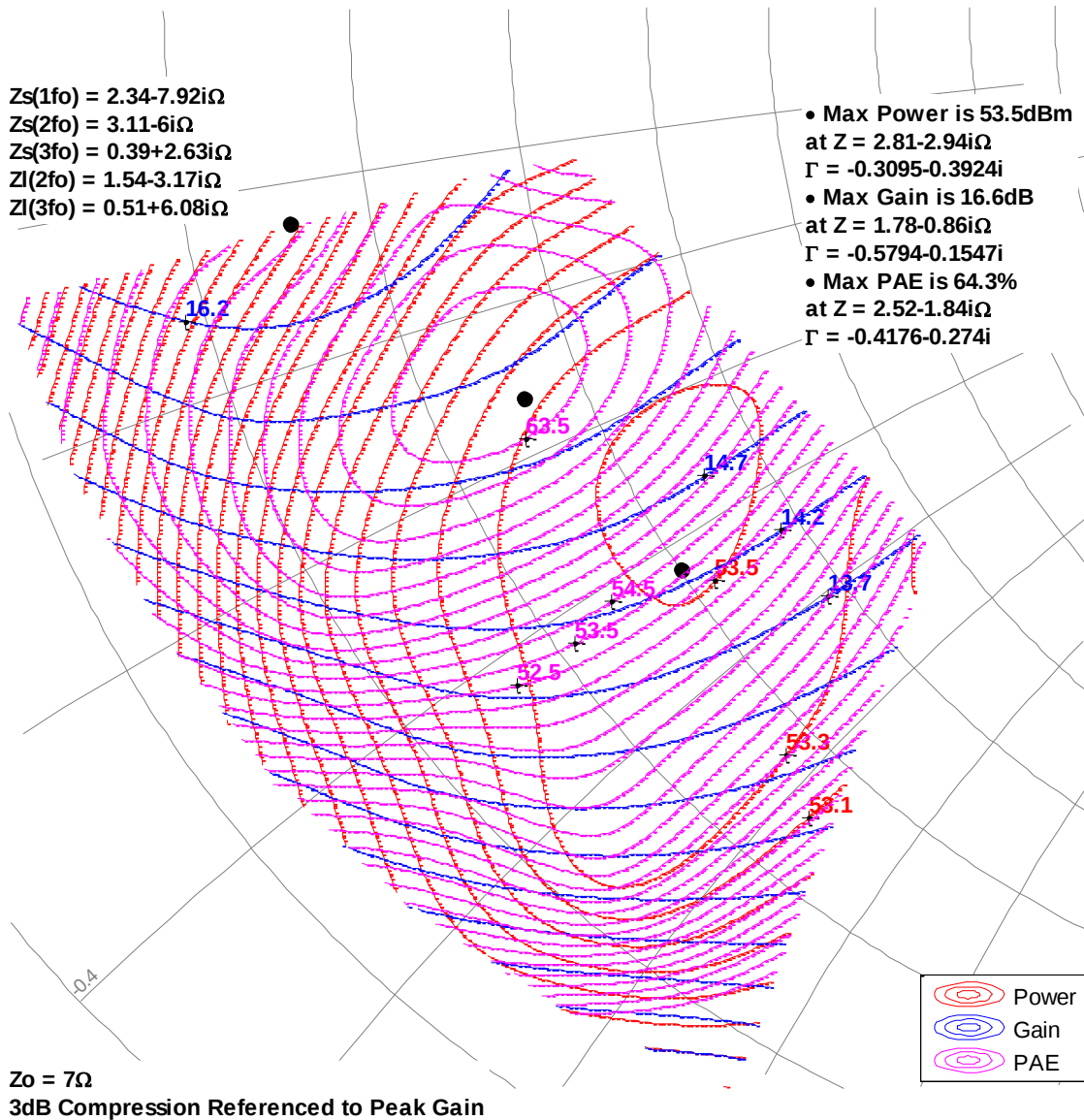


## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

### 2.9GHz, Load-pull

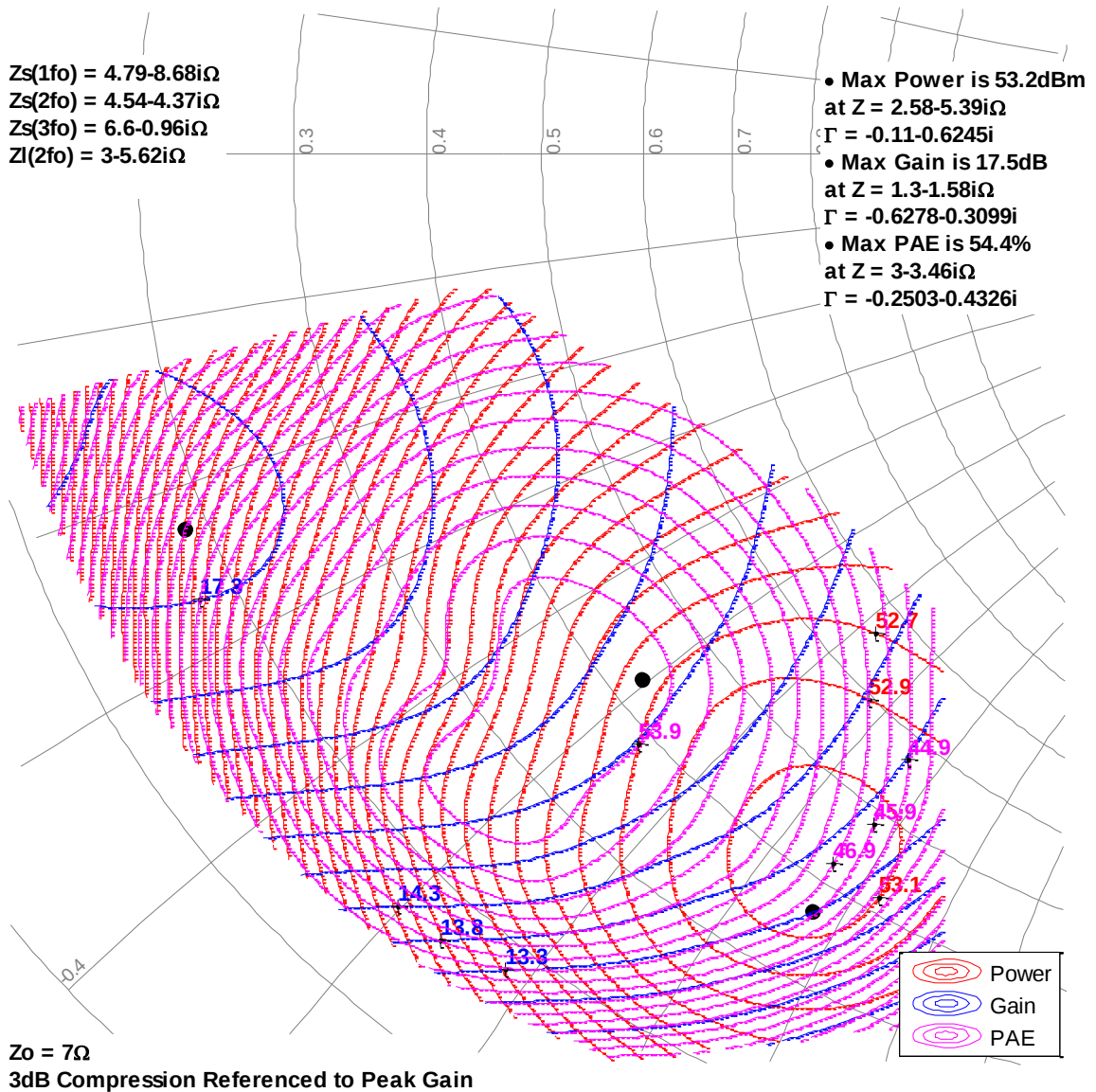


## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

### 3.1GHz, Load-pull

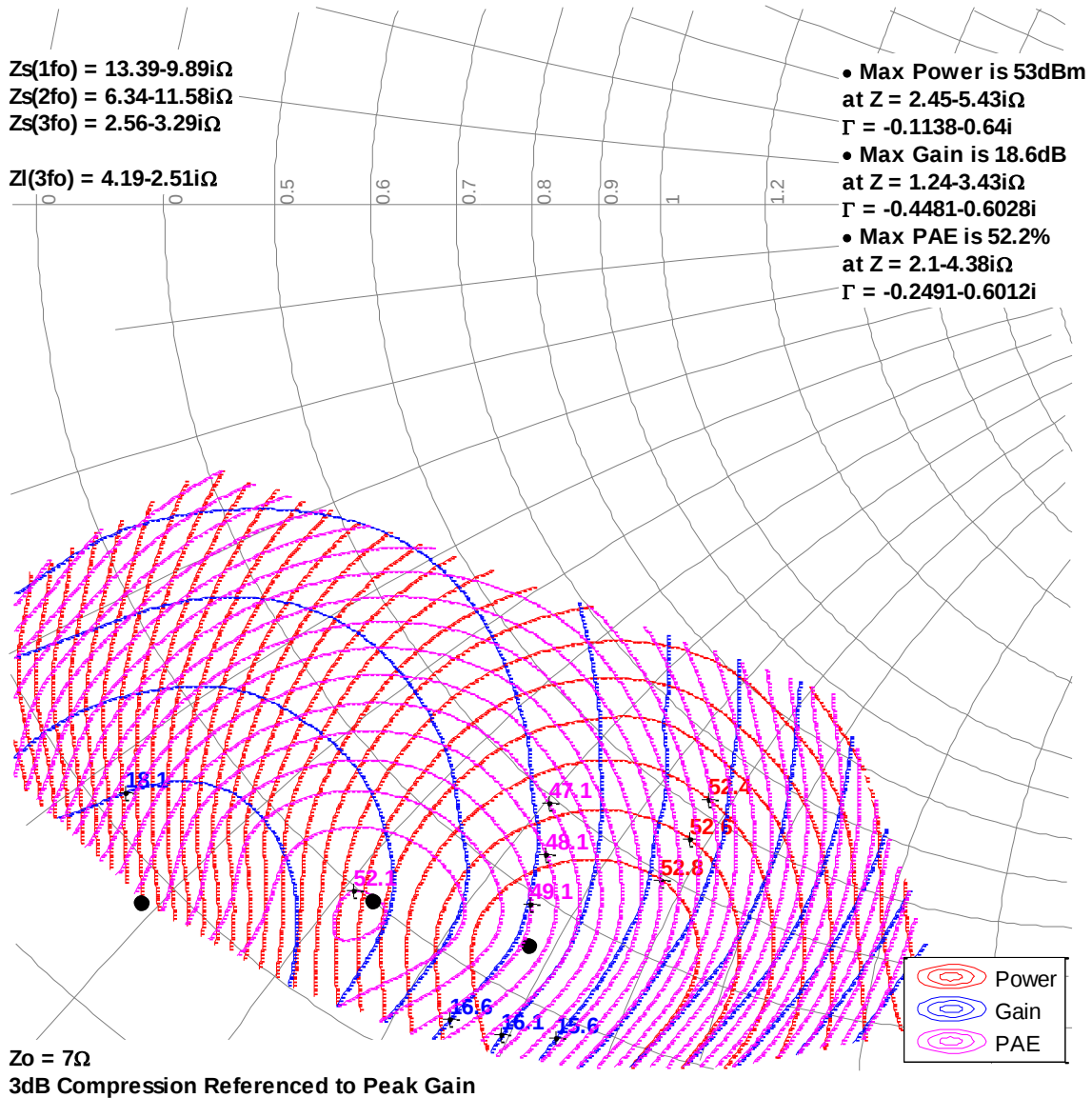


## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

### 3.3GHz, Load-pull

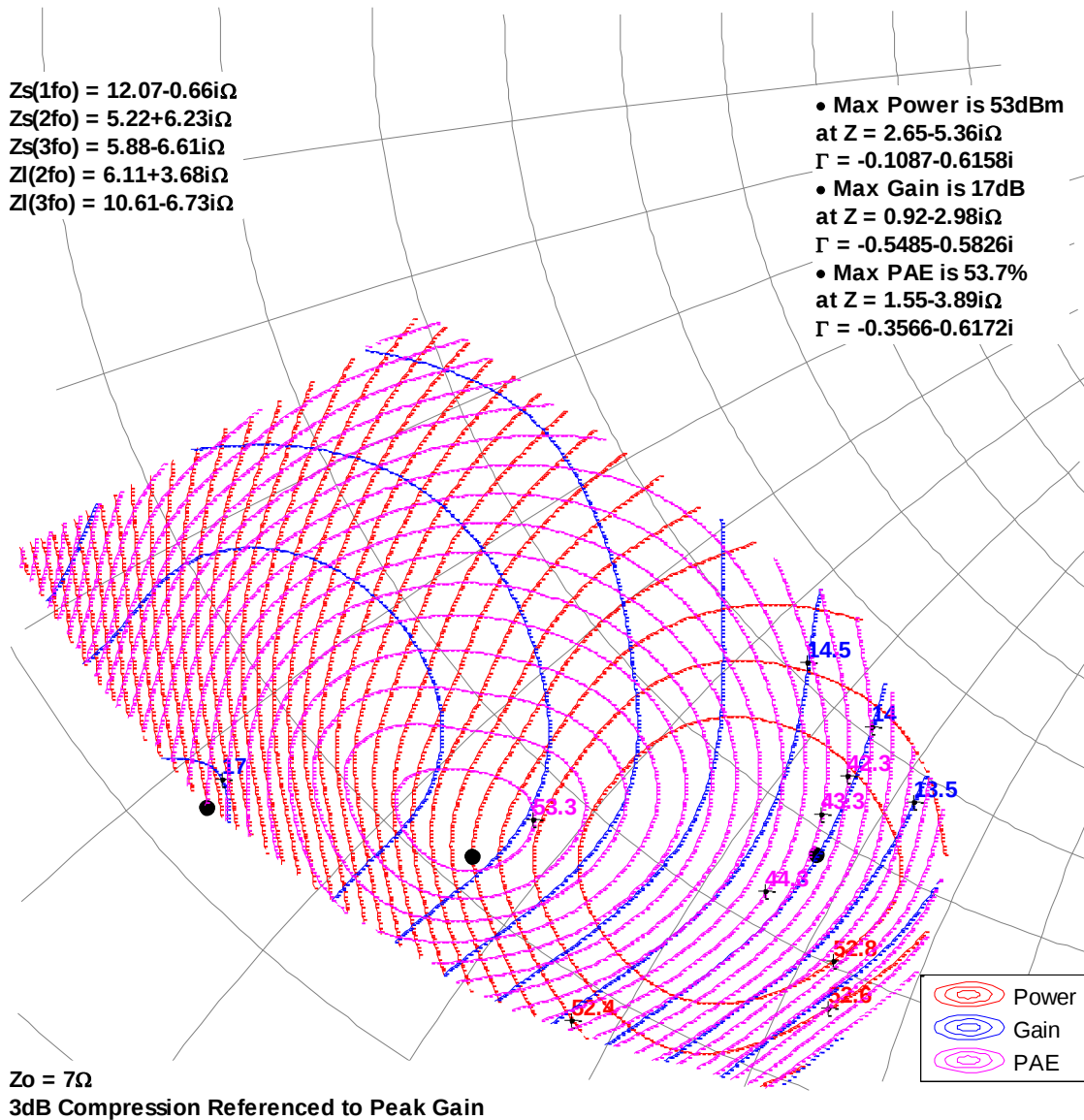


## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

### 3.5GHz, Load-pull

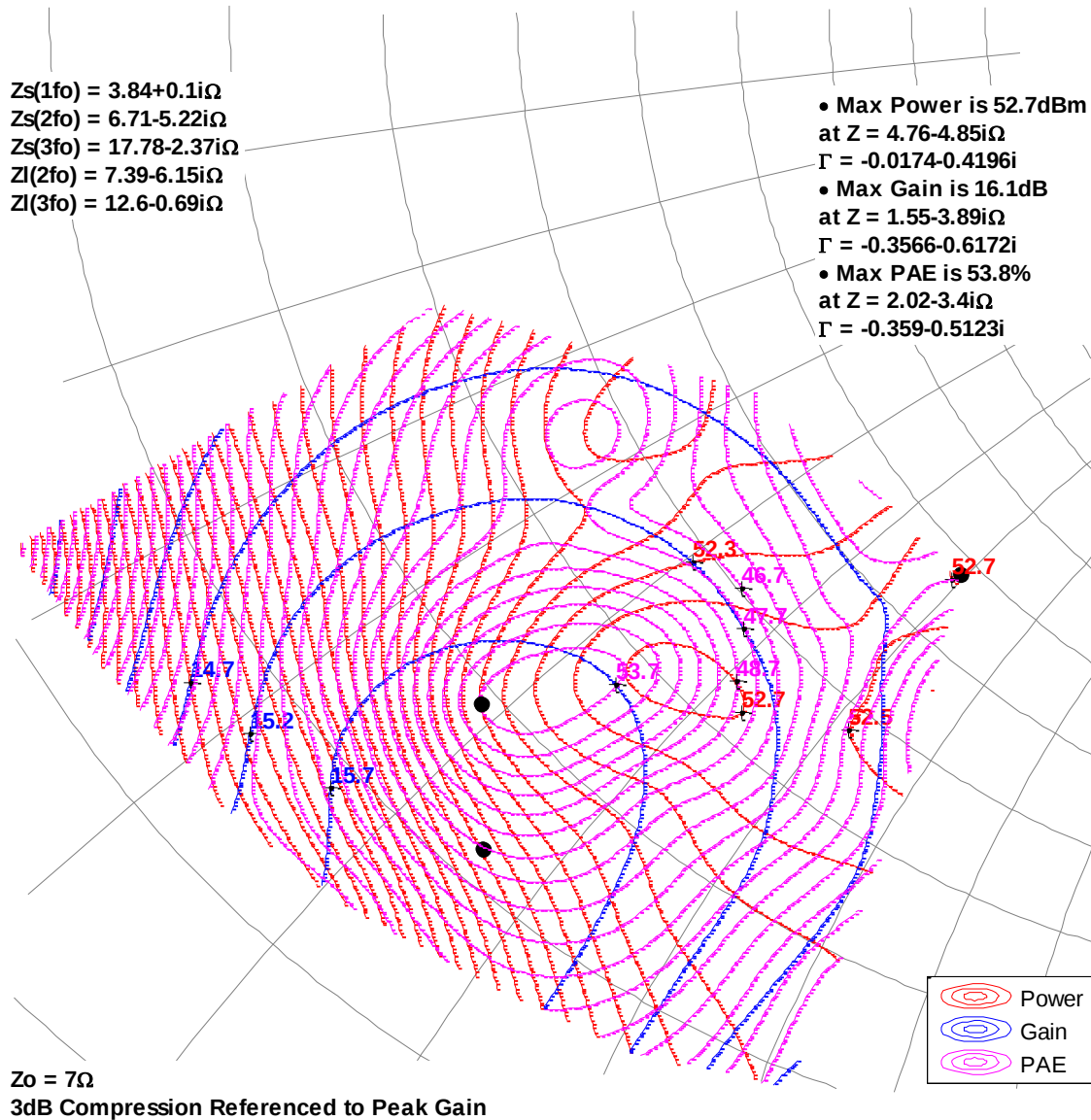


## Measured Load-Pull Smith Charts<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50\text{ V}$ ,  $I_{DQ} = 200\text{ mA}$ ,  $100\text{ }\mu\text{S}$  Pulse Width, 20% Duty Cycle
2. See page 22 for load pull reference planes where the performance was measured.

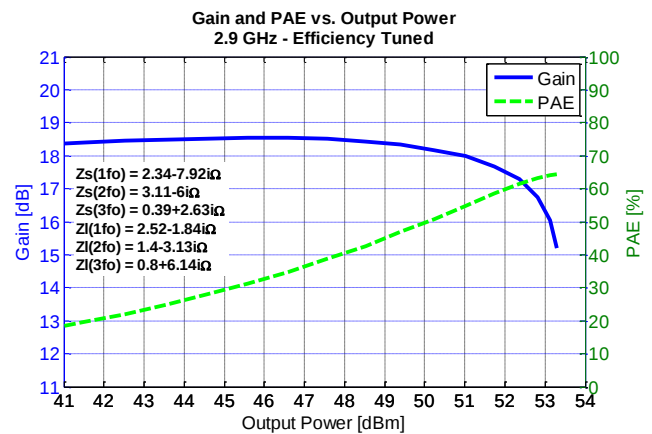
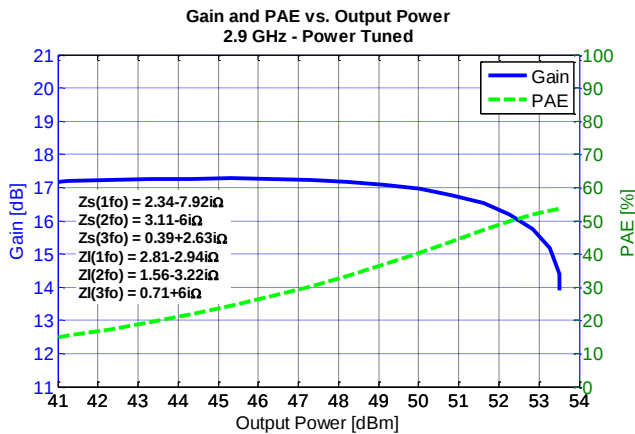
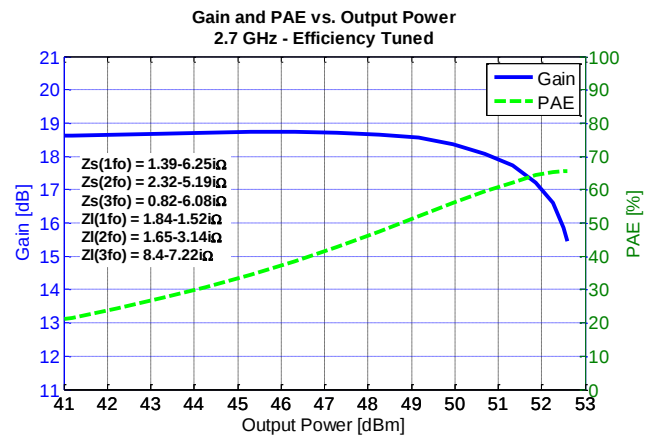
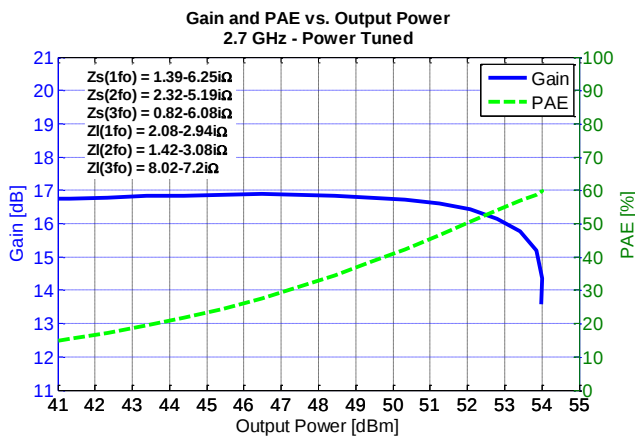
### 3.7GHz, Load-pull



### Typical Measured Performance – Load-Pull Drive-up<sup>1, 2</sup>

Notes:

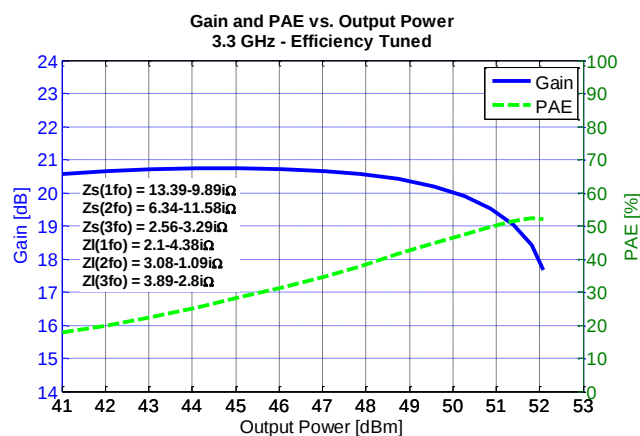
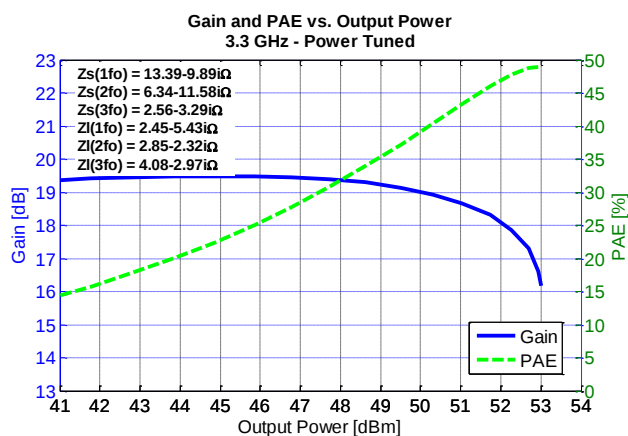
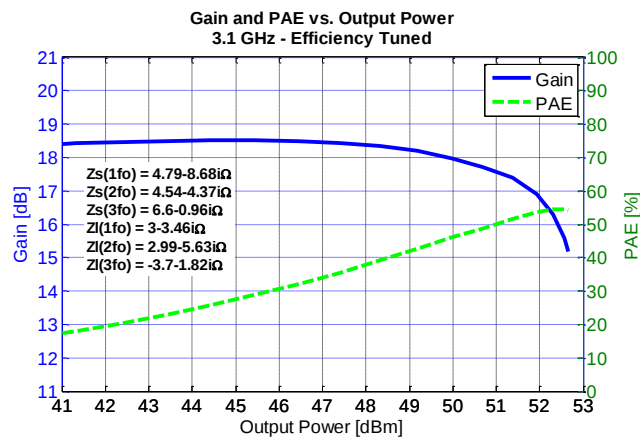
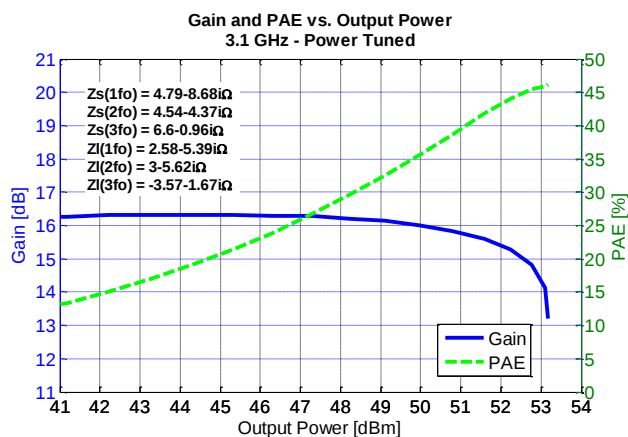
1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



## Typical Measured Performance – Load-Pull Drive-up<sup>1, 2</sup>

Notes:

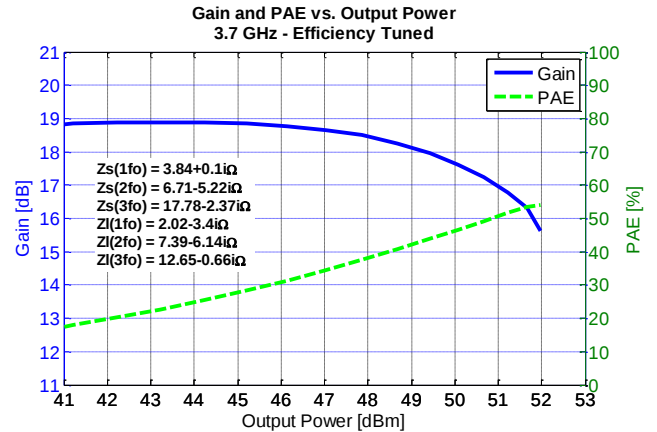
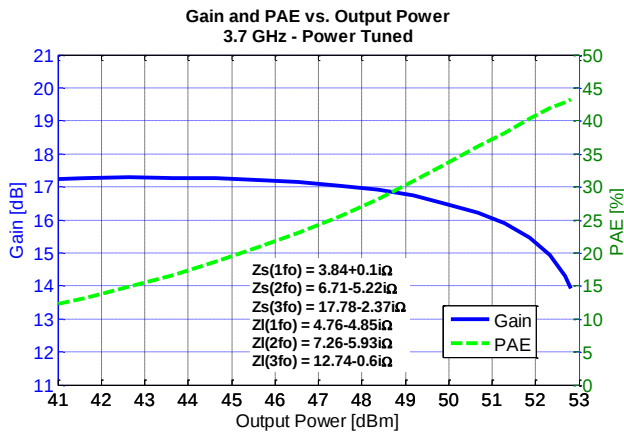
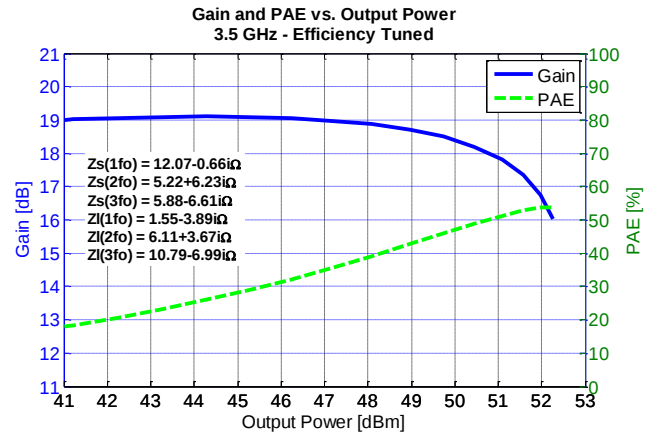
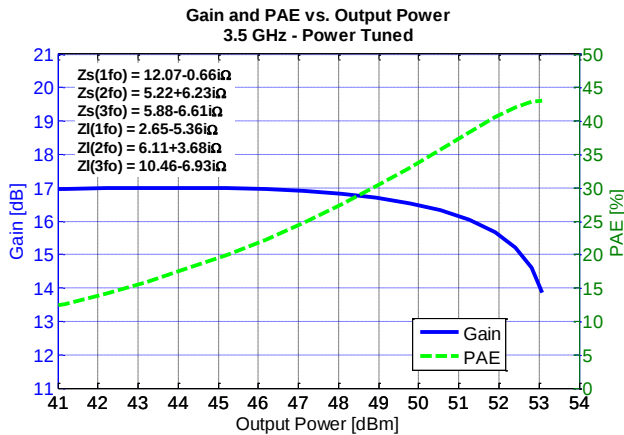
1. C Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ s Pulse Width, 20% Duty Cycle
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



## Typical Measured Performance – Load-Pull Drive-up<sup>1, 2</sup>

Notes:

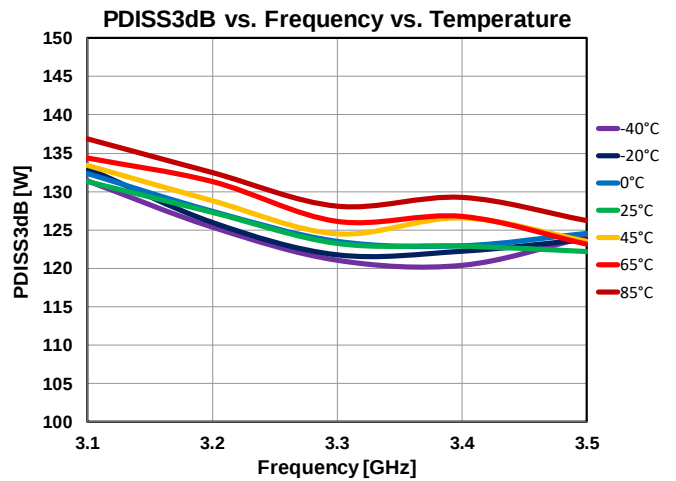
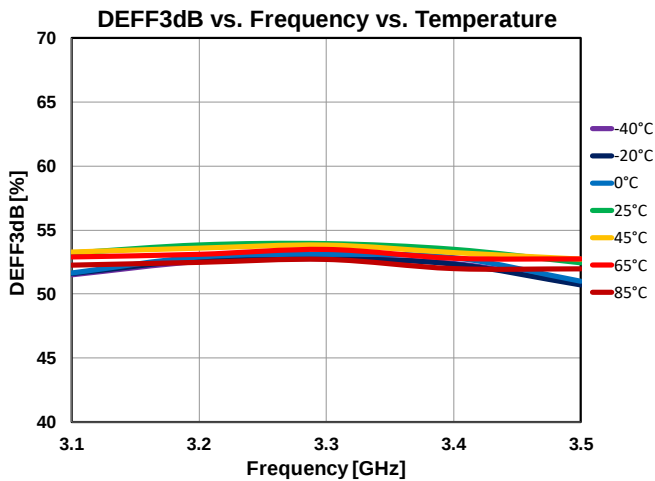
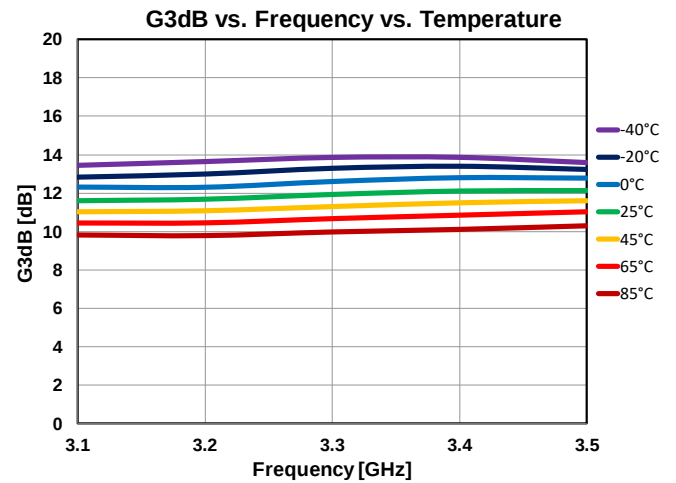
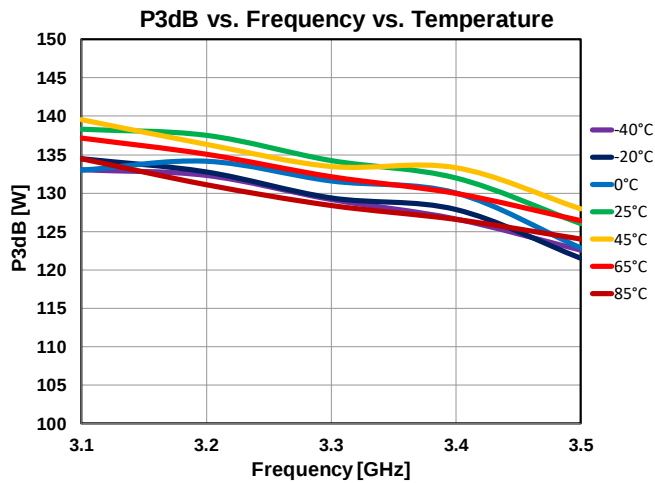
1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 100  $\mu$ S Pulse Width, 20% Duty Cycle
2. See page 22 for load-pull and source-pull reference planes where the performance was measured.



### Power Driveup Performance Over Temperatures Of 3.1 – 3.5 GHz EVB<sup>1, 2</sup>

Notes:

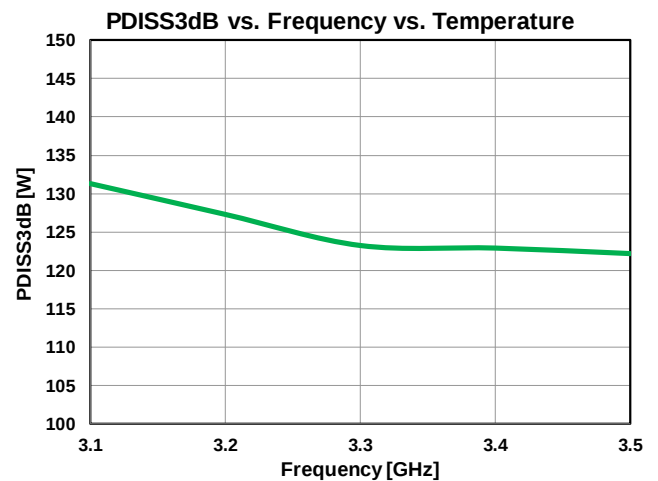
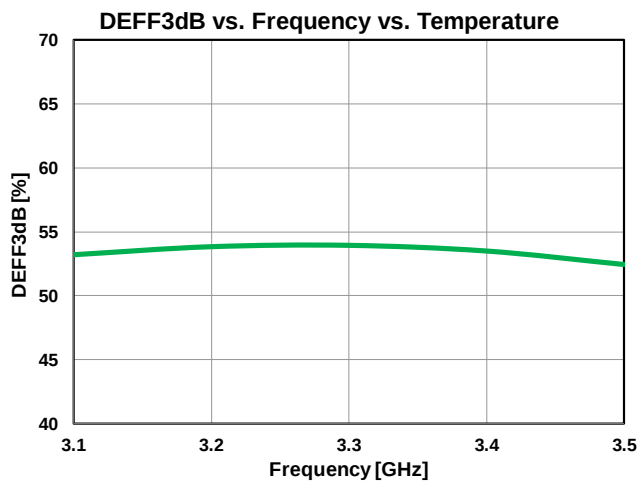
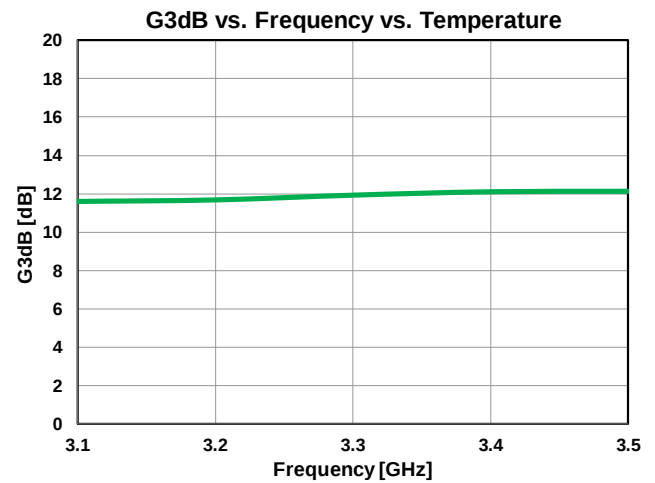
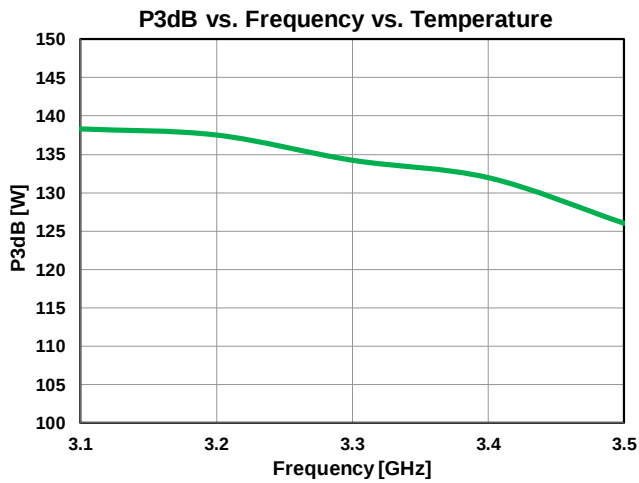
1. Test Conditions:  $V_D = 32$  V,  $I_{DQ} = 250$  mA, 20  $\mu$ S Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network.



### Power Driveup Performance At 25°C Of 3.1 – 3.5 GHz EVB<sup>1, 2</sup>

Notes:

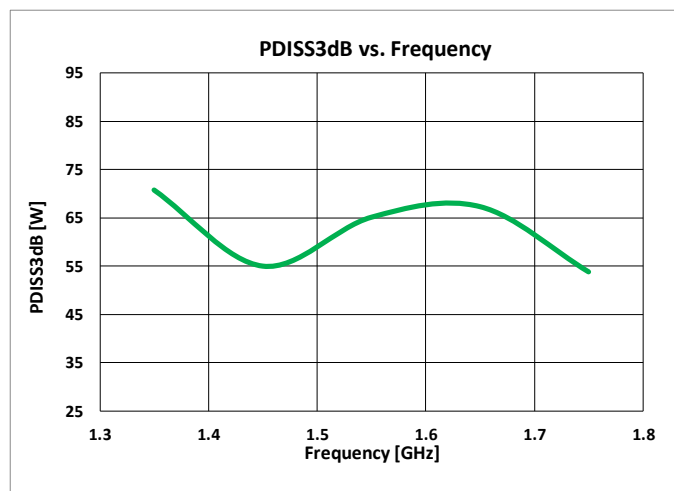
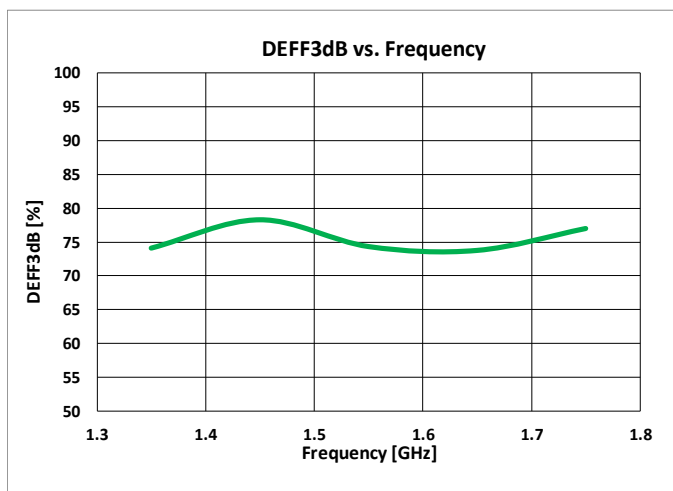
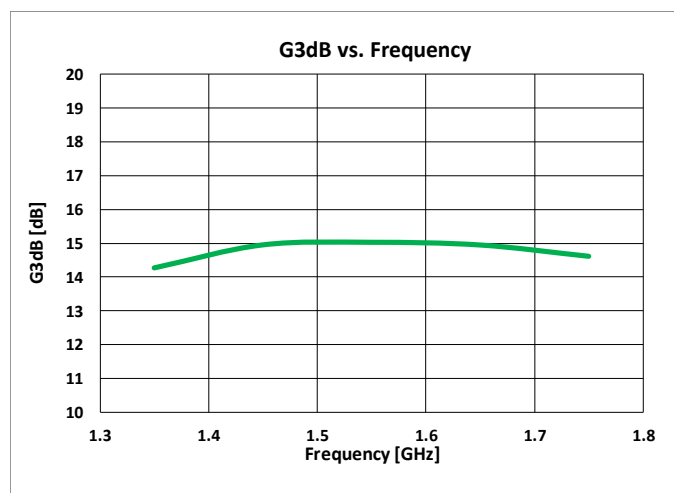
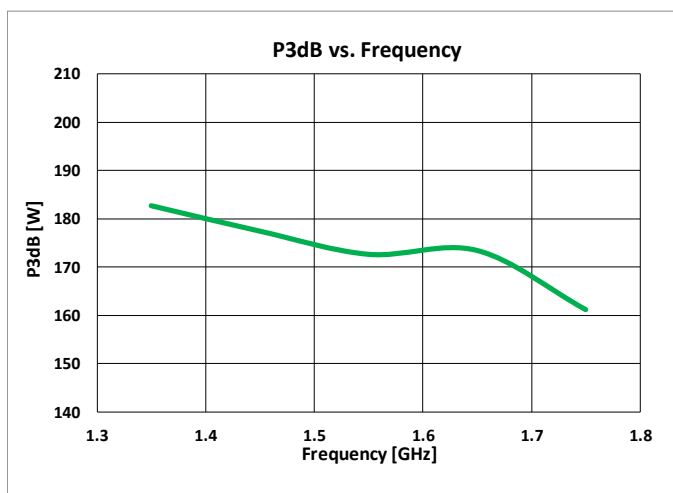
1. Test Conditions:  $V_D = 32$  V,  $I_{DQ} = 250$  mA, 20 uS Pulse Width, 20% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..



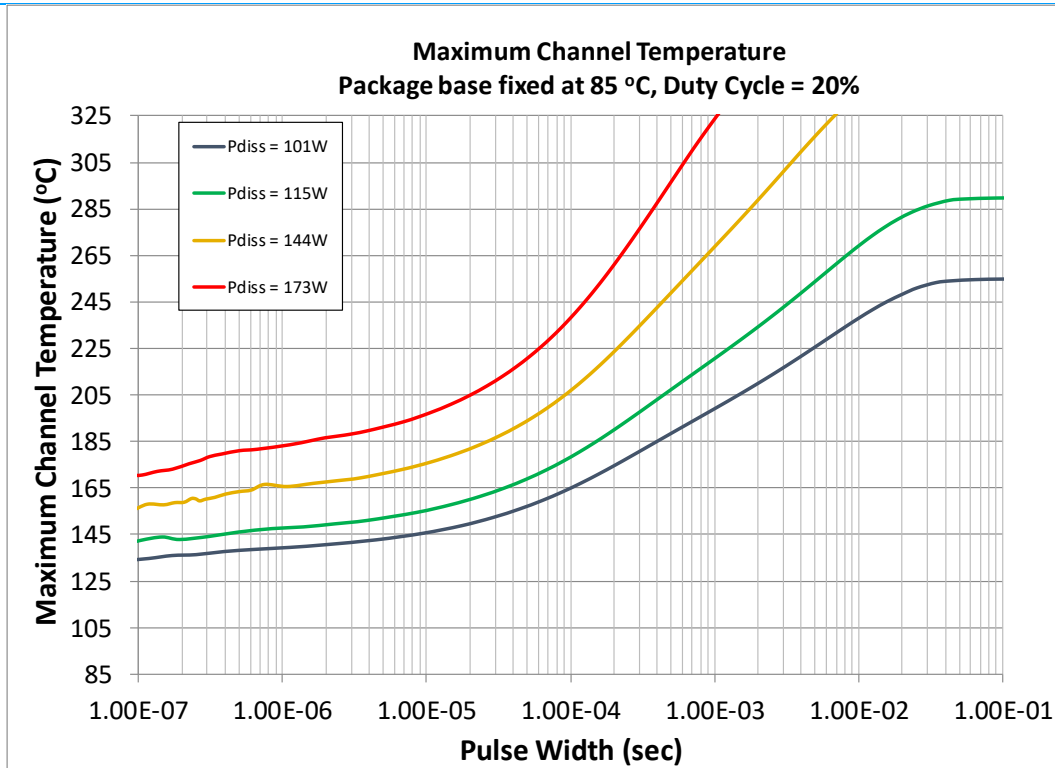
### Power Driveup Performance At 25°C Of 1.35 – 1.75 GHz EVB<sup>1, 2</sup>

Notes:

1. Test Conditions:  $V_D = 50$  V,  $I_{DQ} = 200$  mA, 500  $\mu$ S Pulse Width, 50% Duty Cycle
2. The dissipation power limit is conservative because it is specified at DUT only without accounting for the loss of the output matching network..



### Thermal and Reliability Information – Pulsed<sup>1</sup>

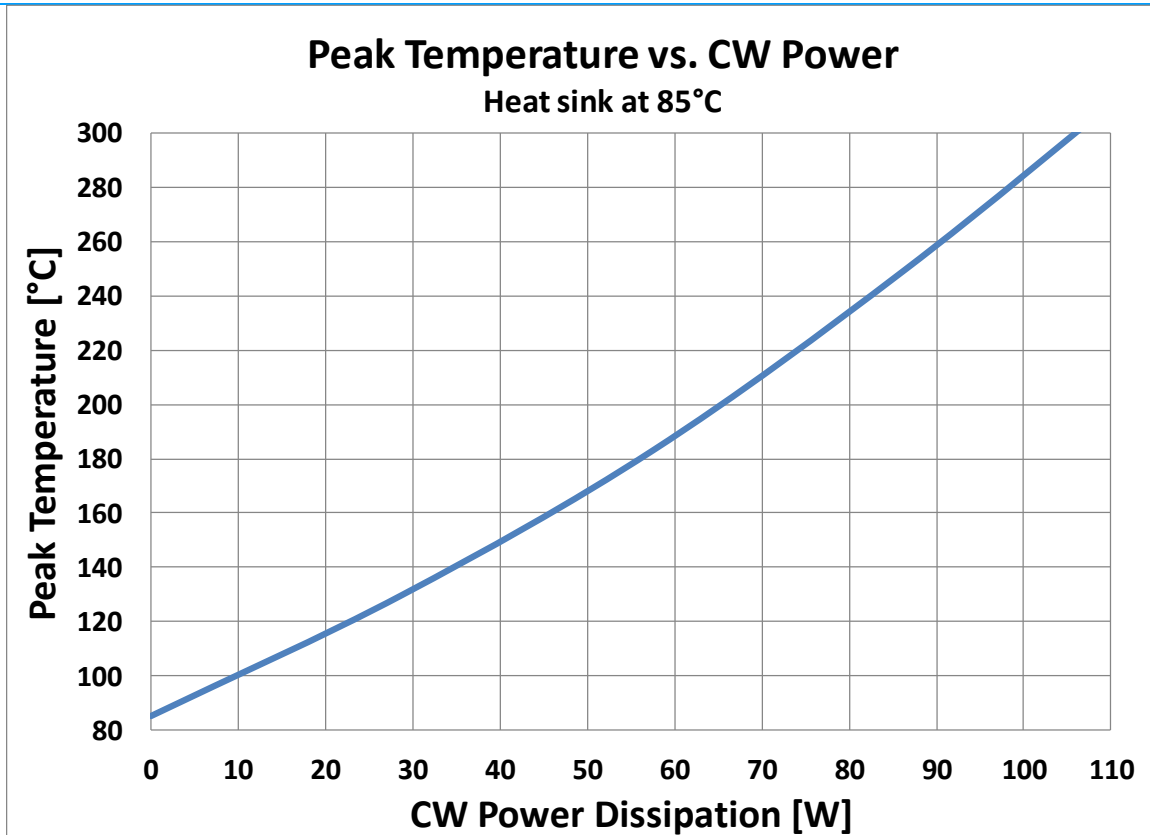


| Parameter                                   | Conditions                     | Values | Units |
|---------------------------------------------|--------------------------------|--------|-------|
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                                | 0.79   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                     | 165    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 101 W Pdiss, 100 uS PW, 20% DC | 5.8E9  | Hrs   |
| Peak Channel Temperature, IR                |                                | 139    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                                | 0.82   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                     | 179    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 115 W Pdiss, 100 uS PW, 20% DC | 1.5E9  | Hrs   |
| Peak Channel Temperature, IR                |                                | 148    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                                | 0.85   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                     | 207    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 144 W Pdiss, 100 uS PW, 20% DC | 1.2E8  | Hrs   |
| Peak Channel Temperature, IR                |                                | 165    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                                | 0.88   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                     | 238    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 173 W Pdiss, 100 uS PW, 20% DC | 1.0E7  | Hrs   |
| Peak Channel Temperature, IR                |                                | 183    | °C    |

Note:

1. FEA: Finite Element Analysis Method, IR: Infra-Red Method
2. Median Lifetime under pulsed condition is that under CW condition divided by duty cycle.

## Thermal and Reliability Information – CW<sup>1</sup>

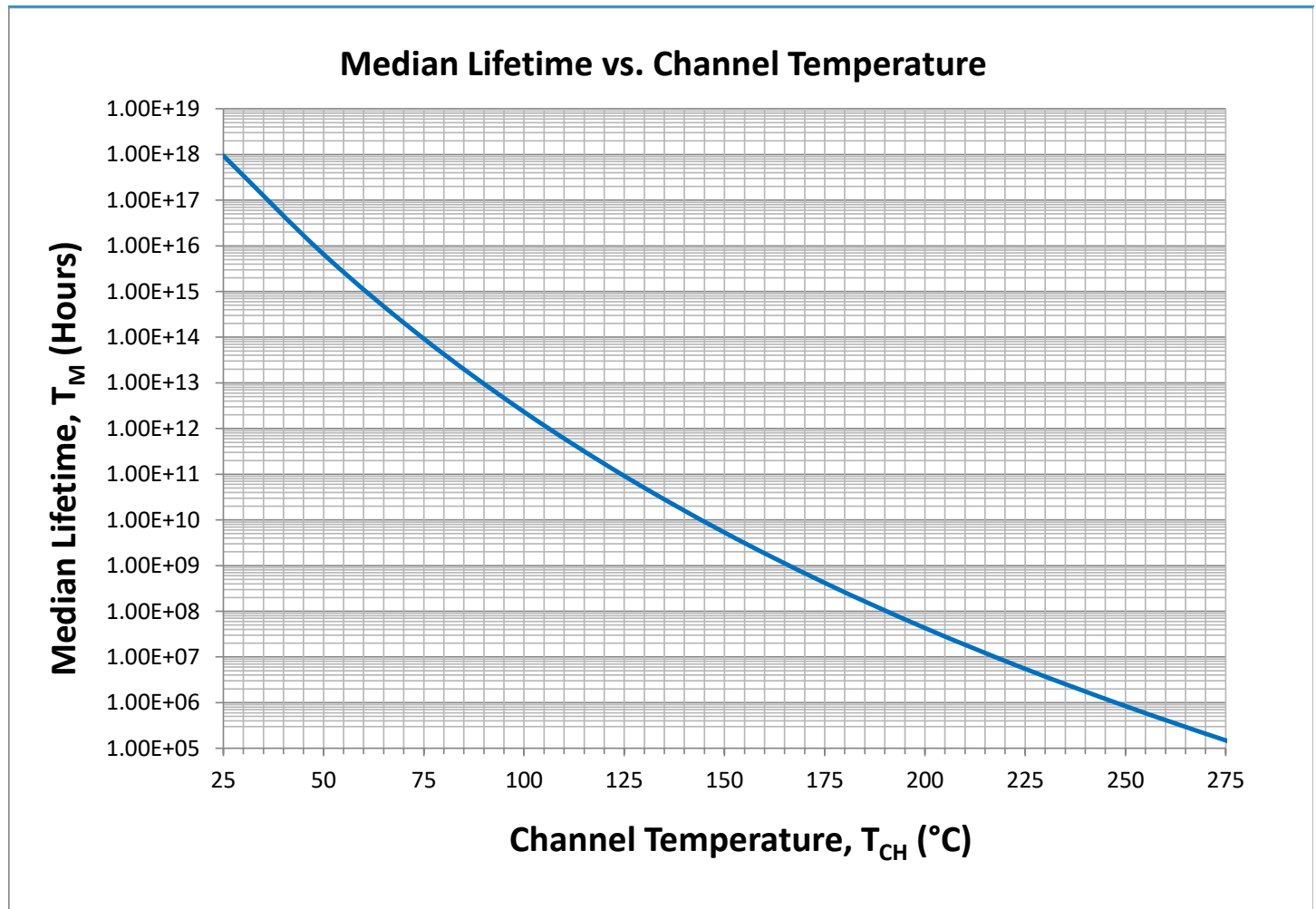


| Parameter                                   | Conditions                | Values | Units |
|---------------------------------------------|---------------------------|--------|-------|
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                           | 1.46   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                | 169    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 57.6 W P <sub>diss</sub>  | 7.7E8  | Hrs   |
| Peak Channel Temperature, IR                |                           | 142    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                           | 1.62   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                | 225    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 86.4 W P <sub>diss</sub>  | 5.5E6  | Hrs   |
| Peak Channel Temperature, IR                |                           | 175    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                           | 1.71   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                | 257    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 100.8 W P <sub>diss</sub> | 5.2E5  | Hrs   |
| Peak Channel Temperature, IR                |                           | 193    | °C    |
| Thermal Resistance, FEA ( $\theta_{JC}$ )   |                           | 1.79   | °C/W  |
| Peak Channel Temperature, FEA ( $T_{CH}$ )  | 85 °C Case                | 291    | °C    |
| Median Lifetime, FEA ( $T_M$ ) <sup>2</sup> | 115.2 W P <sub>diss</sub> | 5.3E4  | Hrs   |
| Peak Channel Temperature, IR                |                           | 213    | °C    |

Note:

1. FEA: Finite Element Analysis Method, IR: Infra-Red Method
2. Median Lifetime under pulsed condition is that under CW condition divided by duty cycle.

Median Lifetime<sup>1</sup>

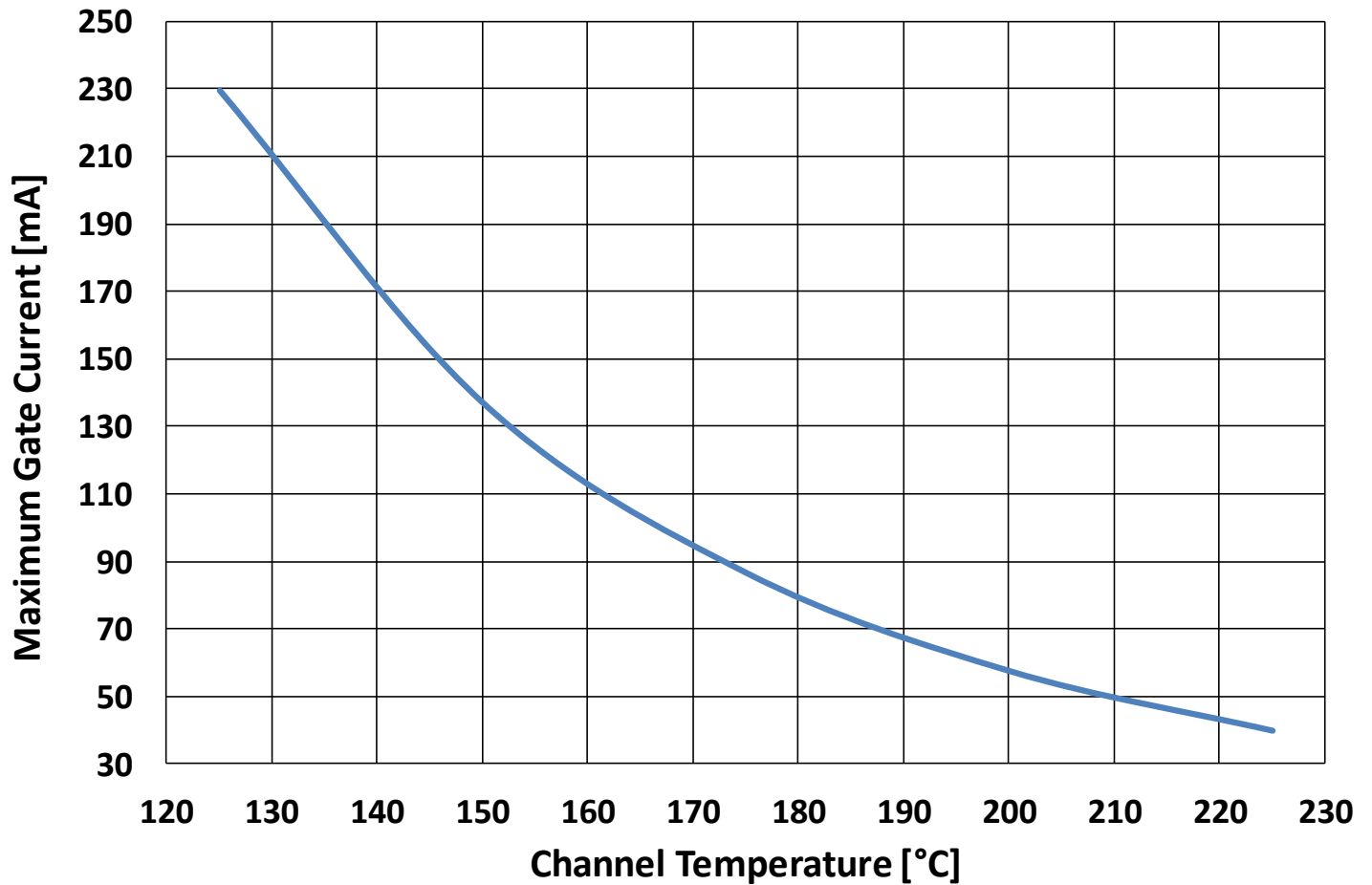


Notes:

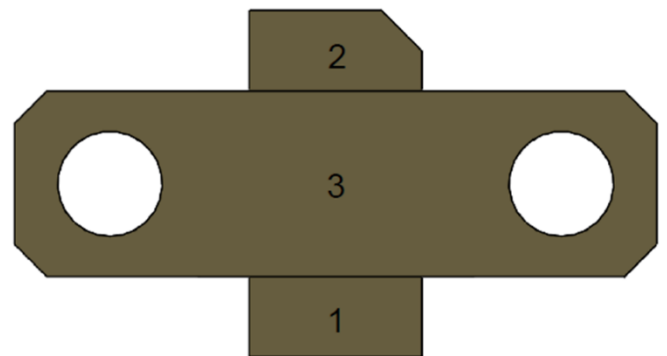
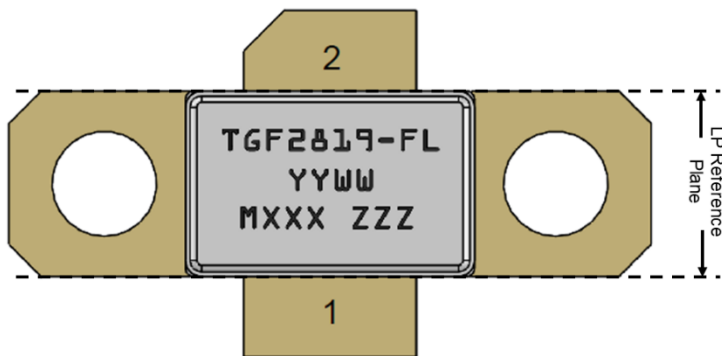
1. Test Conditions:  $V_D = +50\text{ V}$ ; Failure Criteria = 10 % reduction in  $I_{D\_MAX}$  during DC Life Testing .

Maximum Gate Current

**Maximum Gate Current Vs. Channel Temperature**



## Pin Layout<sup>1</sup>

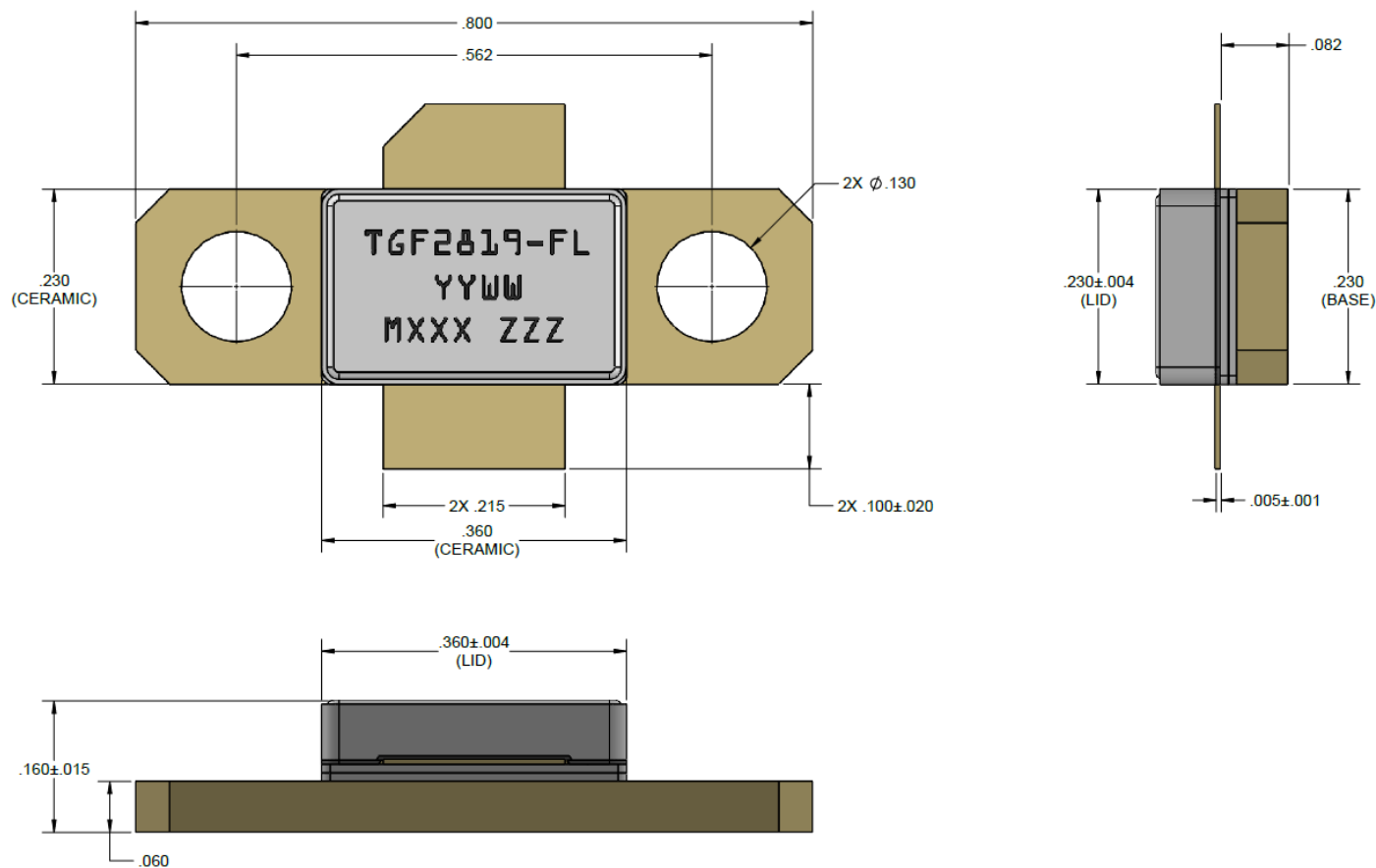


### Notes:

1. The TGF2819-FL will be marked with the "TGF2819-FL" designator and a lot code marked below the part designator. The "YY" represents the last two digits of the calendar year the part was manufactured, the "WW" is the work week of the assembly lot start, the "MXXX" is the production lot number, and the "ZZZ" is an auto-generated serial number.

| Pin | Symbol         | Description                        |
|-----|----------------|------------------------------------|
| 1   | RF IN / $V_G$  | Gate                               |
| 2   | RF OUT / $V_D$ | Drain                              |
| 3   | Source         | Source / Ground / Backside of part |

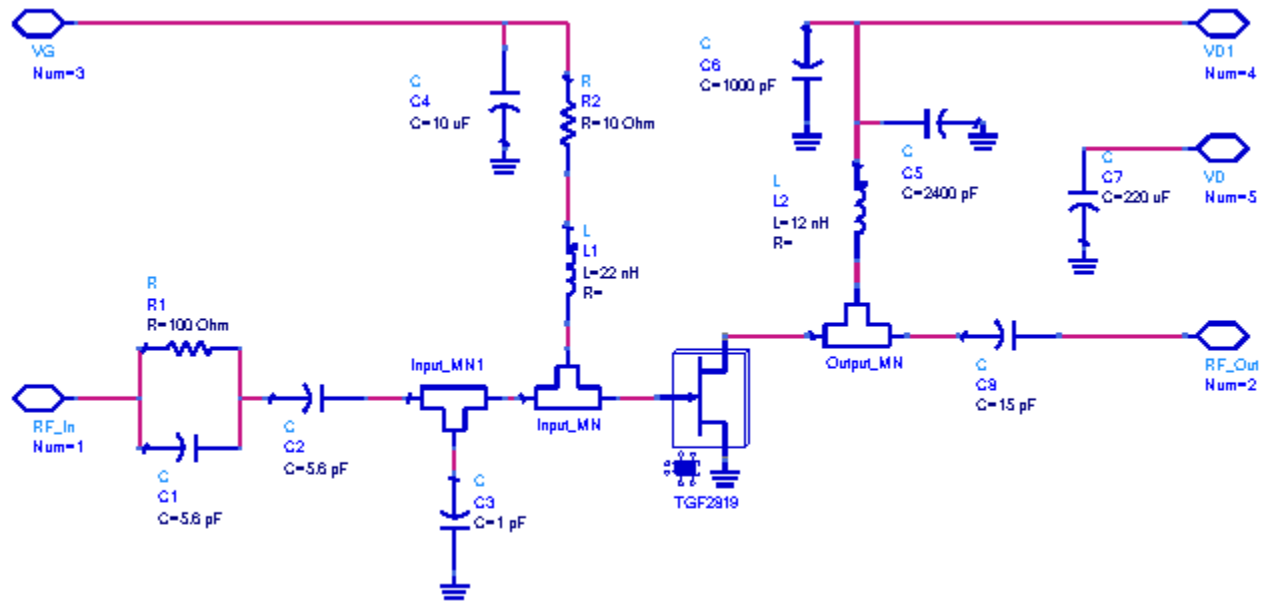
## Mechanical Drawing<sup>1-7</sup>



Note:

1. All dimensions are in inches. Angles are in degrees.
2. Dimension tolerance is  $\pm 0.005$  inches, unless otherwise noted.
3. Material:  
Package Base: Ceramic / Metal  
Package Lid: Ceramic
4. Package exposed metallization is gold plated.
5. Part is epoxy sealed.
6. Part meets industry NI360 footprint.
7. Body dimensions do not include epoxy runout which can be up to 0.020 inches per side.

### 3.1 – 3.5 GHz Application Circuit - Schematic



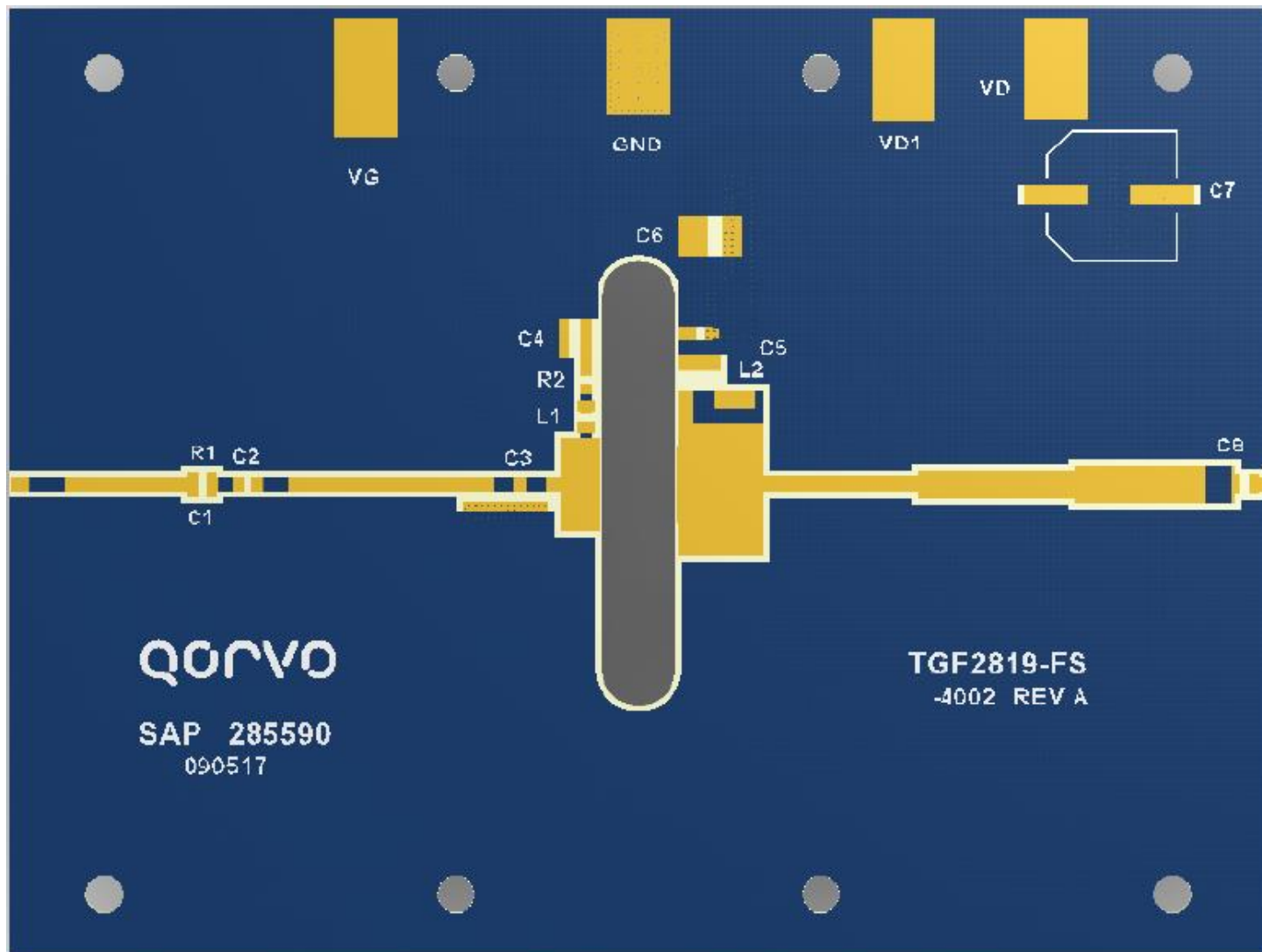
| Bias-up Procedure                                     | Bias-down Procedure                                      |
|-------------------------------------------------------|----------------------------------------------------------|
| 1. Set $V_G$ to -4 V.                                 | 1. Turn off RF signal.                                   |
| 2. Set $I_D$ current limit to 260 mA.                 | 2. Turn off $V_D$ .                                      |
| 3. Apply 32 V $V_D$ .                                 | 3. Wait 2 seconds to allow drain capacitor to discharge. |
| 4. Slowly adjust $V_G$ until $I_D$ is set to 250 mA.  | 4. Turn off $V_G$ .                                      |
| 5. Set $I_D$ current limit to 2 A (Pulsed operation.) |                                                          |
| 6. Apply RF.                                          |                                                          |

### 3.1 – 3.5 GHz Application Circuit - Bill of Materials

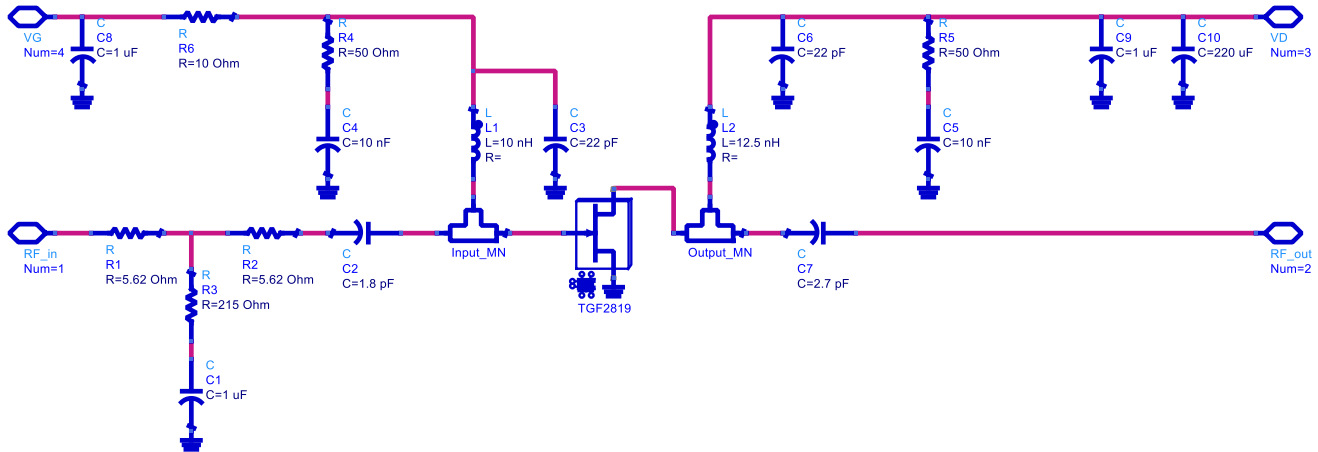
| Reference Design | Value  | Qty | Manufacturer | Part Number         |
|------------------|--------|-----|--------------|---------------------|
| R1               | 100Ω   | 1   | Vishay/Dale  | CRCW0603100RJNTA    |
| C1, C2           | 5.6pF  | 2   | ATC          | 600S5R6BW250XT      |
| C3               | 1.0pF  | 1   | ATC          | 600S1R0AT250XT      |
| L1               | 22nH   | 1   | Coilcraft    | 0805CS-220XJEC      |
| R2               | 10Ω    | 1   | Vishay/Dale  | CRCW060310R0JNTA    |
| C4               | 10uF   | 1   | Murata       | C1632X5R0J106M130AC |
| L2               | 12nH   | 1   | Coilcraft    | A04TJLC             |
| C5               | 2400pF | 1   | Murata       | C08BL242X-5UN-X0T   |
| C6               | 1000pF | 1   | ATC          | 800B102JT50XT       |
| C7               | 220uF  | 1   | Panasonic    | EEEFK1H221P         |
| C8               | 15pF   | 1   | ATC          | 600S150FT250XT      |

### 3.1 – 3.5 GHz Application Circuit - Layout

Board material is RO4350B 0.020" thickness with 2oz copper cladding. Overall EVB size is 3" x 4".



### 1.35 – 1.75 GHz Application Circuit - Schematic



#### Bias-up Procedure

2. Set  $V_G$  to -4 V.
4. Set  $I_D$  current limit to 220 mA.
5. Apply 50 V  $V_D$ .
6. Slowly adjust  $V_G$  until  $I_D$  is set to 200 mA.
8. Set  $I_D$  current limit to 3.5 A (Pulsed operation.)
9. Apply RF.

#### Bias-down Procedure

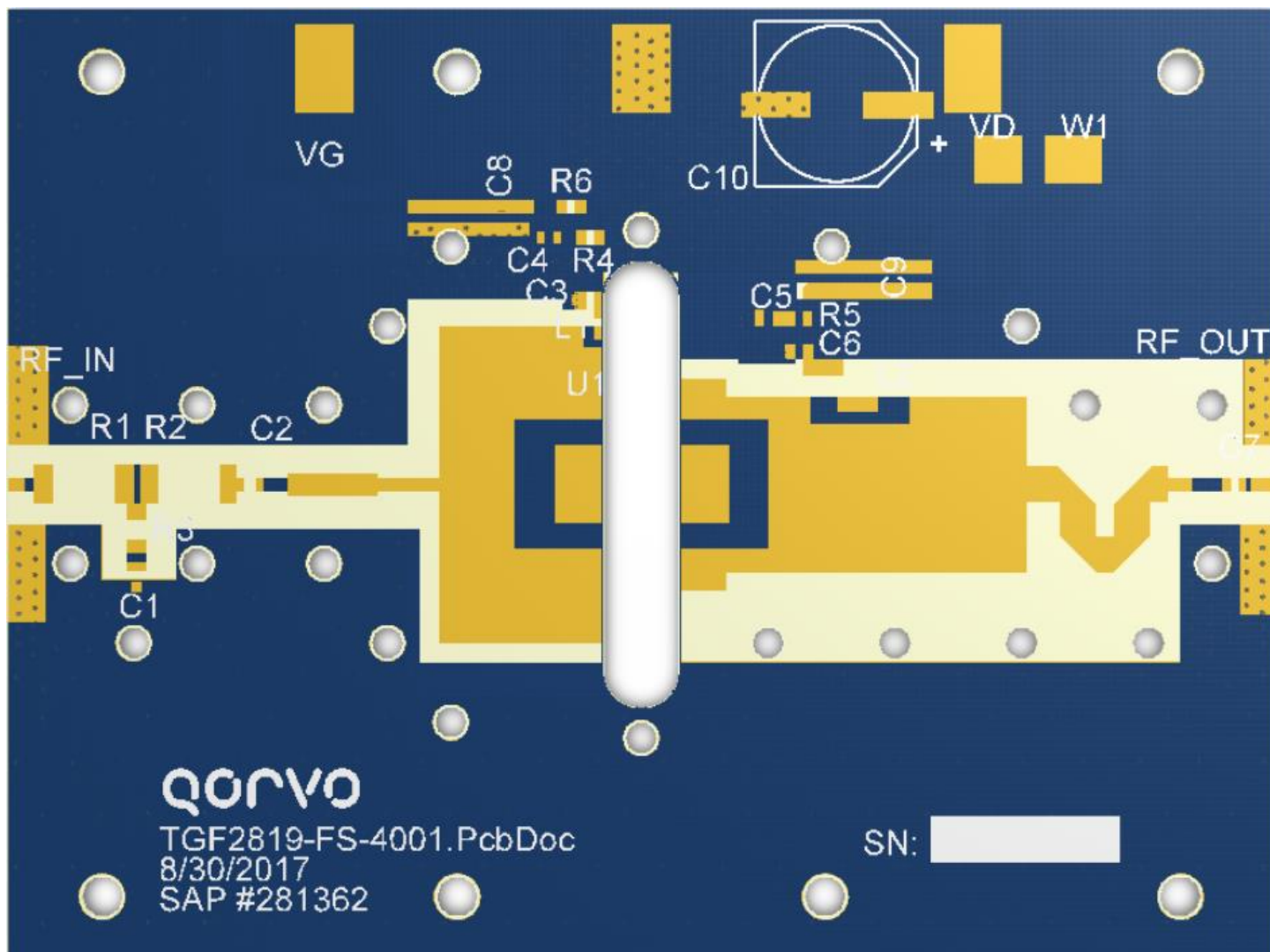
3. Turn off RF signal.
4. Turn off  $V_D$
5. Wait 2 seconds to allow drain capacitor to discharge.
7. Turn off  $V_G$

### 1.35 – 1.75 GHz Application Circuit - Bill of Materials

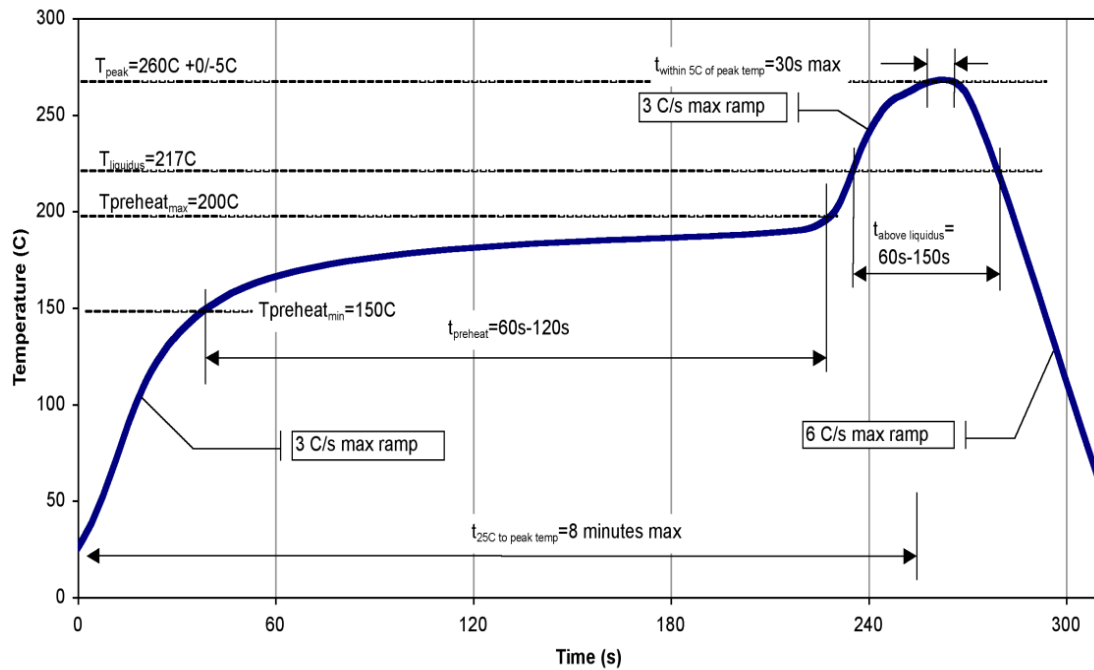
| Reference Design | Value   | Qty | Manufacturer       | Part Number          |
|------------------|---------|-----|--------------------|----------------------|
| C1, C8           | 1 uF    | 2   | Murata             | GCM188R71C105KA64D   |
| C2               | 1.8 pF  | 1   | ATC                | 600S1R8AT250X        |
| C3, C6           | 22 pF   | 2   | ATC                | 600S220FT250XT       |
| C7               | 2.7 pF  | 1   | ATC                | 600S2R7BW250XT       |
| C4, C5           | 10 nF   | 2   | Capax Technologies | 0603X103K101S        |
| C9               | 1 uF    | 1   | TDK                | CGA4J3X7S2A105K125AB |
| C10              | 220 uF  | 1   | Panasonic          | EEVTG1J221Q          |
| L1               | 10 nH   | 1   | Coilcraft          | 0603CS-10NXJEW       |
| L2               | 12.5 nH | 1   | Coilcraft          | A04TJLC              |
| R1, R2           | 5.6 Ohm | 2   | Panasonic          | ERJ-1TRQJ5R6U        |
| R3               | 215 Ohm | 1   | Panasonic          | ERA-8AEB2150V        |
| R6               | 10 Ohm  | 1   | Vishay             | CRCW060310R0JNTA     |
| R4, R5           | 50 Ohm  | 2   | Vishay             | CRCW060351R1FKEA     |

### 1.35 – 1.75 GHz Application Circuit - Layout

Board material is RO4350B 0.020" thickness with 2oz copper cladding. Overall EVB size is 3" x 4".



## Recommended Solder Temperature Profile



### Handling Precautions

| Parameter                        | Rating            | Standard                        |
|----------------------------------|-------------------|---------------------------------|
| ESD – Human Body Model (HBM)     | Class 1B (900 V)  | ANSI/ESDA/JEDEC Standard JS-001 |
| ESD – Charged Device Model (CDM) | Class C3 (1000 V) | ANSI/ESDA/JEDEC Standard JS-002 |
| MSL – Moisture Sensitivity Level | MSL 3             | IPC/JEDEC Standard J-STD-020    |



### Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.

Solder profiles available upon request.

Contact plating: Electrolytic Au over Ni

### RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free



### Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: [www.qorvo.com](http://www.qorvo.com)

Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9