

MOSFET

OptiMOS™5 Power-Transistor, 100 V

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

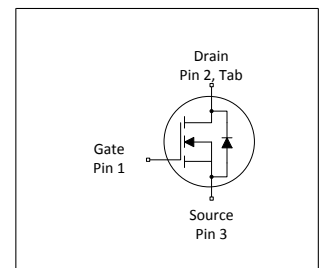
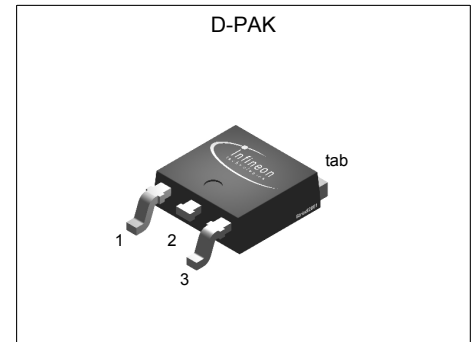


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	5.0	mΩ
I_D	80	A
Q_{OSS}	67	nC
$Q_G(0V..10V)$	51	nC

Type / Ordering Code	Package	Marking	Related Links
IPD050N10N5	P-TO252-3	050N10N5	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	80 80	A	$T_C=25\text{ °C}^{1)}$ $T_C=100\text{ °C}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ²⁾	E_{AS}	-	-	110	mJ	$I_D=80\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	150	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.6	1	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	75	K/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ³⁾	R_{thJA}	-	-	50	K/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL1

¹⁾ See Diagram 3 for more detailed information

²⁾ See Diagram 13 for more detailed information

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=84\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.3 5.1	5 6.7	m Ω	$V_{GS}=10\text{ V}$, $I_D=40\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=20\text{ A}$
Gate resistance ¹⁾	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	48	95	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=40\text{ A}$

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3600	4700	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	560	730	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	25	44	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	7	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	16	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	10	16	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	16	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	51	64	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	67	89	nC	$V_{DD}=50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	80	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=40\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	48	96	ns	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	62	124	nC	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

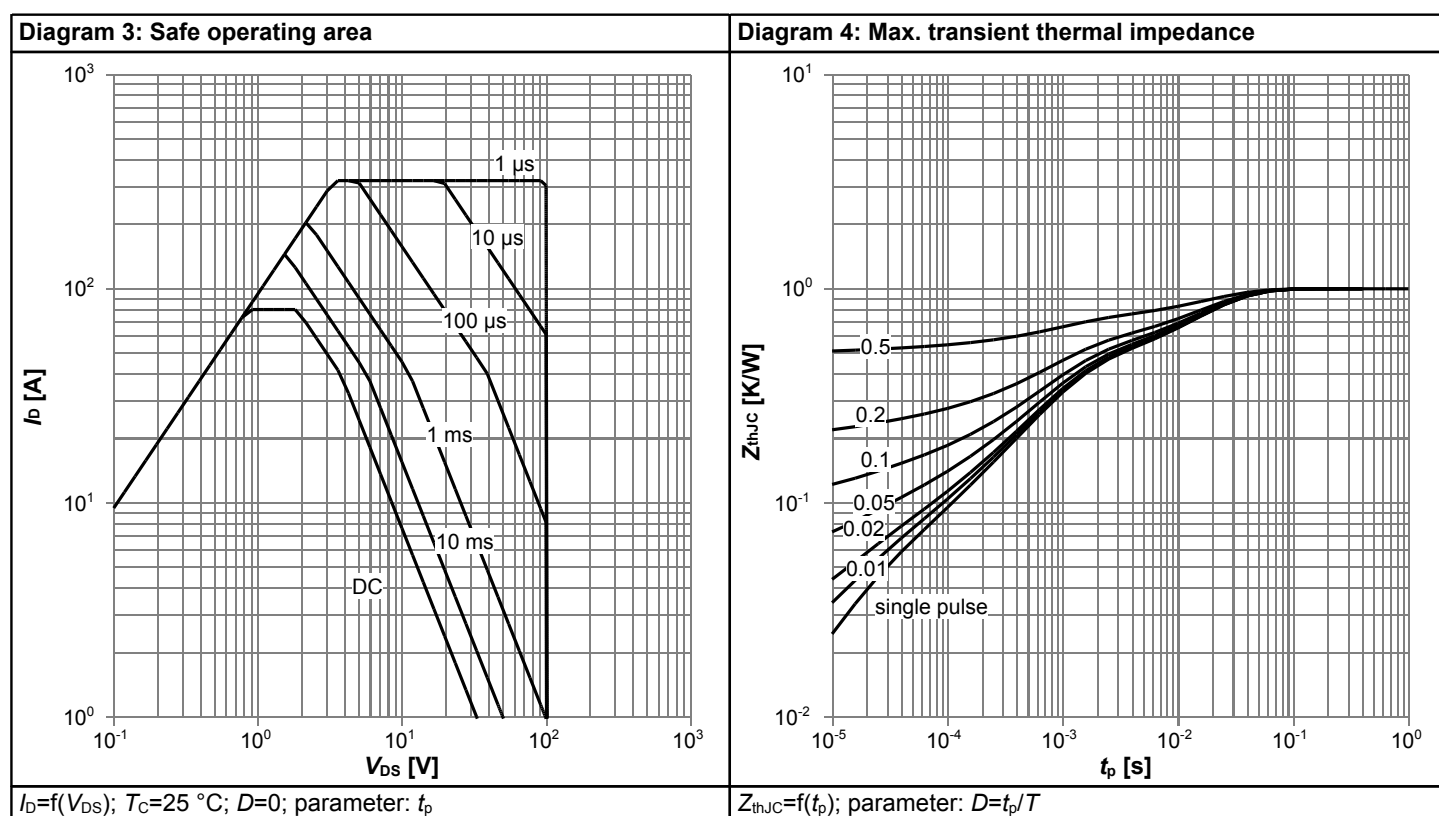
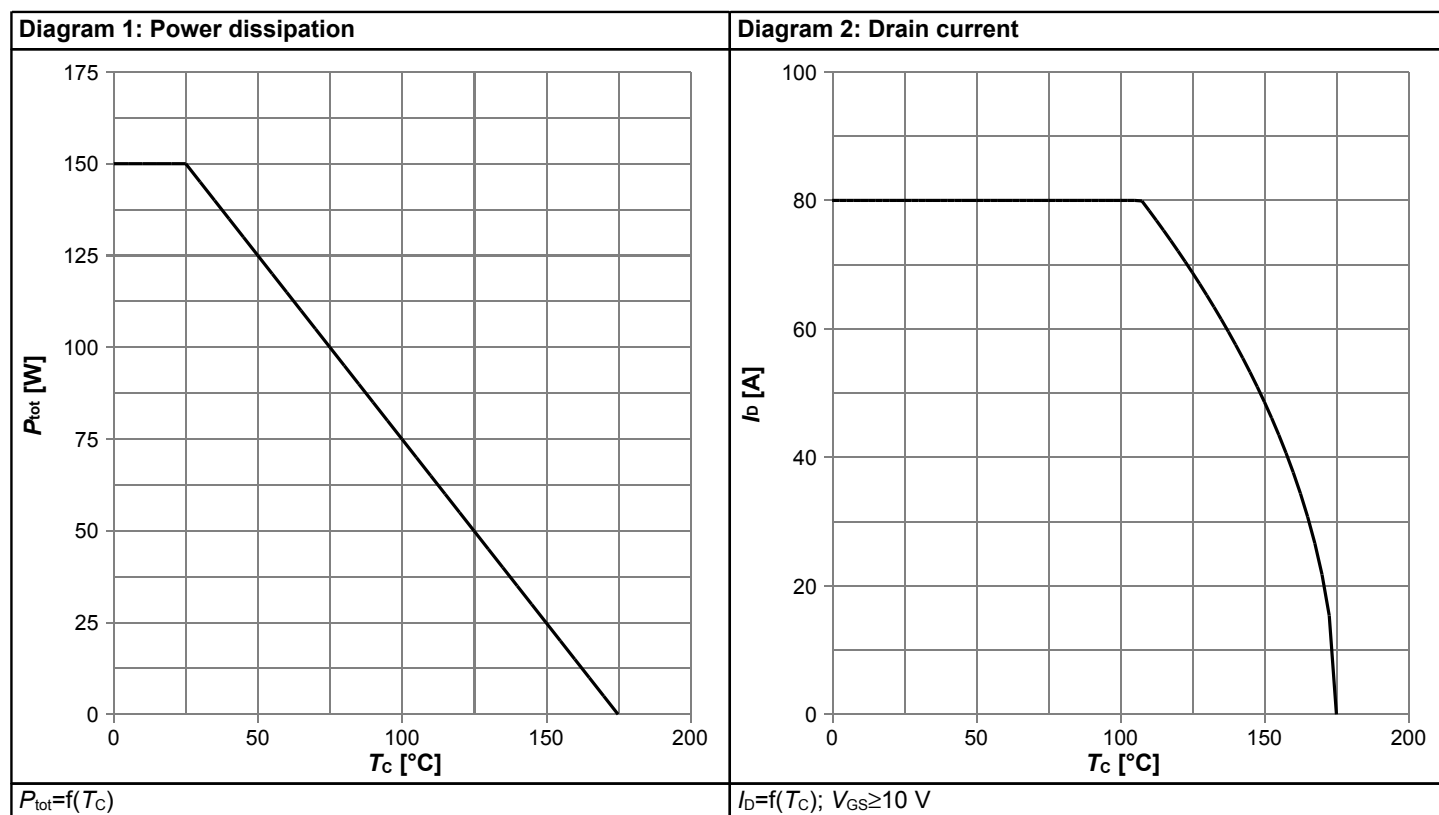
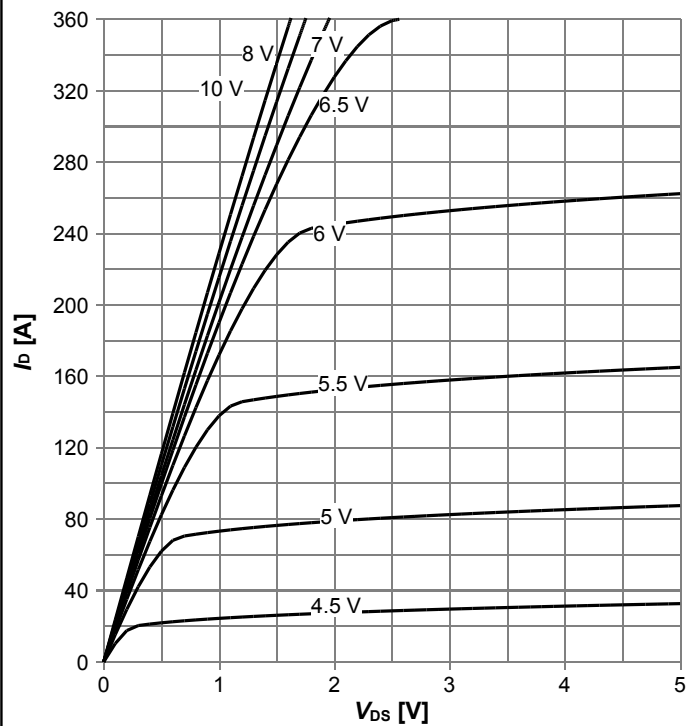
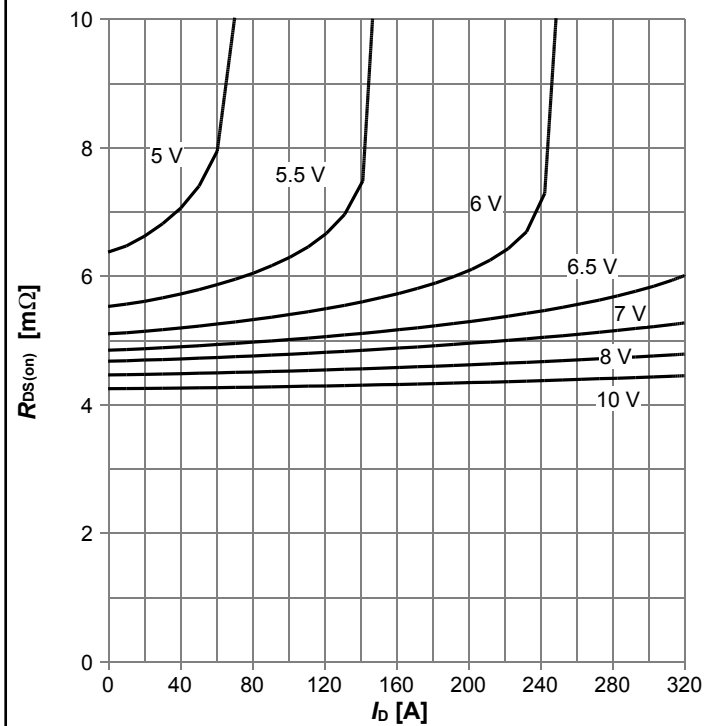


Diagram 5: Typ. output characteristics



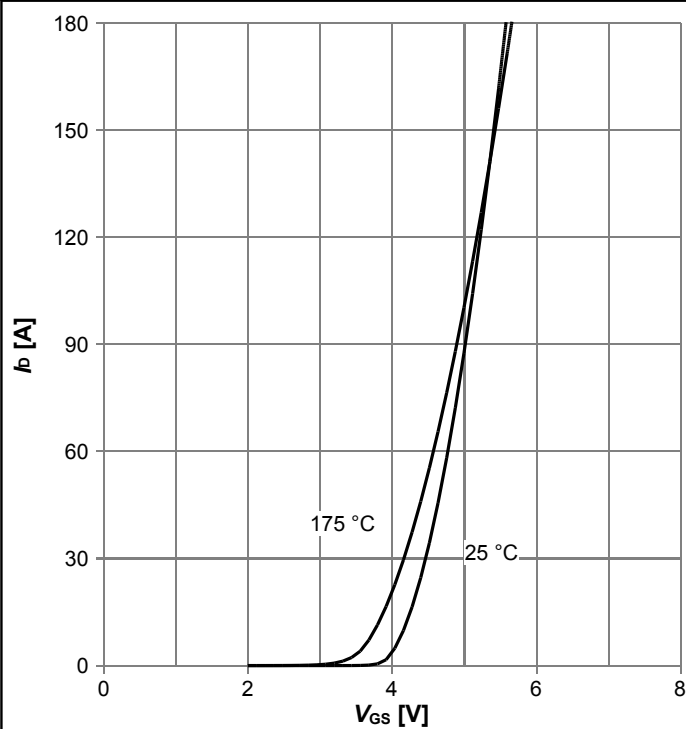
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



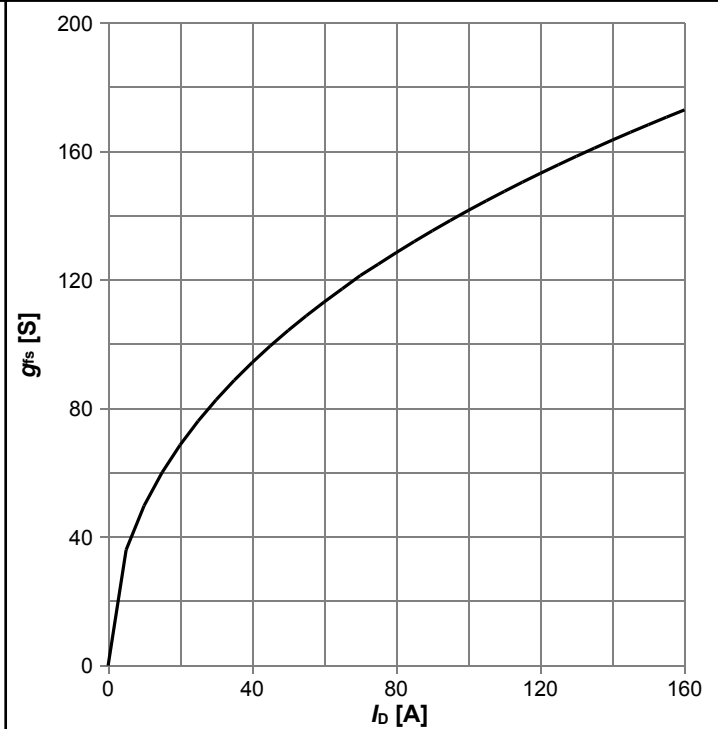
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



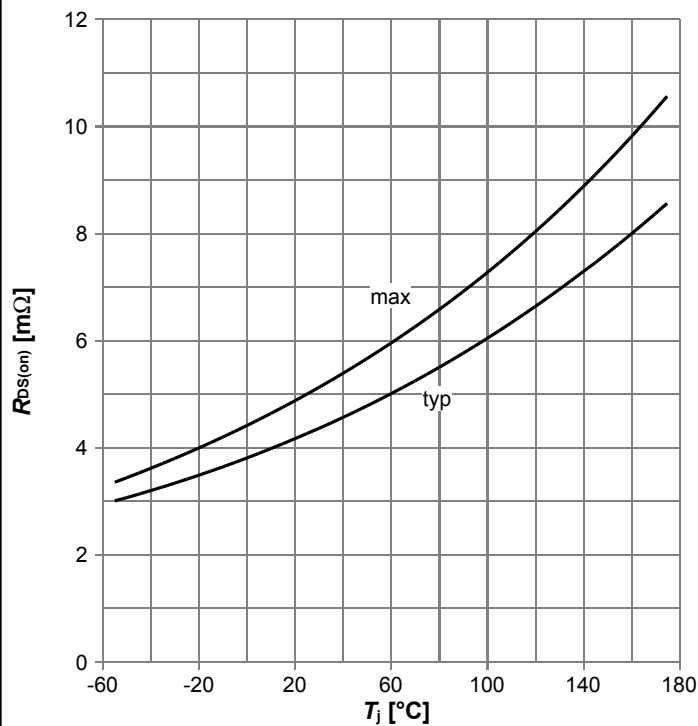
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



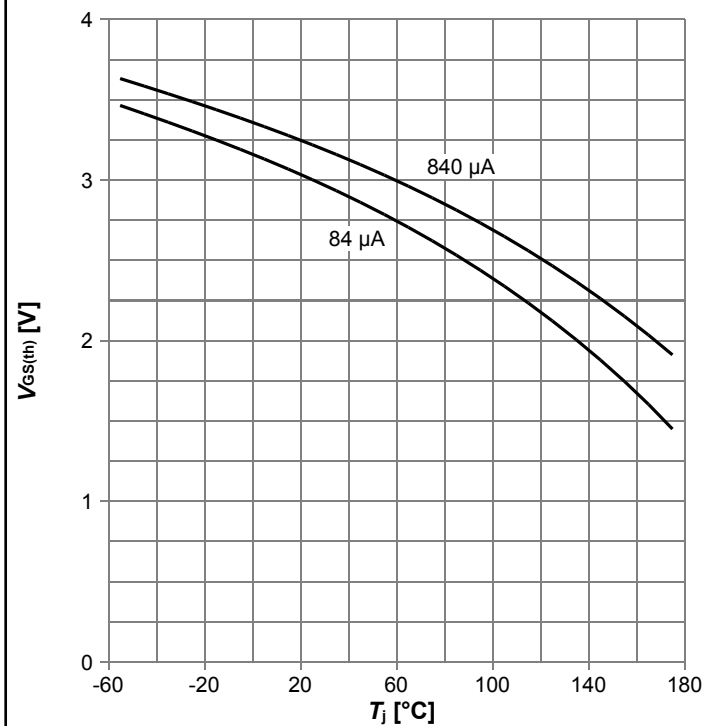
$g_{fs} = f(I_D)$; $T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



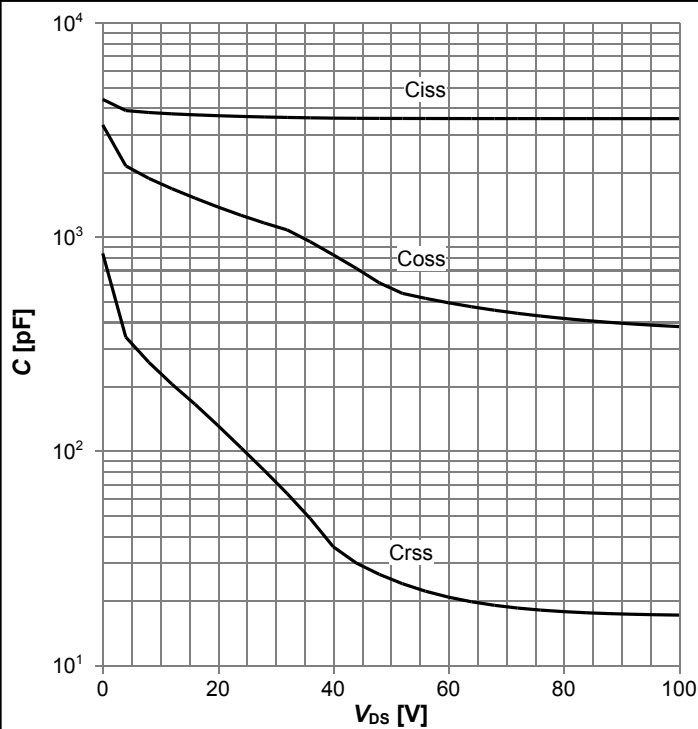
$R_{DS(on)} = f(T_j)$; $I_D = 40$ A; $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



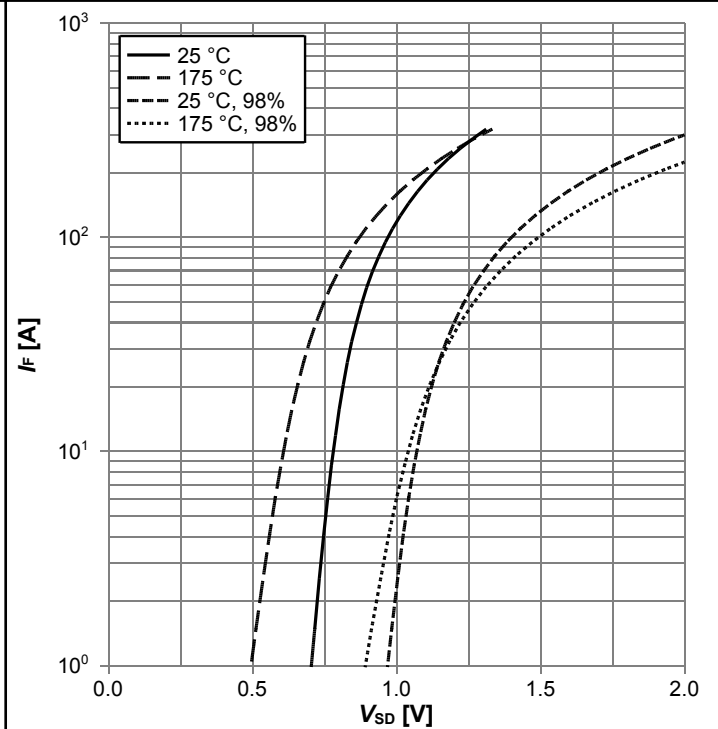
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



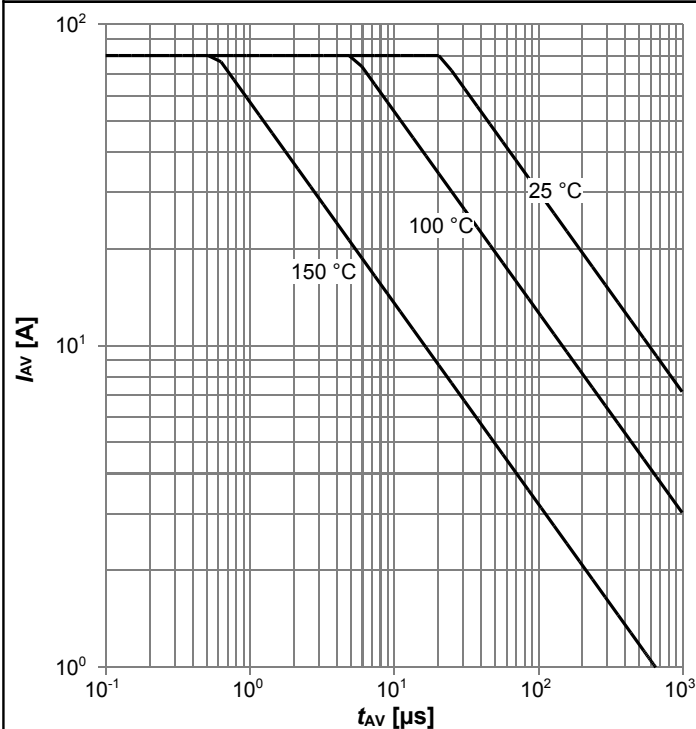
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



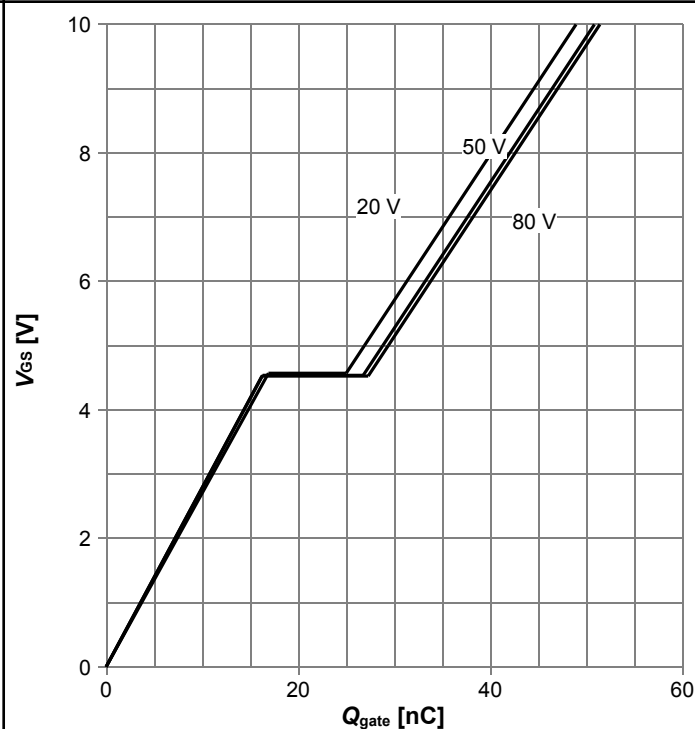
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



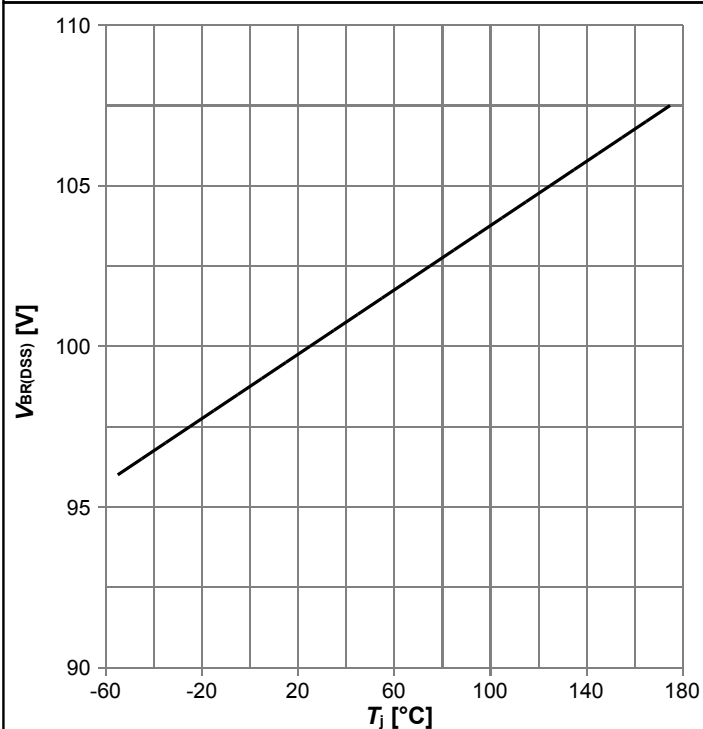
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



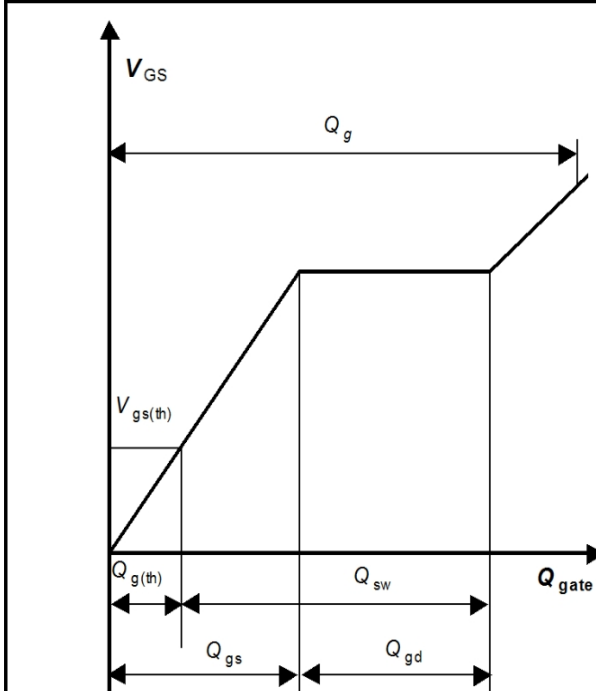
$V_{GS}=f(Q_{gate})$; $I_D=40\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package Outlines

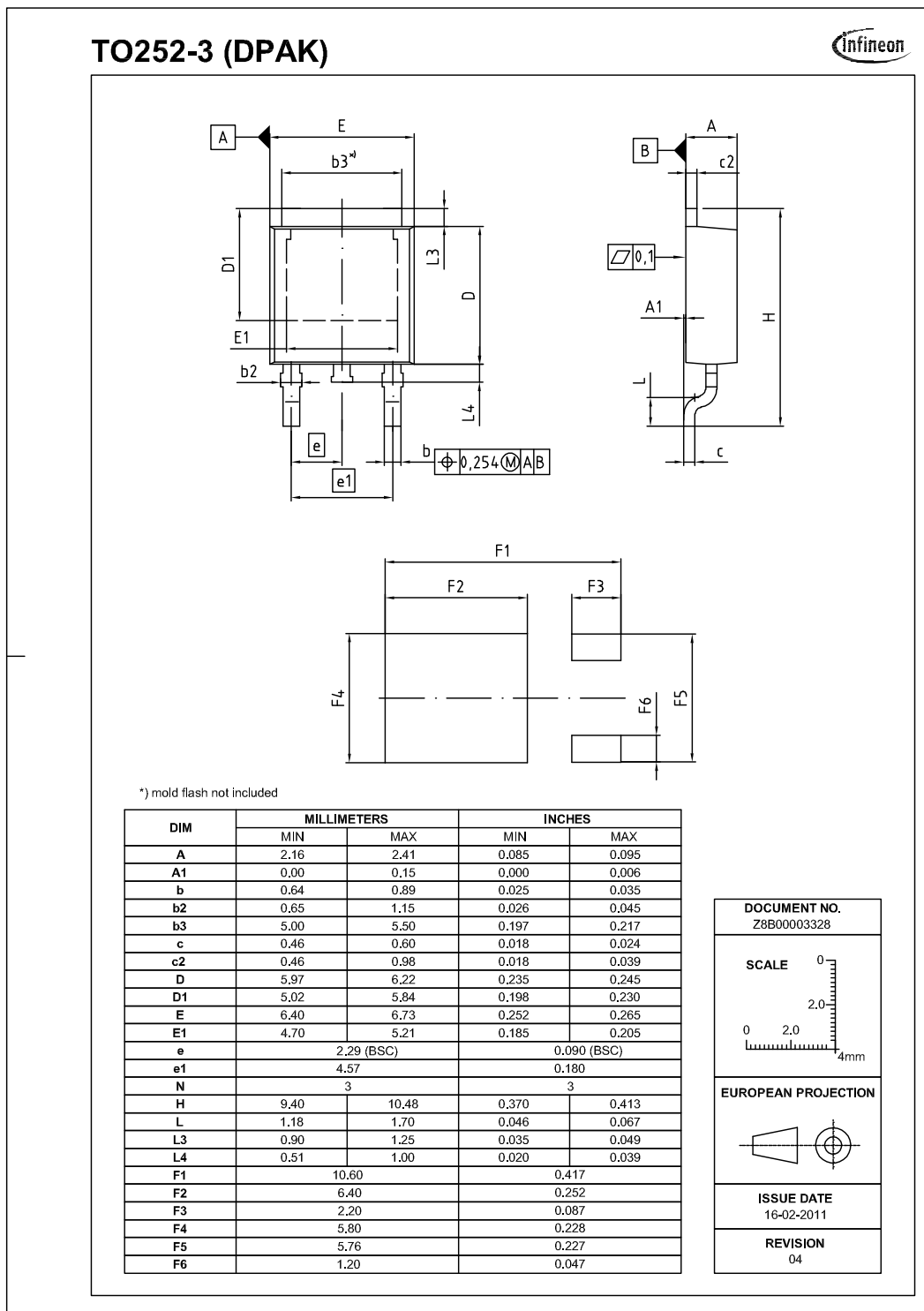


Figure 1 Outline P-TO252-3, dimensions in mm/inches

Revision History

IPD050N10N5

Revision: 2017-01-17, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-11-22	Release of final version
2.1	2017-01-17	Update Idss max at Tj=25°C

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9