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January 2014

# FDMC86340

# N-Channel Shielded Gate Power Trench $^{\circledR}$ MOSFET 80 V, 48 A, 6.5 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 6.5 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 14 A
- Max  $r_{DS(on)} = 8.5 \text{ m}\Omega$  at  $V_{GS} = 8 \text{ V}$ ,  $I_D = 12 \text{ A}$
- High performance technology for extremely low r<sub>DS(on)</sub>
- Termination is Lead-free
- RoHS Compliant

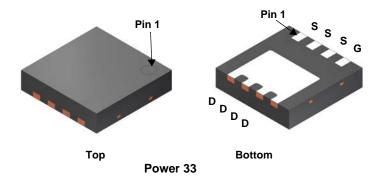


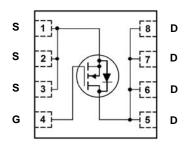
#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

#### **Application**

■ DC-DC Conversion





## MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter				Ratings	Units
V <sub>DS</sub>	Drain to Source \	/oltage			80	V
V <sub>GS</sub>	Gate to Source V	/oltage			±20	V
I <sub>D</sub>	Drain Current	-Continuous	T <sub>C</sub> = 25 °C		48	
		-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	14	Α
		-Pulsed		(Note 4)	200	
E <sub>AS</sub>	Single Pulse Ava	lanche Energy		(Note 3)	216	mJ
D	Power Dissipatio	n	T <sub>C</sub> = 25 °C		54	w
$P_{D}$	Power Dissipation	n	T <sub>A</sub> = 25 °C	(Note 1a)	2.3	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and St	orage Junction Temperate	ure Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86340	FDMC86340	Power33	13 "	12 mm	3000 units

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units		
Off Characteristics								
$BV_DSS$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	80			V		
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		46		mV/°C		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V			1	μΑ		
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA		

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$	2.0	3.4	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		-10		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A		5.0	6.5	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 8 V, I <sub>D</sub> = 12 A		6.0	8.5	mΩ
, ,		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A, T <sub>J</sub> = 125 °C		8.5	11	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 14 A		36		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	.,		2775	3885	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz		468	655	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12		15	25	pF
$R_q$	Gate Resistance		0.1	0.7	2.1	Ω

#### **Switching Characteristics**

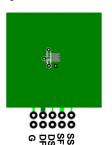
t <sub>d(on)</sub>	Turn-On Delay Time		20	32	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 14 A,	7.9	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	23	37	ns
t <sub>f</sub>	Fall Time		5.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	38	53	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 8 \text{ V}$ $V_{DD} = 40 \text{ V},$	31	44	nC
Q <sub>gs</sub>	Gate to Source Charge	I <sub>D</sub> = 14 A	14		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		8.0		nC
Q <sub>oss</sub>	Output Charge	$V_{DD} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	42		nC

#### **Drain-Source Diode Characteristics**

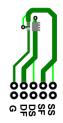
V 6	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 14 A	(Note 2)	0.8	1.3	V
v SD	V <sub>SD</sub> Source to Drain blode Forward voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.9 \text{ A}$	(Note 2)	0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 14 A, di/dt = 100 A/μs		41	66	ns
Q <sub>rr</sub>	Reverse Recovery Charge			25	40	nC

#### Notes:

<sup>1.</sup> R<sub>0JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.
- 3.  $E_{AS}$  of 216 mJ is based on starting  $T_{J} = 25$  °C, L = 3 mH,  $I_{AS} = 12$  A,  $V_{DD} = 80$  V,  $V_{GS} = 10$  V. 100% test at L = 0.1 mH,  $I_{AS} = 37$  A.
- 4. Pulsed Id limited by junction temperature, td<=100  $\mu$ S, please refer to SOA curve for more details.

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

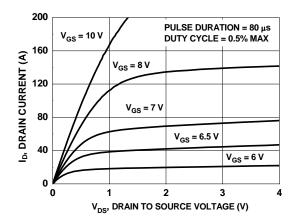


Figure 1. On-Region Characteristics

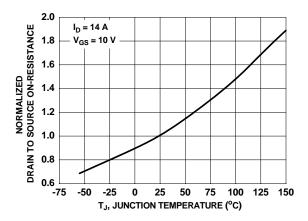


Figure 3. Normalized On-Resistance vs Junction Temperature

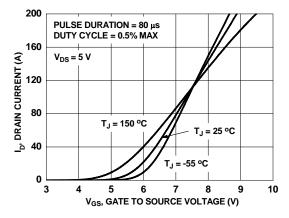


Figure 5. Transfer Characteristics

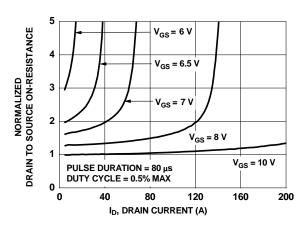


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

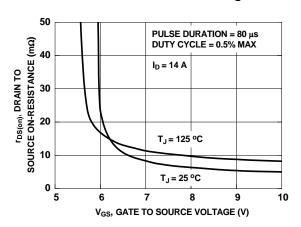


Figure 4. On-Resistance vs Gate to Source Voltage

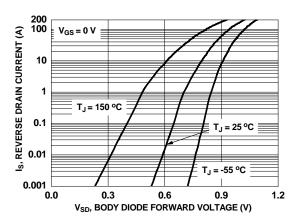


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

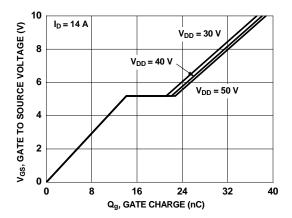


Figure 7. Gate Charge Characteristics

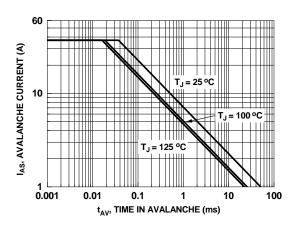


Figure 9. Unclamped Inductive Switching Capability

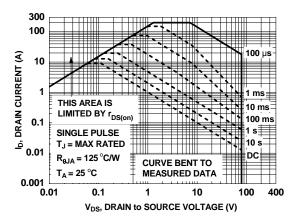


Figure 11. Forward Bias Safe Operating Area

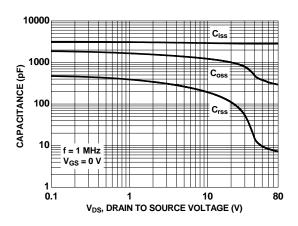


Figure 8. Capacitance vs Drain to Source Voltage

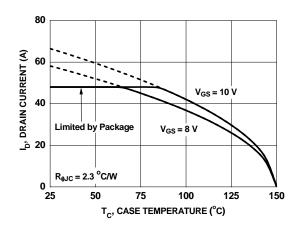


Figure 10. Maximum Continuous Drain Current vs Case Temperature

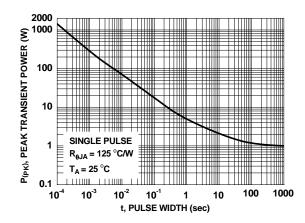


Figure 12. Single Pulse Maximum Power Dissipation



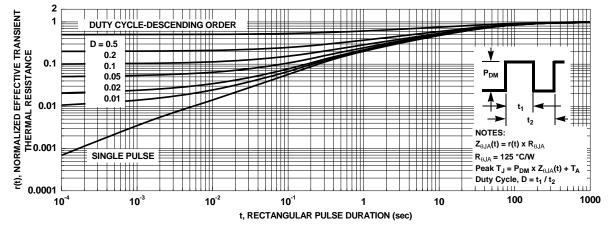
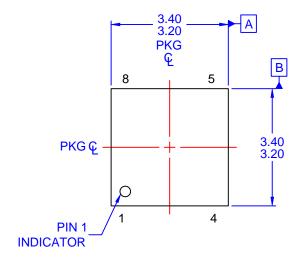
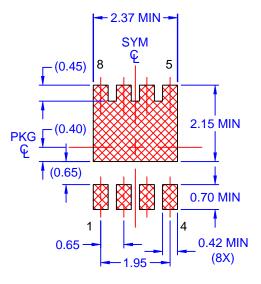
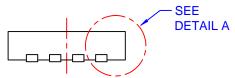


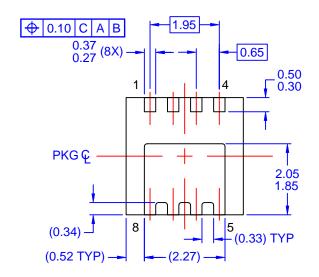
Figure 13. Junction-to-Ambient Transient Thermal Response Curve





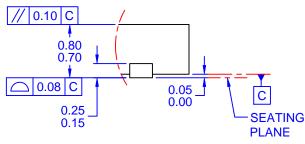


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