

N-channel 650 V, 0.32 Ω typ., 11 A MDmesh™ M2 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

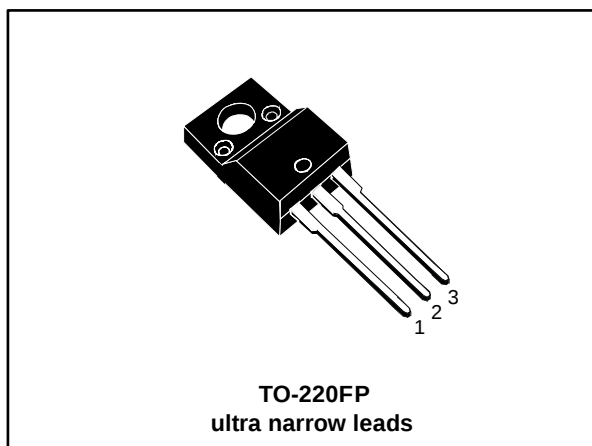
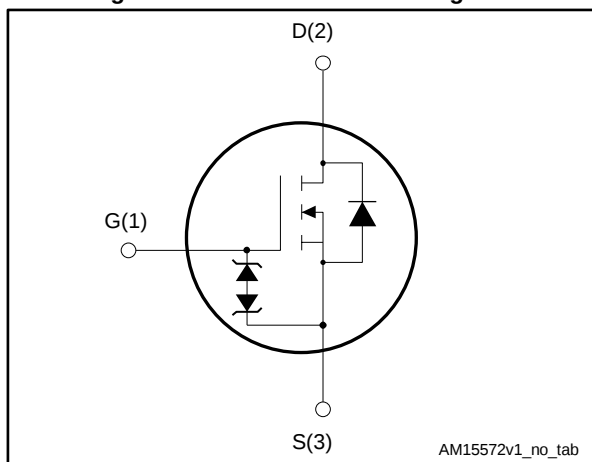


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STFU16N65M2	650 V	0.36 Ω	11 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STFU16N65M2	16N65M2	TO-220FP ultra narrow leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	11 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	6.9 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	44 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:⁽¹⁾Limited by maximum junction temperature..⁽²⁾Pulse width limited by safe operating area.⁽³⁾ $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DSpeak} < V_{(BR)DSS}$, $V_{DD}=400\text{ V}$ ⁽⁴⁾ $V_{DS} \leq 520\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^{\circ}\text{C/W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1.9	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	360	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	650			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{GS} = 0 V, V _{DS} = 650 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 5.5 A		0.32	0.36	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	718	-	pF
C _{oss}	Output capacitance		-	32	-	pF
C _{rss}	Reverse transfer capacitance		-	1.1	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	189	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.2	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 11 A, V _{GS} = 0 to 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	19.5	-	nC
Q _{gs}	Gate-source charge		-	4	-	nC
Q _{gd}	Gate-drain charge		-	8.3	-	nC

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 5.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	11.3	-	ns
t _r	Rise time		-	8.2	-	ns
t _{d(off)}	Turn-off delay time		-	36	-	ns
t _f	Fall time		-	11.3	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	342		ns
Q_{rr}	Reverse recovery charge		-	3.5		μC
I_{RRM}	Reverse recovery current		-	20.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	458		ns
Q_{rr}	Reverse recovery charge		-	4.6		μC
I_{RRM}	Reverse recovery current		-	20.5		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

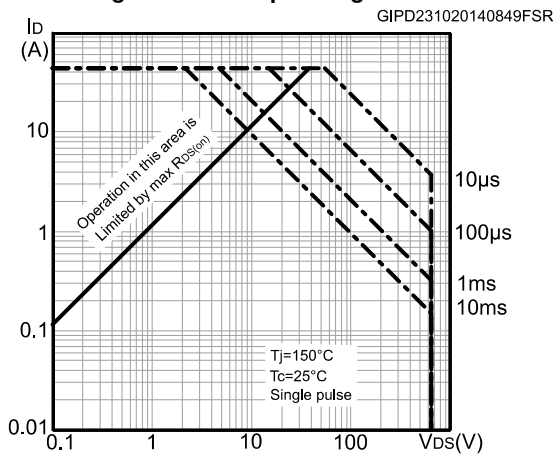


Figure 3: Thermal impedance

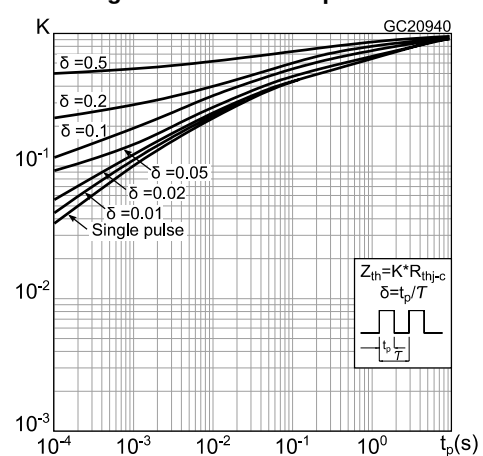


Figure 4: Output characteristics

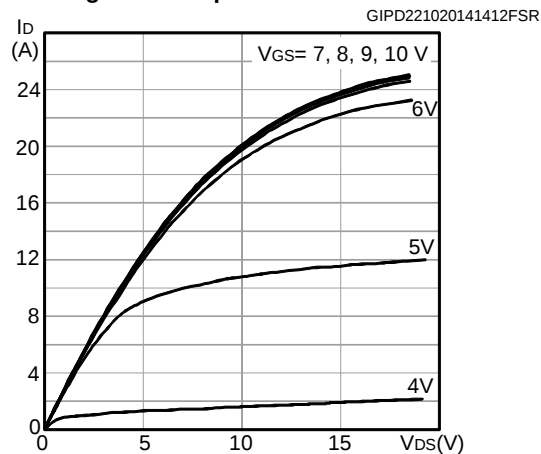


Figure 5: Transfer characteristics

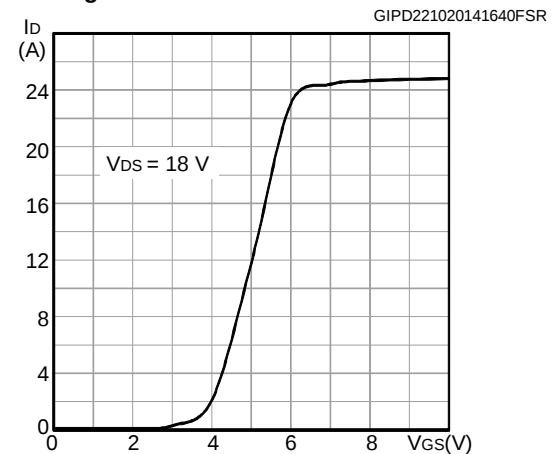


Figure 6: Normalized VBR(DSS) vs. temperature

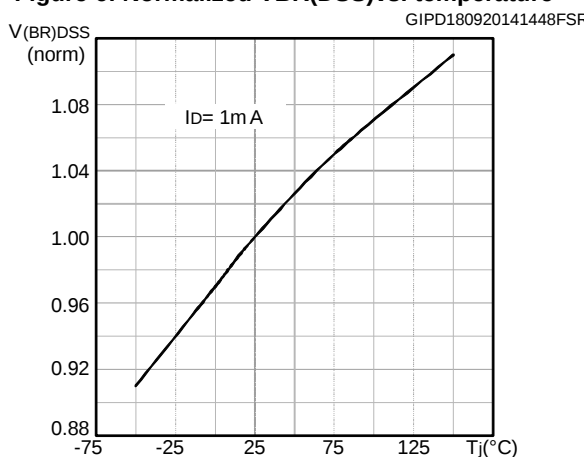


Figure 7: Static drain-source on-resistance

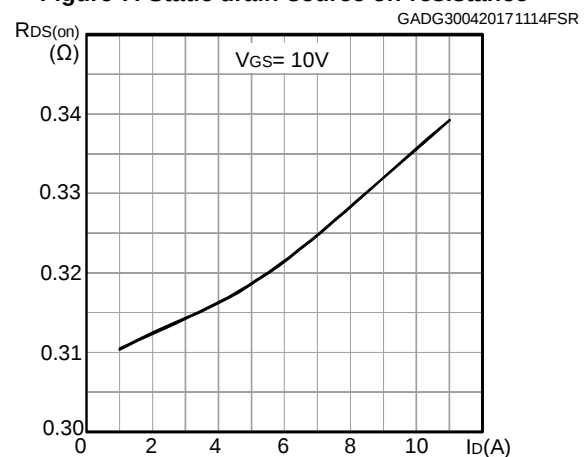


Figure 8: Gate charge vs. gate-source voltage

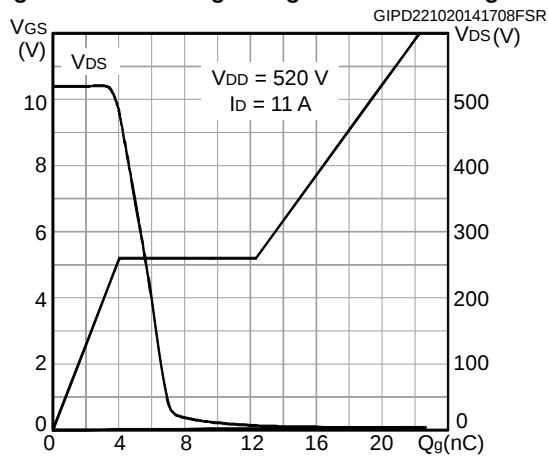


Figure 9: Capacitance variations

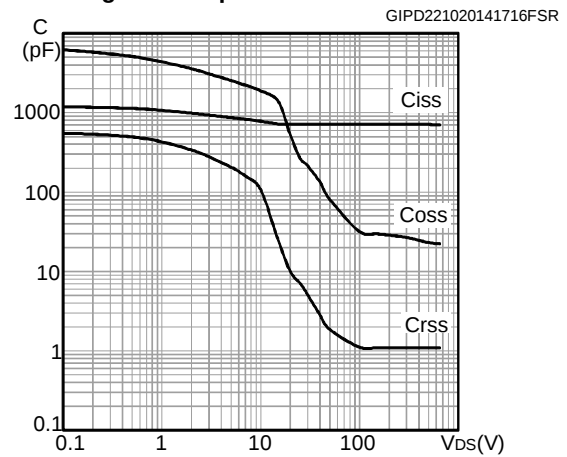


Figure 10: Normalized gate threshold voltage vs. temperature

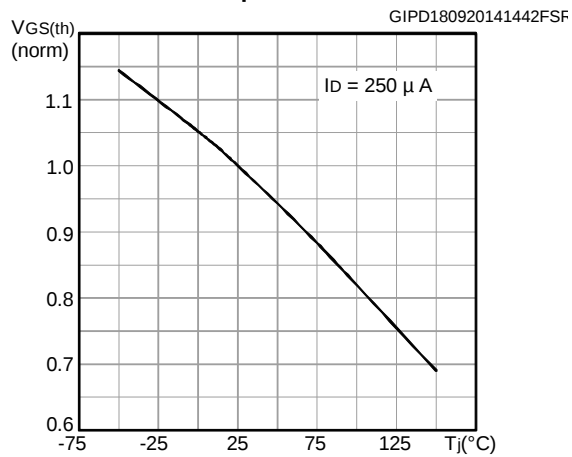


Figure 11: Normalized on-resistance vs. temperature

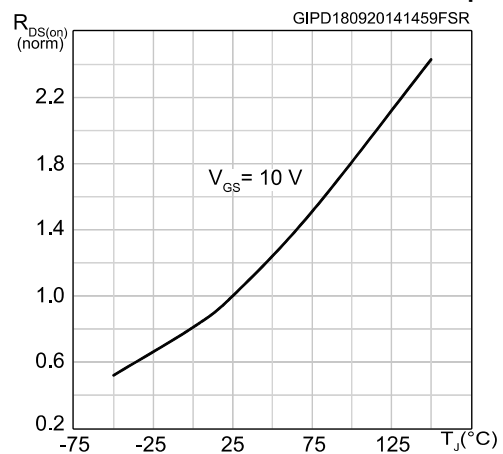


Figure 12: Source-drain diode forward characteristics

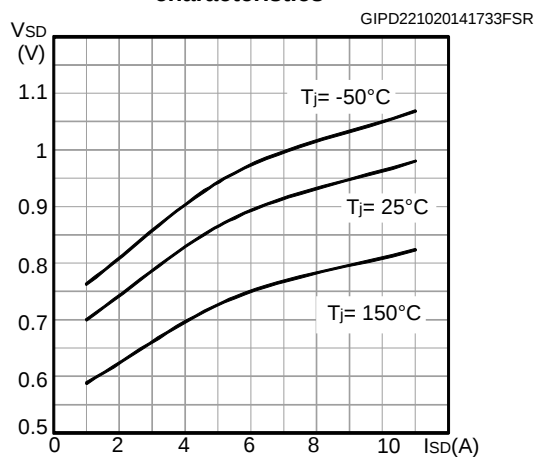
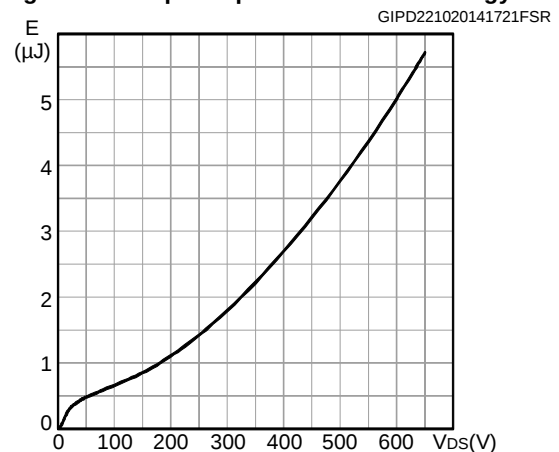
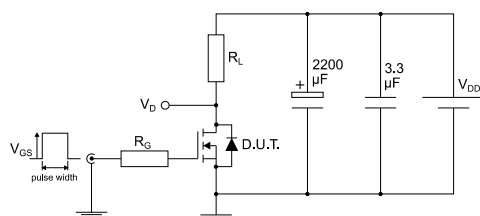


Figure 13: Output capacitance stored energy



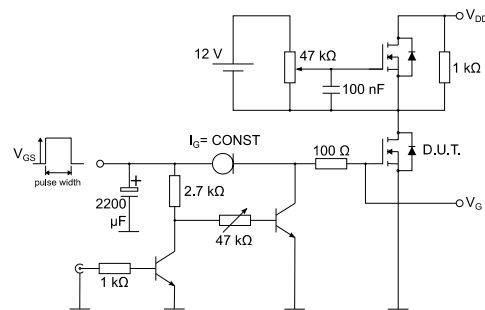
3 Test circuits

Figure 14: Test circuit for resistive load switching times



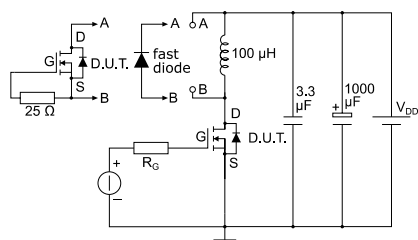
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Figure 15: Test circuit for gate charge behavior



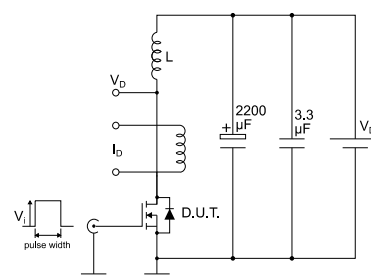
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Figure 16: Test circuit for inductive load switching and diode recovery times



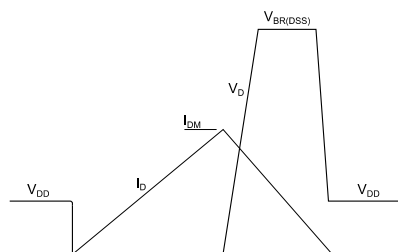
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Figure 17: Unclamped inductive load test circuit



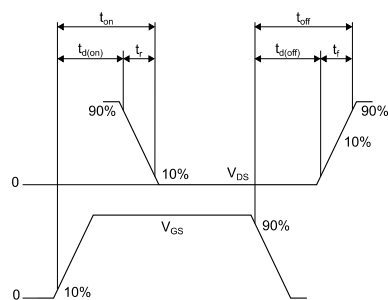
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Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 20: TO-220FP ultra narrow leads package outline

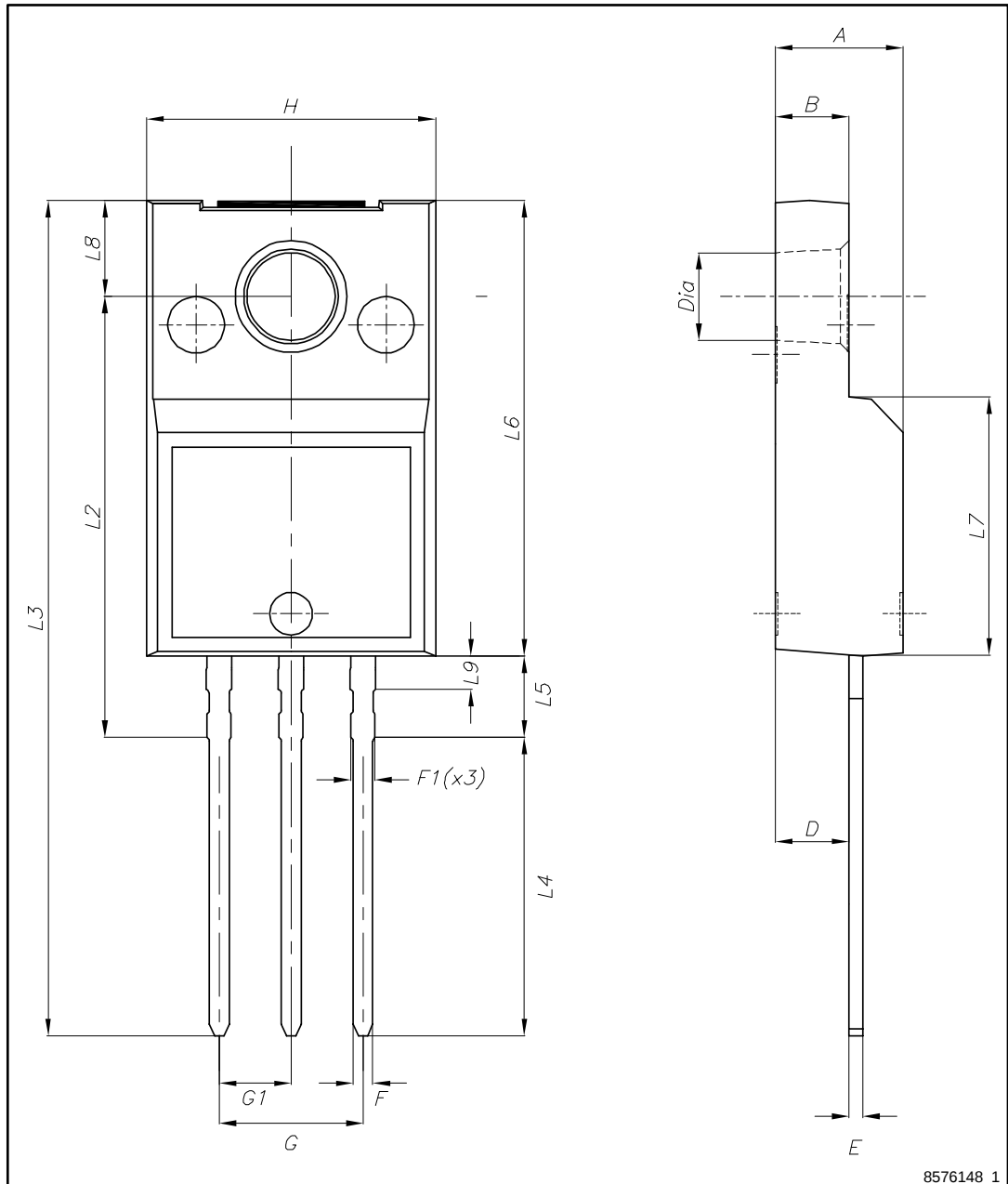


Table 9: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Apr-2017	1	Initial release

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