## 88X5113

Integrated 100G/40G/Quad 25 Gbps Ethernet PHY with Copper Cable and Backplane Drive Capability

## Datasheet - Public

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## PRODUCT OVERVIEW

The Marvell ${ }^{\circledR} 88 \times 5113$ device is a fully integrated single chip Ethernet transceiver that supports 25 GbE full-duplex transmission, over a variety of media including optics, passive copper cables and backplanes.
The device operates as a single port 100 Gbps Ethernet PHY/Quad port 25 Gbps Ethernet PHY. In this mode, the 88X5113 100 GbE and 25 GbE transmission over a variety of media including optics, passive copper cables and backplanes.
The 88X5113 has long reach SERDES, and includes Auto-Negotiation and coefficient training functionality.
In the 100 Gbps and 25 Gbps Ethernet PHY modes, the $88 \times 5113$ connects to the MAC/Switch device over a CAUI-4 or 25GAUI interface respectively. On the host interface, the device also supports the IEEE 802.3 Clause 91 100G Reed Solomon Forward Error Correction (RS-FEC) as well as the IEEE 802.3 Clause 108 RS-FEC and IEEE 802.3 Clause 74 KR-FEC for 25 GbE operation. These along with the support for Auto-Negotiation and training protocol enable the device to interface with the MAC over a 100G-KR4/25G-KR backplane link.
The PHY mode, the line interface of the 88 X 5113 , is fully compliant to the IEEE 802.3bj and IEEE 802.3bm standards for 100 GbE and IEEE 802.3 by specifications for 25 GbE operation over passive copper cables, optics and backplanes. The device supports the IEEE 802.3 Clause 91 and IEEE 802.3 Clause 108 Reed Solomon Forward Error Correction (RS-FEC) features, IEEE 802.3 Clause 74 KR-FEC, and Auto-Negotiation and coefficient training protocol required by the IEEE 802.3bj and IEEE 802.3by standards.

Internal registers can be accessed via an MDIO/MDC serial management interface which is compliant with IEEE 802.3 specification Clause 45 . An MDC frequency of up to 25 MHz supported.

The $88 \times 5113$ is manufactured in a $14 \mathrm{~mm} \times 14 \mathrm{~mm}$ 169-pin FCBGA package.

## Features

- Single port $100 \mathrm{GbE} /$ Quad 25 GbE PHY functionality
- Line equalization capability that meets IEEE 802.3bj and 802.3by specifications
- 100G/40GBASE-KR4/25G-KR compliant Host interface that exceed XLAUI/25GAUI requirements
- Fully autonomous adaptive equalization on line and host receivers
- 3 tap transmit FIR with programmable level and pre-emphasis
- Fully symmetric architecture with 100 GbE and 25 GbE RS-FEC and 10GE/25GE KR-FEC on both line and host interfaces
- Auto-Negotiation for backplanes and cable assemblies as defined by IEEE 802.3 Clause 73 of IEEE 802.3
- Support for transmit coefficient training protocol
- Clause 45 MDIO register access
- Ability to initialize the device from an external EEPROM
- Hardware interrupt pin for hardware interrupt generation capability
- LED pins with fully programmable event mapping and solid/blink modes
- Packet and PRBS pattern generation/checking capability
- Loopback mode for diagnostics
- Non-destructive eye monitors on all high speed interfaces
- IEEE-1149.1 and 1149.6 JTAG support
- Operating temperature range up to $105^{\circ} \mathrm{C}$ Junction
- $14 \mathrm{~mm} \times 14 \mathrm{~mm}$ 169-pin FCBGA package with 1 mm ball pitch


## Applications

- 25 Gbps Ethernet NICs
- $100 \mathrm{Gbps} / 25 \mathrm{Gbps}$ Ethernet line cards
- $100 \mathrm{Gbps} / 25 \mathrm{Gbps}$ Ethernet backplanes

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Figure 1: 88X5113 in a $\mathbf{2 5}$ GbE/100 GE Line Card Application


Figure 2: $88 \times 5113$ in a $\mathbf{2 5}$ GbE/100 GE Blade Switch/Server Application


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## General Device Description

The 88X5113 device is an Ethernet SERDES Transceiver that supports one port of 100GBASE-R4, consortium 50GBASE-R2, overclocked 40GBASE-R2, 40GBASE-R4, and four ports of 25GBASE-R, consortium 25GBASE-R, 10GBASE-R, 5GBASE-R, 2.5GBASE-X, 1000BASE-X, and SGMII on both the line and host interfaces. Auto-Negotiation, equalization and KR training are available to support backplane, twin-ax, and optical options in the various modes. Reed Solomon FEC and KR-FEC can be enabled as well. The various CAUI-4, XLPPI, XLAUI, SFI, XFI interfaces are supported.
The device can be used in PCS mode application where data is passed from one PCS to another PCS.

Device registers can be accessed through standard Clause 45 MDC/MDIO. The device operates from a $0.9 \mathrm{~V} / 0.95 \mathrm{~V}$ (I-temp operation) digital core voltage and a 1.0 V analog voltage. The digital I/O signals can operate at $3.3 \mathrm{~V}, 2.5 \mathrm{~V}, 1.8 \mathrm{~V}, 1.5 \mathrm{~V}, 1.2 \mathrm{~V}$, and 1.05 V . The device utilizes a $14 \mathrm{~mm} \times 14 \mathrm{~mm}$ $169-$ ball FCBGA package, and supports an operating junction temperature of up to $105^{\circ} \mathrm{C}$.

Figure 3: 88X5113 Device Functional Block Diagram


## 2 <br> Signal Description

Table 1: Pin Type Definitions

| Pin Type | Definition |
| :--- | :--- |
| H | Input with hysteresis |
| I/O | Input and output |
| I | Input only |
| O | Output only |
| PU | Internal pull-up |
| PD | Internal pull-down |
| OD | Open drain output |
| Z | Tri-state output |
| mA | DC sink capability |
| AI | Analog input |
| AO | Analog output |
| DI | Digital input |
| DO | Digital output |

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## $2.1 \quad$ Pin Map

|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A | AVSS | AVDDH | AVSS | AVDDH | RESETn | GPIO[3] | GPIO[2] | GPIO[1] | DVDD | AVDDL | AVSS | AVDDL | AVSS | A |
| B | $\mathrm{HIN}[3]$ | AVSS | HOP[3] | AVSS | TRSTn | TDO | GPIO[0] | SCL | SDA | AVSS | LOP[3] | AVSS | LIN[3] | B |
| C | HIP[3] | AVSS | HON[3] | AVSS | TMS | VSEL_N | VDDON | TCK | TDI | AVSS | LON[3] | AVSS | LIP[3] | C |
| D | AVSS | AVSS | AVSS | AVDDH | VSS | DVDD | VSS | DVDD | VSS | AVDDL | AVSS | AVSS | AVSS | D |
| E | HIN[2] | AVSS | HOP[2] | AVSS | DVDD | VSS | DVDD | VSS | DVDD | AVSS | LOP[2] | AVSS | LIN[2] | E |
| F | HIP[2] | AVSS | HON[2] | AVSS | VSS | DVDD | VSS | DVDD | VSS | AVSS | LON[2] | AVSS | LIP[2] | F |
| G | AVSS | AVDDH | AVSS | AVDDH | DVDD | VSS | DVDD | VSS | DVDD | AVDDL | AVSS | AVDDL | AVSS | G |
| H | HIN[1] | AVSS | HOP[1] | AVSS | VSS | DVDD | VSS | DVDD | VSS | AVSS | LOP[1] | AVSS | LIN[1] | H |
| J | HIP[1] | AVSS | HON[1] | AVSS | TEST[1] | CONFIG[2] | VDDOS | CONFIG[1] | CONFIG[0] | AVSS | LON[1] | AVSS | LIP[1] | J |
| K | AVSS | AVSS | AVSS | AVDDH | PHYAD[0] | VSEL_S | VSS | PHYAD[1] | PHYAD[3] | AVDDL | AVSS | AVSS | AVSS | K |
| L | HiN[0] | AVSS | HOP[0] | AVSS | TEST[0] | $\underline{N T n}$ | MDIO | MDC | PHYAD[2] | AVSS | LOP[0] | AVSS | LIN[0] | L |
| M | HIP[0] | AVSS | HON[0] | AVSS | AVSS | ATP | AVDDT | AVDDC | AVSS | AVSS | LON[0] | AVSS | LIP[0] | M |
| N | AVSS | AVDDH | AVSS | AVDDH | CLKP | CLKN | AVSS | CLK25P | CLK25N | AVDDL | AVSS | AVDDL | AVSS | N |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |  |

(Top View)

### 2.2 Pin Description

## Table 2: Line Side Interface

| Pin \# | Pin Name | Pin <br> Type | Description |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { C13 } \\ & \text { F13 } \\ & \text { J13 } \\ & \text { M13 } \end{aligned}$ | $\begin{aligned} & \operatorname{LIP}[3] \\ & \operatorname{LIP}[2] \\ & \operatorname{LIP}[1] \\ & \operatorname{LIP}[0] \end{aligned}$ | AI | Line Input Positive |
| B13 <br> E13 <br> H13 <br> L13 | LIN[3] <br> LIN[2] <br> LIN[1] <br> LIN[0] | AI | Line Input Negative |
| B11 <br> E11 <br> H11 <br> L11 | LOP[3] <br> LOP[2] <br> LOP[1] <br> LOP[0] | AO | Line Output Positive |
| $\begin{aligned} & \text { C11 } \\ & \text { F11 } \\ & \text { J11 } \\ & \text { M11 } \end{aligned}$ | LON[3] <br> LON[2] <br> LON[1] <br> LON[0] | AO | Line Output Negative |

Table 3: Host Side Interface

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| C1 | HIP[3] | AI | Host Input Positive |
| F1 | HIP[2] |  |  |
| J1 | HIP[1] |  |  |
| M1 | HIP[0] | HIN[3] | AI |
| B1 | HIN[2] | Host Input Negative |  |
| E1 | HIN[1] |  |  |
| H1 | HIN[0] |  |  |
| L1 | HOP[3] | AO | Host Output Positive |
| B3 | HOP[2] |  |  |
| E3 | HOP[1] |  |  |
| H3 | HOP[0] |  |  |
| L3 | HON[3] | AO | Host Output Negative |
| C3 | HON[2] |  |  |
| F3 | HON[1] |  |  |
| J3 | HON[0] |  |  |
| M3 |  |  |  |

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Table 4: Clocking and Reference

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| N5 | CLKP | AI | Reference Clock Positive. Refer to Section 7.7 for further details. |
| N6 | CLKN | AI | Reference Clock Negative. Refer to Section 7.7 for further details. |
| N8 | CLK25P | AO | 25 MHz Clock Output Positive. Refer to Section 7.8 for further details. |
| N9 | CLK25N | AO | 25 MHz Clock Output Negative. Refer to Section 7.8 for further <br> details. |

Table 5: Configuration and Reset

| Pin \# | Pin Name | Pin <br> Type | Description |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { K9 } \\ & \text { L9 } \\ & \text { K8 } \\ & \text { K5 } \end{aligned}$ | PHYAD[3] <br> PHYAD[2] <br> PHYAD[1] <br> PHYAD[0] | $\begin{aligned} & \text { DI/ } \\ & \text { PD } \end{aligned}$ | Address <br> In MDIO mode, this sets the PHYAD[3:0] setting. PHYAD[4] is set to 0. <br> In TWSI mode, this sets the $\mathrm{A}[3: 0]$ setting. $\mathrm{A}[6: 4]$ is set to 100. |
| $\begin{aligned} & \text { J6 } \\ & \text { J8 } \\ & \text { J9 } \end{aligned}$ | CONFIG[2] <br> CONFIG[1] <br> CONFIG[0] | DI/PD | $\begin{aligned} & \text { CONFIG[0]-0 }=\text { MDIO } \\ & 1=\text { TWSI } \\ & \text { CONFIG[1]- }=\text { Do not load EEPROM } \\ & 1=\text { Load EEPROM } \\ & \text { CONFIG[2] }- \text { Reserved } \end{aligned}$ |
| A5 | RESETn | DI | Hardware Reset, <br> $0=$ Reset <br> 1 = Normal operation |

Table 6: Management Interface

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| L8 | MDC/SSCL | DI | Management Interface Clock, or SCL for TWSI slave mode <br> See Section 3.4.1, IEEE MDC/MDIO Register Access for details. |
| L7 | MDIO/SSDA | IO,OD | Management Interface Data, or SDA for TWSI slave mode <br> See Section 3.4.1, IEEE MDC/MDIO Register Access for details. <br> This pin can be open drain. |
| L6 | INTn | OD | Interrupt. |

Table 7: EEPROM/GPIO

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| B8 | SCL | IO, OD | Multi-function pin for EEPROM Clock, or GPIO[4]. Primary function is <br> Two Wire Serial Interface Clock, EEPROM Clock. |
| B9 | SDA | IO, OD | Multi-function pin for EEPROM Data, or GPIO[5]. Primary function is <br> Two Wire Serial Interface Data, EEPROM Data. |

Table 8: JTAG

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| C9 | TDI | DI/PU | JTAG Test In |
| B6 | TDO | DO, OD | JTAG Test Out |
| C5 | TMS | DI/PU | JTAG Test Control |
| C8 | TCK | DI/PU | JTAG Test Clock |
| B5 | TRSTn | DI/PU | JTAG Test Reset <br> For normal operation, TRSTn should be pulled low with a 4.7 kohm <br> pull-down resistor. |

Table 9: GPIOILED

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| A6 | GPIO[3] | I/O | GPIO |
| A7 | GPIO[2] |  |  |
| A8 | GPIO[1] |  |  |
| B7 | GPIO[0] |  |  |

Table 10: TEST

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| J5 | TEST[1] | DI | Test pins. Tie to VSS in normal operation. |
| L5 | TEST[0] |  |  |
| M6 | ATP | AO | Analog DC test point. |

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Table 11: Power and Ground

| Pin \# | Pin Name | Pin Type | Description |
| :---: | :---: | :---: | :---: |
| A9 <br> D6 <br> D8 <br> E5 <br> E7 <br> E9 <br> F6 <br> F8 <br> G5 <br> G7 <br> G9 <br> H6 <br> H8 | DVDD | Digital Power | 0.9V/0.95V (I-temp) Digital Core Power |
| A10 <br> A12 <br> D10 <br> G10 <br> G12 <br> K10 <br> N10 <br> N12 | AVDDL | Analog Power | 1.0V Analog Core Power - Line SERDES Side |
| A2 <br> A4 <br> D4 <br> G2 <br> G4 <br> K4 <br> N2 <br> N4 | AVDDH | Analog Power | 1.0V Analog Core Power - Host SERDES Side |
| M8 | AVDDC | Analog Power | 1.0V Common Analog Power. |
| M7 | AVDDT | Analog Power | 2.5 V , or 3.3 V Temperature Sensor and 25 MHz PLL power. AVDDT must be AC coupled to VSS when not used. |
| C7 | VDDON | I/O Power | $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}, 1.8 \mathrm{~V}, 2.5 \mathrm{~V}$, or 3.3 V I/O Power (North side). See Section 3.12 for more details. |
| J7 | VDDOS | I/O Power | $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}, 1.8 \mathrm{~V}, 2.5 \mathrm{~V}$, or $3.3 \mathrm{~V} \mathrm{I} / \mathrm{O}$ Power (South side). See Section 3.12 for more details. |
| C6 | VSEL_N | VDDON Level Select | Tie to VSS for 2.5 V or 3.3 V operation, otherwise tie to VDDON for $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}, 1.8 \mathrm{~V}$ operation |
| K6 | VSEL_S | VDDOS Level Select | Tie to VSS for 2.5 V or 3.3 V operation, otherwise tie to VDDOS for $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}, 1.8 \mathrm{~V}$ operation |

Table 11: Power and Ground (Continued)

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| A1 | AVSS | Ground | Ground |
| A3 |  |  |  |
| A11 |  |  |  |
| A13 |  |  |  |
| B2 |  |  |  |
| B4 |  |  |  |
| B10 |  |  |  |
| B12 |  |  |  |
| C2 |  |  |  |
| C4 |  |  |  |
| C10 |  |  |  |
| C12 |  |  |  |
| D1 |  |  |  |
| D2 |  |  |  |
| D3 |  |  |  |
| D11 |  |  |  |
| D12 |  |  |  |
| D13 |  |  |  |
| E2 |  |  |  |
| E4 |  |  |  |
| E10 |  |  |  |
| E12 |  |  |  |
| F2 |  |  |  |
| F4 |  |  |  |
| F10 |  |  |  |
| F12 |  |  |  |
| G1 |  |  |  |
| G3 |  |  |  |
| G11 |  |  |  |
| G13 |  |  |  |
| H2 |  |  |  |
| H4 |  |  |  |
| H10 |  |  |  |
| H12 |  |  |  |
| J2 |  |  |  |
| J4 |  |  |  |
| J10 |  |  |  |
| J12 |  |  |  |
| K1 |  |  |  |
| K2 |  |  |  |
| K3 |  |  |  |
| K11 |  |  |  |
| K12 |  |  |  |
| K13 |  |  |  |
| L2 |  |  |  |
| L10 |  |  |  |

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Table 11: Power and Ground (Continued)

| Pin \# | Pin Name | Pin <br> Type | Description |
| :--- | :--- | :--- | :--- |
| M4 | AVSS (cont.) | Ground | Ground |
| M5 |  |  |  |
| M9 |  |  |  |
| M10 |  |  |  |
| M12 |  |  |  |
| N1 |  |  |  |
| N3 |  |  |  |
| N7 |  |  |  |
| N11 |  |  |  |
| N13 |  |  |  |
| D5 |  |  |  |
| D7 |  |  |  |
| D9 |  |  |  |
| E6 |  |  |  |
| E8 |  |  |  |
| F5 |  |  |  |
| F7 |  |  |  |
| F9 |  |  |  |
| G6 |  |  |  |
| G8 |  |  |  |
| H5 |  |  |  |
| H7 |  |  |  |
| H9 |  |  |  |
| K7 |  |  |  |

### 2.3 88X5113 Device Pin Assignment List

## Table 12:88X5113 Pin List - Alphabetical by Signal Name

| Pin Number | Pin Name |
| :---: | :---: |
| M6 | ATP |
| M8 | AVDDC |
| A2 | AVDDH |
| A4 | AVDDH |
| D4 | AVDDH |
| G2 | AVDDH |
| G4 | AVDDH |
| N2 | AVDDH |
| N4 | AVDDH |
| K4 | AVDDH |
| A10 | AVDDL |
| A12 | AVDDL |
| D10 | AVDDL |
| G10 | AVDDL |
| G12 | AVDDL |
| K10 | AVDDL |
| N10 | AVDDL |
| N12 | AVDDL |
| M7 | AVDDT |
| A1 | AVSS |
| A3 | AVSS |
| A11 | AVSS |
| A13 | AVSS |
| B2 | AVSS |
| B4 | AVSS |
| B10 | AVSS |
| B12 | AVSS |


| Pin Number | Pin Name |
| :---: | :---: |
| C2 | AVSS |
| C4 | AVSS |
| C10 | AVSS |
| C12 | AVSS |
| D1 | AVSS |
| D2 | AVSS |
| D3 | AVSS |
| D11 | AVSS |
| D12 | AVSS |
| D13 | AVSS |
| E2 | AVSS |
| E4 | AVSS |
| E10 | AVSS |
| E12 | AVSS |
| F2 | AVSS |
| F4 | AVSS |
| F10 | AVSS |
| F12 | AVSS |
| G1 | AVSS |
| G3 | AVSS |
| G11 | AVSS |
| G13 | AVSS |
| H2 | AVSS |
| H4 | AVSS |
| H10 | AVSS |
| H12 | AVSS |
| J2 | AVSS |

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| Pin Number | Pin Name |
| :---: | :---: |
| J4 | AVSS |
| J10 | AVSS |
| J12 | AVSS |
| K1 | AVSS |
| K2 | AVSS |
| K3 | AVSS |
| K11 | AVSS |
| K12 | AVSS |
| K13 | AVSS |
| L2 | AVSS |
| L4 | AVSS |
| L10 | AVSS |
| L12 | AVSS |
| M2 | AVSS |
| M4 | AVSS |
| M5 | AVSS |
| M9 | AVSS |
| M10 | AVSS |
| M12 | AVSS |
| N1 | AVSS |
| N3 | AVSS |
| N7 | AVSS |
| N11 | AVSS |
| N13 | AVSS |
| N9 | CLK25N |
| N8 | CLK25P |
| N6 | CLKN |
| N5 | CLKP |
| J9 | CONFIG[0] |


| Pin Number | Pin Name |
| :---: | :---: |
| J8 | CONFIG[1] |
| J6 | CONFIG[2] |
| A9 | DVDD |
| D6 | DVDD |
| D8 | DVDD |
| E5 | DVDD |
| E7 | DVDD |
| E9 | DVDD |
| F6 | DVDD |
| F8 | DVDD |
| G5 | DVDD |
| G7 | DVDD |
| G9 | DVDD |
| H6 | DVDD |
| H8 | DVDD |
| B7 | GPIO[0] |
| A8 | GPIO[1] |
| A7 | GPIO[2] |
| A6 | GPIO[3] |
| L1 | HIN[0] |
| H1 | HIN[1] |
| E1 | HIN[2] |
| B1 | HIN[3] |
| M1 | HIP[0] |
| J1 | HIP[1] |
| F1 | HIP[2] |
| C1 | HIP[3] |
| M3 | HON[0] |
| J3 | HON[1] |


| Pin Number | Pin Name |
| :---: | :---: |
| F3 | HON[2] |
| C3 | HON[3] |
| L3 | HOP[0] |
| H3 | HOP[1] |
| E3 | HOP[2] |
| B3 | HOP[3] |
| L6 | INTn |
| L13 | LIN[0] |
| H13 | LIN[1] |
| E13 | LIN[2] |
| B13 | LIN[3] |
| M13 | LIP[0] |
| J13 | LIP[1] |
| F13 | LIP[2] |
| C13 | LIP[3] |
| M11 | LON[0] |
| J11 | LON[1] |
| F11 | LON[2] |
| C11 | LON[3] |
| L11 | LOP[0] |
| H11 | LOP[1] |
| E11 | LOP[2] |
| B11 | LOP[3] |
| L8 | MDC |
| L7 | MDIO |
| K5 | PHYAD[0] |
| K8 | PHYAD[1] |
| L9 | PHYAD[2] |
| K9 | PHYAD[3] |


| Pin Number | Pin Name |
| :---: | :---: |
| A5 | RESETn |
| B8 | SCL |
| B9 | SDA |
| C8 | TCK |
| C9 | TDI |
| B6 | TDO |
| L5 | TEST[0] |
| J5 | TEST[1] |
| C5 | TMS |
| B5 | TRSTn |
| C7 | VDDON |
| J7 | VDDOS |
| C6 | VSEL_N |
| K6 | VSEL_S |
| D5 | VSS |
| D7 | VSS |
| D9 | VSS |
| E6 | VSS |
| E8 | VSS |
| F5 | VSS |
| F7 | VSS |
| F9 | VSS |
| G6 | VSS |
| G8 | VSS |
| H5 | VSS |
| H7 | VSS |
| H9 | VSS |
| K7 | VSS |

## Functional Description

This section describes the chip-level functionality. Sections 4 and 5 describe the individual units in detail.

### 3.1 Data Path

Figure 4 shows the chip data path in the main operational mode - PCS mode. The various interface configuration are listed in the Interface Modes of Operation table in Section 4. The register settings to set the various configurations are described in Section 4 and Section 5.

Figure 4: 88X5113 Main Operational Modes


### 3.1.1 PCS Mode

In the PCS mode, the receive data is terminated by the PCS. The data is retransmitted by a second PCS frequency locked to the local reference clock. The FIFO will insert or delete idles during IPG to compensate for any frequency difference between the received data and the retransmitted data.
While in this mode both the line and host side can enable Auto-Negotiation and perform KR training. The host and line interfaces can mix and match PCS and FEC as long as both sides are running at the same nominal speed. The valid combinations between the host and line configurations are shown in Table 13.

Table 13: Valid PCS Mode Interface Connections

| Line | Host |
| :--- | :--- |
| P1X | P1X |
| P1X | P1P |
| P1P | P1X |
| P1S | P1P |
| P2.5X | P2.5X |
| P5 | P5 |
| P10 | P10 |
| P25 | P25 |
| P25 | P40 |
| P40 | P40 |
| P50 | P50 |
| P100 | P100 |

1. Refer to the Interface Modes of Operation table in Section 4 for details.

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### 3.2 Reset

A hardware reset (RESETn) will reset the entire chip and initialize all the registers to their hardware reset default.

A software reset has a similar effect on the affected units as a hardware reset except all Retain-type registers will hold their value, and the Update registers will have the previously written values take effect.

All the reset registers described are self-clear with the exception of on-chip processor and on-chip Processor Block reset bits.

Table 14 describes various reset bits available in the device.

Table 14: Reset Bits

| Reset Description | Unit Affected | Register - Line | Register - Host |
| :---: | :---: | :---: | :---: |
| Global Soft-Reset | Whole Chip | 31.F404.15 |  |
| Global Hard-Reset | Whole Chip | 31.F404.14 |  |
| On-chip Processor Reset | On-chip Processor only | 31.F404.13 |  |
| On-chip Processor Block Reset | On-chip Processor whole block | 31.F404.12 |  |
| Port Soft-Reset <br> This bit soft-reset all the lanes of the respective interface regardless of the interface mode | Port | 31.F003.15 | $31 . \mathrm{F} 003.7$ |
| Port Hardware Reset <br> This bit hard-reset all the lanes of the respective interface regardless of the interface mode | Port | 31.F003.13 | 31.F003.5 |
| Per Lane/Interface Mode Soft-Reset In 40G/50G/100G mode, soft-reset to lane 0 will be applied to all lanes (lane 1, 2, and 3 soft-reset bits are ignored). | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & \text { 3.F000.15 } \\ & \text { 3.F001.15 } \\ & \text { 3.F002.15 } \\ & \text { 3.F003.15 } \end{aligned}$ | $\begin{aligned} & \text { 4.F000.15 } \\ & \text { 4.F001.15 } \\ & \text { 4.F002.15 } \\ & \text { 4.F003.15 } \end{aligned}$ |
| PMA Soft-Reset <br> In 40G/50G/100G mode, soft-reset to lane 0 will be applied to all lanes (lane 1, 2, and 3 soft-reset bits are ignored). | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 1.0000 .15 \\ & 1.2000 .15 \\ & 1.4000 .15 \\ & 1.6000 .15 \end{aligned}$ | $\begin{aligned} & 1.1000 .15 \\ & 1.3000 .15 \\ & 1.5000 .15 \\ & 1.7000 .15 \end{aligned}$ |
| PCS Soft-Reset - 100G | Lane 0/Aggregated Port | 3.0000 .15 | 4.0000 .15 |
| PCS Soft-Reset - 40G/50G | Lane 0/Aggregated Port | 3.1000 .15 | 4.1000 .15 |
| PCS Soft-Reset - 5G/10G/25G | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.2000 .15 \\ & 3.2200 .15 \\ & 3.2400 .15 \\ & 3.2600 .15 \end{aligned}$ | $\begin{aligned} & 4.2000 .15 \\ & 4.2200 .15 \\ & 4.2400 .15 \\ & 4.2600 .15 \end{aligned}$ |
| PCS Soft-Reset - 1G/2.5G | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.3000 .15 \\ & 3.3200 .15 \\ & 3.3400 .15 \\ & 3.3600 .15 \end{aligned}$ | $\begin{aligned} & 4.3000 .15 \\ & 4.3200 .15 \\ & 4.3400 .15 \\ & 4.3600 .15 \end{aligned}$ |

Table 14: Reset Bits (Continued)

| Reset Description | Unit Affected | Register - Line | Register - Host |
| :--- | :--- | :--- | :--- |
| 802.3AP Auto-negotiation Soft-Reset | Lane 0/Aggregated Port | 7.0000 .15 | 7.1000 .15 |
| In 40G/50G/100G mode, soft-reset to lane 0 will | Lane 1 | 7.0200 .15 | 7.1200 .15 |
| be applied to all lanes (lane 1, 2, and 3 | Lane 2 | 7.0400 .15 | 7.1400 .15 |
| soft-reset bits are ignored). | Lane 3 | 7.0600 .15 | 7.1600 .15 |



The Reset table does not include various internal only reset bits.
Note

The Global Hardware Reset register has the same function as the pin reset. It should be issued right after the chip is powered up to make sure the chip starts from a known state. It could be skipped if the pin reset was asserted.
The Port Hardware Reset register resets the line side or host side accordingly. It can be covered by global hardware reset, only apply to one side of the chip, and the same is true for port software reset. This is for debug only.
PMA and PCS software resets are IEEE-compliant registers. They are physically the same but implemented at different register addresses as specified in the IEEE specification. The register will be applied to the corresponding sub-port PCS or the coupled PCS (40G, 100G, or 200G).
During the chip power-on, it is recommended to use global software reset bit or mode software reset bit to apply the configuration (speed, mode) changes. Per lane/interface based mode software reset is often used when changing the operation modes and speeds. They are specifically assigned to the same register as modes setting bits so programming one register can bring up the new mode.

### 3.3 Hardware Configuration

PHYAD[3:0] and CONFIG[2:0] are sampled at the de-assertion of RESETn. PHYAD[3:0] and CONFIG[2:0] must not change after it is sampled. If PHYAD[3:0] and CONFIG[2:0] change when RESETn is high, then the device will have unpredictable behavior as it enters into an invalid mode. The configuration pins are tied either high or low. The settings are shown in Table 15.

The device will exit reset in a powered down state. Software configuration is then required to get the device into an operational state.

Table 15: Hardware Configuration

| Configuration | Setting |
| :--- | :--- |
| PHYAD[3:0] | In MDIO mode, this sets the PHYAD[3:0] setting. PHYAD[4] is set to 0. <br> In TWSI mode, this sets the A[3:0] setting. A[6:4] is set to 100. |
| CONFIG[0] | Register Access Method <br> $0=$ MDIO <br> $1=$ TWSI |
| CONFIG[1] | EEPROM Loading <br> $0=$ Do not load EEPROM on startup. <br> $1=$ Load EEPORM on startup. |
| CONFIG[2] | Reserved. Set to 0. |

### 3.4 Register Access

Registers can be accessed either through MDC/MDIO or the TWSI. Only one mode can be enabled at a time and is configured during hardware reset. For either mode, the MDC pins is used for the clock and MDIO is used for data.

### 3.4.1 IEEE MDC/MDIO Register Access

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 Clause 45. MDC is the management data clock input and it can run to a maximum rate of 25 MHz . At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bidirectional signal that runs synchronously to MDC.
PHY address is configured during the hardware reset sequence. Refer to Section 3.2, Reset, on page 28 for detailed information on how to configure PHY addresses.

Typical read and write operations on the management interface are shown in Figure 5 and Figure 6. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the device registers documentation.

Figure 5: Typical MDC/MDIO Read Operation


Figure 6: Typical MDC/MDIO Write Operation


The extensions for Clause 45 MDIO indirect register accesses are specified in Table 16.

Table 16: Extensions for Management Frame Format for Indirect Access

| Frame | PRE | ST | OP | PHYAD | DEVADR | TA | ADDRESSIDATA | Idle |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Address | $1 \ldots 1$ | 00 | 00 | PPPPP | DDDDD | 10 | AAAAAAAAAAAAAAAA | Z |
| Write | $1 \ldots 1$ | 00 | 01 | PPPPP | DDDDD | 10 | DDDDDDDDDDDDDDDD | Z |
| Read | $1 \ldots 1$ | 00 | 11 | PPPPP | DDDDD | Z0 | DDDDDDDDDDDDDDDD | Z |
| Read <br> Increment | $1 \ldots .1$ | 00 | 10 | PPPPP | DDDDD | Z0 | DDDDDDDDDDDDDDDD | Z |

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The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though only post-read-increment-address frame modifies the contents of the address register.

### 3.4.2 TWSI Register Access

Registers can also be accessed over the TWSI. This TWSI interface is a slave interface and should not be confused with the master interface that is used to read the EEPROM. In the following discussion, SSCL represents the clock and SSDA represents the data. This is to avoid confusion with the SCL and SDA pins used to read the EEPROM. When the TWSI mode is enabled, the MDC and MDIO pins correspond to SSCL and SSDA functions.

For the TWSI device address, the address [4:2] bits from pin PHYADR[3:1] are latched during hardware reset and the device address bits ([6:5]) are fixed at 10 . The address bits [1:0] is fixed at $00,01,10$, and 11 for each 4 -lane port.

The TWSI features are as follows:

- 7-bit device address/8-bit data transfers
- 100 Kbps mode (Standard mode, SSCL up to 100 kHz )
- 400 Kbps mode (Fast mode, SSCL up to 400 kHz )

Multiple devices using the TWSI can share and lump up the MDC and MDIO lines and are pulled up with a resistor ranging from $4.5 \mathrm{k} \Omega$ to $10 \mathrm{k} \Omega$.

### 3.4.2.1 Bus Operation

The Master generates one clock pulse for each data bit transferred. The high or low state of the data line can only change when the clock signal on the SSCL line is low. A high to low transition on the SSDA line while SSCL is high defines a Start. A low to high transition on the SSDA line while the SSCL is high defines a Stop. Start (S), Repeated Start (Sr), and Stop (P) conditions are always generated by the Master. Acknowledge (A) and Not Acknowledge (A) can be generated by either the Slave or Master.

The Master continuously monitors for Start and Stop conditions. Whenever a Stop is detected, the device goes into standby mode, and the current operation is canceled. The Slave recovers from this error condition, and waits for the next transfer to begin.

Data transfer with Acknowledge is always obligatory. The receiver must pull down the SSDA line during the Acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

If the Slave does not Acknowledge the device address, then the Master must abort the transfer. This is indicated by the Slave generating the Not Acknowledge on the first byte to follow. The Slave device then leaves the data line high, and the Master must generate a Stop or a Repeated Start condition. When the Slave is transmitting data on the bus and the Master responds with a Not Acknowledge, the Slave must receive a Stop or a Repeated Start condition. If neither is received, it is an error condition. The Slave recovers from this error condition and waits for the next transfer to begin.

## Functional Description <br> Register Access

### 3.4.2.2 Clause 45 Encapsulation

All TWSI transactions will encapsulate PHYAD and DEVAD along with the R/W bit and 3-bit instruction in the first 2 bytes as shown in Figure 7. In all diagrams, the shaded portion is generated by the master and the unshaded portion by the device. The INS[2:0] definition is summarized in Table 17.

Figure 7: First Two Bytes of All Transactions


## Table 17: INS[2:0] Definition

| INS[2:0] | Header | Address |
| :--- | :--- | :--- |
| 000 | Abbreviated Header - Use stored REGAD | Stored REGAD unchanged |
| 001 | Abbreviated Header - Use stored REGAD | Post-increment REGAD |
| 010 | Full Header - Use specified REGAD | Stored REGAD unchanged |
| 011 | Full Header - Use specified REGAD | Post-increment REGAD |
| 100 | Dummy Write |  |
| 101 | Reserved | Reserved |
| 110 | Reserved | Reserved |
| 111 | Reserved | Reserved |

In Clause 45 MDIO access, the REGAD[15:0] is set independently of the data access. There are two methods to specify the REGAD. The first method is to fully specify the REGAD in the transaction as shown in Figure 8, Figure 9, Figure 12, and Figure 13. The second method is to use abbreviated header where the stored REGAD register is used as shown in Figure 10, Figure 11, Figure 14, and Figure 15.
The stored REGAD register is updated on each TWSI transaction. The stored REGAD register can be updated by a dummy write command as shown in Figure 16.

The Clause 45 encapsulation does not differentiate between random versus sequential read/write. All reads and writes can be sustained by the master by not sending a stop bit. So, one or more 16-bit words can be passed with the same encapsulated header. REGAD may or may not be post-incremented after each 16-bit word transfer depending on the INS[2:0].
All 16-bit read/write operations operate atomically. If a write transaction terminates with only 8 bits of the 16 -bit word written in, then the 8 bit is discarded and REGAD will not post-increment (if selected). If a read transaction terminates with only 8 bits of the 16-bit word read, then the other 8 -bits will be lost forever (that is, in the case of a clear on read register) and REGAD will not post-increment (if selected).
All read transactions must read least one byte of data. Write transactions can be dummy writes if no data is transferred. If no data is transferred, then no post-incrementing will occur.
The slave will acknowledge the first byte only when PHYAD[4:0] matches and the two most significant bits are 10 (binary).

The slave will acknowledge the second byte only if all the following conditions are met:

- The first byte was acknowledged by the slave.

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- The DEVAD[4:0] is among the supported device addresses in the PHY.
- INS[2] bit is a 0 (that is, it will not respond to reserved instructions).

The slave will acknowledge the third and subsequent bytes if all the following conditions are met:

- The first and second bytes was acknowledged by the slave.
- The transaction is a write transaction. $\qquad$
- A start bit or stop bit is not detected since the second acknowledge.

The slave will acknowledge the third and fourth bytes if all the following conditions are met:

- The first and second bytes was acknowledged by the slave.
- The instruction indicates a full header is being sent.
- A start bit (not counting the one at the beginning of the current transaction) or stop bit is not detected since the second acknowledge by the slave.
The slave will output 8 -bit data if all the following conditions are met:
- The first and second bytes was acknowledged by the slave.
- The third and fourth bytes was acknowledge by the slave if instruction indicates a full header is being sent.
- The transaction is a read transaction.
- A start bit (not counting the one at the beginning of the current transaction), stop bit or no-acknowledge is not detected.
The slave will abort the current 16-bit transfer and will not post-increment the REGAD if a stop bit or no-acknowledge is prematurely detected. All further activities on the bus are ignored by the slave until a start bit is detected.

If the first byte of the REGAD is written and the transaction terminates without the second byte of REGAD being written, then the internal REGAD register will not update.
If a start bit is prematurely detected, then the slave will abort the current 16-bit transfer and will not post-increment the REGAD. This premature start bit will immediately trigger the start of the next $I^{2} \mathrm{C}$ transaction.

If post-increment is active and the REGAD is $0 x F F F F$, then the REGAD will roll over to $0 \times 0000$.

Figure 8: Write, Full Header, Retain REGAD


Figure 9: Write, Full Header, Post-Increment


Figure 10: Write, Abbreviated Header, Retain REGAD


Figure 11: Write, Abbreviated Header, Post-Increment


Figure 12: Read, Full Header, Retain REGAD


Figure 13: Read, Full Header, Post-Increment


Figure 14: Read, Abbreviated Header, Retain REGAD


Figure 15: Read, Abbreviated Header, Post-Increment


Figure 16: Dummy Write Command to Set REGAD

$$
\begin{array}{|l|l|l|l|l|l|l|l|l|ll|l|}
\hline \mathrm{S} & 10 & { }_{4} \mathrm{PHYAD}_{0} & \mathrm{~W} & \mathrm{~A} & 01 \mathrm{x} & { }_{4} \mathrm{DEVAD}_{0} & \mathrm{~A} & 15 & \text { REGAD } & 8 & \mathrm{~A} \\
7 & \text { REGAD } & 0 & \mathrm{~A} & \mathrm{P} \\
\hline
\end{array} \quad \text { Address for DEVAD at REGAD }
$$

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### 3.5 TWSI, GPIO, and LED

### 3.5.1 GPIO[3:0] and LED[3:0]

The GPIO pins are shared between the GPIO and LED functional modes. Each pin can be programmed independently to operate in GPIO or LED modes. The pin mapping is summarized in Table 18.

Table 18: GPIO, LED Signal Mapping

| Pin | Special Function | GPIO | LED |
| :--- | :--- | :--- | :--- |
| GPIO[0] | - | GPIO[0] | LED[0] |
| GPIO[1] | - | GPIO[1] | LED[1] |
| GPIO[2] | - | GPIO[2] | LED[2] |
| GPIO[3] | - | GPIO[3] | LED[3] |

GPIO[0] pin is configured to GPIO mode by setting register bits 31.F437.15:14 to 01. This pin can be configured in LED mode by setting register bits 31.F437.15:14 to 10.

The GPIO[3:1] are similar and are configured in GPIO mode by setting register bits 31.F439.15 (for GPIO[1]), 31.F43B. 15 (GPIO[2]), and 31.F43D. 15 (GPIO[3]) to 0 individually. These pins can be configured in LED mode by setting register bits 31.F439.15 (for GPIO[1]), 31.F43B. 15 (GPIO[2]), and 31.F43D. 15 (GPIO[3]) to 1 individually.

In GPIO mode, each pin can operate bidirectionally and can be individually configured. In the input mode, these pins can be used as interrupts. The GPIO operations are described in the sections below.

### 3.5.1.1 Controlling and Sensing

In the GPIO mode, registers 31.F437.13, 31.F439.13, 31.F43B.13, and 31.F43D. 13 control whether the GPIO pins are inputs or outputs. Each pin can be individually controlled. Registers 31.F437.7, 31.F439.7, 31.F43B.7, and 31.F43D. 7 allow the pins to be controlled and sensed. When configured as input, a read to registers 31.F437.7, 31.F439.7, 31.F43B. 7 and 31.F43D. 7 will return the real-time sampled state of the pins GPIO[0], GPIO[1], GPIO[2], and GPIO[3], respectively at the time of the read. A write to these register will write to the output register, but have no immediate effect on the pin since the pin is configured to be an input. The input is sampled once every 6.4 ns (equivalent to one reference clock period). When configured as output, a write will write to the output register which will in turn drive the state of the pin. A read to registers 31.F437.7, 31.F439.7, 31.F43B.7, and 31.F43D. 7 will return the value in the output registers.

### 3.5.1.2 GPIO Interrupts

When the GPIO pins are configured as input, several types of interrupt events can be generated as described in Table 19. Register bits 31.F437.10:8, 31.F439.10:8, 31.F43B.10:8, and 31.F43D.10:8 allow each pin to be configured to generate interrupt on one of 5 types of events - Low Level, High Level, High to Low Transition, Low to High Transition, and Transitions on Either Edge. The interrupt generation can also be disabled. When an interrupt event is generated on pin GPIO[0], it is latched
high in the sticky register 31.F437.11. Similarly, when interrupt event is generated on GPIO[1], GPIO[2] or GPIO[3], they are latched in the sticky register 31.F439.11, 31.F43B.11, and 31.F43D.11. The register bits will remain high until read. The GPIO interrupt can be asserted when an event occurs through pins GPIO[3:0]. Registers 31.F437.12, 31.F439.12, 31.F43B.12, and 31.F43D. 12 set the interrupt enables.

Registers 31.F437.12 and 31.F437.11 are bitwise AND together to generate a GPIO[0] interrupt. Registers 31.F439.12 and 31.F439.11 are bitwise AND together to generate a GPIO[1] interrupt. Similarly, registers 31.F43B. 12 and 31.F43B. 11 are bitwise AND together to generate a GPIO[2] interrupt and registers 31.F43D. 12 and 31.F43D. 11 are bitwise AND together to generate a GPIO[3] interrupt. If the result is non-zero the GPIO interrupt will assert. For interrupt polarity control, refer to Table 19.

Table 19: GPIO/LED Controls

| Register | Function | Setting | Mode |
| :---: | :---: | :---: | :---: |
| 31.F437.15:14 | GPIO 0 Function | $00=$ GPIO[0] is used for signaling. <br> $01=$ GPIO[0] is used for GPIO 0 function. <br> $10=$ GPIO[0] is used for LED 0 function. <br> 11 = Reserved. <br> (LED 0 can only select lane 0 as LED function) | R/W |
| $\begin{aligned} & 31 . F 439.15 \\ & \text { 31.F43B. } 15 \\ & \text { 31.F43D. } 15 \end{aligned}$ | GPIO n Function where $\mathrm{n}=1,2$, 3 | $0=$ GPIO [n] pin is used for GPIO 1 function. <br> 1 = GPIO [ n ] pin is used for LED 1 function. <br> (LED n can only select lane n as LED function) | R/W |
| $\begin{aligned} & \text { 31.F437.13 } \\ & \text { 31.F439.13 } \\ & \text { 31.F43B. } 13 \\ & \text { 31.F43D. } 13 \end{aligned}$ | LED n Output Enable where $\mathrm{n}=0,1,2,3$ | This bit has no effect unless register 31.F437.15:14 = 01. $\begin{aligned} & 0=\text { Input } \\ & 1=\text { Output } \end{aligned}$ | R/W |
| $\begin{aligned} & \text { 31.F437.12 } \\ & \text { 31.F439.12 } \\ & \text { 31.F43B. } 12 \\ & \text { 31.F43D. } 12 \end{aligned}$ | GPIO n Interrupt Enable where $\mathrm{n}=0,1,2,3$ | $\begin{aligned} & 0=\text { Disable } \\ & 1=\text { Enable } \end{aligned}$ | R/W |
| $\begin{aligned} & \text { 31.F437.11 } \\ & \text { 31.F439.11 } \\ & \text { 31.F43B. } 11 \\ & \text { 31.F43D. } 11 \end{aligned}$ | GPIO n Interrupt Status where $\mathrm{n}=0,1,2,3$ | This bit is not valid unless register 31.F437.15:14 = 01 and $31 . F 437.13=0$. <br> $0=$ No interrupt has occurred. <br> 1 = An interrupt has occurred. | RO, LH |
| $\begin{aligned} & \text { 31.437.10:8 } \\ & \text { 31.F439.10:8 } \\ & \text { 31.F43B.10:8 } \\ & \text { 31.F43D.10:8 } \end{aligned}$ | GPIO n Interrupt Select where $\mathrm{n}=0,1,2,3$ | Interrupt is effective only when 31.F437.13 = 0 . <br> $000=$ No Interrupt <br> 001 = Reserved <br> $010=$ Interrupt on Low Level <br> 011 = Interrupt on High Level <br> $100=$ Interrupt on High to Low <br> 101 = Interrupt on Low to High <br> 110 = Reserved <br> 111 = Interrupt on Low to High or High to Low | R/W |

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Table 19: GPIOILED Controls (Continued)

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F437.7 | GPIO $n$ Data <br> where $n=0,1,2,3$ | This bit has no effect unless register 31.F437.15:14 $=01$. <br> When 31.F437.13 $=0$, read to this register will reflect the state <br> of the GPIO[0], and a write will write the output register but have <br> 31.F43B.7 <br> 31.F43D.7 <br> When 31.F437.13 $=1$ a read to this register will reflect the <br> state of the output register, and a write will write the output <br> register and drive the state of the GPIO[n]. | R/W |
| 31.F437.6:0 <br> 31.F439.6:0 <br> 31.F43B.6:0 <br> 31.F43D.6:0 | Reserved | Set to 0s. | RO |

### 3.5.1.3 LED

The GPIO[3:0] pins can be used to drive LED pins. Setting register 31.F437.15:14 to 10 and registers 31.F439.15, 31.F43B.15, and 31.F43D. 15 to 1 will configure the GPIO[0], GPIO[1], GPIO[2], GPIO[3] pin in the LED mode and named as LED[0], LED[1], LED[2] and LED[3]. Registers 31.F438, 31.F43A, 31.F43C, and 31.F43E control the operation of the LED pins. LED[3:0] will operate per this section unless the pin is used for GPIO purposes. Figure 17 shows the general chaining of function for the LEDs. The various functions are described in the following sections. All LED pins are tri-state outputs.

Figure 17: LED Chain


## LED Operations

The LED pins relay various statuses of the PHY so that they can be displayed by the LEDs.
The status that the LEDs display is defined by registers 31.F438, 31.F43A, 31.F43C, and 31.F43E as shown in Table 20. For each LED, if the condition selected by bits 11:8 is true, then the LED will blink. If the condition selected by bits $7: 4$ is true, then the LED will be solid on. If both selected conditions are true, then the blink will take precedence.
LEDO displays the status of lane 0, and LED1 displays the status of lane 1, and so on. Register bit 31.F438.12 is set to 1 to display the status of system (host) side transmit activity, receive activity and link status register on LED 0. Setting 31.F438.12 to 0 will display the status of line side on LED 0 . Similarly, register bits 31.F43A.12, 31.F43C.12, and 31.F43E. 12 are used to select the status of the host side or the line side for LED1, LED2, and LED3.

## Functional Description <br> TWSI, GPIO, and LED

## LED Polarity

There are a variety of methods to hook up the LEDs. Some examples are shown in Figure 18. Registers 31.F438.1:0, 31.F43A.1:0, 31.F43C.1:0, and 31.F43E.1:0 specify the output polarity for the LED function to accommodate a variety of installation options. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z.

Figure 18: Various LED Hookup Configurations


Table 20: LED[3:0] Control and Status Register Bits

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F438.15:13 | Reserved | Scratch reserved register | R/W |
| 31.F43A.15:13 |  |  |  |
| 31.F43C.15:13 |  |  |  |
| 31.F43E.15:13 |  | $0=$ PHY side (line side). |  |
| 31.F438.12 | LED[n] PHY/System side | $1=$ System side (host side). |  |
| 31.F43A.12 | select |  |  |
| 31.F43C.12 | Where $\mathrm{n}=0,1,2,3$ |  | R/W |
| 31.F43E.12 |  | Blink Behavior has higher priority. |  |
| 31.F438.11:8 | LED[n] Blink Behavior | $0000=$ Solid Off |  |
| 31.F43A.11:8 | Where $\mathrm{n}=0,1,2,3$ | $0001=$ System or Line Side Transmit or Receive Activity |  |
| 31.F43C.11:8 |  | $0010=$ System or Line Side Transmit Activity |  |
| 31.F43E.11:8 |  | $0011=$ System or Line Side Receive Activity |  |
|  |  | $0100=$ Reserved |  |
|  |  | $0101=$ Reserved |  |
|  |  | $0110=$ System or Line Side Side Link |  |
|  |  | $0111=$ Solid On |  |
|  |  | $1000=$ Reserved |  |
|  |  | $1001=$ Reserved |  |
|  |  | $1010=$ Blink Mix |  |
|  |  | $11 x=$ Solid Mix | Reserved |

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Table 20: LED[3:0] Control and Status Register Bits (Continued)

| Register | Function | Setting | Mode |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { 31.F438.7:4 } \\ & \text { 31.F43A.7:4 } \\ & \text { 31.F43C.7:4 } \\ & \text { 31.F43E.7:4 } \end{aligned}$ | LED[n] Solid Behavior Where $\mathrm{n}=0,1,2,3$ | Blink Behavior has higher priority. <br> $0000=$ Solid Off <br> 0001 = System or Line Side Transmit or Receive Activity <br> 0010 = System or Line Side Transmit Activity <br> 0011 = System or Line Side Receive Activity <br> 0100 = Reserved <br> 0101 = Reserved <br> $0110=$ System or Line Side Link <br> 0111 = Solid On <br> 1xxx = Reserved | R/W |
| $\begin{aligned} & \text { 31.F438.3 } \\ & \text { 31.F43A. } 3 \\ & \text { 31.F43C. } 3 \\ & \text { 31.F43E. } 3 \end{aligned}$ | Reserved | Set to 0 . | R/W |
| $\begin{aligned} & \text { 31.F438. } 2 \\ & \text { 31.F43A. } 2 \\ & \text { 31.F43C. } 2 \\ & \text { 31.F43E. } 2 \end{aligned}$ | LED[n] Blink Rate Select Where $\mathrm{n}=0,1,2$, 3 | $0=$ Select Blink Rate 1 <br> 1 = Select Blink Rate 2 | R/W |
| $\begin{aligned} & \text { 31.F438.1:0 } \\ & \text { 31.F43A.1:0 } \\ & \text { 31.F43C.1:0 } \\ & \text { 31.F43E.1:0 } \end{aligned}$ | LED[n] Polarity <br> Where $\mathrm{n}=0,1,2,3$ | $00=0 \mathrm{n}$ - drive LED[n] low, Off - drive LED[n] high <br> 01 = On - drive LED[ $n$ ] high, Off - drive LED[ n ] low <br> $10=$ On - drive LED[n] low, Off - tri-state LED[ n ] <br> 11 = On - drive LED[ n ] high, Off - tri-state LED[ n ] |  |

## Pulse Stretching and Blinking

Register 31.F435.14:12 specifies the pulse stretching duration for a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Registers 31.F435.10:8 and 31.F435.6:4 specify the two blink rates. The pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse. Registers 31.F438.2, 31.F43A.2, 31.F43C.2, and 31.F43E. 2 select which of the two blink rates to use for LED0 to LED3, respectively.

- $0=$ Select Blink Rate 1.
- 1 = Select Blink Rate 2.

Table 21: LED Timer Control

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F435.15 | Reserved | Set to 0. | R/W |

Table 21: LED Timer Control (Continued)

| Register | Function | Setting | Mode |
| :---: | :---: | :---: | :---: |
| 31.F435.14:12 | Pulse Stretch Duration | $\begin{aligned} & 000=\text { No pulse stretching } \\ & 001=20 \text { to } 40 \mathrm{~ms} \\ & 010=40 \text { to } 81 \mathrm{~ms} \\ & 011=81 \text { to } 161 \mathrm{~ms} \\ & 100=161 \text { to } 322 \mathrm{~ms} \\ & 101=322 \text { to } 644 \mathrm{~ms} \\ & 110=644 \mathrm{~ms} \text { to } 1.3 \mathrm{~s} \\ & 111=1.3 \text { to } 2.6 \mathrm{~s} \end{aligned}$ | R/W |
| 31.F435.11 | Reserved | Set to 0 . | R/W |
| 31.F435.10:8 | Blink Rate 2 | $\begin{aligned} & 000=40 \mathrm{~ms} \\ & 001=81 \mathrm{~ms} \\ & 010=161 \mathrm{~ms} \\ & 011=322 \mathrm{~ms} \\ & 100=644 \mathrm{~ms} \\ & 101=1.3 \mathrm{~s} \\ & 110=2.6 \mathrm{~s} \\ & 110=5.2 \mathrm{~s} \end{aligned}$ | R/W |
| 31.F435.7 | Reserved | Set to 0 . | R/W |
| 31.F435.6:4 | Blink Rate 1 | $\begin{aligned} & 000=40 \mathrm{~ms} \\ & 001=81 \mathrm{~ms} \\ & 010=161 \mathrm{~ms} \\ & 011=322 \mathrm{~ms} \\ & 100=644 \mathrm{~ms} \\ & 101=1.3 \mathrm{~s} \\ & 110=2.6 \mathrm{~s} \\ & 110=5.2 \mathrm{~s} \end{aligned}$ | R/W |
| 31.F435.3:0 | Reserved | Set to 0 . | R/W |

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### 3.5.2 TWSI, GPIO 4, and GPIO 5

The SCL and SDA pins are for TWSI mode and have the option to be used for GPIO functional mode. In TWSI mode, the SCL and SDA pins are coupled together, where the SCL pin is used as a clock, and SDA is used as a serial bidirectional data. The pin mapping is summarized in Table 22.

Table 22: TWSI and GPIO Signal Mapping

| Pin | GPIO | TWSI |
| :--- | :--- | :--- |
| SCL | GPIO[4] | TWSI clock (SCL) |
| SDA | GPIO[5] | TWSI serial data (SDA) |

The SCL and SDA pins are configured to TWSI mode by setting 31.F430.14 to 0 . TWSI is the default mode for these pins. SCL pin is configured in GPIO mode by setting register bits 31.F430.14 to 1 . Similarly, SDA pin is configured in GPIO mode by setting register bits 31.F432.14 to 1 .

TWSI is the two-wire serial interface standard. In a special mode, TWSI is used to load the SERDES and chip management firmware from an external EEPROM immediately after the reset is de-asserted. EEPROM is attached to the TWSI interface via the SCL and SDA pins. This interface can also be used to write the external EEPROM from an internal RAM using the embedded processor.

Table 23: SCL Control

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F430.15 | Reserved | Reserved | RO |
| 31.F430.14 | SCL Function | TWSI mode for SCL and SDA pins are selected by 31.F430.14 only. <br> Register 31.F432.14 has no effect on TWSI mode. <br> GPIO functions are controlled individually for each pin. <br> $0=$ SCL/SDA is used for TWSI Function. <br> $1=$ SCL is used for GPIO Function, if 31.F427.7 = 0. <br> $1=$ SCL is used for divided recovered clock B, when 31.F427.7 = 1. | R/W |
| 31.F430.13 | SCL Output <br> Enable | This bit has no effect unless register 31.F430.14 = 1 and 31.F427.7 = 0. <br> $0=$ Input <br> $1=$ Output | R/W |
| 31.F430.12 | SCL Interrupt <br> Enable | $0=$ Disable <br> $1=$ Enable | R/W |
| 31.F430.11 | SCL Interrupt <br> Status | This bit is not valid unless register 31.F430.14 = 1 and 31.F430.13 = 0. <br> $0=$ No interrupt has occurred. <br> $1=$ An interrupt has occurred. | RO, LH |

Table 23: SCL Control (Continued)

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F430.10:8 | SCL Interrupt <br> Select | Interrupt is effective only when 31.F430.13 = 0. <br> $000=$ No Interrupt <br> $001=$ Reserved <br> $010=$ Interrupt on Low Level <br> $011=$ Interrupt on High Level <br> $100=$ Interrupt on High to Low <br> $101=$ Interrupt on Low to High <br> $110=$ Reserved <br> $111=$ Interrupt on Low to High or High to Low | R/W |
| 31.F430.7 | SCL GPIO <br> Data | This bit has no effect unless register 31.F430.14 = 1. <br> When 31.F430.13 = 0, a read to this register will reflect the state of the <br> SCL pin, and a write will write the output register but have no effect on <br> the SCL pin. <br> When 31.F430.13 = 1, a read to this register will reflect the state of the <br> output register, and a write will write the output register and drive the <br> state of the SCL pin. | R/W |
| 31.F430.6:0 | Reserved | Set to 0s. | RO |

Table 24: SDA Control

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F432.15 | Reserved | Reserved. | RO |
| 31.F432.14 | SDA Function | TWSI mode for SCL and SDA pins are selected by 31.F430.14 only. <br> Register 31.F432.14 has no effect on TWSI mode, but can enable <br> the GPIO or Recovered clock output function on this pin. <br> $0=$ Reserved <br> $1=$ SDA is used for GPIO 5 Function if 31.F427.11 = 0. <br> $1=$ SDA is used for divided recovered clock C if 31.F427.11 $=1$. | R/W |
| 31.F432.13 | SDA Output Enable | This bit has no effect unless register 31.F432.14 =1 and register <br> 31. LT27.11 $=0$. <br> $0=$ Input <br> $1=$ Output | R/W |
| 31.F432.12 | SDA Interrupt Enable | $0=$ Disable <br> $1=$ Enable |  |
| 31.F432.11 | SDA Interrupt Status | This bit is not valid unless register 31.F432.14 = 1 and register <br> $31 . F 432.13=0$. <br> $0=$ No interrupt has occurred. <br> $1=$ An interrupt has occurred. | RO, LH |

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Table 24: SDA Control (Continued)

| Register | Function | Setting | Mode |
| :--- | :--- | :--- | :--- |
| 31.F432.10:8 | SDA Interrupt Select | Interrupt is effective only when 31.F432.13 = 0. <br> $000=$ No Interrupt <br> $001=$ Reserved <br> $010=$ Interrupt on Low Level <br> $011=$ Interrupt on High Level <br> $100=$ Interrupt on High to Low <br> $101=$ Interrupt on Low to High <br> $110=$ Reserved <br> $111=$ Interrupt on Low to High or High to Low | R/W |
| 31.F432.7 | SDA GPIO Data | This bit has no effect unless register 31.F432.14 =1. <br> When 31.F432.13 = 0, a read to this register will reflect the state of <br> the SDA pin, and a write will write the output register but have no <br> effect on the SDA pin. <br> When 31.F432.13 = 1, a read to this register will reflect the state of <br> the output register, and a write will write the output register and <br> drive the state of the SDA pin. | R/W |
| 31.F432.6:0 | Reserved | Set to 0s. |  |

Table 25: I/O Open Drain Control

| Register | Function | Setting | Mode |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Port0 } \\ & \text { 31.F436.15:3 } \end{aligned}$ | Reserved | Set to 0 . | R/W |
| $\begin{aligned} & \text { Port0 } \\ & \text { 31.F436.2 } \end{aligned}$ | GPIO1 pin (port0 GPIO[0]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| $\begin{aligned} & \text { Port0 } \\ & \text { 31.F436.1:0 } \end{aligned}$ | Reserved | Set to 0 . | R/W |
| Port1 31.F436.15:7 | Reserved | Set to 0 . | R/W |
| Port1 31.F436.6 | GPIO2 pin (port1 GPIO[4]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| Port1 31.F436.5:4 | Reserved | Set to 0 . | R/W |
| $\begin{aligned} & \text { Port2 } \\ & \text { 31.F436.15:3 } \end{aligned}$ | Reserved | Set to 0. | R/W |
| $\begin{aligned} & \text { Port2 } \\ & \text { 31.F436.2 } \end{aligned}$ | GPIO3 pin (port2 GPIO[0]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| Port2 31.F436.1:0 | Reserved | Set to 0 . | R/W |
| $\begin{aligned} & \text { Port3 } \\ & \text { 31.F436.7 } \end{aligned}$ | CLK_OUT_SE2 pin (port3 GPIO[5]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| $\begin{aligned} & \text { Port3 } \\ & \text { 31.F436.6 } \end{aligned}$ | CLK_OUT_SE1 pin (port3 GPIO[4]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| Port3 31.F436.5 | Reserved | Set to 0 . | R/W |
| $\begin{aligned} & \text { Port3 } \\ & \text { 31.F436.4 } \end{aligned}$ | GPIO4 pin (port3 GPIO[2]) open drain control | $0=$ Pad can drive high. <br> 1 = Pad cannot drive high (Set to high when open drain pad is used). | R/W |
| $\begin{aligned} & \text { Port3 } \\ & \text { 31.F436.3:0 } \end{aligned}$ | Reserved | Set to 0 . | R/W |

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### 3.5.3 Two-wire Serial Interface (TWSI)

TWSI is used to load the SERDES and chip management firmware from an external EEPROM. EEPROM is attached to the TWSI interface via the SCL and SDA pins. This interface can also be used to write the external EEPROM from an internal RAM using the embedded processor. External pull up resisters are required to connect to SCL and SDA pins.

### 3.6 Interrupt

Various functional units in the device can generate interrupt on the INTn pin. The INTn interrupt pin will be active if any of the events enabled in the interrupt enable register occurs. If an interrupt event corresponding to a disabled interrupt enable bit occurs, then the corresponding interrupt status bit will be set even though the event does not activate the INTn pin.
By default, the INTn is driven low when an enabled interrupt is active. The polarity of the INTn pin can be changed by programming register 31.F421.2:1. The INTn pin can also be forced to be active by setting the register 31.F421.0 to 1.

Table 26: Global Interrupt Control

| Register | Function | Setting |
| :--- | :--- | :--- |
| 31.F421.2:1 | Interrupt Polarity | $00=$ Active - drive INT low, Inactive - drive INT high <br> $01=$ Active - drive INT high, Inactive - drive INT low <br> $10=$ Active - drive INT Iow, Inactive - tri-state INT <br> $11=$ Active - drive INT high, Inactive - tri-state INT |
| 31.F421.0 | Force Interrupt Pin <br> Active | $0=$ Normal operation <br> $1=$ Force interrupt pin active. |

The interrupts are cleared after a read to the interrupt status register. F

The Global Interrupt Status register (Table 27) summarizes which unit is requesting the interrupt. The interrupts are logically ORed along with register 31.F421.0 to form the interrupt output (INTn). The Global Interrupt Status register bits do not have corresponding Interrupt Enable bits. All the interrupt enables/masks are located within each unit.

Figure 19 diagram shows the interrupt hierarchy and aggregation from different blocks.
Figure 19: Interrupt Hierarchy and Aggregation from Different Blocks


Table 27: Global Interrupt Status

| Bit Descriptions | Register |
| :--- | :--- |
| Temp Sensor Interrupt Status | $31 . \mathrm{F} 420.11$ |
| GPIO Interrupt Status | $31 . \mathrm{F} 420.10$ |
| RM_FIFO Interrupt Status | $31 . \mathrm{F} 420.9$ |
| On-chip Processor Interrupt Status | $31 . \mathrm{F420.8}$ |
| M0 Interrupt Status | $31 . \mathrm{F} 420.4$ |
| N0 Interrupt Status | $31 . \mathrm{F} 420.0$ |

Table 28, Table 29, Table 30, and Table 31 summarize the Line Side (N Unit) interrupt control and statuses for various interface modes. Excessive link error can be monitored to generate an interrupt event (See Table 32).

The Host Side (M Unit) has the same set of interrupt function with the exception that the device register is 4 (instead of 3 ).
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Each bit of the Interrupt Status register will be masked with the Interrupt Enable register, respectively, and each enabled output is ORed to form the aggregated unit interrupt. The Port Interrupt Statuses (register 31.F004.0 - Line Side Interrupt, register 31.F004.2 - System Side Interrupt) are the result of logical OR of the aggregated unit interrupt.

Table 28: 1G/2.5G Interrupt Enable, Interrupt Status, and Real-Time Status

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| Speed Changed | $3 . B n 01.14$ | $3 . B n 02.14$ | - |
| Duplex Changed | $3 . B n 01.13$ | $3 . B n 02.13$ | - |
| Page Received | $3 . B n 01.12$ | $3 . B n 02.12$ | - |
| Auto-Negotiation Completed | $3 . B n 01.11$ | $3 . B n 02.11$ | - |
| Link Up to Link Down | $3 . B n 01.10$ | $3 . B n 02.10$ | - |
| Link Down to Link Up | $3 . B n 01.9$ | $3 . B n 02.9$ | - |
| Symbol Error | $3 . B n 01.8$ | $3 . B n 02.8$ | - |
| False Carrier | $3 . B n 01.7$ | $3 . B n 02.7$ | - |

Where $\mathrm{n}=0,2,4$, 6 for Lane $0,1,2$, and 3 , respectively.
Table 29: 10G/25G Interrupt Enable, Interrupt Status, and Real-Time Status

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| Local Fault Transmitted | 3. An00.11 | 3. An01.11 | 3.An02.11 |
| Local Fault Received | $3 . A n 00.10$ | $3 . A n 01.10$ | 3.An02.10 |
| Rx FIFO Full | $3 . A n 00.6$ | $3 . A n 01.6$ | 3.An02.6 |
| Rx FIFO Empty | $3 . A n 00.5$ | $3 . A n 01.5$ | 3.An02.5 |
| Link Status Change | $3 . A n 00.2$ | $3 . A n 01.2$ | $3 . A n 02.2$ |
| High BER Change | $3 . A n 00.1$ | $3 . A n 01.1$ | 3.An02.1 |
| Block Lock Change | $3 . A n 00.0$ | $3 . A n 01.0$ | $3 . A n 02.0$ |
| CRC | $3 . A n 4 A .2$ | $3 . A n 4 B .2$ | - |
| FIFO Overflow | $3 . A n 4 A .1$ | $3 . A n 4 B .1$ | - |
| FIFO Underflow | $3 . A n 4 A .0$ | $3 . A n 4 B .0$ | - |

Where $\mathrm{n}=0,2,4$, 6 for Lane 0, 1, 2, and 3, respectively.

Table 30: 40G/50G Interrupt Enable, Interrupt Status, and Real-Time Status

| Bit Descriptions | Interrupt Enable | Interrupt Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| Local Fault Transmitted | 3.9001 .11 | 3.9002 .11 | 3.9003 .11 |
| Local Fault Received | 3.9001 .10 | 3.9002 .10 | 3.9003 .10 |
| Lane Alignment | 3.9001 .9 | 3.9002 .9 | 3.9003 .9 |
| Tx Lane Count err | 3.9001 .8 | 3.9002 .8 | 3.9003 .8 |
| JIT 0 Lock Change | 3.9001 .7 | 3.9002 .7 | 3.9003 .7 |
| JIT Local-Fault Lock Change | 3.9001 .6 | 3.9002 .6 | 3.9003 .6 |
| Link Status Change | 3.9001 .5 | 3.9002 .5 | 3.9003 .5 |
| High BER Change | 3.9001 .4 | 3.9002 .4 | 3.9003 .4 |
| Lane 3:0 Block Lock Change | $3.9001 .3: 0$ | $3.9002 .3: 0$ | $3.9003 .3: 0$ |
| CRC | 3.904 A .2 | 3.904 B .2 | - |
| FIFO Overflow | 3.904 A .1 | 3.904 B .1 | - |
| FIFO Underflow | 3.904 A .0 | 3.904 B .0 | - |

Where $\mathrm{n}=0,2,4,6$ for Lane $0,1,2$, and 3, respectively.

Table 31: 100G Interrupt Enable, Interrupt Status, and Real-Time Status

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| 100G PCS Rx FIFO Empty | 3.8001 .15 | 3.8003 .15 | 3.8005 .15 |
| 100G PCS Rx FIFO Full | 3.8001 .14 | 3.8003 .14 | 3.8005 .14 |
| 100G PCS Tx PPM FIFO Overflow | 3.8001 .13 | 3.8003 .13 | 3.8005 .13 |
| 100G PCS Tx PPM FIFO Underflow | 3.8001 .12 | 3.8003 .12 | 3.8005 .12 |
| Rising Edge of the Local Fault Condition on Tx Path | 3.8001 .11 | 3.8003 .11 | 3.8005 .11 |
| Rising Edge of the Local Fault Condition on Rx Path | 3.8001 .10 | 3.8003 .10 | 3.8005 .10 |
| 100G Packet Check CRC Error | 3.8001 .7 | 3.8003 .7 | 3.8005 .7 |
| Link Change | 3.8001 .5 | 3.8003 .5 | 3.8005 .5 |
| High BER Change | 3.8001 .4 | 3.8003 .4 | 3.8005 .4 |
| Lane 3:0 Block Lock Change | $3.8001 .3: 0$ | $3.8003 .3: 0$ | $3.8005 .3: 0$ |
| Lane 19:4 Block Lock Change | $3.8002 .15: 0$ | $3.8004 .15: 0$ | $3.8006 .15: 0$ |

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Where $\mathrm{n}=0,2$ for Lane 0, 2, respectively.

Table 32: Excessive Link Error Interrupt Enable, Interrupt Status, and Real-Time Status

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| Excessive Link Error - Lane 0 <br> In 40G/50G/100G mode, only Lane 0 interrupt is used <br> (Lane 1, 2, and 3 interrupts bits are ignored). <br> Register 3.F041.6:0 sets the link error threshold setting. <br> Register 3.F041.7 sets the link down or link up error <br> setting. | 3. F041.8 | 3. F040.15 | 3.F040.14 |
| Excessive Link Error - Lane 1 <br> Register 3.F043.6:0 sets the link error threshold setting. <br> Register 3.F043.7 sets the link down or link up error <br> setting. | 3. F043.8 | 3. F042.15 | 3.F042.14 |
| Excessive Link Error - Lane 2 <br> Register 3.F045.6:0 sets the link error threshold setting. <br> Register 3.F045.7 sets the link down or link up error <br> setting. | $3 . F 045.8$ | $3 . F 044.15$ | 3.5044 .14 |
| Excessive Link Error - Lane 3 <br> Register 3.F047.6:0 sets the link error threshold setting. <br> Register 3.F047.7 sets the link down or link up error <br> setting. | 3. F047.8 | 3.F046.15 | 3.F046.14 |

The interrupt from the processor block is for debug or patch program: details are not provided here (For further details, refer to Section 3.10).
All of the GPIO interrupts are only valid when the multi-function pins are configured as GPIO Inputs.

Table 33: GPIO1, GPIO2, GPIO3, GPIO4, CLK_OUT_SE1, CLK_OUT_SE2 Pins Interrupt

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| GPIO1 Pin (Port0, GPIO[0]) <br> Valid only when register port0.31.F437.15:14 $=01$ and <br> port0.31.F437.13 $=0$. <br> Register port0.31.F437.10:8 is used to select the <br> interrupt behavior. | port0. <br> $31 . F 437.12$ | port0. <br> $31 . F 437.11$ | port0. <br> $31 . F 437.7$ |
| GPIO2 Pin (Port1, GPIO[4]) <br> Valid only when register port1.31.F430.15:14 $=01$ and <br> port1.31.F430.13 $=0$. | port1. <br> Register port1.31.F430.10:8 is used to select the <br> interrupt behavior. |  |  |
| GPIO3 Pin (Port2, GPIO[0]) <br> Valid only when register port2.31.F437.15:14 $=01$ and <br> port2.31.F437.13 $=0$. | port2. <br> Register port2.31.F437.10:8 is used to select the | port1. <br> interrupt behavior. | $31 . \mathrm{F} 430.11$ |

Table 34 summarizes the temperature sensor and GPIOs interrupt.

Table 34: Temp Sensor and GPIOs, Interrupt Enable, Interrupt Status

| Bit Descriptions | Interrupt <br> Enable | Interrupt <br> Status | Real-Time <br> Status |
| :--- | :--- | :--- | :--- |
| Temperature Sensor <br> Register 31.F707.15:8 sets the temperature threshold. | 31. F41F.15 | 31. F705.6 | See the Temp <br> Sensor <br> section. |

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Table 34: Temp Sensor and GPIOs, Interrupt Enable, Interrupt Status (Continued)

| Bit Descriptions | Interrupt Enable | Interrupt Status | Real-Time Status |
| :---: | :---: | :---: | :---: |
| GPIO 0 (LED 0) <br> Valid only when register 31.F437.15:14 = 01 and 31.F437.13 $=0$. <br> Register 31.F437.10:8 is used to select the interrupt behavior. | 31.F437.12 | 31.F437.11 | 31.F437.7 |
| GPIO 1 (LED 1) <br> Valid only when register 31.F439.15=0 and 31.F439.13 = 0 . <br> Register 31.F439.10:8 is used to select the interrupt behavior. | 31.F439.12 | 31.F439.11 | 31.F439.7 |
| GPIO 2 (LED 2) <br> Valid only when register 31.F43B.15=0 and 31.F43B. $13=0$. <br> Register 31.F43B.10:8 is used to select the interrupt behavior. | 31.F43B. 12 | 31.F43B. 11 | 31.F43B. 7 |
| GPIO 3 (LED 3) <br> Valid only when register 31.F43D.15=0 and 31.F43D. $13=0$. Register 31.F43D.10:8 is used to select the interrupt behavior. | 31.F43D. 12 | 31.F43D. 11 | 31.F43D. 7 |
| GPIO 4 (SCL) <br> Valid only when register 31.F430.14 = 1, 31.F427.7 = 0, and 31.F430.13 = 0 . <br> Register 31.F430.10:8 is used to select the interrupt behavior. | 31.F430.12 | 31.F430.11 | 31.F430.7 |
| GPIO 5 (SDA) <br> Valid only when register 31.F432.14 = 1, 31.F427.11 = 0, and 31.F432.7 = 0 . <br> Register 31.F432.10:8 is used to select the interrupt behavior. | 31.F432.12 | 31.F432.11 | 31.F432.7 |

### 3.7 Power Management

The device will exit reset in a powered down state.
In general, it is not necessary to power down an unused interface. The device will automatically power down any unused circuits. Each of the ports or blocks can be manually powered down by setting the respective power down control bits as described in Table 35.
To prevent fragmentation, the power down control function is designed to wait until the datapath is IDLE with the exception of Per Lane/Interface Mode Power Down control bits that are activated immediately and may cause fragmentation in the datapath.

Table 35: Power Down Control Bits

| Power Down Bits Description | Unit Affected | Register Line | $\begin{aligned} & \text { Register - } \\ & \text { Host } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| Port Power Down <br> This bit power-down all the lanes of the respective interface regardless of the interface mode. | Port | 31.F003.14 | 31.F003.6 |
| Per Lane/Interface Mode Power Down In 40G/50G/100G mode, power-down to lane 0 will be applied to all lanes (Lane 1, 2, and 3 power-down bits are ignored). | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & \text { 3.F000.13 } \\ & \text { 3.F001.13 } \\ & \text { 3.F002.13 } \\ & \text { 3.F003.13 } \end{aligned}$ | 4.F000.13 <br> 4.F001.13 <br> 4.F002.13 <br> 4.F003.13 |
| PMA Power Down <br> In 40G/50G/100G mode, power-down to lane 0 will be applied to all lanes (Lane 1, 2, and 3 power-down bits are ignored). | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 1.0000 .11 \\ & 1.2000 .11 \\ & 1.4000 .11 \\ & 1.6000 .11 \end{aligned}$ | $\begin{aligned} & 1.1000 .11 \\ & 1.3000 .11 \\ & 1.5000 .11 \\ & 1.7000 .11 \end{aligned}$ |
| PCS Power-Down - 100G | Lane 0/Aggregated Port (lane 0-3 coupled) | 3.0000.11 | 4.0000 .11 |
| PCS Power-Down - 40G/50G | Lane 0/Aggregated Port (lane 0-3 coupled) | 3.1000 .11 | 4.1000 .11 |
| PCS Power-Down - 5G/10G/25G | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.2000 .11 \\ & 3.2200 .11 \\ & 3.2400 .11 \\ & 3.2600 .11 \end{aligned}$ | $\begin{aligned} & 4.2000 .11 \\ & 4.2200 .11 \\ & 4.2400 .11 \\ & 4.2600 .11 \end{aligned}$ |
| PCS Power-Down - 1G/2.5G | Lane 0/Aggregated Port <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.3000 .11 \\ & 3.3200 .11 \\ & 3.3400 .11 \\ & 3.3600 .11 \end{aligned}$ | $\begin{aligned} & 4.3000 .11 \\ & 4.3200 .11 \\ & 4.3400 .11 \\ & 4.3600 .11 \end{aligned}$ |

Registers 3.F000 through 3.F003 or 4.F000 through 4.F003 define the operation modes for fixed mode. The power down bit 13 of them is only to be used for fixed mode. When Aneg is enabled, these registers are ignored.

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### 3.8 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC-coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The device implements the instructions shown in Table 36. Upon reset, ID_CODE instruction is selected. The instruction opcodes are shown in Table 36.

Table 36: TAP Controller Opcodes

| Instruction | OpCode |
| :--- | :--- |
| EXTEST | $00 \_0 \times 0$ |
| SAMPLE/PRELOAD | $00 \_0000 \_0001$ |
| CLAMP | $00 \_0000 \_0010$ |
| HIGH-Z | $00 \_0000 \_0011$ |
| ID_CODE | $00 \_0000 \_0100$ |
| EXTEST_PULSE | $00 \_0000 \_0101$ |
| EXTEST_TRAIN | $00 \_0000 \_0110$ |
| BYPASS | $11 \_1111 \_1111$ |

The device reserves five pins called the Test Access Port (TAP) to provide test access:

- Test Mode Select Input (TMS)
- Test Clock Input (TCK)
- Test Data Input (TDI)
- Test Data Output (TDO)
- Test Reset Input (TRSTn)

To ensure race-free operation all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

### 3.8.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the 88X5113 device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

### 3.8.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the device. Two functions are performed when this instruction is selected: sample and preload.
Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.
The boundary scan register for CONFIG[2] is closest to TDO.
Table 37 lists the boundary scan order where:
TDI $\rightarrow$ LIN[0] $\rightarrow \ldots \rightarrow$ CONFIG[2] $\rightarrow$ TDO
Table 37: Boundary Scan Chain Order

| Order | Ball | Type |
| :--- | :--- | :--- |
| 1 | CONFIG[2] | Input |
| 2 | CONFIG[1] | Input |
| 3 | CONFIG[0] | Input |
| 4 | PHYAD[2] | Input |
| 5 | PHYAD[3] | Input |
| 6 | PHYAD[1] | Input |
| 7 | INTN | Input |
| 8 | MDC | Output |
| 9 | MDIO | Output Enable |
| 10 | MDIO | Input |
| 11 | MDIO | Output |
| 12 | HOP[3] | Output Enable |
| 13 | HON[3] | AC Output |
| 14 | HIP[3] | AC Output |
| 15 | HIN[3] | AC Input |
| 16 |  | AC Input |
| 17 |  |  |

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Table 37: Boundary Scan Chain Order (Continued)

| Order | Ball | Type |
| :---: | :---: | :---: |
| 18 | HOP[2] | AC Output |
| 19 | HON[2] | AC Output |
| 20 | HIP[2] | AC Input |
| 21 | HIN[2] | AC Input |
| 22 | HOP[1] | AC Output |
| 23 | HON[1] | AC Output |
| 24 | HIP[1] | AC Input |
| 25 | HIN[1] | AC Input |
| 26 | HOP[0] | AC Output |
| 27 | HON[0] | AC Output |
| 28 | HIP[0] | AC Input |
| 29 | HIN[0] | AC Input |
| 30 | SCL | Output Enable |
| 31 | SCL | Output |
| 32 | SCL | Input |
| 33 | SDA | Output Enable |
| 34 | SDA | Output |
| 35 | SDA | Input |
| 36 | RESETN | Input |
| 37 | GPIO[0] | Output Enable |
| 38 | GPIO[0] | Output |
| 39 | GPIO[0] | Input |
| 40 | GPIO[1] | Output Enable |
| 41 | GPIO[1] | Output |
| 42 | GPIO[1] | Input |
| 43 | GPIO[2] | Output Enable |
| 44 | GPIO[2] | Output |
| 45 | GPIO[2] | Input |
| 46 | GPIO[3] | Output Enable |

Table 37: Boundary Scan Chain Order (Continued)

| Order | Ball | Type |
| :---: | :---: | :---: |
| 47 | GPIO[3] | Output |
| 48 | GPIO[3] | Input |
| 49 | LOP[3] | AC Output |
| 50 | LON[3] | AC Output |
| 51 | LIP[3] | AC Input |
| 52 | LIN[3] | AC Input |
| 53 | LOP[2] | AC Output |
| 54 | LON[2] | AC Output |
| 55 | LIP[2] | AC Input |
| 56 | LIN[2] | AC Input |
| 57 | LOP[1] | AC Output |
| 58 | LON[1] | AC Output |
| 59 | LIP[1] | AC Input |
| 60 | LIN[1] | AC Input |
| 61 | LOP[0] | AC Output |
| 62 | LON[0] | AC Output |
| 63 | LIP[0] | AC Input |
| 64 | LIN[0] | AC Input |

### 3.8.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the 88X5113 device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. So, when the change to the extest instruction occurs, known data is driven immediately from the 88X5113 to its external connections. The SERDES output pins will be driven to static levels. The positive and negative legs of the SERDES output pins are controlled via a single boundary scan cell. The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

### 3.8.4 CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

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### 3.8.5 HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

The SERDES outputs cannot be tri-stated.
Note

### 3.8.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.
Table 38: ID CODE Instruction

| Version | Part Number | Manufacturer Identity |  |
| :--- | :--- | :--- | :--- |
| Bit 31 to 28 | Bit 27 to 12 | Bit 11 to 1 | Bit 0 |
| 0000 | 0000000001000110 | 00111101001 | 1 |

### 3.8.7 EXTEST PULSE Instruction

When the AC/DC select is set to DC the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the SERDES output pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers Upon the execution of the EXTEST_PULSE instruction the SERDES positive output pins output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the SERDES positive output pins output the inverted level specified by the test stimulus and SERDES negative output pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the SERDES positive output pins again output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

### 3.8.8 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the SERDES output pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the SERDES positive output pins output the level specified by the test stimulus and SERDES negative output pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the SERDES output pins will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

## Functional Description <br> Temperature Sensor

When the TAP controller exits the Run-Test/Idle state, the SERDES positive output pins again output the level specified by the test stimulus and SERDES negative output pins output the opposite level. Reference Clock

An external oscillator provides a reference for the on-board transmit Phase Lock Loop (PLL) and clock generation block that provides internal clocks for both the transmit and receive data paths. A 156.25 MHz differential clock should be connected to the CLKP/CLKN pins. AC coupling is required for the pins. The detail requirements for CLKP/CLKN inputs are listed in Section 7.7.

The device can generate a 25 MHz differential output clock on the CLK25P/CLK25N pins that is frequency locked to the 156.25 MHz clock on the CLKP/CLKN pins. If AVDDT is connected to 2.5 V or 3.3 V supply, then the CLK25P/CLK25N will start oscillating when CLKP/CLKN oscillates at start up. The 25 MHz clock can be disabled by coupling AVDDT to VSS. Additional details on the 25 MHz clock can be found in Section 6.1.

### 3.9 Temperature Sensor

The device contains an internal temperature sensor.

### 3.10 On-chip Processor

The chip has a small, efficient microcontroller with supporting hardware designed to offload the system's CPU by automating configuration and workaround tasks.

The processor block can access any register with a PHY and Dev address. It monitors the status of the chip, such as PCS mode, temperature reading, link status, and when it detects an irregularity, it initiates software routines to reconfigure or recover the chip. It supports the boot code loading function through the dedicated TWSI interface from external EEPROM to the internal RAM. There is also a provision to program the external EEPROM from the internal RAM through the common TWSI interface.

### 3.11 Synchronous Ethernet Mode

The device can output a divide-down version of recovered clock for other chips to synchronize to it. It has two applications as shown in following figures.

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Figure 20: Synchronous Ethernet with 88X5113 in a Non-Ethernet Application such as CPRI


Note: Only relevant signals paths shown in figure for clarity

Figure 21: Synchronous Ethernet with $88 \times 5113$ in an Ethernet Application


Note: Only relevant signal paths shown in figure for clarity

The recovered clock can be chosen from line side or host side, and from lane 0 to lane 3. The device has three methods to send out recovered clock (called RCLK A,B,C). RCLK A is sent to Interrupt pin (INTn). The RCLK B is sent to SCL pin. RCLK C is sent to SDA pin.
Figure 22 shows the registers to configure final recovered clock RCLK A to INTn pin. Register 31.F422 is controlling Line side clock divider 1 . Bit 0 will choose 32T clock when set to 1 and choose 40 T clock when set to 0 . Bit $2: 1$ will choose clock from lane 0~3. Bit 4 is set to 1 to enable the clock divider 1. Bit 5 will set whether to enable clock divider after SERDES clock is ready (set 1). Bit 15:8 configures the divider ratio for clock divider 1 . The divide ratio is 2 to the power of $([15: 8]+1)$.

Figure 22: Multiplexing Scheme for Recovered Clock RCLKA


Register 31.F424 controls the host-side clock divider 1. It has same definition as 31.F422.
Register 31.F423 and 31.F425 control Recovered Clock divider 2 of Line Side and Host side correspondingly.
The Line divider 1 clock and divider 2 clock go through MUX 1 and MUX2 to output two clocks (clock1 and clock2) for top-level. It is controlled by 31.F426.0 and 31.F426.2.

The Host divider 1 clock and divider 2 clock go through MUX1 and MUX2 to output two clocks (clock1 and clock2) for top-level. It is controlled by 31.F426.4 and 31.F426.6.

Line clock1, clock2 and Host clock1, clock2 will go through top-level two-level multiplexes to generate final RCLK A, B or C. Each of them can be chosen from either Line or Host side, either from clock1 or clock2 individually.

As shown in Figure 22, 31.F427.3:0 configures the final 4 to 1 selection for RCLK A (to INTn pin). Bit 0 selects Line clock1 or clock2. Bit 1 selects Host clock1 or clock2. Bit 3 choose the clock from Line or Host. Bit 4 is the final clock enable. The controls for RCLK B (to SCL) is 31.F427.7:4. The controls for RCLK C (to SDA) is 31.F427.11:8.

### 3.12 Power Supplies

The device requires the following supplies to power the core and I/O.

- AVDDL, AVDDH, and AVDDC should be tied together and sourced from the same power supply on the board.
- AVDDL: Line SERDES 1.0 V supply
- AVDDH: Host SERDES 1.0 V supply
- AVDDC: Common analog 1.0 V supply
- AVDDT: For 25 MHz PLL and temperature sensor function. 3.3 V or 2.5 V is required for operation.
- Couple AVDDT to VSS if the 25 MHz PLL and the temperature sensor functions are not needed. This pin can be tied together with VDDON or VDDOS with filtering to separate it from the digital supply.
- Core 0.9 V (Commercial) digital supply
- VDDON: Digital I/O supply. For 2.5 V or 3.3 V operation, the VSEL_N pin should be tied to VSS. For $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}, 1.8 \mathrm{~V}$ operation, the VSEL N pin should be tied to VDDON. The pins running on the VDDON supply are RESETn, SCL, SDA, TDI, TDO, TCK, TMS, TRSTn, GPIO[3:0].
- VDDOS: Digital I/O supply. For 2.5 V or 3.3 V operation, the VSEL_S pin should be tied to VSS. For $1.05 \mathrm{~V}, 1.2 \mathrm{~V}, 1.5 \mathrm{~V}$, and 1.8 V operation, the VSEL _S pin should be tied to VDDOS. The pins running on the VDDOS supply are MDC, MDIO, INTn, PHYAD[3:0], CONFIG[2:0], TEST[1:0].


## 4 <br> Line Side Description

The line interface comprises four differential input lanes and four differential output lanes. Table 40 lists out what is active for all the modes. The device can be configured to operate in single-port operation or four sub-port operation depending on how many SERDES lanes are used to form the port. Each sub-port's mode of operation can be configured via Auto-Negotiation or forced mode. Any of the modes shown in Table 40 can be set via forced mode. However, only the modes with the Y in the last column can be configured via Clause 73 Auto-Negotiation. Table 41 shows the register setting required to force a particular mode. Register 3.F000n is used to select the sub-port n .40 Gbps, 50 Gbps , and 100 Gbps speeds are not supported by sub-ports 1, 2, and 3.
For the purpose of the subsequent discussion, we will refer only to the registers in sub-port 0 unless otherwise noted. The registers in ports 1, 2, and 3 are offset as shown in the Equivalent Registers Between Line and Host Interface table in Section 5 and behave in the same way as sub-port 0. Single-port operation (multi-lane port operation) maps into sub-port 0 . That is, sub-port 0 supports all speeds, while sub-port 1,2 , and 3 supports neither $40 \mathrm{Gbps}, 50 \mathrm{Gbps}$, nor 100 Gbps speeds.

The priority for mode selection is listed in decreasing order of priority:

1. If Auto-Negotiation of sub-port 0 is enabled $(7.0000 .12=1)$ and any capability that requires multiple lanes is advertised (for example, $40 \mathrm{Gbps}, 50 \mathrm{Gbps}$, or 100 Gbps ), then operation on sub-ports 1, 2, and 3 are disabled. Registers 3.F000 to $3 . \mathrm{F0003}$ are ignored. Auto-Negotiation will determine the mode to operate. Even if the Auto-Negotiation result in a single-lane operation, sub-ports 1,2 , and 3 will still be disabled.
2. If Auto-Negotiation of sub-port 0 is disabled $(7.0000 .12=0)$, then register 3.F000 is used to force the mode of operation on sub-port 0 . If a capability that requires multiple lanes is selected, then operation on sub-ports 1, 2, and 3 are disabled and registers 3.F001 to 3.F003 are ignored.
3. If neither \#1 nor \#2 above are in effect, then each sub-port operates independently. If sub-port $n$ Auto-Negotiation is enabled then Auto-Negotiation will determine the mode to operate and register 3.F00n is ignored.
4. If none of the above are in effect, then register 3.F00n will determine the mode of operation.

If Auto-Negotiation is disabled on sub-port n and register 3.F00n selects a mode that requires Clause 72 training, then it is the user's responsibility to properly set the Auto-Negotiation registers to advertise only the capability that is consistent with the mode requested in register 3.F00n even though register 7.0000 .12 is set to 0 . The Auto-Negotiation in this case is used only to synchronize the two link partners in order to start the Clause 72 training. As part of the Clause 72 training procedure, the device will automatically initiate Auto-Negotiation even though register 7.0000.12 is set to 0 . When Auto-Negotiation completes the device will commence Clause 72 training for the mode selected in register 3.F00n. The device only checks that Auto-Negotiation completes, and does not check whether the resolved capability matches the mode selected in register 3.F00n.

### 4.1 Interface Modes of Operation

Table 39 provides a description of the interface modes of operations detailed in Table 40.
Table 39: Mode Definition Reference

| Symbol | Description |
| :---: | :---: |
| Type | $\begin{aligned} & P=P C S \\ & R=\text { Retimer } \end{aligned}$ |
| Speed | $1=1 \mathrm{Gbps}$ - single lane <br> $2.5=2.5 \mathrm{Gbps}$ - single lane <br> $5=5 \mathrm{Gbps}$ - single lane <br> $10=10 \mathrm{Gbps}$ - single lane <br> $25=25 \mathrm{Gbps}-1$ lane $\times 25 \mathrm{Gbps}$ or 2 lanes $\times 12.5 \mathrm{Gbps}$ or 4 lanes $\times 6.25 \mathrm{G}$ <br> $40=40 \mathrm{Gbps}-4$ lanes $\times 10 \mathrm{Gbps}$ <br> $50=50 \mathrm{Gbps}-1$ lane $\times 50 \mathrm{Gbps}$ or 2 lanes $\times 25 \mathrm{Gbps}$ or 4 lanes $\times 12.5 \mathrm{Gbps}$ <br> $100=100 \mathrm{Gbps}-2$ lanes $\times 50 \mathrm{Gbps}$ or 4 lanes $\times 25 \mathrm{Gbps}$ <br> $200=200$ Gbps -4 lanes $\times 50 \mathrm{Gbps}$ |
| Training/AN/Co ding | X = BASE-X <br> S = SGMII System <br> P = SGMII PHY <br> L = NRZ BASE-R/X, no Auto-Negotiation <br> K = NRZ BASE-R/X, Backplane <br> C = NRZ BASE-R, Twinax <br> $J=$ Same as K except consortium <br> B = Same as C except consortium <br> M = same as L Non-Standard 50GBASE-R2 <br> U = PAM4 BASE-R, no Auto-Negotiation <br> Q = PAM4 BASE-R, Twin ax/Backplane <br> Y = Same as L for Non-Standard 25GBASE-R2, no Auto-Negotiation <br> Z = Same as C for Non-Standard 25GBASE-R2, Auto-Negotiation <br> A = Same as L for Non-Standard 25GBASE-R4, no Auto-Negotiation <br> G = Same as C for Non-Standard 25GBASE-R4, Auto-Negotiation <br> H = Same as K for Non-Standard 25GBASE-R4, Auto-Negotiation |
| FEC | $\begin{aligned} & N=\text { No FEC } \\ & F=\text { KR-FEC (Firecode) } \\ & R=\text { RS-FEC }(528,514) \\ & P=\text { RS-FEC }(544,514) \end{aligned}$ |

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Table 40: Interface Modes of Operation

| Mode | Description | PCS | FEC | PMA | Autoneg | Training | Line I/O | Multi-speed AP Autoneg Resolution |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P1X | 1000BASE-X | $\begin{aligned} & \text { 1000BASE-X (CL } \\ & 36) \end{aligned}$ | None | Clause 36 | $\begin{aligned} & \text { Clause } \\ & 37 / 73 \end{aligned}$ | None | N/A | Y |
| P1S | SGMII (System) | 1000BASE-X (SGMII) | None | Clause 36 | SGMII | None | N/A |  |
| P1P | SGMII (PHY) | 1000BASE-X (SGMII) | None | Clause 36 | SGMII | None | N/A |  |
| P2.5X | 2.5GBASE-X | $\begin{aligned} & \text { 2.5GBASE-X (* CL } \\ & 36 \text { ) } \end{aligned}$ | None | Clause $36{ }^{1}$ | Clause $73^{2}$ | None | CU4HDD ${ }^{1}$ | Y |
| P5L | 5GBASE-R | $\begin{aligned} & \text { 5GBASE-R (* CL } \\ & \text { 49) } \end{aligned}$ | None | Clause $51{ }^{1}$ | Clause $73^{2}$ | None | CU4HDD ${ }^{1}$ | Y |
| P10LN | 10GBASE-LR/SR | $\begin{aligned} & \text { 10GBASE-R (CL } \\ & \text { 49) } \end{aligned}$ | None | Clause 51 | None | None | SFI/SFP+ |  |
| P10KN | 10GBASE-KR (No FEC) | $\begin{aligned} & \text { 10GBASE-R (CL } \\ & \text { 49) } \end{aligned}$ | None | Clause 51 | Clause 73 | CL 72.6.10 | KR (CL 72) | Y |
| P10KF | $\begin{aligned} & \text { 10GBASE-KR } \\ & \text { (FEC) } \end{aligned}$ | $\begin{aligned} & \text { 10GBASE-R (CL } \\ & \text { 49) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 51 | Clause 73 | CL 72.6.10 | KR (CL 72) | Y |
| P10LF | 10G <br> (Non-standard) | $\begin{aligned} & \text { 10GBASE-R (CL } \\ & \text { 49) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 51 | None | None | SFI/SFP+ |  |
| P25LN | 25G (Non-standard) <br> (No FEC) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | None | Clause 109 | None | None | 25GAUI <br> (109A, 109B) |  |
| P25LF | 25G (Non-standard) <br> (KR-FEC) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 109 | None | None | $\begin{aligned} & \text { 25GAUI } \\ & \text { (109A, 109B) } \end{aligned}$ |  |
| P25LR | 25GBASE-SR | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & \text { 108) } \end{aligned}$ | Clause 109 | None | None | 25GAUI <br> (109A, 109B) |  |
| P25CN | 25GBASE-CR <br> (No FEC) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | None | Clause 109 | Clause 73 | CL 72.6.10 | CR (CL 110) | Y |
| P25CF | 25GBASE-CR <br> (KR-FEC) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\mathrm{KR}(\mathrm{CL}$ <br> 74) | Clause 109 | Clause 73 | CL 72.6.10 | CR (CL 110) | Y |
| P25CR | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (RS-FEC) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & \text { 108) } \end{aligned}$ | Clause 109 | Clause 73 | CL 72.6.10 | CR (CL 110) | Y |
| P25KN | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (No FEC) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | None | Clause 109 | Clause 73 | CL 72.6.10 | KR (CL 111) | Y |
| P25KF | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (KR-FEC) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { KR (CL } \\ & 74) \end{aligned}$ | Clause 109 | Clause 73 | CL 72.6.10 | KR (CL 111) | Y |
| P25KR | 25GBASE-KR (RS-FEC) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & \text { 108) } \end{aligned}$ | Clause 109 | Clause 73 | CL 72.6.10 | KR (CL 111) | Y |
| P25BN | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (No FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | None | Clause 109 | Con OUI | CL 72.6.10 | CR (CL 110) | Y |
| P25BF | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (KR-FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 109 | Con OUI | CL 72.6.10 | CR (CL 110) | Y |
| P25BR | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (RS-FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & 108) \end{aligned}$ | Clause 109 | Con OUI | CL 72.6.10 | CR (CL 110) | Y |

Table 40: Interface Modes of Operation (Continued)

| Mode | Description | PCS | FEC | PMA | Autoneg | Training | Line I/O | Multi-speed AP Autoneg Resolution |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P25JN | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (No FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | None | Clause 109 | Con OUI | CL 72.6.10 | KR (CL 111) | Y |
| P25JF | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (KR-FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | KR (CL <br> 74) | Clause 109 | Con OUI | CL 72.6.10 | KR (CL 111) | Y |
| P25JR | 25GBASE-KR <br> (RS-FEC) <br> (Consortium) | $\begin{aligned} & \text { 25GBASE-R (CL } \\ & \text { 107) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & \text { 108) } \end{aligned}$ | Clause 109 | Con OUI | CL 72.6.10 | KR (CL 111) | Y |
| P40LN | 40GBASE-LR4/SR4 | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | None | None | XLAUI (CL <br> 83A, 83B) |  |
| P40CN | 40GBASE-CR4 (No FEC) | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | Clause 73 | CL 72.6.10 | CR4 (CL 85) | Y |
| P40CF | 40GBASE-CR4 (FEC) | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 83 | Clause 73 | CL 72.6.10 | CR4 (CL 85) | Y |
| P40KN | 40GBASE-KR4 (No FEC) | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | Clause 73 | CL 72.6.10 | KR4 (CL 84) | Y |
| P40KF | 40GBASE-KR4 (FEC) | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \text { KR (CL } \\ & 74) \end{aligned}$ | Clause 83 | Clause 73 | CL 72.6.10 | KR4 (CL 84) | Y |
| P40LF | 40G <br> (Non-standard) | $\begin{aligned} & \text { 40GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 83 | None | None | $\begin{aligned} & \text { XLAUI (CL } \\ & \text { 83A, 83B) } \end{aligned}$ |  |
| P50LN | 50GBASE-LR4/SR4 | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | None | None | XLAUI (CL 83A, 83B) |  |
| P50CN | 50GBASE-CR4 (No FEC) | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | Clause $73^{4}$ | CL 72.6.10 | CR4 (CL 85) |  |
| P50CF | 50GBASE-CR4 (FEC) | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 83 | Clause $73^{4}$ | CL 72.6.10 | CR4 (CL 85) |  |
| P50KN | 50GBASE-KR4 (No FEC) | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | None | Clause 83 | Clause $73^{4}$ | CL 72.6.10 | KR4 (CL 84) |  |
| P50KF | 50GBASE-KR4 (FEC) | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | Clause 83 | Clause $73^{4}$ | CL 72.6.10 | KR4 (CL 84) |  |
| P50LF | 50G <br> (Non-standard) | $\begin{aligned} & \text { 50GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | KR (CL <br> 74) | Clause 83 | None | None | $\begin{aligned} & \text { XLAUI (CL } \\ & \text { 83A, 83B) } \end{aligned}$ |  |
| P50MN | 50G <br> (Non-standard) <br> (No FEC) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | None | 4:2 (CL 83) | None | None | $\begin{aligned} & 2 \text { lane (CL } \\ & 83 \mathrm{~A}, 83 \mathrm{~B}) \end{aligned}$ |  |
| P50MF | 50G <br> (Non-standard) (KR-FEC) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \mathrm{KR}(\mathrm{CL} \\ & 74) \end{aligned}$ | 4:2 (CL 83) | None | None | $\begin{aligned} & 2 \text { lane (CL } \\ & \text { 83A, 83B) } \end{aligned}$ |  |
| P50MR | 50G <br> (Non-standard) (RS-FEC) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | RS (Con) | 4:2 (CL 83) | None | None | $\begin{aligned} & 2 \text { lane (CL } \\ & 83 A, 83 B) \end{aligned}$ |  |
| P50BN | 50GBASE-CR2 <br> (No FEC) <br> (Consortium) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | None | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane CR (CL } \\ & 85) \end{aligned}$ | Y |
| P50BF | $\begin{aligned} & \text { 50GBASE-CR2 } \\ & \text { (KR-FEC) } \\ & \text { (Consortium) } \end{aligned}$ | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | KR (CL <br> 74) | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane CR (CL } \\ & 85) \end{aligned}$ | Y |

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Table 40: Interface Modes of Operation (Continued)

| Mode | Description | PCS | FEC | PMA | Autoneg | Training | Line I/O | Multi-speed AP Autoneg Resolution |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P50BR | 50GBASE-CR2 (RS-FEC) (Consortium) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | RS (Con) | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane CR (CL } \\ & \text { 85) } \end{aligned}$ | Y |
| P50JN | 50GBASE-KR2 (No FEC) (Consortium) | 50GBASE-R2 (CL <br> 82) | None | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane KR (CL } \\ & \text { 84) } \end{aligned}$ | Y |
| P50JF | 50GBASE-KR2 (KR-FEC) (Consortium) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \text { KR (CL } \\ & 74) \end{aligned}$ | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane KR (CL } \\ & 84) \end{aligned}$ | Y |
| P50JR | 50GBASE-KR2 (RS-FEC) (Consortium) | $\begin{aligned} & \text { 50GBASE-R2 (CL } \\ & \text { 82) } \end{aligned}$ | RS (Con) | 4:2 (CL 83) | Con OUI | CL 72.6.10 | $\begin{aligned} & 2 \text { lane KR (CL } \\ & \text { 84) } \end{aligned}$ | Y |
| P100LN | 100GBASE-LR4 | 100GBASE-R4 (CL | None | Clause 83 | None | None | $\begin{aligned} & \text { CAUI-4 (CL } \\ & \text { 83D, 83E) } \end{aligned}$ |  |
| P100LR | 100GBASE-SR4 | $\begin{aligned} & \text { 100GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & 91) \end{aligned}$ | Clause 83 | None | None | $\begin{aligned} & \text { CAUI-4 (CL } \\ & \text { 83D, 83E) } \end{aligned}$ |  |
| $\begin{aligned} & \text { P100C } \\ & \text { R } \end{aligned}$ | 100GBASE-CR4 | $\begin{aligned} & \text { 100GBASE-R4 (CL } \\ & \text { 82) } \end{aligned}$ | $\begin{aligned} & \text { RS (CL } \\ & \text { 91) } \end{aligned}$ | Clause 83 | Clause 73 | CL 72.6.10 | CR4 (CL 92) | Y |
| $\begin{aligned} & \text { P100K } \\ & \text { R } \end{aligned}$ | 100GBASE-KR4 | 100GBASE-R4 (CL 82) | $\begin{aligned} & \text { RS (CL } \\ & \text { 91) } \end{aligned}$ | Clause 83 | Clause 73 | CL 72.6.10 | KR4 (CL 92) | Y |
| $\begin{aligned} & \text { P100K } \end{aligned}$ | $\begin{aligned} & \text { 100G } \\ & \text { (Non-standard) } \end{aligned}$ | ```100GBASE-R4 (CL 82)``` | None | Clause 83 | Clause $73{ }^{3}$ | CL 72.6.10 | KR4 (CL 92) |  |
| R1 | 1G - Transparent | 1G - Retimer | None | None | None | None | N/A |  |
| R2.5 | 2.5G - Transparent | 2.5G - Retimer | None | None | Clause $73^{2}$ | None | CU4HDD ${ }^{1}$ |  |
| R5 | 5G - Transparent, (No Training) | 5G - Retimer | None | None | Clause $73^{2}$ | None | CU4HDD ${ }^{1}$ |  |
| R10L | 10G - Transparent, (No Training) | 10G - Retimer | None | None | None | None | SFI/SFP+ |  |
| R10K | 10G - Transparent, (KR Training) | 10G - Retimer | None | None | Clause 73 | CL 72.6.10 | KR (CL 72) |  |
| R25L | 25G - Transparent, (No Training) | 25G - Retimer | None | None | None | None | $\begin{aligned} & \text { 25GAUI } \\ & (109 \mathrm{~A}, 109 \mathrm{~B}) \end{aligned}$ |  |
| R25C | 25G - Transparent, (CR Training) | 25G - Retimer | None | None | Clause 73 | CL 72.6.10 | CR4 (CL 110) |  |
| R25K | 25G - Transparent, (KR Training) | 25G - Retimer | None | None | Clause 73 | CL 72.6.10 | KR4 (CL 111) |  |
| R40L | 40G - Transparent, (No Training) | 40G - Retimer | None | None | None | None | XLAUI (CL 83A, 83B) |  |
| R40C | 40G - Transparent, (CR Training) | 40G - Retimer | None | None | Clause 73 | CL 72.6.10 | CR4 (CL 85) |  |
| R40K | 40G - Transparent, (KR Training) | 40G - Retimer | None | None | Clause 73 | CL 72.6.10 | KR4 (CL 84) |  |
| R100L | 100G - Transparent, (No Training) | 100G - Retimer | None | None | None | None | $\begin{aligned} & \text { CAUI-4 (CL } \\ & \text { 83D, 83E) } \end{aligned}$ |  |
| R100C | 100G - Transparent, (CR Training) | 100G - Retimer | None | None | Clause 73 | CL 72.6.10 | CR4 (CL 92) |  |
| R100K | 100G - Transparent, (KR Training) | 100G - Retimer | None | None | Clause 73 | CL 72.6.10 | KR4 (CL 92) |  |



- 2.5 G and 5 G mode currently being defined in IEEE 802.3 CU4HDD study group.
- Clause 73 Auto-Negotiation can be turned on or off. Bits being defined by CU4HDD.
Note
- The P100KN mode is non-standard but requires Auto-Negotiation to be on to start training. The 100GBASE-CR4 bit will be used.
- 50GBASE-R4 uses 40GBASE-R4 Auto-Negotiation ability bits to negotiate. This is a custom mode where both link partners know a-priori to negotiate to 50G
- R400Q uses AN based on Clause 73, with use of allocated next page field for CR-8 and Clause 136 start up protocol for pre-coder/training options.

Table 41: Register Control to Select Mode of Operation

| TBD | Reimport | 3.F00n.2:0 ${ }^{1}$ | 3.F00n. 4 | 3.F00n. 5 | 3.F00n.7:6 | 3.F00n.9:8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P1X | 1000BASE-X | 000 | 0 | 1 | 00 | 00 |
| P1S | SGMII (System) | 000 | 0 | 1 | 00 | 11 |
| P1P | SGMII (PHY) | 000 | 0 | 1 | 00 | 10 |
| P2.5X | 2.5GBASE-X | 001 | 0 | 1 | 00 | $x x^{2}$ |
| P5L | 5GBASE-R | 010 | 0 or 1 | 1 | 00 | XX |
| P10LN | 10GBASE-LR/SR | 011 | 0 | 1 | 00 | XX |
| P10KN | 10GBASE-KR <br> (No FEC) | 011 | 1 | 1 | 00 | XX |
| P10KF | 10GBASE-KR (FEC) | 011 | 1 | 1 | 01 | XX |
| P10LF | $\begin{aligned} & \text { 10G } \\ & \text { (Non-standard) } \end{aligned}$ | 011 | 0 | 1 | 01 | XX |
| P25LN | $\begin{aligned} & \text { 25G } \\ & \text { (Non-standard) (No FEC) } \end{aligned}$ | 100 | 0 | 1 | 00 | XX |
| P25LF | $\begin{aligned} & \text { 25G } \\ & \text { (Non-standard) (KR-FEC) } \end{aligned}$ | 100 | 0 | 1 | 01 | XX |
| P25LR | 25GBASE-SR | 100 | 0 | 1 | 10 | XX |
| P25CN | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (No FEC) } \end{aligned}$ | 100 | 1 | 1 | 00 | 00 |
| P25CF | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (KR-FEC) } \end{aligned}$ | 100 | 1 | 1 | 01 | 00 |
| P25CR | $\begin{aligned} & \text { 25GBASE-CR } \\ & \text { (RS-FEC) } \end{aligned}$ | 100 | 1 | 1 | 10 | 00 |
| P25KN | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (No FEC) } \end{aligned}$ | 100 | 1 | 1 | 00 | 01 |
| P25KF | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (KR-FEC) } \end{aligned}$ | 100 | 1 | 1 | 01 | 01 |

Table 41: Register Control to Select Mode of Operation (Continued)

| TBD | Reimport | 3.F00n.2:01 | 3.F00n. 4 | 3.F00n. 5 | 3.F00n.7:6 | 3.F00n.9:8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P25KR | $\begin{aligned} & \text { 25GBASE-KR } \\ & \text { (RS-FEC) } \end{aligned}$ | 100 | 1 | 1 | 10 | 01 |
| P25BN | 25GBASE-CR <br> (No FEC) (Consortium) | 100 | 1 | 1 | 00 | 10 |
| P25BF | 25GBASE-CR <br> (KR-FEC) (Consortium) | 100 | 1 | 1 | 01 | 10 |
| P25BR | 25GBASE-CR <br> (RS-FEC) (Consortium) | 100 | 1 | 1 | 10 | 10 |
| P25JN | 25GBASE-KR <br> (No FEC) (Consortium) | 100 | 1 | 1 | 00 | 11 |
| P25JF | 25GBASE-KR <br> (KR-FEC) (Consortium) | 100 | 1 | 1 | 01 | 11 |
| P25JR | 25GBASE-KR <br> (RS-FEC) (Consortium) | 100 | 1 | 1 | 10 | 11 |
| P40LN | 40GBASE-LR4/SR4 | 101 | 0 | 1 | 00 | OX |
| P40CN | 40GBASE-CR4 <br> (No FEC) | 101 | 1 | 1 | 00 | 00 |
| P40CF | $\begin{aligned} & \text { 40GBASE-CR4 } \\ & \text { (FEC) } \end{aligned}$ | 101 | 1 | 1 | 01 | 00 |
| P40KN | 40GBASE-KR4 <br> (No FEC) | 101 | 1 | 1 | 00 | 01 |
| P40KF | 40GBASE-KR4 (FEC) | 101 | 1 | 1 | 01 | 01 |
| P40LF | 40G <br> (Non-standard) | 101 | 0 | 1 | 01 | 0X |
| P50LN | 50GBASE-LR4/SR4 | 110 | 0 | 1 | 00 | 0X |
| P50CN | $\begin{aligned} & \text { 50GBASE-CR4 } \\ & \text { (No FEC) } \end{aligned}$ | 110 | 1 | 1 | 00 | 00 |
| P50CF | $\begin{aligned} & \text { 50GBASE-CR4 } \\ & \text { (FEC) } \end{aligned}$ | 110 | 1 | 1 | 01 | 00 |
| P50KN | 50GBASE-KR4 <br> (No FEC) | 110 | 1 | 1 | 00 | 01 |
| P50KF | 50GBASE-KR4 (FEC) | 110 | 1 | 1 | 01 | 01 |
| P50LF | 50G <br> (Non-standard) | 110 | 0 | 1 | 01 | 0X |
| P50MN | $\begin{aligned} & \text { 50G } \\ & \text { (Non-standard) (No FEC) } \end{aligned}$ | 110 | 0 | 1 | 00 | 1X |
| P50MF | $\begin{aligned} & \text { 50G } \\ & \text { (Non-standard) KR-FEC } \end{aligned}$ | 110 | 0 | 1 | 01 | 1X |

Table 41: Register Control to Select Mode of Operation (Continued)

| TBD | Reimport | 3.F00n.2:0 ${ }^{1}$ | 3.F00n. 4 | 3.F00n. 5 | 3.F00n.7:6 | 3.F00n.9:8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P50MR | $\begin{aligned} & \text { 50G } \\ & \text { (Non-standard) (RS-FEC) } \end{aligned}$ | 110 | 0 | 1 | 10 | 1X |
| P50BN | 50GBASE-CR2 <br> (No FEC) (Consortium) | 110 | 1 | 1 | 00 | 10 |
| P50BF | 50GBASE-CR2 <br> (KR-FEC) (Consortium) | 110 | 1 | 1 | 01 | 10 |
| P50BR | 50GBASE-CR2 <br> (RS-FEC) (Consortium) | 110 | 1 | 1 | 10 | 10 |
| P50JN | 50GBASE-KR2 <br> (No FEC) (Consortium) | 110 | 1 | 1 | 00 | 11 |
| P50JF | 50GBASE-KR2 <br> (KR-FEC) (Consortium) | 110 | 1 | 1 | 01 | 11 |
| P50JR | 50GBASE-KR2 <br> (RS-FEC) (Consortium) | 110 | 1 | 1 | 10 | 11 |
| P100LN | 100GBASE-LR4 | 111 | 0 | 1 | 00 | XX |
| P100LR | 100GBASE-SR4 | 111 | 0 | 1 | 10 | XX |
| P100CR | 100GBASE-CR4 | 111 | 1 | 1 | 10 | 00 |
| P100KR | 100GBASE-KR4 | 111 | 1 | 1 | 10 | 01 |
| P100KN | $\begin{aligned} & \text { 100G } \\ & \text { (Non-standard) } \end{aligned}$ | 111 | 1 | 1 | 00 | 00 |

1. 3.FOOn where $n$ is sub-port $n$.
2. Where $X$ means don't care.

Table 42: Base Link Register on PCS Modes

| $\mathbf{8 8 X 5 1 1 3}$ | Base Link Register (3.x for <br> Line Side, 4.x for Host Side) | Modes |
| :--- | :--- | :--- |
| 1G | 3001 | $\mathrm{P} 1^{*}$ |
| 2.5 G | 3001 | $\mathrm{P} 2 \mathrm{p} 5^{\star *}$ |
| 5 G | 2001 | $\mathrm{P} 5^{*}$ |
| 10G | 2001 | $\mathrm{P} 10^{* *}$ |
| $25 \mathrm{GR1}$ | 2001 | $\mathrm{P} 25 \mathrm{~B} / \mathrm{C} / \mathrm{J} / \mathrm{K} / \mathrm{L}^{*}$ |
| $25 \mathrm{GR2}$ | 1001 | $\mathrm{P} 25 \mathrm{Y} / \mathrm{Z}^{*}$ |
| 25 GR 4 | 1001 | $\mathrm{P} 25 \mathrm{~A} / \mathrm{G} / \mathrm{H}^{\star}$ |
| 40GR2 | 1001 | $\mathrm{P} 40 \mathrm{~B} / \mathrm{J}^{*}$ |
| 40GR4 | 1001 | $\mathrm{P} 40 \mathrm{C} / \mathrm{K} / \mathrm{L}^{*}$ |
| 50GR1 | 1001 | $\mathrm{P} 50 \mathrm{U} / \mathrm{Q}^{*}$ |
| 50GR2 | 1001 | $\mathrm{P} 50 \mathrm{~B} / \mathrm{J} / \mathrm{M}^{*}$ |

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Table 42: Base Link Register on PCS Modes (Continued)

| 88X5113 | Base Link Register (3.x for <br> Line Side, 4.x for Host Side) | Modes |
| :--- | :--- | :--- |
| 50GR4 | 1001 | $\mathrm{P} 50 \mathrm{C} / \mathrm{K} / L^{*}$ |
| 100GR2 | 1 | $\mathrm{P} 100 \mathrm{U} / \mathrm{Q}^{*}$ |
| 100GR4 | 1 | $\mathrm{P} 100 \mathrm{C} / \mathrm{K} / L^{*}$ |
| 200GR4 | 4001 | $\mathrm{P} 200^{* *}$ |
| NOTE: **The dsp lock for lane 0, 1, 2, and 3 are at registers 0xF201.5, 0xF221.5, 0xF241.5, and 0xF261. |  |  |

### 4.2 Electrical Interface

The input of the SERDES ( $R x$ ) is AC coupled on die while the output ( $T x$ ) is not AC coupled. All SERDES inputs and outputs are internally terminated by $50 \Omega$ each (or $100 \Omega$ differential).
The SERDES transmitter uses has a three-tap ( 1 pre-tap and 1 post-tap) FIR filter is implemented for the purpose of channel equalization. The FIR tap values are automatically adjusted during Clause 72 training or can be manually adjusted to optimize the transmit eye over a particular channel.

Table 40 Line I/O column lists out the supported electrical interfaces. Refer to the appropriate standards for detailed information.

### 4.3 PCS and PMA

The device supports many different modes of operation as shown in Table 40, all the PCS modes reduce down to four PCS types as shown in Table 43. There are four copies of each single-lane PCS types forming four sub-ports and one copy of each multi-lane PCS on sub-port 0 . The register location of each PCS type are summarized in the Equivalent Registers Between Line and Host Interface table in Section 5.

Table 43: PCS Types

| PCS Mode | PCS Type | Sub-Port 0 | Sub-Port 1 | Sub-Port 2 | Sub-Port 3 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1000BASE-X | 1000BASE-X | X | X | X | X |
| SGMII PHY |  |  |  |  |  |
| SGMII System |  |  |  |  |  |
| 2.5GBASE-X |  |  |  |  |  |
| 5GBASE-R | 10GBASE-R | X | X | X | X |
| 10GBASE-R |  |  |  |  |  |
| 25GBASE-R |  |  |  |  |  |
| 40GBASE-R4 | 40GBASE-R4 | X |  |  |  |
| 50GBASE-R4 |  |  |  |  |  |
| 50GBASE-R2 |  |  |  |  |  |
| 100GBASE-R4 | 100GBASE-R4 | X |  |  |  |

### 4.3.1 100GBASE-R4 PCS (Modes P100*)

The various 100GBASE-R4 PCS and PMA operate according to IEEE 802.3ba, 802.3bj, and 802.3bm specifications depending on the type selected. In general, a 64B/66B coding and scrambling is used to improve the transmission characteristics of the serial data and ease clock recovery at the receiver. The data stream is distributed across 20 virtual lanes. The alignment markers allows the lanes to be aligned and lanes to be reordered at the receiver. The Reed Solomon FEC reduces the bit error rate of the recovered data.
100GBASE-LR4 up to the CAUI-4 interface takes the path from the CGMII through the 20:4 bit multiplexer to the serializer on the egress direction. It takes the path from the de-serializer though the $4: 20$ de-multiplexer to the CGMII in the ingress direction. The Reed Solomon FEC is not used and there is no training of the transmitter FIR coefficients.

100GBASE-SR4 up to the CAUI-4 interface takes the path from the CGMII through the transcoder through the Reed Solomon encoder through the symbol distribution to the serializer on the egress direction. The alignment marker is remapped and sent to the Reed Solomon encoder. The receive path starts from the de-serializer through the alignment/de-skew/reorder though the Reed Solomon to the CGMII in the ingress direction. There is no training of the transmitter FIR coefficients. The Reed Solomon uses the RS $(528,514)$ code.
100GBASE-CR4 (to the CR4 PMD) path is identical to 100GBASE-SR4 except IEEE 802.3 Clause 72.6.10 training occurs to set the transmitter FIR coefficients and the receiver equalization is tuned for shielded balanced copper cabling.
100GBASE-KR4 path is identical to 100GBASE-CR4 except the transmitter FIR and the receiver equalization is tuned for KR4 electrical backplanes.

RS $(528,514)$. In modes where the Reed Solomon FEC is active, the behavior of the FEC can be modified by setting register 1.00C8.1:0.

- $00=$ Full error detection and correction, set $1.00 \mathrm{C} 8=16$ 'h0000.
- 01 = Error detection without correction. Blocks with errors will be intentionally corrupted to prevent uncorrectable errors from propagating, set $1.00 \mathrm{C} 8=16$ 'h0001.
- $10=$ Error detection without correction. Blocks with errors will be passed as received.
- The detected error will be reported in registers 1.00 CC and 1.00 CD .

Each of the bit settings requires a software reset to take effect.
P100KN is a non-standard mode that operates similarly to 100GBASE-LR4 without FEC, but IEEE 802.3 Clause 72.6.10 training occurs. When in this mode, the 100GBASE-CR4 Auto-Negotiation ability is set to initiate the training.

Figure 23: 100GBASE-R4 Data Path


### 4.3.2 40GBASE-R4, 50GBASE-R4, 50GBASE-R2 PCS (Modes P40*, P50*)

The 40GBASE-R4 PCS operates according to the IEEE 802.3ba specification. The PCS uses a 64B/66B coding and scrambling to improve the transmission characteristics of the serial data and ease clock recovery at the receiver. The data stream is distributed across 4 lanes. The alignment markers allow the lanes to be aligned and lanes to be swapped at the receiver. The synchronization headers for 64B/66B code enable the receiver to achieve block alignment on the receive data.
The 40GBASE-R4 datapath is shown in Figure 24. The Reed-Solomon encoder/FEC path and 4:2 Mux/2:4 De-Mux paths are bypassed in the 40GBASE-R4 and 50GBASE-R4. The differences among the various types are described below.
40GBASE-LR4 up to the XLAUI-4 interface has no training of the transmitter FIR coefficients.
40GBASE-CR4 uses IEEE 802.3 Clause 72.6 .10 training to set the transmitter FIR coefficients. The receiver equalization is tuned for shielded balanced copper cabling. The optional Clause 74 KR-FEC can be enabled or disabled.

40GBASE-KR4 path is identical to 40GBASE-CR4 except the transmitter FIR and the receiver equalization is tuned for KR4 electrical backplanes. The optional Clause 74 KR-FEC can be enabled or disabled.

P40LF is a non-standard mode that operates similarly to 40GBASE-LR4 with the KR-FEC enabled. IEEE 802.3 Clause 72.6.10 training does not takes place.
P50L* ${ }^{\text {P50C*}}$, P50K* modes are identical to each corresponding P40* modes except the line rate is 1.25 times faster.

The 50GBASE-R2 datapath is shown in Figure 24. The path either goes through the Reed-Solomon encoder/FEC path or the 4:2 Mux/2:4 De-Mux paths.

50GBASE-CR2 without FEC and with KR-FEC is similar to 40GBASE-CR4 except the data rate is 1.25 time faster and 4 virtual lanes are bit interleaved onto 2 lanes. This mode uses IEEE 802.3 Clause 72.6.10 training to set the transmitter FIR coefficients. The receiver equalization is tuned for shielded balanced copper cabling.
50GBASE-CR2 with RS-FEC is similar to 40GBASE-CR4 except the data rate is 1.25 times faster and 4 virtual lanes are transcoded and put through the Reed-Solomon encoder. The Reed-Solomon symbols are symbol interleaved onto two lanes. This mode uses IEEE 802.3 Clause 72.6.10 training to set the transmitter FIR coefficients. The receiver equalization is tuned for shielded balanced copper cabling.

50GBASE-KR2 path is identical to 50GBASE-CR2 except the transmitter FIR and the receiver equalization is tuned for KR electrical backplanes.

P50M* modes are identical to each corresponding P50B* modes except IEEE 802.3 Clause 72.6.10 training is not used.

Figure 24: 40GBASE-R4, 50GBASE-R4, and 50GBASE-R2 Datapath


### 4.3.3 5GBASE-R, 10GBASE-R, and 25GBASE-R PCS (Modes P5L, P10*, P25*)

The 10GBASE-R PCS operates according to the IEEE 802.3 Clause 49 specification. The 25GBASE-R PCS operates according to the IEEE 802.3by specification. The PCS uses a 64B/66B coding and scrambling to improve the transmission characteristics of the serial data and ease clock recovery at the receiver.

The 5GBASE-R, 10GBASE-R, and 25GBASE-R datapath is shown in Figure 25.
10GBASE-SR/LR has no training of the transmitter FIR coefficients.
10GBASE-KR uses IEEE 802.3 Clause 72.6.10 training to set the transmitter FIR coefficients. The receiver equalization is tuned for either shielded balanced copper cabling or KR electrical backplanes. The optional Clause 74 KR-FEC can be enabled or disabled.

P10LF is a non-standard mode that operates similarly to 10GBASE-LR with the KR-FEC enabled. IEEE 802.3 Clause 72.6.10 training does not occur.

5GBASE-R is identical to 10GBASE-SR/LR running at half speed.
25GBASE-SR uses the Clause 108 RS-FEC but has no training of the transmitter FIR coefficients.
25GBASE-CR is similar to 25GBASE-SR except it uses IEEE 802.3 Clause 72.6 .10 training to set the transmitter FIR coefficients. The receiver equalization is tuned for shielded balanced copper cabling. The optional Clause 74 KR-FEC can be enabled or disabled. The optional Clause 108 RS-FEC can be enabled or disabled.

25GBASE-KR path is identical to 25GBASE-CR except the transmitter FIR and the receiver equalization is tuned for KR electrical backplanes. The optional Clause 74 KR-FEC can be enabled or disabled. The optional Clause 108 RS-FEC can be enabled or disabled.

P25B* modes are identical to each corresponding P25C* modes except the Auto-Negotiation used is per the Consortium specification.
P25J* modes are identical to each corresponding P25K* modes except the Auto-Negotiation used is per the Consortium specification.

P25LN is identical to 10GBASE-SR/LR except running 2.5 times faster.
P25LF is identical to P10LF except running 2.5 times faster.

Figure 25: 5GBASE-R, 10GBASE-R, and 25GBASE-R Datapath


### 4.3.4 SGMII, 1000BASE-X, and 2.5GBASE-X

### 4.3.4.1 PCS

The 1000BASE-X PCS operates according to Clause 36 of the IEEE 802.3 specification. The PCS uses a $8 / 10$ bit coding for $D C$ line balancing. For further details, refer to the IEEE 802.3 specification.

The SGMII protocol is also supported over 1000BASE-X. The SGMII allows $10 \mathrm{Mbps}, 100 \mathrm{Mbps}$, and 1000 Mbps throughput over 1000BASE-X line coding.
When SGMII Auto-Negotiation is turned off $(3.3 \mathrm{n} 00.12=0)$, the speed setting is programmed via register $3.3 n 00$ bits 13 and 6 . ( $n=0,2,4,6$ for sub-ports $0,1,2$, and 3 , respectively). Link is established when the underlying 1000BASE-X establishes link.
When SGMII Auto-Negotiation is turned on (3.3n00.12 = 1) , the SGMII is set to the speed setting is determined by the Auto-Negotiation speed advertised by the link partner if the device is in SGMII (System) mode. Auto-Negotiations have to complete prior to link being established.
2.500BASE-X is identical to 1000GBASE-X operation as described except it runs 2.5 times faster. Clause 37 Auto-Negotiation is not supported in 2.500BASE-X.

### 4.3.4.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE 802.3 specification. It is used to auto-negotiate duplex and flow control over fiber cable. Registers 3.3n00, 3.3n04, 3.3n05, 3.3n06, $3.3 n 07,3.3 n 08$, and $3.3 n 0 F$ are used to enable AN, advertise capabilities, determine the link partner's capabilities, show AN status, and show the duplex mode of operation, respectively.

The device supports Next Page option for 1000BASE-X Auto-Negotiation. Register $3.3 n 07$ of the fiber pages is used to transmit Next Pages, and register 3.3n08 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set register 3.3n04.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in register 3.3n07.

If the PHY enables 1000BASE-X Auto-Negotiation and the link partner does not, then the link cannot be established. The device implements an Auto-Negotiation bypass mode. See Section 4.3.4.4 for details.

### 4.3.4.3 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the Cisco SGMII Specification and the MAC Interfaces and Auto-Negotiation Application Note for further details.

The device supports SGMII interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register $3.3 n 00.12$ followed by a soft reset. If SGMII Auto-Negotiation is disabled, then the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other manner (for example, by reading PHY registers for link, speed, and duplex status).

### 4.3.4.4 Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the other does not implement the function, then two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Interface Auto-Negotiation Bypass Mode. When entering the state Ability_Detect, a bypass timer begins to count down from an initial value of approximately 200 ms . If the device receives idles during the 200 ms , then the device will interpret that the other side is live, but cannot send configuration codes to perform Auto-Negotiation. After 200 ms , the state machine will move to a new state called Bypass_Link_Up in which the device assumes a link-up status and the operational mode is set to the value listed under the Comments column of Table 44.

Table 44: SGMII Auto-Negotiation Modes

| Register <br> 3.3n00.12 | Register <br> 3.Bn000.13 | Comments |
| :--- | :--- | :--- |
| 0 | X | No Auto-Negotiation. The user is responsible for determining the speed, <br> link, and duplex status by reading PHY registers. |
| 1 | 0 | Normal SGMII Auto-Negotiation. Speed, link, and duplex status are <br> automatically communicated to the MAC during Auto-Negotiation. |
| 1 | 1 | Media Auto-Negotiation is enabled. <br> Normal operation. |
|  | Media Auto-Negotiation is disabled. <br> After 200 ms, the PHY will disable Auto-Negotiation and the link based <br> on idles. |  |

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### 4.4 Auto-Negotiation

The device supports 802.3ap Clause 73 Auto-Negotiation as well as the next pages required for the $25 / 50 \mathrm{G}$ consortium specifications. When the Auto-Negotiation configuration bits are set correctly and Auto-Negotiation is enabled, no further user intervention is required for Auto-Negotiation to complete.

There are four copies of the Auto-Negotiation circuit on the line interface. Sub-port 0 supports all abilities shown in Table 40 with a $Y$ in the last column. Sub-ports 1, 2, and 3 is similar to sub-port 0 except 40G, 50G, and 100G modes are not supported.
The enabling and disabling of the Auto-Negotiation circuit for each sub-port is discussed in Section 4. If Auto-Negotiation is disabled and the device is manually set to a mode that KR training is required, then Auto-Negotiation will still run automatically. It is the user's responsibility to properly set the Auto-Negotiation registers to advertise only the capability that is consistent with the manually set mode.

The registers to control the 802.3ap Auto-Negotiation for sub-port 0 can be found starting at register 7.0000. The registers to control sub-port 0 consortium Auto-Negotiation can be found starting at register 7.8010. The registers for sub-port 1, 2, and 3 can be found in their corresponding offset addresses as mapped in the 88X5113 Registers documentation.

### 4.5 Loopback

### 4.5.1 Line-side Loopbacks

Figure 26 shows shallow line loopback (path A), deep loopbacks for line side. The deep loopback can be enabled at PCS to PMA boundary which is called PCS deep loopback (path B). The deep loopback can be at PMA to SERDES boundary so called PMA deep loopback (path C).
Table 45 shows how to turn on shallow line loopback. Table 46 shows how to turn on deep loopbacks for line side.

Figure 26: Line-side Loopback


Table 45: Shallow Line Loopback Control Bits

| Line Loopback Bits Description | Unit Affected | Register - Line |
| :--- | :--- | :--- |
| 1G/2.5G, 5G/10G/25G lane 0, 40G/50G, 100G | Lane 0 | Set 3.F010.12 = 1 (Loopback A in Figure 26) |
| 1G/2.5G, 5G/10G/25G lane 1 | Lane 1 | Set 3.F010.13 = 1 (Loopback A in Figure 26) |
| 1G/2.5G, 5G/10G/25G lane 2 | Lane 2 | Set 3.F010.14 = 1 (Loopback A in Figure 26) |
| 1G/2.5G, 5G/10G/25G lane 3 | Lane 3 | Set 3.F010.15 = 1 (Loopback A in Figure 26) |

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The couple modes such as 40G/50G-R4, 50G-R2, and 100G-R4 always use lane 0 .
Table 46: Deep Loopback Control Bits

| Deep Loopback Bits Description | Unit Affected | Register - Line <br> (PCS Deep Loopback) | Register - Line <br> (PMA Deep Loopback) |
| :---: | :---: | :---: | :---: |
| Deep loopback - 100G | Lane 0 | 3.0000.14 (Loopback E in Figure 27) | 1.0000 .0 (Loopback F in Figure 27) |
| Deep loopback 40G/50G | Lane 0 | 3.1000.14 (Loopback E in Figure 27) | 1.2000 .0 (Loopback F in Figure 27) |
| Deep loopback 5G/10G/25G | Lane 0 <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.2000 .14 \text { (Loopback E in Figure 27) } \\ & 3.2200 .14 \\ & 3.2400 .14 \\ & 3.2600 .11 \end{aligned}$ | 1.4000 .0 (Loopback F in Figure 27) |
| $\begin{aligned} & \text { Deep loopback - } \\ & \text { 1G/2.5G } \end{aligned}$ | Lane 0 <br> Lane 1 <br> Lane 2 <br> Lane 3 | $\begin{aligned} & 3.3000 .14 \\ & 3.3200 .14 \\ & 3.3400 .14 \text { (Loopback F in Figure 27) } \\ & 3.3600 .14 \end{aligned}$ | 1.6000 .0 (Loopback F in Figure 27) |

### 4.5.2 Host-side Loopbacks

Figure 27 shows the paths for shallow host loopback (D), PCS deep loopback (E), and PMA deep loopback ( $F$ ) for the host side.

Table 47 shows how to turn on a shallow host loopback. Table 48 shows how to turn on deep loopbacks for the host side.

Figure 27: Turn On Deep Host Loopback


Table 47: Shallow Line Loopback Control Bits

| Line Loopback Bits Description | Unit <br> Affected | Register - Line |
| :--- | :--- | :--- |
| 1G/2.5G, 5G/10G/25G lane 0, 40G/50G, 100G | Lane 0 | Set 4.F010.12 = 1 (Loopback D in Figure 27). |
| 1G/2.5G, 5G/10G/25G lane 1 | Lane 1 | Set 4.F010.13 = 1 (Loopback D in Figure 27). |
| 1G/2.5G, 5G/10G/25G lane 2 | Lane 2 | Set 4.F010.14 = 1 (Loopback D in Figure 27). |
| 1G/2.5G, 5G/10G/25G lane 3 | Lane 3 | Set 4.F010.15 = 1 (Loopback D in Figure 27). |

The couple modes such as 40G/50G-R4, 50G-R2, and 100G-R4 always use lane 0 .

Table 48: Deep Loopback Control Bits

| Deep Loopback Bits <br> Description | Unit <br> Affected | Register - Line <br> (PCS Deep Loopback) | Register - Line <br> (PMA Deep Loopback) |
| :--- | :--- | :--- | :--- |
| Deep loopback - 100G | Lane 0 | 4.0000 .14 (Loopback B in Figure 26) | 1.1000 .0 (Loopback C in Figure 26) |
| Deep loopback - 40G/50G | Lane 0 | 4.1000 .14 (Loopback B in Figure 26) | 1.3000 .0 (Loopback C in Figure 26) |
| Deep loopback - <br> 5G/10G/25G | Lane 0 | 4.2000 .14 | 1.5000 .0 (Loopback C in Figure 26) |
|  | Lane 1 | 4.2200 .14 |  |
|  | Lane 2 | 4.2400 .14 (Loopback B in Figure 26) |  |
| Lane 3 | 4.2600 .11 | 1.7000 .0 (Loopback C in Figure 26) |  |
|  | Lane 0 |  |  |
|  | Lane 1 | 4.3200 .14 |  |
|  | Lane 2 | 4.3400 .14 |  |
|  | 4.3600 .14 (Loopback B in Figure 26) |  |  |

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### 4.6 Synchronized FIFO

There is a transmit synchronizing FIFO in all PCS including 1G, 10G, 25G, 40G/50G, and 100G PCS. Each of the FIFOs reconciles the frequency differences between the internal bus clock and the clock used to transmit data onto the media interface. It also buffers the data when inserting Alignment Maker. Each of the FIFOs can support a maximum frame size of 10 KB with up to $\pm 100$ PPM clock jitter.

### 4.7 Traffic Generation and Checking

There are several packet generator and checkers in the device. There are 22 16-bit registers associated with each generator and checker. This section will refer to these registers as R00 to R21. The register mapping is shown in Table 49.

Table 49: Packet Generator and Checker Register Mapping ${ }^{1}$ Data

| Register | Description | P100* | $\begin{aligned} & \text { P40*, } \\ & \text { P50* } \end{aligned}$ | $\begin{aligned} & \text { P5* } \\ & \text { P10* } \\ & \text { P25* } \end{aligned}$ | $\begin{aligned} & \text { P1*, } \\ & \text { P2.5* } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R00 | Packet Generation Control 1 | 3.8100 | 3.9010 | 3.An10 | 3.Bn10 |
| R01 | Packet Generation Control 2 | 3.8101 | 3.9011 | 3.An11 | $3 . \mathrm{Bn} 11$ |
| R02 | Initial Payload 0-1/Packet Generation | 3.8102 | 3.9012 | 3.An12 | 3.Bn12 |
| R03 | Initial Payload 2-3/Packet Generation | 3.8103 | 3.9013 | 3.An13 | 3.Bn13 |
| R04 | Packet Generation Length | 3.8106 | 3.9016 | 3.An16 | 3.Bn16 |
| R05 | Packet Generation Burst Sequence | 3.8107 | 3.9017 | 3.An17 | 3.Bn17 |
| R06 | Packet Generation IPG | 3.8108 | 3.9018 | 3.An18 | 3.Bn18 |
| R07 | Transmit Packet Counter [15:0] | 3.810B | 3.901B | 3.An1B | 3.Bn1B |
| R08 | Transmit Packet Counter [31:16] | 3.810C | 3.901C | 3.An1C | 3.Bn1C |
| R09 | Transmit Packet Counter [47:32] | 3.810D | 3.901D | 3.An1D | 3.Bn1D |
| R10 | Transmit Byte Counter [15:0] | 3.810E | 3.901E | 3.An1E | 3.Bn1E |
| R11 | Transmit Byte Counter [31:16] | 3.810F | 3.901F | 3.An1F | 3.Bn1F |
| R12 | Transmit Byte Counter [47:32] | 3.8110 | 3.9020 | 3.An20 | 3.Bn20 |
| R13 | Receive Packet Counter [15:0] | 3.8111 | 3.9021 | 3.An21 | 3.Bn21 |
| R14 | Receive Packet Counter [31:16] | 3.8112 | 3.9022 | 3.An22 | 3.Bn22 |
| R15 | Receive Packet Counter [47:32] | 3.8113 | 3.9023 | 3.An23 | 3.Bn23 |
| R16 | Receive Byte Count [15:0] | 3.8114 | 3.9024 | 3.An24 | 3.Bn24 |
| R17 | Receive Byte Count [31:16] | 3.8115 | 3.9025 | 3.An25 | 3.Bn25 |
| R18 | Receive Byte Count [47:32] | 3.8116 | 3.9026 | $3 . A n 26$ | 3.Bn26 |
| R19 | Receive Packet Error Count [15:0] | 3.8117 | 3.9027 | 3.An27 | $3 . \mathrm{Bn} 27$ |

Table 49: Packet Generator and Checker Register Mapping ${ }^{1}$ Data (Continued)

| Register | Description | P100* | $\begin{aligned} & \text { P40*, } \\ & \text { P50* } \end{aligned}$ | P5*, <br> P10*, <br> P25* | $\begin{aligned} & \text { P1* } \\ & \text { P2.5* } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R20 | Receive Packet Error Count [31:16] | 3.8118 | 3.9028 | 3.An28 | 3.Bn28 |
| R21 | Receive Packet Error Count [47:32] | 3.8119 | 3.9029 | 3.An29 | 3.Bn29 |

1. $N=0,2,4,6$ for sub-ports $0,1,2$, and 3 , respectively.

The packet generator and packet checker are enabled by separate control bits - R00.0 controls the packet checker and R00.1 controls the packet generator. (Table 50).
When the packet Generator is enabled, packet stream is generated and a pair of 48 -bit counters tracks the packet stream. Transmit Packet Counter (R07, R08, and R09) counts number of packets sent. Transmit Byte Counter (R10, R11, and R12) counts number of bytes sent.
Similarly, when the packet checker is enabled, received packets are examined and a set of three 48-bit counters are updated. Received Packet Counter (R13, R14, and R15) counts number of packets received. Received Byte Counter (R16, R17, and R18) counts number of bytes received, and Received Error Counter (R19, R20, and R21) counts number of received packets with CRC error.

Table 50: Packet Generator and Checker Control and Counters

| Register | Function | Description |
| :---: | :---: | :---: |
| R00.0 | Enable Packet Checker | 1: Packet Checker is enabled. 0: Packet Checker is disabled. |
| R00.1 | Enable Packet Generator | 1: Packet Generator is enabled. 0 : Packet Generator is disabled. |
| R00.6 | Counter reset | 1: Clear counters. <br> 0 : Normal operation <br> This bit clears itself after counter reset. |
| R00.15 | Counter reset on read | 1: Clear the counter as it is read. <br> 0 : The counter value is not cleared when it is read. |
| $\begin{aligned} & \text { R07 } \\ & \text { R08 } \\ & \text { R09 } \end{aligned}$ | Transmit Packet Counter | These are the 48 -bit Tx packet counters, they are incremented as each packet is sent. <br> A reset of these counters is controlled by the Counter reset bit (R00.6) and the Counter reset on read bit (R00.15) above. |
| $\begin{aligned} & \text { R10 } \\ & \text { R11 } \\ & \text { R12 } \end{aligned}$ | Transmit Byte Counter | These are the 48 -bit Tx byte counters, they are incremented as each data byte is sent, including CRC bytes. <br> A reset of these counters is controlled by the Counter reset bit (R00.6) and the Counter reset on read bit (R00.15) above. |
| $\begin{aligned} & \text { R13 } \\ & \text { R14 } \\ & \text { R15 } \end{aligned}$ | Received Packet Counter | These are the 48 -bit Rx packet counters, they are incremented as each packet is received. <br> A reset of these counters is controlled by the Counter reset bit (R00.6) and the Counter reset on read bit (R00.15) above. |

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Table 50: Packet Generator and Checker Control and Counters (Continued)

| Register | Function | Description |
| :--- | :--- | :--- |
| R16 | Received Byte Counter | These are the 48-bit Rx byte counters, they are incremented as each data <br> R17 <br> R18 is received, including CRC bytes. <br> A reset of these counters is controlled by the Counter reset bit (R00.6) <br> and the Counter reset on read bit (R00.15) above. |
| R19 | Received Error Counter | These are the 48-bit Rx error counters, they are incremented as each <br> packet is received with a CRC error. <br> R20 |
| R21 |  | A reset of these counters is controlled by the Counter reset bit (R00.6) <br> and the Counter reset on read bit (R00.15) above. |

### 4.7.1 Packet Generator

A packet generator enables the device to generate traffic onto the media without a requirement to receive data from the host.

As a reference, the following depicts the basic structure of Packet Generator output in XLGMII (40G) and CGMII (100G) format.

Figure 28: Packet Format

| TXC[7:0] | TXD[63:0] | Bit 0 is first bit shifted out. Packet starts at CGMII boundary of 64 bit. |
| :---: | :---: | :---: |
| 01 | <sfd> 555555555555 [S] | Lane0 [S] = 0xFB. Lane7 <sfd> = 0xD5 |
| 00 | (data 7) - (data 0) |  |
| 00 | - • • • • - - | n bytes of data specified by Packet Length register |
| 00 | (data $\mathrm{n}-2) \bullet \bullet \bullet$ • • |  |
| E0 | [1] [1] [T] (crc[31:0]) (data n-1) | $[T]=0 \times F D \quad[1]=0 \times 07$ |

Table 51: Registers Controlling Packet Generation

| Register | Function | Description |
| :---: | :---: | :---: |
| R00.1 | Enable Packet Generator | 1: The packet generator is enabled. 0 : The packet generator is disabled. |
| $\begin{aligned} & \text { R01.3 } \\ & \text { R00.2 } \end{aligned}$ | CRC Disable <br> SFD Enable | \{CRC,SFD $\}=00$ : <br> CRC calculation is enabled and CGMII word 0 lane 7 <sfd> $=0 x D 5$. CRC calculation starts after <sfd> byte in packet |
|  |  | $\{C R C, S F D\}=01:$ <br> CRC calculation is enabled and CGMII word 0 lane 7 <preA> $=0 \times 55$. CRC calculation start after 8th byte in packet |
|  |  | $\{C R C, S F D\}=11$ : <br> Extended CRC calculation is enabled and CGMII word 0 lane 7 <preA> $=0 \times 55$. <br> Extended CRC calculation starts after [S] byte. <br> NOTE: Extended CRC function is only available in 40G and 100G modes. |
|  |  | $\{C R C, S F D\}=10:$ <br> CRC calculation is disabled and CGMII word 0 lane 7 <sfd> $=0 x D 5$. |
| R04 | Packet Length | 0x0000: Random length between 64 bytes to 1518 bytes 0x0001: Random length between 64 bytes to 0x0FFF bytes 0x0002: Random length between 64 bytes to 0x1FFF bytes 0x0003: Random length between 64 bytes to 0x3FFF bytes 0x0004: Random length between 64 bytes to 0x7FFF bytes 0x0005: Random length between 64 bytes to 0xFFFF bytes 0x0006-0x0007: undefined $0 \times 0008-0 \times F F F F=$ length in number of bytes. |
| R05 | Number of Packets to Generate | $0 \times 0000$ : Stop generation <br> $0 \times 0001$ - 0xFFFE: number of packets to send <br> 0xFFFF = Continuous |

Figure 29: Normal CRC Calculation (in XLGMII/40G and CGMII/100G Format)

| FB | 55 | 55 | 55 | 55 | 55 | 55 | D5 | Data - - Data n-1 | CRC |  |  |  | FD | 07 | 07 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| [S] | <====== SFD/PreAmble =====> |  |  |  |  |  |  | $<==========$ CRC calculation $=========>$ | 0 | 1 | 2 | 3 | [T] |  | IPG |

Figure 30: Extended CRC Calculation (in XLGMII/40G and CGMII/100G Format)


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Figure 31: Packet without CRC (in XLGMII/40G and CGMII/100G Format)

| FB | 55 | 55 | 55 | 55 | 55 | 55 | D5 | Data 0 • • - Data n-1 | FD | 07 | 07 | 07 | 07 | 07 | 07 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| [S] |  |  |  |  |  |  |  |  | [T] |  |  |  | IPG |  |  |

Table 52: IPG Configuration

| Register \# | Function | Description |
| :---: | :---: | :---: |
| R06 | Inter Packet Gap (IPG) | IPG.15:14 = 00: Fixed number of idle bytes is specified by IPG.13:0 <br> For P100*, P50* and P40* modes, IPG is in 8-byte resolution (1 CGMII word). <br> For example: <br> IPG. 13:0 $=0 \times 0000-0 \times 0007$ : Next packet starts at the following CGMII word (next 8byte boundary) <br> IPG.13:0 = 0x0008-0x000F: After the end of current packet 8-byte boundary, insert 1 CGMII (8 byte) idle before start of next packet. <br> IPG. 13:0 = 0x0010-0x00017: After the end of current packet 8-byte boundary, insert 2 CGMII (16 byte) idle before start of next packet. For 10G, the resolution is 4 bytes. |
|  |  | IPG.15:14 = 10: Random number of IPG up to the value specified by IPG.13:0 |
|  |  | IPG.15:14 = 01: Deficit Idle Count specified by IPG.13:0. Valid IPG.13:0 value is limited to minimum of 8 and maximum of 20. NOTE: Idle Deficit function only available in $40 \mathrm{G} / 50 \mathrm{G}$ and 100 G modes. |
|  |  | IPG. 15:14 = 11: Zero IPG. <br> 1 CGMII word ( 8 byte) of idle is inserted after $n$ bytes of data, $n$ is specified by IPG.13:0 as following: <br> IPG. 13:0 = 0x0080: $\mathrm{n}=128$ bytes <br> IPG. 13:0 = 0x0100: $\mathrm{n}=256$ bytes <br> IPG. 13:0 = 0x0200: $\mathrm{n}=512$ bytes <br> IPG. 13:0 = 0x0400: $\mathrm{n}=1024$ bytes <br> IPG. 13:0 $=0 \times 0800: \mathrm{n}=2048$ bytes <br> IPG. 13:0 $=0 \times 1000: \mathrm{n}=4096$ bytes <br> IPG. 13:0 = 0x2000: $\mathrm{n}=8196$ bytes <br> NOTE: Zero IPG function only available in 40G/50G and 100G modes. |
| $\begin{aligned} & \text { R07 } \\ & \text { R08 } \\ & \text { R09 } \end{aligned}$ | Transmit <br> Packet <br> Counter | These are the 48-bit Tx packet counters, they are incremented as each packet is sent. |
| $\begin{aligned} & \text { R10 } \\ & \text { R11 } \\ & \text { R12 } \end{aligned}$ | Transmit Byte Counter | These are the 48 -bit Tx byte counters, they are incremented as each data byte is sent, including 4 CRC bytes. |

Table 53: Packet Data Generation

| Register \# | Function | Description |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { R02 } \\ & \text { R03 } \end{aligned}$ | Initial Generation | Initial Payload register specifies the initial value of the payload or the fixed value of the payload. The four bytes in this register corresponds to the first 4 bytes of the frame data. |
| R01 | Data <br> Generation | $0 \times 0$ or $0 \times 1$ : No mask Value of Initial Payload registers are used as payload repeatedly. |
|  |  | $0 \times 2$ : Invert every other word Value of Initial Payload registers are used as payload repeatedly but every other CGMII word should be inverted. For example: A payload of 034EA675 will result in a sequence of 034EA675, FCB1598A, 034EA675, FCB1598A, and so on. |
|  |  | $0 \times 3$ : Invert every second word Value of Initial Payload registers are used as payload repeatedly but inverted every second CGMII word should be inverted. <br> For example: A payload of 034EA675 will result in a sequence of 034EA675, 034EA675, FCB1598A, FCB1598A, 034EA675, 034EA675, and so on. |
|  |  | $0 \times 4$ : Left shift byte <br> Value of Initial Payload registers are used as the initial value and each byte subsequently bitwise left shifted. <br> For example: A payload of 034EA675 will result in a sequence of 034EA675, 069C4DEA, 0C399AD5, 187235AB, and so on. |
|  |  | $0 \times 5$ : Right shift byte <br> Value of Initial Payload registers are used as the initial value and each byte subsequently bitwise right shifted. |
|  |  | 0x6: Left shift word <br> Value of Initial Payload registers are used as the initial value and each 32-bit word subsequently bitwise left shifted. For example: A payload of C34EA675 will result in a sequence of C34EA675, 869D4CEB, 0D3A99D7, 1A7533AE, and so on. |
|  |  | 0x7: Right shift word <br> Value of Initial Payload registers are used as the initial value and each 32-bit word subsequently bitwise right shifted. |
|  |  | 0x8: Increment byte <br> Value of Initial Payload registers are used as the initial value and subsequently bytewise incremented. For example: A payload of FFFE0055 will result in a sequence of FFFE0055, 00FF0156, 01000257, 02010358, and so on. |
|  |  | 0x9: Decrement byte <br> Value of Initial Payload registers are used as the initial value and subsequently bytewise decremented. |
|  |  | 0xA: Pseudo-random byte <br> Initial Payload registers are ignored and a pseudo-random payload is generated. All 4 bytes are the same value for each cycle. |
|  |  | 0xB: Pseudo-random word Initial Payload registers are ignored and a pseudo-random payload is generated. All 4 bytes are randomly generated for each cycle. |
|  |  | 0xC-0xF: Reserved |

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### 4.7.2 Packet Checker

## Table 54: Registers Controlling Packet Checker

| Register \# | Function | Description |
| :---: | :---: | :---: |
| R00.0 | Enable Packet Checker | 1: Packet Checker is enabled. 0 : Packet Checker is disabled. |
| R01.3 <br> R00.2 | CRC disable SFD enable | $\{C R C, S F D\}=00$ : <br> CRC calculation is enabled and started after detection of frame delimiter <sfd> |
|  |  | \{CRC,SFD $\}=01$ : <br> CRC calculation is enabled and started after eight byte of the packet. <br> The checker assumes the first 8 bytes of packet is the preamble. |
|  |  | $\{C R C, S F D\}=11$ : <br> Extended CRC calculation is enabled and started after second byte of the packet. <br> NOTE: Extended CRC function only available in 40G and 100G modes. |
|  |  | $\{C R C, S F D\}=10:$ <br> CRC calculation is disabled and data field starts after detection of frame delimited <sfd> |
| $\begin{aligned} & \text { R13 } \\ & \text { R14 } \\ & \text { R15 } \end{aligned}$ | Received Packet Counter | These are 48-bit Rx packet counters, they are incremented as each packet is received. |
| $\begin{aligned} & \text { R16 } \\ & \text { R17 } \\ & \text { R18 } \end{aligned}$ | Received Byte Counter | These are 48-bit Rx byte counters, they are incremented as each data byte is received, including 4 CRC bytes. |
| $\begin{aligned} & \text { R19 } \\ & \text { R20 } \\ & \text { R21 } \end{aligned}$ | Received Error Counter | These are 48-bit Rx error counters, they are incremented as each packet is received with a CRC error. |

### 4.8 PRBS Generation and Checking

The device supports various IEEE defined and proprietary PRBS generators and checkers, and transmit waveform pattern generators. Only one generator and checker may be enabled at a time per lane. Unpredictable results may occur if multiple generators are enabled simultaneously.

### 4.8.1 General PRBS Generators and Checkers

Each lane has its own general PRBS generator and checker. The register definitions for all PRBSs are same except for register offsets. Table 55 shows all PRBS register address offsets. Lane 0 PRBS register address will be used to describe the functionality of PRBS generator and checkers.

To maintain consistency, the address offsets for the host side are listed here.

Table 55: PRBS Register Address Offsets

| Register | Description | Line Side |  |  |  | Host Side |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Lo | L1 | L2 | L3 | Lo | L1 | L2 | L3 |
| R0 | PRBS control | 3.F100 | 3.F110 | 3.F120 | 3.F130 | 4.F100 | 4.F110 | 4.F120 | 4.F130 |
| $\begin{aligned} & \text { R1 } \\ & \text { R2 } \\ & \text { R3 } \end{aligned}$ | Transmit bit counter | $\begin{aligned} & \text { 3.F101 } \\ & \text { 3.F102 } \\ & \text { 3.F103 } \end{aligned}$ | $3 . F 111$ 3.F112 3.F113 | $\begin{aligned} & \text { 3.F121 } \\ & \text { 3.F122 } \\ & \text { 3.F123 } \end{aligned}$ | $\begin{aligned} & \text { 3.F131 } \\ & \text { 3.F132 } \\ & \text { 3.F133 } \end{aligned}$ | $\begin{aligned} & \text { 4.F101 } \\ & \text { 4.F102 } \\ & \text { 4.F103 } \end{aligned}$ | 4.F111 <br> 4.F112 <br> 4.F113 | 4.F121 4.F122 <br> 4.F123 | $\begin{aligned} & \text { 4.F131 } \\ & \text { 4.F132 } \\ & \text { 4.F133 } \end{aligned}$ |
| $\begin{aligned} & \text { R4 } \\ & \text { R5 } \\ & \text { R6 } \end{aligned}$ | Receive bit counter | $\begin{aligned} & \text { 3.F104 } \\ & \text { 3.F105 } \\ & \text { 3.F106 } \end{aligned}$ | $\begin{aligned} & \text { 3.F114 } \\ & \text { 3.F115 } \\ & \text { 3.F116 } \end{aligned}$ | $\begin{aligned} & \text { 3.F124 } \\ & \text { 3.F125 } \\ & \text { 3.F126 } \end{aligned}$ | $\begin{aligned} & \text { 3.F134 } \\ & \text { 3.F135 } \\ & \text { 3.F136 } \end{aligned}$ | $\begin{aligned} & \text { 4.F104 } \\ & \text { 4.F105 } \\ & \text { 4.F106 } \end{aligned}$ | $\begin{aligned} & \text { 4.F114 } \\ & \text { 4.F115 } \\ & \text { 4.F116 } \end{aligned}$ | $\begin{aligned} & \text { 4.F124 } \\ & \text { 4.F125 } \\ & \text { 4.F126 } \end{aligned}$ | $\begin{aligned} & \text { 4.F134 } \\ & \text { 4.F135 } \\ & \text { 4.F136 } \end{aligned}$ |
| $\begin{aligned} & \text { R7 } \\ & \text { R8 } \\ & \text { R9 } \end{aligned}$ | Receive error counter | $\begin{aligned} & \text { 3.F107 } \\ & \text { 3.F108 } \\ & \text { 3.F109 } \end{aligned}$ | 3. F117 3.F118 3.F119 | $\begin{aligned} & \text { 3.F127 } \\ & \text { 3.F128 } \\ & \text { 3.F129 } \end{aligned}$ | $\begin{aligned} & \text { 3.F137 } \\ & \text { 3.F138 } \\ & \text { 3.F139 } \end{aligned}$ | $\begin{aligned} & \text { 4.F107 } \\ & \text { 4.F108 } \\ & \text { 4.F109 } \end{aligned}$ | 4.F117 <br> 4.F118 <br> 4.F119 | 4.F127 4.F128 <br> 4.F129 | $\begin{aligned} & \text { 4.F137 } \\ & \text { 4.F138 } \\ & \text { 4.F139 } \end{aligned}$ |

Register 3.F100 controls the generator and checker. Setting register 3.F100.5 to 1 enables the generator, and setting register 3.F100.4 to 1 enables the checker. If either of these bits is set to 1 , then the general PRBS generator and checker overrides the PCS-specific generators and checkers. The port should be set to the selected PCS mode before enabling the PRBS mode to achieve the desired line rate for PRBS testing. When PRBS is enabled, this has higher priority over PCS datapath. Register 3.F100.3:0 controls the pattern that is generated and checked. There is no checker for the high-frequency, low-frequency, mixed-frequency, and square-wave patterns as there are waveforms to check the transmitter performance.
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Table 56: Supported Line-side PRBS Patterns

| 3.F100.3:0 | PRBS Pattern Format |
| :---: | :---: |
| 0000 | IEEE 49.2.8-PRBS 31 |
| 0001 | PRBS 7 |
| 0010 | PRBS 9 IEEE 83.7 |
| 0011 | PRBS 23 |
| 0100 | PRBS 31 Inverted |
| 0101 | PRBS 7 Inverted |
| 1000 | PRBS 15 |
| 1001 | PRBS 15 Inverted |
| 0110 | PRBS 9 Inverted |
| 0111 | PRBS 23 Inverted |
| 1010 | PRBS 58 |
| 1011 | PRBS 58 Inverted |
| 1100 | PRBS 13 |
| 1101 | PRBS 13 Inverted |
| 1110 | JB03 register address <br> Lane 0 pattern A 3.F10A pattern B 3.F10B <br> Lane 1 pattern A 3.F11A pattern B 3.F11B <br> Lane 2 pattern A 3.F12A pattern B 3.F12B <br> Lane 3 pattern A 3.F13A pattern B 3.F13B |
| 1111 | Line-side PRBS square-wave pattern consists of 10 1's followed by 10 0's. |

All counters are 48 bits long. If register 3.F100.13 is set to 1 , then the counters will clear on read. If register $3 . \mathrm{F} 100.13$ is set to 0 , then the counters continue counting until register 3.F100.6 is set to 1 to clear the contents. If register 3.F100.7 is set to 0 , then the PRBS counters will not start to count until the checker first locks onto the incoming PRBS data. If register 3.F100.7 is set to 1, then the PRBS checker will start counting errors without first locking to the incoming PRBS data. Register 3.F100.8 indicates whether the PRBS checker has locked. All 48-bit counters are formed by three 16 -bit registers. The lowest addressed register is the least significant 16 bits and the highest addressed register is the most significant 16 bits of the counter. When the least significant register is read, the two upper registers are updated and frozen so that the three register read is atomic. It is not necessary to read the upper registers. However, on subsequent reads of the least significant register, the values of the upper registers from the previous reads are lost. To get the correct upper register value the least significant register must be read first. Register 3.F101, 3.F102, and 3.F103 is the transmit bit counter. Registers 3.F104, 3.F105, and 3.F106 is the receive bit counter. Registers 3.F107, 3.F108, and 3.F109 is the receive bit error counter.

### 4.8.2 40GBASE-R4-specific Generators and Checkers

Register 1.05DD. 7 when set to 1 selects PRBS31 pattern. Registers 1.05DD. 3 when set to 1 enables Tx generator. Register 1.05DD. 0 when set to 1 enables Rx checker. The error counters for individual lanes are in register 1.06A4, 1.06A5, 1.06A6, and 1.06A7, which will be cleared on read.
Register 1.05DD. 6 when set to 1 selects PRBS9 pattern. Registers 1.05DD. 3 when set to 1 enables Tx generator.

Register 1.05E6.3:0 when set to 1 selects SW (square wave) pattern for individual lanes.
The Line Side Lane 0 to Lane 3 Registers are 3.F100, 3.F110, 3.F120, and 3.F130, respectively.

### 4.8.3 100GBASE-R4-specific Generators and Checkers

Register 1.05DD. 7 when set to 1 selects PRBS31 pattern. Registers 1.05DD. 3 when set to 1 enables Tx generator. Register 1.05DD. 0 when set to 1 enables Rx checker. The error counters for individual lanes are in registers 1.06A4, 1.06A5, 1.06A6, and 1.06A7, which will be cleared on read.
Register 1.05DD. 6 when set to 1 selects PRBS9 pattern. Registers 1.05DD. 3 when set to 1 enables Tx generator.
Register 1.05E6.3:0 when set to 1 selects SW (square wave) pattern for individual lanes.
Table 57 lists IEEE registers to control PRBS.
Table 57: IEEE PCS and PMA PRBS Control Register

|  | Line Side | Host Side |
| :--- | :--- | :--- |
| PCS $10 \mathrm{G} / 25 \mathrm{G}$ lane 0 | $3.202 \mathrm{~A}, 3.202 \mathrm{~B}$ | $4.202 \mathrm{~A}, 4.202 \mathrm{~B}$ |
| PCS $10 \mathrm{G} / 25 \mathrm{G}$ lane 1 | $3.222 \mathrm{~A}, 3.222 \mathrm{~B}$ | $4.222 \mathrm{~A}, 4.222 \mathrm{~B}$ |
| PCS 10G/25G lane 2 | 3.242A, 3.242B | $4.242 \mathrm{~A}, 4.242 \mathrm{~B}$ |
| PCS 10G/25G lane 3 | 3.262A, 3.262B | $4.262 \mathrm{~A}, 4.262 \mathrm{~B}$ |
| PMA lane 0 | 1.05DD, 1.05E6, 1.06A4-7 | $1.15 \mathrm{DD}, 1.15 \mathrm{E} 6,1.16 \mathrm{~A} 4-7$ |
| PMA lane 1 | 1.25DD, 1.25E6, 1.26A4-7 | $1.35 \mathrm{DD}, 1.35 \mathrm{E} 6,1.36 \mathrm{~A} 4-7$ |
| PMA lane 2 | 1.45DD, 1.45E6, 1.46A4-7 | $1.55 \mathrm{DD}, 1.55 \mathrm{E} 6,1.56 \mathrm{~A} 4-7$ |
| PMA lane 3 | 1.65DD, 1.65E6, 1.66A4-7 | $1.75 \mathrm{DD}, 1.75 \mathrm{E} 6,1.76 \mathrm{~A} 4-7$ |

### 4.9 Eye Monitor

Each lane has its own non-destructive eye monitor to determine the quality of the received signal in traffic mode.

## 5 <br> Host Side Description

The host interface functionality is identical to the line interface in Section 4 with the following exceptions.

The host interface comprises four differential input lanes and four differential output lanes.
All line side registers have equivalent registers in the host side as shown in Table 58. The address either has a different DEVAD or an offset in the REGAD. All the description of the line interface functionality in Section 4 applies to the host interface except for the register address location.

Table 58: Equivalent Registers Between Line and Host Interface

| Line Interface |  | Host Interface |  | Description |
| :---: | :---: | :---: | :---: | :---: |
| Start | End | Start | End | -- |
| 1.0000 | 1.00FF | 1.1000 | 1.10FF | PMA (IEEE) Sub-Port 0 |
| 1.2000 | 1.20FF | 1.3000 | 1.30FF | PMA (IEEE) Sub-Port 1 |
| 1.4000 | 1.40FF | 1.5000 | 1.50FF | PMA (IEEE) Sub-Port 2 |
| 1.6000 | 1.60FF | 1.7000 | 1.70FF | PMA (IEEE) Sub-Port 3 |
| 1.8000 | 1.80FF | 1.9000 | 1.90FF | PMA FEC (IEEE) Sub-Port 0 |
| 1.0100 | 1.01FF | 1.1100 | 1.11FF | PMA (IEEE) Sub-Port 0 |
| 1.2100 | 1.21FF | 1.3100 | 1.31FF | PMA (IEEE) Sub-Port 1 |
| 1.4100 | 1.41FF | 1.5100 | 1.51FF | PMA (IEEE) Sub-Port 2 |
| 1.6100 | 1.61FF | 1.7100 | 1.71FF | PMA (IEEE) Sub-Port 3 |
| 1.8100 | 1.80FF | 1.9100 | 1.90FF | PMA FEC (IEEE) Sub-Port 0 |
| 1.0200 | 1.02FF | 1.1200 | 1.12FF | PMA (IEEE) Sub-Port 0 |
| 1.2200 | 1.22FF | 1.3200 | 1.32FF | PMA (IEEE) Sub-Port 1 |
| 1.4200 | 1.42FF | 1.5200 | 1.52FF | PMA (IEEE) Sub-Port 2 |
| 1.6200 | 1.62FF | 1.7200 | 1.72FF | PMA (IEEE) Sub-Port 3 |
| 1.0300 | 1.03FF | 1.1300 | 1.13FF | PMA (IEEE) Sub-Port 0 |
| 1.2300 | 1.23FF | 1.3300 | 1.33FF | PMA (IEEE) Sub-Port 1 |
| 1.4300 | 1.43FF | 1.5300 | 1.53FF | PMA (IEEE) Sub-Port 2 |
| 1.6300 | 1.63FF | 1.7300 | 1.73FF | PMA (IEEE) Sub-Port 3 |
| 1.0400 | 1.04FF | 1.1400 | 1.14FF | PMA (IEEE) Sub-Port 0 |
| 1.2400 | 1.24 FF | 1.3400 | 1.34 FF | PMA (IEEE) Sub-Port 1 |

Table 58: Equivalent Registers Between Line and Host Interface (Continued)

| Line Interface |  | Host Interface |  | Description |
| :---: | :---: | :---: | :---: | :---: |
| Start | End | Start | End | -- |
| 1.4400 | 1.44FF | 1.5400 | 1.54FF | PMA (IEEE) Sub-Port 2 |
| 1.6400 | 1.64FF | 1.7400 | 1.74FF | PMA (IEEE) Sub-Port 3 |
| 1.0500 | 1.05FF | 1.1500 | 1.15FF | PMA (IEEE) Sub-Port 0 |
| 1.2500 | 1.25FF | 1.3500 | 1.35FF | PMA (IEEE) Sub-Port 1 |
| 1.4500 | 1.45FF | 1.5500 | 1.55 FF | PMA (IEEE) Sub-Port 2 |
| 1.6500 | 1.65FF | 1.7500 | 1.75FF | PMA (IEEE) Sub-Port 3 |
| 1.0600 | 1.06FF | 1.1600 | 1.16FF | PMA (IEEE) Sub-Port 0 |
| 1.2600 | 1.26FF | 1.3600 | 1.36FF | PMA (IEEE) Sub-Port 1 |
| 1.4600 | 1.46FF | 1.5600 | 1.56FF | PMA (IEEE) Sub-Port 2 |
| 1.6600 | 1.66FF | 1.7600 | 1.76FF | PMA (IEEE) Sub-Port 3 |
| $1 . \mathrm{C000}$ | 1.COFF | $1 . \mathrm{D} 000$ | 1.D0FF | PMA (Marvell) Sub-Port 0 |
| $1 . \mathrm{C} 200$ | 1.C2FF | $1 . \mathrm{D} 200$ | 1.D2FF | PMA (Marvell) Sub-Port 1 |
| $1 . \mathrm{C400}$ | 1.C4FF | $1 . \mathrm{D} 400$ | 1.D4FF | PMA (Marvell) Sub-Port 2 |
| $1 . \mathrm{C} 600$ | 1.C6FF | $1 . \mathrm{D} 600$ | 1.D6FF | PMA (Marvell) Sub-Port 3 |
| $1 . \mathrm{C} 800$ | 1.C8FF | $1 . \mathrm{D} 800$ | 1.D8FF | PMA (Marvell) All ports |
| $1 . \mathrm{C} 100$ | 1.C1FF | $1 . \mathrm{D} 100$ | 1.D1FF | PMA (Marvell) Sub-Port 0 |
| $1 . \mathrm{C} 300$ | 1.C3FF | $1 . \mathrm{D} 300$ | 1.D3FF | PMA (Marvell) Sub-Port 1 |
| $1 . \mathrm{C} 500$ | 1.C5FF | $1 . \mathrm{D} 500$ | 1.D5FF | PMA (Marvell) Sub-Port 2 |
| $1 . \mathrm{C700}$ | 1.C7FF | $1 . \mathrm{D} 700$ | 1.D7FF | PMA (Marvell) Sub-Port 3 |
| $1 . \mathrm{C900}$ | 1.C9FF | $1 . \mathrm{D900}$ | 1.D9FF | PMA (Marvell) All ports |
| $1 . \mathrm{CB} 00$ | 1.CBFF | $1 . \mathrm{DB00}$ | 1.DBFF | PMA (Marvell) All ports |
| 1.CD00 | 1.CDFF | 1. DD00 | 1.DDFF | PMA (Marvell) All ports |
| $1 . \mathrm{CF} 00$ | 1.CFFF | $1 . \mathrm{DF} 00$ | 1.DFFF | PMA (Marvell) All ports |
| 3.4000 | 3.40FF | 4.4000 | 4.40FF | 200GBASE-R4 (IEEE) |
| 3.4100 | 3.41FF | 4.4100 | 4.41FF | 200GBASE-R4 (IEEE) |
| 3.3000 | 3.30 FF | 4.3000 | 4.30FF | 1/2.5GBASE-R (IEEE) Sub-Port 0 |
| 3.3200 | 3.32FF | 4.3200 | 4.32FF | 1/2.5GBASE-R (IEEE) Sub-Port 1 |
| 3.3400 | 3.34FF | 4.3400 | 4.34FF | 1/2.5GBASE-R (IEEE) Sub-Port 2 |

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Table 58: Equivalent Registers Between Line and Host Interface (Continued)

| Line Interface |  | Host Interface |  | Description |
| :---: | :---: | :---: | :---: | :---: |
| Start | End | Start | End | -- |
| 3.3600 | 3.36FF | 4.3600 | 4.36FF | 1/2.5GBASE-R (IEEE) Sub-Port 3 |
| 3.3100 | 3.31 FF | 4.3100 | 4.31FF | 1/2.5GBASE-R (IEEE) Sub-Port 0 |
| 3.3300 | 3.33FF | 4.3300 | 4.33FF | 1/2.5GBASE-R (IEEE) Sub-Port 1 |
| 3.3500 | 3.35FF | 4.3500 | 4.35FF | 1/2.5GBASE-R (IEEE) Sub-Port 2 |
| 3.3700 | 3.37 FF | 4.3700 | 4.37FF | 1/2.5GBASE-R (IEEE) Sub-Port 3 |
| 3.2000 | 3.20 FF | 4.2000 | 4.20FF | 5/10/25GBASE-R (IEEE) Sub-Port 0 |
| 3.2200 | 3.22FF | 4.2200 | 4.22FF | 5/10/25GBASE-R (IEEE) Sub-Port 1 |
| 3.2400 | 3.24 FF | 4.2400 | 4.24FF | 5/10/25GBASE-R (IEEE) Sub-Port 2 |
| 3.2600 | 3.26 FF | 4.2600 | 4.26FF | 5/10/25GBASE-R (IEEE) Sub-Port 3 |
| 3.2100 | 3.21FF | 4.2100 | 4.21FF | 5/10/25GBASE-R (IEEE) Sub-Port 0 |
| 3.2310 | 3.23FF | 4.2310 | 4.23FF | 5/10/25GBASE-R (IEEE) Sub-Port 1 |
| 3.2500 | 3.25 FF | 4.2500 | 4.25FF | 5/10/25GBASE-R (IEEE) Sub-Port 2 |
| 3.2700 | 3.27FF | 4.2700 | 4.27FF | 5/10/25GBASE-R (IEEE) Sub-Port 3 |
| 3.1000 | 3.10FF | 4.1000 | 4.10FF | 40GBASE-R4 (IEEE) Sub-Port 0 |
| 3.1200 | 3.12FF | 4.1200 | 4.12FF | 40GBASE-R4 (IEEE) Sub-Port 1 |
| 3.1400 | 3.14FF | 4.1400 | 4.14FF | 40GBASE-R4 (IEEE) Sub-Port 2 |
| 3.1600 | 3.16FF | 4.1600 | 4.16FF | 40GBASE-R4 (IEEE) Sub-Port 3 |
| 3.1100 | 3.11FF | 4.1100 | 4.11FF | 40GBASE-R4 (IEEE) Sub-Port 0 |
| 3.1300 | 3.13FF | 4.1300 | 4.13FF | 40GBASE-R4 (IEEE) Sub-Port 1 |
| 3.1500 | 3.15FF | 4.1500 | 4.15FF | 40GBASE-R4 (IEEE) Sub-Port 2 |
| 3.1700 | 3.17FF | 4.1700 | 4.17FF | 40GBASE-R4 (IEEE) Sub-Port 3 |
| 3.0000 | 3.00 FF | 4.0000 | 4.00FF | 100GBASE-R4 (IEEE) sub-port 0 |
| 3.0400 | 3.04FF | 4.0400 | 4.04FF | 100GBASE-R4 (IEEE) sub-port 1 |
| 3.0500 | 3.05FF | 4.0100 | 4.01FF | 100GBASE-R4 (IEEE) sub-port 0 |
| 3.0100 | 3.05FF | 4.0500 | 4.05FF | 100GBASE-R4 (IEEE) sub-port 1 |
| 3.0700 | 3.07FF | 4.0700 | 4.07FF | 100GBASE-R4 (IEEE) sub-port 0 |
| 3.0B00 | 3.0BFF | 4.0B00 | 4.0BFF | 100GBASE-R4 (IEEE) sub-port 1 |
| $3 . C 000$ | 3.COFF | $4 . \mathrm{C000}$ | 4.COFF | 200GBASE-R4 (Marvell) |

Table 58: Equivalent Registers Between Line and Host Interface (Continued)

| Line Interface |  | Host Interface |  | Description |
| :---: | :---: | :---: | :---: | :---: |
| Start | End | Start | End | -- |
| 3.C100 | 3.C1FF | $4 . \mathrm{C} 100$ | 4.C1FF | 200GBASE-R4 (Marvell) |
| 3.B000 | 3.B0FF | 4.B000 | 4.B0FF | 1/2.5GBASE-R (Marvell) Sub-Port 0 |
| 3.8200 | 3.B2FF | 4.8200 | 4.B2FF | 1/2.5GBASE-R (Marvell) Sub-Port 1 |
| 3.B400 | 3.B4FF | 4.8400 | 4.B4FF | 1/2.5GBASE-R (Marvell) Sub-Port 2 |
| 3.8600 | 3.B6FF | 4.8600 | 4.B6FF | 1/2.5GBASE-R (Marvell) Sub-Port 3 |
| 3.B100 | 3.B1FF | 4.8100 | 4.B1FF | 1/2.5GBASE-R (Marvell) Sub-Port 0 |
| 3.8300 | 3.B3FF | 4.8300 | 4.B3FF | 1/2.5GBASE-R (Marvell) Sub-Port 1 |
| 3.8500 | 3.B5FF | 4.8500 | 4.B5FF | 1/2.5GBASE-R (Marvell) Sub-Port 2 |
| 3.8700 | 3.B7FF | 4.8700 | 4.B7FF | 1/2.5GBASE-R (Marvell) Sub-Port 3 |
| $3 . \mathrm{A} 000$ | 3.A0FF | $4 . \mathrm{A} 000$ | 4.A0FF | 5/10/25GBASE-R (Marvell) Sub-Port 0 |
| $3 . \mathrm{A} 200$ | 3.A2FF | $4 . \mathrm{A} 200$ | 4.A2FF | 5/10/25GBASE-R (Marvell) Sub-Port 1 |
| $3 . \mathrm{A} 400$ | 3.A4FF | $4 . \mathrm{A} 400$ | 4.A4FF | 5/10/25GBASE-R (Marvell) Sub-Port 2 |
| 3.4600 | 3.A6FF | 4.4600 | 4.A6FF | 5/10/25GBASE-R (Marvell) Sub-Port 3 |
| $3 . \mathrm{A} 100$ | 3.A1FF | $4 . \mathrm{A} 100$ | 4.A1FF | 5/10/25GBASE-R (Marvell) Sub-Port 0 |
| $3 . \mathrm{A} 300$ | 3.A3FF | $4 . \mathrm{A} 300$ | 4.A3FF | 5/10/25GBASE-R (Marvell) Sub-Port 1 |
| $3 . A 500$ | 3.A5FF | $4 . A 500$ | 4.A5FF | 5/10/25GBASE-R (Marvell) Sub-Port 2 |
| $3 . A 700$ | 3.A7FF | 4.4700 | 4.A7FF | 5/10/25GBASE-R (Marvell) Sub-Port 3 |
| 3.9000 | 3.90FF | 4.9000 | 4.90FF | 40GBASE-R4 (Marvell) Sub-Port 0 |
| 3.9200 | 3.92FF | 4.9200 | 4.92FF | 40GBASE-R4 (Marvell) Sub-Port 1 |
| 3.9400 | 3.94FF | 4.9400 | 4.94FF | 40GBASE-R4 (Marvell) Sub-Port 2 |
| 3.9600 | 3.96FF | 4.9600 | 4.96FF | 40GBASE-R4 (Marvell) Sub-Port 3 |
| 3.9100 | 3.91FF | 4.9100 | 4.91FF | 40GBASE-R4 (Marvell) |
| 3.8000 | 3.80FF | 4.8000 | 4.80FF | 100GBASE-R4 (Marvell) |
| 3.8100 | 3.81 FF | 4.8000 | 4.80FF | 100GBASE-R4 (Marvell) |
| 3.F000 | 3.FOFF | $4 . \mathrm{F} 000$ | 4.FOFF | Line or Host Common |
| 3.F100 | 3.F1FF | 4.F100 | 4.F1FF | Line or Host Common |
| 7.0000 | 7.00FF | 7.1000 | 7.10FF | AP Auto-Negotiation (IEEE) Sub-Port 0 |
| 7.0200 | 7.02FF | 7.1200 | 7.12FF | AP Auto-Negotiation (IEEE) Sub-Port 1 |

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Table 58: Equivalent Registers Between Line and Host Interface (Continued)

| Line Interface |  | Host Interface |  | Description |
| :---: | :---: | :---: | :---: | :---: |
| Start | End | Start | End | -- |
| 7.0400 | 7.04FF | 7.1400 | 7.14FF | AP Auto-Negotiation (IEEE) Sub-Port 2 |
| 7.0600 | 7.06FF | 7.1600 | 7.16FF | AP Auto-Negotiation (IEEE) Sub-Port 3 |
| 7.0100 | 7.01FF | 7.1100 | 7.11FF | AP Auto-Negotiation (IEEE) Sub-Port 0 |
| 7.0300 | 7.03FF | 7.1300 | 7.13FF | AP Auto-Negotiation (IEEE) Sub-Port 1 |
| 7.0500 | 7.05FF | 7.1500 | 7.15FF | AP Auto-Negotiation (IEEE) Sub-Port 2 |
| 7.0700 | 7.07FF | 7.1700 | 7.17FF | AP Auto-Negotiation (IEEE) Sub-Port 3 |
| 7.8000 | 7.80FF | 7.9000 | 7.90FF | AP Auto-Negotiation (Marvell) Sub-Port 0 |
| 7.8200 | 7.82FF | 7.9200 | 7.92FF | AP Auto-Negotiation (Marvell) Sub-Port 1 |
| 7.8400 | 7.84FF | 7.9400 | 7.94FF | AP Auto-Negotiation (Marvell) Sub-Port 2 |
| 7.8600 | 7.86FF | 7.9600 | 7.96FF | AP Auto-Negotiation (Marvell) Sub-Port 3 |
| 7.8100 | 7.81FF | 7.9100 | 7.91FF | AP Auto-Negotiation (Marvell) Sub-Port 0 |
| 7.8300 | 7.83FF | 7.9300 | 7.93FF | AP Auto-Negotiation (Marvell) Sub-Port 1 |
| 7.8500 | 7.85FF | 7.9500 | 7.95FF | AP Auto-Negotiation (Marvell) Sub-Port 2 |
| 7.8700 | 7.87FF | 7.9700 | 7.97FF | AP Auto-Negotiation (Marvell) Sub-Port 3 |
| 30.0000 | 30.7FFF | 30.8000 | 30.FFFF | SERDES Access |

In most cases, the data flow between the line and host are symmetrical and the mode settings for line and host are interchangeable. The configurations shown in Table 59 are not reversible.
The SGMII (PHY) mode is used on the host interface instead of the SGMII (System) mode. When SGMII Auto-Negotiation is turned on ( $4.3 \mathrm{n} 00.12=1, \mathrm{n}=0,2,4,6$ for sub-ports $0,1,2,3$ respectively), the speed advertised is set by the operational speed of the corresponding sub-port on the line interface.

Table 59: Non-Reversible Mode Combinations

| Line | Host |
| :--- | :--- |
| P1S | P1P |
| P25* | P40* |

## 6 <br> Chip Bring Up

The chip bring up process involves applying power and supplying a clock to the device, hardware resetting and configuring the device, load the firmware either through the EEPROM, or through the MDIO/TWSI slave, and finally configuring the registers and engaging the data path. The firmware will be reset by hardware reset. Firmware requires a reload if a hardware reset is issued.

### 6.1 Power Sequencing

VDDON, VDDOS, AVDDL, AVDDH, AVDDC, and DVDD is applied to the device and the 156.25 MHz differential clock is applied to the CLKP/CLKN pins. This device requires no power up sequencing. However, the recommendation is to power up VDDO and AVDDT first, followed by AVDDH/L/C, followed by DVDD.

If the 25 MHz output clock is to be used on the CLK25P/CLK25N pins, then the AVDDT supply should be tied to 3.3 V or 2.5 V . Otherwise, it should be AC coupled to ground. AVDDT can be combined with VDDON and VDDOS but with a filtering scheme.

After all the power supplies stabilize, the 25 MHz clock will be stable 7 to 10 ms after the 156.25 MHz clock is stable. The 25 MHz clock is not dependent on the state of the RESETn pin.

### 6.2 Reset and Configuration

RESETn should be asserted as shown in Section 7.5.3. At the de-assertion of RESETn, hardware configuration values are latched into the device as described in Section 3.3.

## 7 <br> Electrical Specifications

### 7.1 Absolute Maximum Ratings

Table 60: Absolute Maximum Ratings
Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied Exposure to absolute maximum ratings for extended periods may affect device reliability.

| Symbol | Parameter | Min | Max | Units |
| :--- | :--- | :--- | :--- | :--- |
| V $_{\text {DDAL }}$ | Power Supply Voltage on AVDDL with respect to VSS | -0.5 | 1.5 | V |
| V $_{\text {DDAH }}$ | Power Supply Voltage on AVDDH with respect to VSS | -0.5 | 1.5 | V |
| V $_{\text {DDAC }}$ | Power Supply Voltage on AVDDC with respect to VSS | -0.5 | 1.5 | V |
| V $_{\text {DDAT }}$ | Power Supply Voltage on AVDDT with respect to VSS | -0.5 | 3.6 | V |
| $\mathrm{V}_{\text {DDON }}$ | Power Supply Voltage on VDDON with respect to VSS | -0.5 | 3.6 | V |
| $\mathrm{V}_{\text {DDOS }}$ | Power Supply Voltage on VDDOS with respect to VSS | -0.5 | 3.6 | V |
| $\mathrm{~V}_{\text {DD }}$ | Power Supply Voltage on DVDD with respect to VSS | -0.5 | 1.5 | V |
| TSTORAGE | Storage temperature | -40 | $+125^{1}$ | ${ }^{\circ} \mathrm{C}$ |

1. $125^{\circ} \mathrm{C}$ is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) should be kept at $85^{\circ} \mathrm{C}$ or lower.

### 7.2 Recommended Operating Conditions

Table 61: Recommended Operating Conditions (Commercial)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DDAL }}{ }^{1}$ | AVDDL Supply | For AVDDL | 0.95 | 1.0 | 1.05 | V |
| $V_{\text {DDAH }}$ | AVDDH Supply | For AVDDH | 0.95 | 1.0 | 1.05 | V |
| $V_{\text {DDAC }}$ | AVDDC Supply | For AVDDC | 0.95 | 1.0 | 1.05 | V |
| $V_{\text {DDAT }}$ | AVDDT Supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
|  |  | 2.5 V | 2.375 | 2.5 | 2.625 |  |
| $\mathrm{V}_{\text {VDDO }}$ | VDDON or VDDOS Supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
|  |  | 2.5 V | 2.375 | 2.5 | 2.625 |  |
|  |  | 1.8 V | 1.71 | 1.8 | 1.89 |  |
|  |  | 1.2 V | 1.14 | 1.2 | 1.26 |  |
|  |  | 1.05 V | 0.998 | 1.05 | 1.103 |  |
| $V_{D D}$ | DVDD Supply (C Temp) | - | 0.855 | 0.9 | 0.945 | V |
| $V_{D D}$ | DVDD Supply (I Temp) | - | 0.902 | 0.95 | 0.997 | V |
| $\mathrm{T}_{J}$ | Maximum junction temperature | - | - | - | $105^{2}$ | ${ }^{\circ} \mathrm{C}$ |

1. Maximum noise allowed on supplies is 5 mVppd .
2. Refer to the white paper on $T_{J}$ Thermal Calculations for detailed information.
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### 7.3 Package Thermal Information

### 7.3.1 Thermal Conditions for 169-pin, FCBGA Package

Table 62: Thermal Conditions for 169-pin, FCBGA Package

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\theta_{J A}$ | Thermal resistance ${ }^{1}$ junction to ambient for the 169-pin FCBGA package $\theta_{\mathrm{JA}}=\left(\mathrm{T}_{\mathrm{J}}-\mathrm{T}_{\mathrm{A}}\right) / \mathrm{P}$ <br> $\mathrm{P}=$ Total power dissipation | JEDEC 3 in. x 4.5 in. 12-layer PCB with no air flow | - | 16.28 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 1 meter/sec air flow | - | 14.00 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 2 meter/sec air flow | - | 12.98 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 3 meter/sec air flow | - | 12.36 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\psi_{\text {JT }}$ | Thermal characteristic parameter ${ }^{\text {a }}$ - junction to top center of the 169-pin FCBGA package $\psi_{\mathrm{JT}}=\left(\mathrm{T}_{\mathrm{J}}-\mathrm{T}_{\text {top }}\right) / \mathrm{P}$ <br> $\mathrm{P}=$ Total power dissipation, $T_{\text {top: }}$ Temperature on the top center of the package | JEDEC 3 in. x 4.5 in. 12-layer PCB with no air flow | - | 1.30 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 1 meter/sec air flow | - | 1.31 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 2 meter/sec air flow | - | 1.32 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | JEDEC 3 in. x 4.5 in. 12-layer PCB with 3 meter/sec air flow | - | 1.33 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\text {JC }}$ | Thermal resistance ${ }^{\text {a }}$ junction to case for the 169-pin FCBGA package $\begin{aligned} & \theta_{J C}=\left(T_{J}-T_{C}\right) / P_{\text {top }} \\ & P_{\text {top }}=\text { Power dissipation } \\ & \text { from the top of the package } \end{aligned}$ | JEDEC with no air flow | - | 1.70 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\mathrm{JB}}$ | Thermal resistance ${ }^{\text {a }}$ junction to board for the 169-pin FCBGA package $\theta_{\mathrm{JB}}=\left(\mathrm{T}_{\mathrm{J}}-\mathrm{T}_{\mathrm{B}}\right) / \mathrm{P}_{\text {bottom }}$ $P_{\text {bottom }}=$ Power dissipation from the bottom of the package to the PCB surface | JEDEC with no air flow | - | 5.81 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. Refer to the white paper on $T_{\jmath}$ Thermal Calculations for detailed information.

### 7.4 Current Consumption

### 7.4.1 $\quad 88 \times 5113$ Current Consumption (Commercial)

Table 63: DVDD Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DVDD | Base | Chip Base Power including leakage | - | 84 | 941 | mA |
|  | 1G PCS (1 lane power) | P1X, P1S, P1P | - | 6 | 8 | mA |
|  | 2.5G PCS (1 lane power) | P2.5X | - | 13 | 16 | mA |
|  | 5G PCS (1 lane power) | P5L, P5K | - | 13 | 13 | mA |
|  | 10G PCS - No FEC (1 lane power) | P10LN, P10KN | - | 26 | 29 | mA |
|  | 10G PCS - KR FEC (1 lane power) | P10KF, P10LF | - | 31 | 37 | mA |
|  | 25G PCS - No FEC (1 lane power) | $\begin{aligned} & \text { P25LN, P25LR, P25CN, P25KN, } \\ & \text { P25BN, P25JN } \end{aligned}$ | - | 54 | 60 | mA |
|  | 25G PCS - KR FEC (1 lane power) | P25LF, P25CF, P25KF, P25BF, P25JF | - | 67 | 76 | mA |
|  | 25G PCS - RS FEC (1 lane power) | $\begin{aligned} & \text { P25LR, P25CR, P25KR, P25BR, } \\ & \text { P25JR } \end{aligned}$ | - | 99 | 111 | mA |
|  | 40G PCS - No FEC (4 lane power) | P40LN, P40CN, P40KN | - | 97 | 109 | mA |
|  | 40G PCS - KR FEC (4 lane power) | P40CF, P40KL, P40LF | - | 119 | 135 | mA |
|  | 50G PCS - No FEC (4 lane power) | P50LN, P50CN, P50KN | - | 110 | 124 | mA |
|  | 50G PCS - KR FEC (4 lane power) | P50CF, P50KF, P50LF | - | 139 | 160 | mA |
|  | 50G PCS - No FEC (2 lane power) | P50MN, P50BN, P50JN | - | 107 | 122 | mA |
|  | 50G PCS - KR FEC (2 lane power) | P50MF, P50BF, P50JF | - | 120 | 135 | mA |
|  | 50G PCS - RS FEC (2 lane power) | P50MR, P50BR, P50JR | - | 221 | 231 | mA |
|  | 100G PCS - No FEC (4 lane power) | P100LN, P100KN | - | 228 | 263 | mA |
|  | 100G PCS - RS FEC (4 lane power) | P100LR, P100CR, P100KR | - | 430 | 481 | mA |

Example: P100LN to P100CR operation
Current consumption on DVDD = DVDD Base + P100LN + P100CR

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Table 64: AVDDL and AVDDH Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AVDDL or AVDDH | Base | Chip Base Power including leakage | - | 54 | 350 | mA |
|  | 1G Speed (1 lane power) | P1*, R1 | - | 74 | 90 | mA |
|  | 2.5G Spkvban641eed (1 lane power) | P2.5X, R2.5 | - | 89 | 111 | mA |
|  | 5G Speed (1 lane power) | P5*, R5* | - | 106 | 125 | mA |
|  | 10G Speed (1 lane power) | P10*, R10* | - | 144 | 164 | mA |
|  | 25G Speed (1 lane power) | P25*, R25* | - | 256 | 292 | mA |
|  | 40G Speed (4 lane power) | P40*, R40* | - | 567 | 653 | mA |
|  | 50G Speed (4 lane power) | P50L*, P50C*, P50K* | - | 641 | 739 | mA |
|  | 50G Speed (2 lane power) | P50M*, P50B*, P50J* | - | 509 | 583 | mA |
|  | 100G Speed (4 lane power) | P100*, R100* | - | 1003 | 1156 | mA |

Example: P100LN to P100CR operation
Current consumption on AVDD = AVDDL Base + AVDDH Base + P100* + P100* + AVDDC

Table 65: AVDDC and AVDDT Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AVDDC | Base | Chip Base Power including leakage | - | - | 10 | mA |
| AVDDT | Base | Chip Base Power including leakage | - | - | 34 | mA |

### 7.4.2 88X5113 Current Consumption (Industrial)

Table 66: DVDD Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DVDD | Base | Chip Base Power including leakage | - | 84 | 941 | mA |
|  | 1G PCS (1 lane power) | P1X, P1S, P1P | - | 6 | 8 | mA |
|  | 2.5G PCS (1 lane power) | P2.5X | - | 13 | 16 | mA |
|  | 5G PCS (1 lane power) | P5L, P5K | - | 13 | 13 | mA |
|  | 10G PCS - No FEC (1 lane power) | P10LN, P10KN | - | 26 | 29 | mA |
|  | 10G PCS - KR FEC (1 lane power) | P10KF, P10LF | - | 31 | 37 | mA |
|  | 25G PCS - No FEC (1 lane power) | P25LN, P25LR, P25CN, P25KN, P25BN, P25JN | - | 54 | 60 | mA |
|  | 25G PCS - KR FEC (1 lane power) | P25LF, P25CF, P25KF, P25BF, P25JF | - | 67 | 76 | mA |
|  | 25G PCS - RS FEC (1 lane power) | P25LR, P25CR, P25KR, P25BR, P25JR | - | 99 | 111 | mA |
|  | 40G PCS - No FEC (4 lane power) | P40LN, P40CN, P40KN | - | 97 | 109 | mA |
|  | 40G PCS - KR FEC (4 lane power) | P40CF, P40KL, P40LF | - | 119 | 135 | mA |
|  | 50G PCS - No FEC (4 lane power) | P50LN, P50CN, P50KN | - | 110 | 124 | mA |
|  | 50G PCS - KR FEC (4 lane power) | P50CF, P50KF, P50LF | - | 139 | 160 | mA |
|  | 50G PCS - No FEC (2 lane power) | P50MN, P50BN, P50JN | - | 107 | 122 | mA |
|  | 50G PCS - KR FEC (2 lane power) | P50MF, P50BF, P50JF | - | 120 | 135 | mA |
|  | 50G PCS - RS FEC (2 lane power) | P50MR, P50BR, P50JR | - | 221 | 231 | mA |
|  | 100G PCS - No FEC (4 lane power) | P100LN, P100KN | - | 228 | 263 | mA |
|  | 100G PCS - RS FEC (4 lane power) | P100LR, P100CR, P100KR | - | 430 | 481 | mA |

Example: P100LN to P100CR operation
Current consumption on DVDD = DVDD Base + P100LN + P100CR

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Table 67: AVDDL and AVDDH Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AVDDL or AVDDH | Base | Chip Base Power including leakage | - | 54 | 350 | mA |
|  | 1G Speed (1 lane power) | P1*, R1 | - | 74 | 90 | mA |
|  | 2.5G Spkvban641eed (1 lane power) | P2.5X, R2.5 | - | 89 | 111 | mA |
|  | 5G Speed (1 lane power) | P5*, R5* | - | 106 | 125 | mA |
|  | 10G Speed (1 lane power) | P10*, R10* | - | 144 | 164 | mA |
|  | 25G Speed (1 lane power) | P25*, R25* | - | 256 | 292 | mA |
|  | 40G Speed (4 lane power) | P40*, R40* | - | 567 | 653 | mA |
|  | 50G Speed (4 lane power) | P50L*, P50C*, P50K* | - | 641 | 739 | mA |
|  | 50G Speed (2 lane power) | P50M*, P50B*, P50J* | - | 509 | 583 | mA |
|  | 100G Speed (4 lane power) | P100*, R100* | - | 1003 | 1156 | mA |

Example: P100LN to P100CR operation
Current consumption on AVDD = AVDDL Base + AVDDH Base + P100* + P100* + AVDDC

### 7.5 Digital I/O Electrical Specifications

Table 68: AVDDC and AVDDT Current Consumption

| Pins | Parameter | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AVDDC | Base | Chip Base Power including leakage | - | - | 10 | $m A$ |
| AVDDT | Base | Chip Base Power including leakage | - | - | 34 | $m A$ |

### 7.5.1 DC Operating Conditions

## Table 69: DC Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VIH | Input High Voltage | All digital inputs | VDDO* $=3.3 \mathrm{~V}$ | 2.0 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
|  |  |  | VDDO* $=2.5 \mathrm{~V}$ | 1.75 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
|  |  |  | VDDO* $=1.8 \mathrm{~V}$ | 1.26 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
|  |  |  | $V D^{*}{ }^{*}=1.5 \mathrm{~V}$ | 1.05 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
|  |  |  | VDDO* $=1.2 \mathrm{~V}$ | 0.84 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
|  |  |  | VDDO* $=1.05 \mathrm{~V}$ | 0.74 | - | $\begin{aligned} & \text { VDDO + } \\ & 0.3 \mathrm{~V} \end{aligned}$ | V |
| VIL | Input Low Voltage | All digital inputs | VDDO* $=3.3 \mathrm{~V}$ | -0.3 | - | 0.8 | V |
|  |  |  | VDDO* $=2.5 \mathrm{~V}$ | -0.3 | - | 0.75 | V |
|  |  |  | VDDO* $=1.8 \mathrm{~V}$ | -0.3 | - | 0.54 | V |
|  |  |  | VDDO* $=1.5 \mathrm{~V}$ | -0.3 | - | 0.45 | V |
|  |  |  | VDDO* $=1.2 \mathrm{~V}$ | -0.3 | - | 0.36 | V |
|  |  |  | VDDO* $=1.05 \mathrm{~V}$ | -0.3 | - | 0.31 | V |
| VOH | High-level Output Voltage | All digital outputs | $\mathrm{IOH}=-4 \mathrm{~mA}$ | $\begin{aligned} & \text { VDDO } \\ & -0.4 \mathrm{~V} \end{aligned}$ | - | - | V |
| VOL | Low-level Output Voltage | All digital outputs | $\mathrm{IOL}=4 \mathrm{~mA}$ | - | - | 0.4 | V |

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Table 69: DC Operating Conditions
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| IILK | Input <br> Leakage <br> Current | With internal <br> pull-up/pull-down <br> resistor | - | 10 | - | 70 | $\mu \mathrm{~A}$ |
|  | All others <br> without resistor | - | - | - | 10 | $\mu \mathrm{~A}$ |  |
| CIN | Input <br> Capacitance | All pins | - | - | - | 5 | pF |

### 7.5.2 AC Operating Conditions

Table 70: AC Operating Conditions
(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $T_{R}$ | Rise Time | GPIO[0] | 20 to $80 \%$ of $V p p d$ | - | 0.87 | - | ns |
| $T_{F}$ | Fall Time | GPIO[ 0$]$ | 20 to $80 \%$ of $V p p d$ | - | 0.68 | - | $n s$ |

### 7.5.3 Reset Timing

Table 71: Reset Timing
(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| T PU_RESET | Valid Power to RESET <br> De-asserted | - | 10 | - | - | ms |
| TSU_CLK | Number of Valid CLK Cycles <br> Prior to RESET <br> De-asserted | - | 50 | - | - | clks |
| TRESET | Minimum Reset Pulse Width <br> During Normal Operation | - | 10 | - | - | ms |

Figure 32: Reset Timing


### 7.5.4 MDC/MDIO Management Interface Timing

## Table 72: MDC/MDIO Management Interface Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol. | Parameter. | Condition. | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| T DLY_MDIO | MDC to MDIO (Output) Delay Time | 25 pf load on MDIO | 3.5 | - | 19 | ns |
| TSU_MDIO | MDIO (Input) to MDC Setup Time | - | 6.5 | - | - | ns |
| THD_MDIO | MDIO (Input) to MDC Hold Time | - | 0.5 | - | - | ns |
| $\mathrm{T}_{\mathrm{P}_{\text {_ }}} \mathrm{MDC}$ | MDC Period | Subject to TREAD _DLY | $40^{1,2}$ | - | - | ns |
| $\mathrm{T}_{\mathrm{H} \text { _ MDC }}$ | MDC High | - | 12 | - | - | ns |
| $\mathrm{T}_{\mathrm{L}_{-} \mathrm{MDC}}$ | MDC Low | - | 12 | - | - | ns |
| $\mathrm{T}_{\text {READ_DLY }}$ | Two MDC Period During Read Turnaround | - | 80 | - | - | ns |

1. $\mathrm{T}_{\mathrm{P} \text { _MDC }}$ is minimum of 25 ns for 40 MHz MDC clock support with stretched TA , but $40 \mathrm{~ns}(25 \mathrm{MHz})$ with standard TA as per IEEE specification. MDC of 40 MHz is supported only with VDDO supply of 1.8 V and above. For lower VDDO, MDC frequency of up to 25 MHz is supported.
2. The maximum MDC frequency is dependent on the Reference Clock used (CLK1P/N). The $T_{P \_M D C}$ listed is based on 156.25 MHz reference clock.

Figure 33: MDC/MDIO Management Interface


### 7.5.5 JTAG Timing

## Table 73: JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\text {P_TCK }}$ | TCK Period | - | 60 | - | - | ns |
| $\mathrm{T}_{\mathrm{H}+}$ TCK | TCK High | - | 12 | - | - | ns |
| TL_TCK | TCK Low | - | 12 | - | - | ns |
| TSU_TDI | TDI, TMS-to-TCK Setup Time | - | 10 | - | - | ns |
| $\mathrm{T}_{\text {HD_TDI }}$ | TDI, TMS-to-TCK Hold Time | - | 10 | - | - | ns |
| TDLY_TDO | TCK-to-TDO Delay | - | 0 | - | 15 | ns |

Figure 34: JTAG Timing


### 7.6 SERDES Electrical Specifications

### 7.6.1 Chip-to-Module 100 Gbps/25 Gbps Electrical Characteristics

### 7.6.1.1 Chip-to-Module 100 Gbps/25 Gbps Transmitter and Receiver Characteristics

Table 74: Chip-to-Module CAUI-4/XXVAUI-1 Transmitter and Receiver Characteristics

| Symbol | Description | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 25.78125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 38.787879 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 35 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 900 | mV | - |
| Tr | Output transition time | 10 | - | ps | 8 |
| Vosdc | DC Common-mode voltage limits | -0.3 | 2.8 | V | - |
| Vosac | AC Common-mode voltage limits (RMS) | - | 17.5 | mV | - |
| RLOD | Return loss differential output | - | - | dB | 2, 4 |
| RLOCD | Common to differential mode output return loss | See |  | dB | 3, 4 |
| Ehatx | Differential output eye height A | 95 | - | mV | 10 |
| Ehbtx | Differential output eye height B | 80 | - | mV | 10 |
| Ew tx | Differential output eye width | 0.46 | - | UI | 5,10 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 900 | mV | 7, 11 |
| RLID | Return loss differential input | See note \#2. |  | dB | 2, 4 |
| RLIDC | Differential to common mode input return loss | See note \#3. |  | dB | 3, 4 |
| Ehrx | Receiver stress tolerance -eye height | 228 | - | mV | 5, 6, 11 |
| Ew rx | Receiver stress tolerance -eye width | 0.57 | - | UI | 5, 6, 11 |

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The load is $100 \Omega$ differential for these parameters, unless otherwise specified. The Tx table is defined on TP1a and Rx table is defined on TP4a refer to 83E. 2 CAUI-4 chip-to-module compliance point definitions in the IEEE 802.3 standard.
Note - Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock(Oppmdelta).

- RLOD and RLID are defined accordingly: For $10 \mathrm{MHz}-8 \mathrm{GHz}$ RLOD/RLID>9.5-0.37*f [dB] (Frequency defined in GHz). For $8 \mathrm{GHz}-19 \mathrm{GHz}$ RLOD/RLID>4.75-7.4Log(f/14) [dB] (Frequency defined in GHz).
- RLOCD and RLID Care defined accordingly: For $10 \mathrm{MHz}-12.89 \mathrm{GHz}$ RLOCD/RLIDC>22-(20/25.78)*f [dB] (Frequency defined in GHz). For $12.89 \mathrm{GHz}-19$ GHz RLOCD/RLIDC>15-(6/25.78)*f [dB] (Frequency defined in GHz).
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode.
- Defined with a Bit Error Rate (BER) of 10^-15.
- Defined according to IEEE 802.3 section 83E.3.3.2 Host stressed input test.
- Vidpp refers to the peak-to-peak.
- Defined 20 to $80 \%$ of the signal. Refer to section 83E.3.1.5 Transition time in the IEEE 802.3 standard.
- Refer to section 83E.3.1.4 Differential termination mismatch in IEEE 802.3 standard.
- Refer to section 83E.3.1.6 Host output eye width and eye height in IEEE 802.3 standard. Defined on TP4 as defined in 83E. 2 CAUI-4 chip-to-module compliance point definitions in IEEE 802.3 standard.

Table 75: Chip-to-Module CAUI-4/XXVAUI-1 Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP=TBD and <br> PRE=TBD, and the maximum value is achieved with AMP=TBD and PRE=TBD. <br> Output amplitude and pre-emphasis are configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) <br> must not exceed 1.8V. |
| Vodpp | To achieve the specifications at Tp1a, the use of emphasis may be needed. |
| Output <br> Equalization | For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.1.2 Chip-to-Module CAUI-4/XXVAUI-1 Interface Transmitter Output Voltage Limits and Definitions

Figure 35: Chip-to-Module CAUI-4/XXVAUI-1 Interface Transmitter Output Voltage Limits and Definitions



Figure 36: Chip-to-Module CAUI-4/XXVAUI-1 Transmitter Output Differential Amplitude and Eye Opening


### 7.6.2 Chip-to-Chip 100 Gbps/25 Gbps (CAUI-4/XXVAUI-1) Electrical Characteristics

### 7.6.2.1 Chip-to-Chip 100 Gbps/25 Gbps (CAUI-4/XXVAUI-1) Transmitter and Receiver Characteristics

Table 76: Chip-to-Chip Gbps CAUI-4/XXVAUI-1 Interface Transmitter and Receiver Characteristics

| Symbol | Description | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 25.78125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 38.787879 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 30 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| Vf | Output waveform -Steady-state voltage | 0.4 | 0.6 | V | 12 |
| VIfpp | Output waveform -Linear fit pulse peak | 0.71 *Vf | - | V | 12 |
| Prec | Output waveform -Pre-cursor full-scale range | See note \#13. |  | - | 13 |
| Pstc | Output waveform - Post-cursor full-scale range | See note \#13. |  | - | 13 |
| Vsnr | Transmitter signal-to-noise-and-distortion ratio | 27 | - | dB | 14 |
| Vosdc | DC Common-mode voltage limits | 0.0 | 1.9 | V | - |
| Vosac | AC Common-mode voltage limits (RMS) | - | 12 | mV | - |
| RLOD | Return loss differential output | See note \#2. |  | dB | 2, 5 |
| RLOC | Return loss Common-Mode output | See note \#3. |  | dB | 3,5 |
| Juctx | Output jitter -Effective bounded uncorrelated, peak-to-peak | - | 0.1 | UI | 10 |
| Jeotx | Output Even-Odd jitter | - | 0.035 | UI | 11 |
| Jtpptx | Output jitter -Effective total uncorrelated, peak-to-peak | - | 0.26 | UI | 6, 9, 10 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 8 |
| RLID | Return loss differential input | See note \#2. |  | dB | 2,5 |
| RLIDC | Differential to common mode input return loss | See note \#4. |  | dB | 4, 5 |
| Rit | Receiver interference tolerance | See note \#7. |  | UI | 7 |

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The load is $100 \Omega$ differential for these parameters, unless otherwise specified. General Comment: The Tx table is defined on TP0a as defined in 93.8.1.1 Transmitter test fixture in IEEE 802.3 standard. General Comment: The Rx table is defined on TP5a as defined in Note 93.8.2.1 Receiver test fixture in 802.3 IEEE standard.

- Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- RLOD and RLID are defined accordingly: For $50 \mathrm{MHz}-6 \mathrm{GHz}$ RLOD/RLID>12.05-f [dB] (Frequency defined in GHz). For $6 \mathrm{GHz}-19 \mathrm{GHz}$ RLOD/RLID>6.5-0.075*f [dB] (Frequency defined in GHz ).
- RLOC is defined accordingly: For $50 \mathrm{MHz}-6 \mathrm{GHz}$ RLOC $>9.05-\mathrm{f}$ [dB] (Frequency defined in GHz ). For $6 \mathrm{GHz}-19 \mathrm{GHz}$ RLOC $>3.5-0.075^{\star f}$ [dB] (Frequency defined in GHz ).
- RLIDC is defined accordingly: For $50 \mathrm{MHz}-6.95 \mathrm{GHz}$ RLIDC>25-1.44*f [dB] (Frequency defined in GHz ). For $6.95 \mathrm{GHz}-19 \mathrm{GHz}$ RLIDC>15 [dB].
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode.
- Defined with a Bit Error Rate (BER) of 10^-15.
- Defined according to IEEE 802.3 section 83D.3.3.1 Receiver interference tolerance.
- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 10 MHz .
- The transmitter output waveform follows IEEE requirements as specified in section 92.8.3.8.2 Effective bounded uncorrelated jitter and effective random jitter, (except that the range for fitting CDFLi and CDFRi will be from10^-6 to 10^-4).
- Defined for a PRBS9 pattern according to section 92.8.3.8.1 Even-odd jitter in 802.3 IEEE standard.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.5.2 Steady-state voltage and linear fit pulse peak, (except that the values of Np and Nw are 5).
- The transmitter output waveform follows IEEE requirements as specified in section 83D.3.1.1 Transmitter equalization settings.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.6 Transmitter output noise and distortion (except that the values of Np and Nw are 5).

Table 77: Chip-to-Chip CAUI-4/XXVAUI-1 Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP=TBD and PRE=TBD, and the <br> maximum value is achieved with AMP $=$ TBD and PRE=TBD. Output amplitude and pre-emphasis are <br> configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> 1.8 V. |
| Vodpp | To achieve the specifications at Tp1a, the use of emphasis may be required. |

Table 77: Chip-to-Chip CAUI-4/XXVAUI-1 Settings and Configuration (Continued)

| Parameter | Setting/Configuration |
| :--- | :--- |
| Output <br> Equalization | For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.2.2 Chip-to-Chip CAUI-4IXXVAUI-1 Interface Transmitter Output Voltage Limits and Definitions

Figure 37: Chip-to-Chip CAUI-4/XXVAUI-1 Interface Transmitter Output Voltage Limits and Definitions



Figure 38: Chip-to-Chip CAUI-4/XXVAUI-1 Transmitter Output Differential Amplitude and Eye Opening


### 7.6.3 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Electrical Characteristics

### 7.6.3.1 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Interface Transmitter and Receiver Characteristics

Table 78: 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 25.78125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 38.787879 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 35 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| Vf | Output waveform - Steady-state voltage | 0.34 | 0.6 | V | 12 |
| VIfpp | Output waveform -Linear fit pulse peak | $0.45 * \mathrm{Vf}$ | - | V | 12 |
| Ncs | Output waveform - Normalized coefficient step size | 0.0083 | 0.05 | - | 13 |
| Prec | Output waveform - Pre-cursor full-scale range | 1.54 | - | - | 14 |
| Pstc | Output waveform - Post-cursor full-scale range | 4 | - | - | 14 |
| Vsnr | Transmitter signal-to-noise-and-distortion ratio | 26 | - | dB | 15 |
| Vosdc | DC Common-mode voltage limits | 0.0 | 1.9 | V | - |
| Vosac | AC Common-mode voltage limits (RMS) | - | 30 | mV | - |
| RLOD | Return loss differential output | See note \#2. |  | dB | 2, 5 |
| RLOCD | Return loss Common-Mode to Differential output | See note \#3. |  | dB | 3,5 |
| RLOC | Return loss Common-Mode output | 2 | - | dB | 5, 16 |
| Juctx | Output jitter -Effective bounded uncorrelated, peak-to-peak | - | 0.1 | UI | 17 |
| Jeotx | Output Even-Odd jitter | - | 0.035 | UI | 11 |
| Jtpptx | Output jitter - Effective total uncorrelated, peak-to-peak | - | 0.18 | UI | 6, 9, 17 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 8 |
| RLID | Return loss differential input | See note \#2. |  | dB | 2,5 |
| RLIDC | Differential to common mode input return loss | See note \#4. |  | dB | 4,5 |

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Table 78: 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Interface Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units |
| :--- | :--- | :--- | :--- | :--- |
| Notes |  |  |  |  |
| Rit | Receiver interference tolerance | See note \#7. | UI | 7 |
| Rjt | Receiver jitter tolerance | See note \#10. | UI | 6,10 |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified. General Comment: The Tx table is defined on TP2 as defined in 92.11 Test fixtures in 802.3 IEEE standard. General Comment: The Rx table is defined onTP3 as defined in 92.11 Test fixtures in 802.3 IEEE standard.

- Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- RLOD and RLID are defined accordingly: For $10 \mathrm{MHz}-8 \mathrm{GHz}$ RLOD/RLID>9.5-0.37*f [dB] (Frequency defined in GHz). For $8 \mathrm{GHz}-19 \mathrm{GHz}$ RLOD/RLID>4.75-7.4*Log(f/14) [dB] (Frequency defined in GHz).
- RLOCD and RLID Care defined accordingly: For $10 \mathrm{MHz}-12.89 \mathrm{GHz}$ RLOCD/RLIDC>22-(20/25.78)*f [dB] (Frequency defined in GHz). For 12.89 GHz -19 GHz RLOCD/RLIDC>15-(6/25.78)*f [dB] (Frequency defined in GHz).
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode.
- Defined with a Bit Error Rate (BER) of $10^{\wedge}-5$.
- Defined according to IEEE 802.3 section 92.8.4.4 Receiver interference tolerance test.
- Vidpp refers to the peak-to-peak. Defined according to IEEE 802.3 section 92.8.4.1 Receiver input amplitude tolerance.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 10 MHz .
- Defined according to IEEE802.3 section 92.8.4.5 Receiver jitter tolerance.
- Defined for a PRBS9 pattern according to section 92.8.3.8.1 Even-odd jitter in 802.3 IEEE standard.
- The transmitter output waveform follows IEEE requirements as specified in section 92.8.3.5.2 Steady-state voltage and linear fit pulse peak.
- The transmitter output waveform follows IEEE requirements as specified in section 92.8.3.5.4 Coefficient step size.
- The transmitter output waveform follows IEEE requirements as specified in section 92.8.3.5.5 Coefficient range.
- The transmitter output waveform follows IEEE requirements as specified in section 92.8.3.7 Transmitter output noise and distortion.
- Defined from 200 MHz to 19 GHz .
- The transmitter jitter follows IEEE requirements as specified in section 92.8.3.8.2 Effective bounded uncorrelated jitter and effective random jitter.

Table 79: 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP=TBD and PRE $=$ TBD, and the <br> maximum value is achieved with AMP $=$ TBD and PRE=TBD. Output amplitude and pre-emphasis are <br> configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> 1.8 V. |
| Vodpp | To achieve the specifications at Tp1a, the use of emphasis may be needed. |
| Output <br> Equalization | For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

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### 7.6.3.2 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Interface Transmitter Output Voltage Limits and Definitions

Figure 39: 100GBASE-CR4/50GBASE-CR2/25GBASE-CR Interface Transmitter Output Voltage Limits and Definitions



### 7.6.4 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Electrical Characteristics

### 7.6.4.1 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Interface Transmitter and Receiver Characteristics

Table 80: 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 25.78125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 38.787879 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 30 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| Vf | Output waveform - Steady-state voltage | 0.4 | 0.6 | V | 12 |
| VIfpp | Output waveform -Linear fit pulse peak | 0.71*Vf | - | V | 12 |
| Ncs | Output waveform - Normalized coefficient step size | 0.0083 | 0.05 | - | 13 |
| Prec | Output waveform - Pre-cursor full-scale range | 1.54 | - | - | 14 |
| Pstc | Output waveform - Post-cursor full-scale range | 4 | - | - | 14 |
| Vsnr | Transmitter signal-to-noise-and-distortion ratio | 27 | - | dB | 15 |
| Vosdc | DC Common-mode voltage limits | 0.0 | 1.9 | V | - |
| Vosac | AC Common-mode voltage limits (RMS) | - | 12 | mV | - |
| RLOD | Return loss differential output | See note \#2. |  | dB | 2, 5 |
| RLOC | Return loss Common-Mode output | See note \#3. |  | dB | 5,16 |
| Juctx | Output jitter - Effective bounded uncorrelated, peak-to-peak | - | 0.1 | UI | 17 |
| Jeotx | Output Even-Odd jitter | - | 0.035 | UI | 11 |
| Jtpptx | Output jitter - Effective total uncorrelated, peak-to-peak | - | 0.18 | UI | 6, 9, 17 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 8 |
| RLID | Return loss differential input | See note \#2. |  | dB | 2,5 |
| RLIDC | Differential to common mode input return loss | See note \#4. |  | dB | 4, 5 |

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Table 80: 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Interface Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units | Notes |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Rit | Receiver interference tolerance | See note \#7. | UI | 7 |  |
| Rjt | Receiver jitter tolerance | See note \#10. | UI | 6,10 |  |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified. General Comment: The Tx table is defined on TPOa as defined in 93.8.1.1 Transmitter test fixture in the IEEE 802.3 standard. General Comment: The Rx table is defined on TP5a as defined in 93.8.2.1 Receiver test Micmac in the IEEE 802.3 standard.

- Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- RLOD and RLID are defined accordingly: For $50 \mathrm{MHz}-6 \mathrm{GHz}$ RLOD/RLID>12.05-f [Frequency] (Frequency defined in GHz ). For $6 \mathrm{GHz}-19 \mathrm{GHz}$ RLOD/RLID>6.5-0.075*f [dB] (Frequency defined in GHz).
- RLOC is defined accordingly: For $50 \mathrm{MHz}-6 \mathrm{GHz}$ RLOC $>9.05-\mathrm{f}$ [dB] (Frequency defined in GHz ). For $6 \mathrm{GHz}-19 \mathrm{GHz}$ RLOC>3.5-0.075*f [dB] (Frequency defined in GHz).
- RLIDC is defined accordingly: For $50 \mathrm{MHz}-6.95 \mathrm{GHz}$ RLIDC>25-1.44*f [dB] (Frequency defined in GHz ). For $6.95 \mathrm{GHz}-19 \mathrm{GHz}$ RLIDC>15 [dB].
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode.
- Defined with a Bit Error Rate (BER) of 10^-5.
- Defined according to IEEE 802.3 section 93.8.2.3 Receiver interference tolerance.
- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 10 MHz .
- Defined according to IEEE 802.3 section 93.8.2.4 Receiver jitter tolerance
- Defined for a PRBS9 pattern according to section 92.8.3.8.1 Even-odd jitter in the IEEE 802.3 standard.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.5.2 Steady-state voltage and linear fit pulse peak.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.5.4 Coefficient step size.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.5.5 Coefficient range.
- The transmitter output waveform follows IEEE requirements as specified in section 93.8.1.6 Transmitter output noise and distortion.
- The transmitter output jitter follows IEEE requirements as specified.

Table 81: 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP = TBD and PRE $=$ TBD, and the <br> maximum value is achieved with AMP $=$ TBD and PRE $=$ TBD. Output amplitude and pre-emphasis are <br> configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> $1.8 V$. |
| Vodpp | To achieve the specifications at Tp1a, the use of emphasis may be needed. |
| Output <br> Equalization | For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

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### 7.6.4.2 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Interface Transmitter Output Voltage Limits and Definitions

Figure 40: 100GBASE-KR4/50GBASE-KR2/25GBASE-KR Interface Transmitter Output Voltage Limits and Definitions



### 7.6.5 $\quad 40$ Gbps Parallel Physical Interface (XLPPI) Electrical Characteristics

### 7.6.5.1 $\quad 40$ Gbps Parallel Physical Interface (XLPPI) Interface Transmitter and Receiver Characteristics

Table 82: XLPPI Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodpp | Output differential maximum peak-to-peak | 190 | 700 | mV | - |
| Vos | Single-ended output voltage | -0.3 | 1.9 | V | 11 |
| $\mathrm{Q}_{\text {SQ }}$ | Signal-to-noise-ratio | 45 | - | V/V | 14 |
| Tr/Tf | Output differential transition time | 28 | - | ps | 2, 11 |
| RLOD | Return loss differential output | See note \#3. |  |  | 3, 4,11 |
| RLOC | Return loss common mode output | See note \#3. |  |  | 3, 4, 11 |
| TIskew | Output lane-to-lane skew | - | 29 | ns | - |
| Tlskew v | Output lane-to-lane skew variation | - | 200 | ps | - |
| dZM | Termination mismatch | - | 5 | \% | 9, 11 |
| Vocmac | Output AC common mode voltage, RMS | - | 15 | mV | 11, 12 |
| Jddpw st | Output jitter - Data dependent pulse width shrinkage | - | 0.07 | UI | 11 |
| J2tx | Output 99\% jitter - J2, peak-to-peak | - | 0.17 | UI | 8,11 |
| J9tx | Output jitter - J9, peak-to-peak | - | 0.29 | UI | 8, 11 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.22 | UI | 5, 8, 11 |


| Receiver Parameters |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: | :---: |
| Vidpps | Input differential sensitivity | 300 | - | mV | $5,7,11$ |  |  |
| Vidpp | Input differential voltage $-850 \mathrm{mV} \mathrm{5,7.11}$ | - | 850 | mV | $5,7,11$ |  |  |
| RLID | Return loss differential input | See note \# 3. | dB | $3,4,11$ |  |  |  |
| RLICD | Reflected input common mode to differential conversion | 10 | - | dB | 10,11 |  |  |
| RIskew | Input lane-to-lane skew | - | 160 | ns | - |  |  |

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Table 82: XLPPI Interface Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units | Notes |
| :--- | :--- | :--- | :--- | :--- | :--- |
| RIskew v | Input lane-to-lane skew variation | - | 4 | ns | - |
| J2rx | Input 99\% jitter - J2, peak-to-peak | - | 0.42 | UI | 6,11 |
| J9rx | Input jitter - J9, peak-to-peak | - | 0.65 | UI | 11 |
| Jddpw sr | Input jitter - Data dependent pulse width shrinkage | - | 0.34 | UI | 11,13 |
| Vicmac | Input AC common mode voltage, RMS | - | 7.5 | mV | 11,12 |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified. The reference points are according to Figure 86-2 in the IEEE Std 802.3-2010.

- Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock (zero ppm delta).
- Defined from 20 to $80 \%$ of the signal's voltage levels when driving a pattern consisting of eight consecutive ones followed by an equal run of zeros with no equalization. Maximum transition time is limited by mask as defined in IEEE 802.3 section 86A.5.3.6 Eye mask for TP1a and TP4.
- RLOD/RLID are defined from:
- 10.0 MHz to 4.11 GHz RLOD/RLID>12-2(Frequency)^0.5 [dB] (Frequency defined in GHz ). For 4.11 GHz to 11.1 GHz RLOD/RLID>6.3-13log(Frequency/5.5)[dB] (Frequency defined in GHz ). RLOC is defined from:
- 10.0 MHz to 2.5 GHz RLOC>7-1.6*(Frequency) [dB] (Frequency defined in GHz ). For 2.5 GHz to 11.1 GHz RLOC $>3 \mathrm{~dB}$.
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Hit Ratio of $5^{*} 10^{\wedge}-5$.
- Defined with all but 1 percent of occurrences.
- Vidpps refers to the internal eye opening while Vidp prefers to the peak-to-peak.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the-jitter. The high-pass filter 3 dB point is located at 4 MHz .
- Defined at 1 MHz frequency. Defined according to section 86A.5.3.2 Termination mismatch in the IEEE Std 802.3-2010.
- Defined from 10 MHz to 11.1 GHz .
- Defined at reference points TP1A or TP4A. For maximal allowed interconnect characteristics between points TP0 and TP1A or pointsTP4A and TP5, refer to Section 86A.5.1.1.1 Reference insertion losses of HC Band MCB in IEEE Std 803.2-2010.
- The parameter at any time is the average of signal(+) and signal(-) at that time. This parameter is calculated by applying the histogram function over 1 UI to the common mode signal.
- Defined in coherence with Section 86A.5.3.4 Data Dependent Pulse Width Shrinkage in IEEE Std 803.2-2010.
- The Qdq ratio is defined under the restrictions of the eye mask as defined in IEEE 802.3 section 86A.5.3.6 Eye mask for TP1a and TP4.

Table 83: XLPPI Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP=TBD and PRE=TBD, and the <br> maximum value is achieved with AMP=TBD and PRE=TBD. Output amplitude and pre-emphasis are <br> configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> 1.8 V. |
| Vodpp | To achieve the specifications at P1a, the use of emphasis may be needed. |
| Output <br> Equalization | Tx emphasis may be configured to achieve the required deterministic jitter at the module connector. <br> For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.5.2 XLPPI Interface Transmitter Output Voltage Limits and Definitions

Figure 41: XLPPI Interface Transmitter Output Voltage Limits and Definitions



Figure 42: XLPPI Transmitter Output Differential Amplitude and Eye Opening


### 7.6.6 $\quad 40$ Gbps Attachment Unit Interface (XLAUI) Electrical Characteristics

### 7.6.6.1 $\quad 40$ Gbps Attachment Unit Interface (XLAUI) Interface Transmitter and Receiver Characteristics

Table 84: XLAUI Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter parameters |  |  |  |  |  |
| Vodpp | Output differential peak-to-peak | 400 | 760 | mV | 9 |
| Vos | Single-ended output voltage | -0.4 | 1.9 | V | - |
| DEtx | Output de-emphasis | 4.4 | 7 | dB | - |
| Tr/Tf | Output differential transition time | 24 | - | ps | 2 |
| RLOD | Return loss differential output | 12 | - | dB | 3,4 |
| RLOC | Return loss common mode output | 9 | - | dB | 3,4 |
| Tlskew | Output lane-to-lane skew | - | 28 | ns | - |
| Tlskew v | Output lane-to-lane skew variation | - | 200 | ps | - |
| dZM | Termination mismatch | - | 5 | \% | 10 |
| Vocmac | Output AC common mode voltage | - | 15 | mVRMS | - |
| Jdtx | Output jitter - Deterministic, peak-to-peak | - | 0.17 | UI | - |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.32 | UI | 5, 8 |
| Evodpp | Output eye width at Vodpp (min) | 0.24 | - | UI | - |
|  | Receive |  |  |  |  |
| Vidpps | Input differential sensitivity | 85 | - | mV | 7 |
| Vidpp | Input differential voltage | - | 850 | mV | 7 |
| RLID | Return loss differential input | 12 | - | dB | 3, 4 |
| RLICD | Return loss common to differential input | 15 | - | dB | 11 |
| RIskew | Input lane-to-lane skew | - | 161 | ns | - |
| RIskew v | Input lane-to-lane skew variation | - | 3.8 | ns | - |
| Jtrisx | Input jitter - Sinusoidal, low frequency | - | 5 | UI | 12 |

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Table 84: XLAUI Interface Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units | Notes |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Jtrsx | Input jitter - Sinusoidal, high frequency | - | 0.05 | UI | 13 |
| Jdrx | Input jitter - Deterministic, peak-to-peak | - | 0.42 | UI | - |
| Jtpprx | Input jitter - Total, peak-to-peak | - | 0.62 | UI | 5,6 |
| Vicmac | Input AC common mode voltage | - | 20 | mVRMS | - |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- Defines the allowable reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- Defined from 20 to $80 \%$ of the signal's voltage levels when driving a pattern consisting of eight consecutive ones followed by an equal run of zeros with no equalization. Max transition time is limited by mask as defined in IEEE 802.3 section 83A.3.3.5 Transmitter eye mask and transmitter jitter definition.
- Defined from 10 MHz to 2.125 GHz . For $2.125 \mathrm{GHz}-11.1 \mathrm{GHz}$ RLOD/RLID>6.5-13.33log(Frequency/5.5)[dB] (Frequency defined in GHz). For 2.125 GHz-7.1 GHz RLOC>3.5-13.33log(Frequency/5.5)[dB] (Frequency defined in $\mathrm{GHz})$. For $7.1 \mathrm{GHz}-11.1 \mathrm{GHz}$ RLOC>2[dB].
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- This parameter does not include sinusoidal components.
- Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- Defined with emphasis disabled.
- Defined at 1 MHz frequency. Defined according to section 86A.5.3.2 Termination mismatch in IEEE Std 802.3ba.
- Defined from 10 MHz to 11.1 GHz .
- Defined below 40 kHz .
- Defined from 4 MHz to 20 MHz .

Table 85: XLAUI Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Vods | The Vods is the output differential amplitude configurable range. <br> When driving a test load, the minimum value is achieved with AMP=TBD and PRE=TBD, and the <br> maximum value is achieved with AMP $=$ TBD and PRE=TBD. Output amplitude and pre-emphasis are <br> configurable. |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> $1.8 V$. |
| Output <br> Equalization | Tx emphasis may be configured to achieve the required deterministic jitter at the module connector. <br> For emphasis control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.6.2 XLAUI Interface Transmitter Output Voltage Limits and Definitions

Figure 43: XLAUI Interface Transmitter Output Voltage Limits and Definitions


Figure 44: XLAUI Transmitter Output Differential Amplitude and Eye Opening


### 7.6.7 40GBASE-CR4 Electrical Characteristics

### 7.6.7.1 40GBASE-CR4 Interface Transmitter and Receiver Characteristics

Table 86: 40GBASE-CR4 Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 30 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| DEtx | Output de-emphasis | See note 12. |  | - | 12 |
| Vos | Common-mode voltage limits | 0.0 | 1.9 | V | - |
| RLOD | Return loss differential output | 10 | - | dB | 2, 3 |
| Tlskew | Output lane-to-lane skew | - | 54 | ns | - |
| Tlskew v | Output lane-to-lane skew variation | - | 600 | ps | - |
| Jdtx | Output jitter - Deterministic, peak-to-peak | - | 0.15 | UI | - |
| Jdcdtx | Output duty cycle distortion | - | 0.035 | UI | 9, 10 |
| Jrndtx | Output jitter - Random | - | 0.15 | UI | 4 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.28 | UI | 4, 7, 11 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 6 |
| RLID | Return loss differential input | 10 | - | dB | 2, 3 |
| RLIDC | Differential to common mode input return loss | 10 | - | dB | 13 |
| RIskew | Input lane-to-lane skew | - | 134 | ns | - |
| Rlskew v | Input lane-to-lane skew variation | - | 3.4 | ns | - |
| Js | Input sinusoidal jitter | - | 0.115 | UI | 5 |
| Jrndrx | Input random jitter | - | 0.13 | UI | 4, 5 |
| Jdcd | Input duty cycle distortion | - | 0.035 | UI | 5 |
| Vinamp | Calibrated far-end crosstalk | - | 6.3 | mVRMS | 5, 8 |
| ICN | Calibrated integrated crosstalk noise | - | 3.7 | mVRMS | 5 |

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The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- Defines the allow able reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock (zero ppm delta).
- Defined from 50 MHz to 2.5 GHz .

For $2.5 \mathrm{GHz}-7.5 \mathrm{GHz}$ RLOD>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz ).
For 2.5 GHz -7.5 GHz RLID>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz ).

- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- Defined for interference tests according IEEE 802.3 section 85.8.4.2 Receiver interference tolerance test.
- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined $w$ hen applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- The receiver tolerates noise at an amplitude specified under receiver interference tolerance test1.
The value for test2 is 2.2 mV .
- Jdcdtx is included as a part of Jdtx.
- Defined for a 1010 pattern and includes the entire range of emphasis.
- The jitter is defined with emphasis off.
- The transmitter output waveform follow s IEEE requirements as specified in section 85.8.3.3 Transmitter output waveform.
- Defined from 10 MHz to 10 GHz .

Table 87: 40GBASE-CR4 Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> 1.8 V. |
| Output <br> Equalization | The default as determined by the IEEE is 3 TAP FIR optimized per interconnect. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.7.2 40GBASE-CR4 Interface Transmitter Output Voltage Limits and Definitions

Figure 45: 40GBASE-CR4Interface Transmitter Output Voltage Limits and Definitions


Figure 46: 40GBASE-CR4Transmitter Output Differential Amplitude and Eye Opening


### 7.6.8 40GBASE-KR4 Electrical Characteristics

### 7.6.8.1 40GBASE-KR4 Interface Transmitter and Receiver Characteristics

Table 88: 40GBASE-KR4 Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval |  | 69697 | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 30 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| Vos | Common-mode voltage limits | 0 | 1.9 | V | - |
| Tr/Tf | Output differential transition time | 24 | 47 | ps | 10 |
| RLOD | Return loss differential output | 9 | - | dB | 2, 3 |
| RLOC | Return loss common mode output | 6 | - | dB | 2, 3 |
| Tlskew | Output lane-to-lane skew | - | 557 | UI | - |
| TIskew v | Output lane-to-lane skew variation | - | 6 | UI | - |
| Jdtx | Output jitter - Deterministic, peak-to-peak | - | 0.15 | UI | - |
| Jdcdtx | Output duty cycle distortion | - | 0.035 | UI | 10, 11 |
| Jrndtx | Output jitter - Random | - | 0.15 | UI | 4 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.28 | UI | 4, 7 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 6 |
| RLID | Return loss differential input | 9 | - | dB | 2, 3 |
| Rlskew | Input lane-to-lane skew | - | 1382 | UI | - |
| RIskew v | Input lane-to-lane skew variation | - | 35 | UI | - |
| Js | Input sinusoidal jitter | - | 0.115 | UI | 5 |
| Jrndrx | Input random jitter | - | 0.13 | UI | 4, 5 |
| Jdcd | Input duty cycle distortion | - | 0.035 | UI | 5 |
| Vinamp | Input broadband noise amplitude | - | 5.2 | mVRMS | 5, 9 |

## Table 88: 40GBASE-KR4 Interface Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units | Notes |
| :--- | :--- | :--- | :--- | :--- | :--- |
| mTC | Test Channel Magnitude factor |  | 1 | - | 5,8 |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- Defines the allow able reference clock difference and Rx baud rate tolerance relative to nominal.
Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- Defined from 50 MHz to 2.5 GHz .

For $2.5 \mathrm{GHz}-7.5 \mathrm{GHz}$ RLOD>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz ).

For 2.5 GHz -7.5 GHz RLOC>6-12log(Frequency/2.5)[dB] (Frequency defined in GHz ).
For 2.5 GHz -7.5 GHz RLID>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz ).

- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- Defined for interference tests according IEEE 802.3 Annex 69A.

For informative interconnect characteristics, refer to IEEE 802.3 Annex 69B.

- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined w hen applying the effect of a single-pole high-pass filter on the jitter.
The high-pass filter 3 dB point is located at 4 MHz .
- mTC describes the insertion loss transmission magnitude relative to the maximal allowed fitted attenuation mask Amax over a predefined frequency range.
Defined for test1. The value for test2 is 0.5 .
- The receiver tolerates noise at an amplitude specified under receiver interference tolerance test1. The value for test2 is 12 mV .
- Jdcdtx is included as a part of Jdtx.
- Defined for a 1010 pattern and includes the entire range of emphasis.
- The transmitter output waveform follow s IEEE requirements as specified in section 72.7.1.10 Transmitter output waveform requirements.

Table 89: 40GBASE-KR4 Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) <br> must not exceed 1.8 V. |

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Table 89: 40GBASE-KR4 Settings and Configuration (Continued)

| Parameter | Setting/Configuration |
| :--- | :--- |
| Output <br> Equalization | The default as determined by the IEEE is 3 TAP FIR optimized per interconnect. |
| NOTE: For further information, refer to the Functional Specifications. |  |

### 7.6.8.2 40GBASE-KR4 Interface Transmitter Output Voltage Limits and Definitions

Figure 47: 40GBASE-KR4 Interface Transmitter Output Voltage Limits and Definitions



Figure 48: 40GBASE-KR4 Transmitter Output Differential Amplitude and Eye Opening


### 7.6.9 SFP+ Interface (SFI) Limiting Module Electrical Characteristics

### 7.6.9.1 SFI Transmitter and Receiver Characteristics

## Table 90: SFI Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval |  | 6969 | ps | - |
| Transmitter parameters |  |  |  |  |  |
| Vodpp | Output differential peak-to-peak | 190 | 700 | mV | 9,14,7 |
| Vos | Single-ended output voltage | -0.3 | 1.9 | V | 13 |
| DEtx | Output de-emphasis | 4.4 | 7 | dB | 13 |
| Tr/Tf | Output differential transition time | 24 | - | ps | 2, 13 |
| RLOD | Return loss differential output | 12 | - | dB | 3,4,13 |
| RLOC | Return loss common mode output | 9 | - | dB | 3,4,13 |
| dZM | Termination mismatch | - | 5 | \% | 10,13 |
| Vocmac | Output AC common mode voltage | - | 12 | mVRMS | 13,15 |
| Jutx | Output jitter - Uncorrelated, RMS | - | 0.023 | UI | 5,14,12 |
| Jddpw st | Output jitter - Data dependent pulse width shrinkage | - | 0.055 | UI | 14 |
| Jddtx | Output jitter - Data dependent, peak-to-peak | - | 0.1 | UI | 14 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.28 | UI | 8,14,17 |
| Receiver parameters |  |  |  |  |  |
| Vidpps | Input differential sensitivity | 300 | - | mV | 7,14 |
| Vidpp | Input differential voltage | - | 850 | mV | 7,14 |
| RLID | Return loss differential input | 12 | - | dB | 3,4,13 |
| RLICD | Reflected input common mode to differential conversion | 15 | - | -dB | 11,13 |
| J2 | Input 99\% jitter - peak-to-peak | - | 0.42 | UI | 6,14,16 |
| Jddpw sr | Input jitter - Data dependent pulse width shrinkage | - | 0.3 | UI | 14, 16 |
| Jtpprx | Input jitter - Total, peak-to-peak | - | 0.7 | UI | 5,14,16 |
| Vicmac | Input AC common mode voltage, RMS | - | 7.5 | mVRMS | 14,15,16 |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.
The reference points are according to Table 10 SFI Reference Points in SFF 8431 Rev. 4.1 standard.
Note - Defines the allow able reference clock difference and $R x$ baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock (zero ppm delta).

- Defined from 20 to $80 \%$ of the signal's voltage levels $w$ hen driving a pattern consisting of 8 consecutive ones follow ed by an equal run of zeros with no equalization. Max transition time is limited by mask as defined in SFF 8431 Rev. 4.1 standard. Figure 19 Transmitter Differential Output Compliance Mask at B and B .
- RLOD/RLID are defined from 10 MHz to 2.8 GHz .
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- Defines with all but 1 percent of occurrences.
- Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined w hen applying the effect of a single-pole, high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- Defined with emphasis disabled.
- Defined at 1 MHz frequency. Defined according to section D. 16 Termination Mismatch in SFF 8431 Rev. 4.1 standard.
- Defined from 10 MHz to 11.1 GHz .
- Jutx includes random jitter.
- Defined at reference points A or D .
- Defined at reference points $B$ or $C$. For maximal allow ed interconnect characteristics between points A and B or points C and D, refer to Appendix A SFI Channel Recommendation in SFF 8431 Rev. 4.1 standard.
- The parameter at any time is the average of signal(+) and signal(-) at that time. This parameter is calculated by applying the histogram function over one UI to the common mode signal.
- Defined in coherence with Table 14 Host receiver supporting limiting module input in SFF-8431 Rev4.1 standard.
- Defined with a Hit Ratio of $5^{*} 10^{\wedge}-5$.

Table 91: SFI Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> $1.8 V$. |
| Output <br> Equalization | De-emphasis to be set to minimize data dependent jitter at compliance point B. For compliance point <br> definition refer to chapter 3.3 SFI Test Points Definition and Measurements in the SFF-8431 standard. |
| NOTE: For further information, refer to the Functional Specifications. |  |

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### 7.6.9.2 SFP+ Direct Attach Cable (10GSFP+CU Appendix E) Transmitter and Receiver Characteristics

Table 92: 10GSFP+CU Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodpp | Output differential peak-to-peak | 190 | 700 | mV | 9,14,17 |
| VMAT | Output voltage modulation amplitude peak-to-peak | 300 | - | mV | 6, 14 |
| Vos | Single-ended output voltage | -0.3 | 1.9 | V | 13 |
| Qsq | Signal to noise ratio quality | 63 | - | - | 14, 18 |
| DEtx | Output de-emphasis | 4.4 | 7 | dB | 13 |
| Tr/Tf | Output differential transition time | 24 | - | ps | 2, 13 |
| RLOD | Return loss differential output | 12 | - | dB | 3, 4, 13 |
| RLOC | Return loss common mode output | 9 | - | dB | 3, 4,13 |
| dZM | Termination mismatch | - | 5 | \% | 10, 13 |
| Vocmac | Output AC common mode voltage | - | 12 | mVRMS | 13, 15 |
| TWDPc | Copper cable stressor transmitter penalty | - | 10.7 | dBe | 14, 19 |
| Jutx | Output jitter - Uncorrelated, RMS | - | 0.023 | UI | 5, 14, 12 |
| Jddpw st | Output jitter - Data dependent pulse width shrinkage | - | 0.055 | UI | 14 |
| Jddtx | Output jitter - Data dependent, peak-to-peak | - | 0.1 | UI | 14 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.28 | UI | 8, 4, 17 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 850 | mV | 7, 14 |
| VMAR | Input voltage modulation amplitude peak-to-peak | 180 | - | mV | 6, 14 |
| RLID | Return loss differential input | 12 | - | dB | 3, 4, 13 |
| RLICD | Reflected input common mode to differential conversion | 15 | - | dB | 11, 13 |
| WDPc | Waveform distortion penalty of the ISI generator | - | 9.3 | dBe | 14, 19 |
| Vinamp | Input broadband noise amplitude | - | 2.14 | mVRMS | 14, 20 |

Table 92: 10GSFP+CU Transmitter and Receiver Characteristics (Continued)

| Symbol | Parameter | Min | Max | Units | Notes |
| :--- | :--- | :--- | :---: | :--- | :--- |
| Vicmac | Input AC common mode voltage, RMS | - | 13.5 | mVRMS | $14,15,16$ |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- The reference points are according to Table 10 SFI Reference Points in SFF 8431 Rev. 4.1 standard.
- Defines the allow able reference clock difference and $R x$ baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock (zero ppm delta).
- Defined from 20 to $80 \%$ of the signal's voltage levels $w$ hen driving a pattern consisting of 8 consecutive ones follow ed by an equal run of zeros with no equalization. Max transition time is limited by mask as defined in SFF 8431 Rev. 4.1 standard. Figure 19 Transmitter Differential Output Compliance Mask at B and B.
- RLOD/RLID are defined from 10 MHz to 2.8 GHz .
- For $2.8 \mathrm{GHz}-11.1 \mathrm{GHz}$ RLOD/RLID>8.15-13.33log(Frequency/5.5)[dB] (Frequency defined in GHz ). RLOC is defined from 10.0 MHz to 4.74 GHz . For $4.74 \mathrm{GHz}-7.1 \mathrm{GHz}$ RLOC>8.1-13.33log(Frequency/5.5)[dB] (Frequency defined in GHz).
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- For test definition refer to section D. 7 Voltage Modulation Amplitude (VMA) in SFF 8431 Rev. 4.1 standard.
- Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined w hen applying the effect of a single-pole, high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- Defined with emphasis disabled.
- Defined at 1 MHz frequency. Defined according to section D. 16 Termination Mismatch in SFF 8431 Rev. 4.1 standard.
- Defined from 10 MHz to 11.1 GHz .
- Jutx includes random jitter.
- Defined at reference points A or D.
- Defined at reference points $B$ or $C$. For maximal allowed interconnect characteristics between points $A$ and $B$ or points $C$ and D, refer to Appendix A SFI Channel Recommendation in SFF 8431 Rev. 4.1 standard.
- The parameter at any time is the average of signal(+) and signal(-) at that time. This parameter is calculated by applying the histogram function over one UI to the common mode signal.
- Defined in coherence with Table 14 Host receiver supporting limiting module input in SFF-8431 Rev4.1 standard.
- Defined with a Hit Ratio of $5^{*} 10^{\wedge}-5$.
- $\quad$ Qsq $=1 / R N$. For test definition of RN refer to section D. 8 Relative noise (RN) in SFF 8431 Rev. 4.1 standard.
- For calculation, refer to Appendix G Mat-lab code for TWDP in SFF 8431 Rev. 4.1 standard.
- Defined for interference tests according to D. 11 Test Method For A Host Receiver For A Limiting Module in SFF 8431 Rev. 4.1 standard.

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Table 93: 10GSFP+CU Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed <br> 1.8 V. |
| Output <br> Equalization | The default as determined by the IEEE is 3 TAP FIR optimized per interconnect. |
| NOTE: For further information, refer to the Functional Specifications. |  |

Figure 49: SFI Transmitter Output Voltage Limits and Definitions



Figure 50: SFI Transmitter Output Differential Amplitude and Eye Opening

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### 7.6.10 $\quad 10$ Gigabit Small Form Factor Pluggable Interface (XFI) Electrical Characteristics

### 7.6.10.1 XFI Interface Transmitter and Receiver Characteristics

Table 94: XFI Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Zod | Reference output differential impedance | 100 |  | $\Omega$ | 1 |
| dRom | Termination output mismatch | - | 5 | \% | 1 |
| Vcm | DC Common Mode Voltage | 0 | 1.9 | V | - |
| tRH/tFH | Output rise and fall time | 24 | - | ps | 2 |
| Vocm | Output AC common mode voltage - 15 mV (RMS) 1,7 | - | 15 | mVRMS | 1,7 |
| SDD22 |  | 20 | - | dB | 3 |
|  | Differential output return loss | 10 | - | dB | 4 |
|  |  | See note \#5. |  | dB | 5,12 |
| SCC22 | Common mode output return loss | 6 | - | dB | 6, 12 |
| Txjit | Transmitter output jitter specifications | See note \# 7 . |  | - | 1,7 |
| Receiver Parameters |  |  |  |  |  |
| Zid | Reference input differential impedance | 100 |  | $\Omega$ | 1 |
| dRim | Termination input mismatch | - | 5 | \% | 1 |
| Vicm | Input AC common mode voltage | - | 25 | mVRMS | 1 |
| SDD22 |  | 20 | - | dB | 3 |
|  | Differential output return loss | 10 | - | dB | 4 |
|  |  | See note \#5. |  | dB | 5, 12 |
| SCC11 | Common mode input return loss | 6 | - | dB | 9,10,12 |
| SCD11 | Differential to common mode input conversion | 12 | - | dB | 9 |
| Rxjit | Receiver input jitter specifications | See noter | 11. | - | 1, 11 |

## Electrical Specifications SERDES Electrical Specifications

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- Defines the allow able reference clock difference and $R x$ baud rate tolerance relative to nominal.

Note

- Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- Defined from 50.0 MHz to 2.5 GHz .
- For $2.5 \mathrm{GHz}-7.5 \mathrm{GHz}$ RLOD>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz).
- For $2.5 \mathrm{GHz}-7.5 \mathrm{GHz}$ RLID>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz).
- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.

■ Defined for compliant transmitter and interference tests according to IEEE 802.3 section 85.8.4.2 Receiver interference tolerance test.

- Defined with a cable interconnect $4.6<$ WDPC $<4.8$ that complies with interconnect parameters definition.
- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined w hen applying the effect of a single-pole, high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- As calculated using code in Appendix G Matlab Code For TWDP in SFF-8431 version 4.1 standard.
- The parameter value includes the module compliance boards.
- Jdcdtx is included as a part of Jdtx.
- Defined for a 1010 pattern and includes the entire range of emphasis.
- The jitter is defined with emphasis off.
- Transmitter output waveform follow s IEEE requirements as specified in IEEE Std 802.3-2008 section 72.7.1.11 Transmitter output waveform requirements.
- Defined from 10 MHz to 10 GHz
- As defined in D. 7 Voltage Modulation Amplitude in SFF-8431 version 4.1 standard.
- Defined between host device pins (with host device removed) and Host Compliance Board (HCB) SMAs.
- Defined from 10.0 MHz to 5 GHz .

For $5 \mathrm{GHz}-11.1 \mathrm{GHz}$ HBRL>23.25-8.75log(Frequency/5)[dB] (Frequency defined in GHz).
■ Defined for a 1010 pattern according to IEEE Std 802.3-2008 section 72.6.10.4.2 Training.

- The interconnect parameters are defined with compliant transmitter as defined in Transmitter Parameters section.
- This value is applied for Vamp (min).


### 7.6.11 10GBASE-KR Electrical Characteristics

### 7.6.11.1 10GBASE-KR Interface Transmitter and Receiver Characteristics

Table 95: 10GBASE-KR Interface Transmitter and Receiver Characteristics

| Symbol | Parameter | Min | Max | Units | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BR | Baud rate | 10.3125 |  | Gbps | - |
| Bppm | Baud rate tolerance | -100 | 100 | ppm | 1 |
| UI | Unit interval | 96.969697 |  | ps | - |
| Transmitter Parameters |  |  |  |  |  |
| Vodis | Transmitter disabled output differential noise level | - | 30 | mV | - |
| Vodpp | Output differential maximum peak-to-peak | - | 1200 | mV | - |
| Vos | Common-mode voltage limits | 0 | 1.9 | V | - |
| Tr/Tf | Output differential transition time | 24 | 47 | ps | 10 |
| RLOD | Return loss differential output | 9 | - | dB | 2, 3 |
| RLOC | Return loss common mode output | 6 | - | dB | 2, 3 |
| Jdtx | Output jitter - Deterministic, peak-to-peak | - | 0.15 | UI | - |
| Jdcdtx | Output duty cycle distortion | - | 0.035 | UI | 10, 11 |
| Jrndtx | Output jitter - Random | - | 0.15 | UI | 4 |
| Jtpptx | Output jitter - Total, peak-to-peak | - | 0.28 | UI | 4, 7 |
| Receiver Parameters |  |  |  |  |  |
| Vidpp | Input differential voltage | - | 1200 | mV | 6 |
| RLID | Return loss differential input | 9 | - | dB | 2, 3 |
| Js | Input sinusoidal jitter | - | 0.15 | UI | 5 |
| Jrndrx | Input random jitter | - | 0.13 | UI | 4,5 |
| Jdcd | Input duty cycle distortion | - | 0.035 | UI | 5 |
| Vinamp | Input broadband noise amplitude | - | 5.2 | mVRMS | 5,9 |
| mTC | Test channel magnitude factor | 1 | - | - | 5, 8 |

The load is $100 \Omega$ differential for these parameters, unless otherwise specified.

- Defines the allow able reference clock difference and Rx baud rate tolerance relative to nominal. Tx baud rate is derived from multiplication of the reference clock ( 0 ppm delta).
- Defined from 50 MHz to 2.5 GHz .

For 2.5 GHz -7.5 GHz RLOD>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz).
For $2.5 \mathrm{GHz}-7.5 \mathrm{GHz}$ RLOC>6-12log(Frequency/2.5)[dB] (Frequency defined in GHz).
For 2.5 GHz -7.5 GHz RLID>9-12log(Frequency/2.5)[dB] (Frequency defined in GHz).

- Relative to $100 \Omega$ differential and $25 \Omega$ common mode. Return loss includes contributions from on-chip circuitry, chip packaging, and off-chip optimized components related to the transmitter/receiver breakout.
- Defined with a Bit Error Rate (BER) of 10^-12.
- Defined for interference tests according IEEE 802.3 Annex 69A. For informative interconnect characteristics, refer to IEEE 802.3 Annex 69B.
- Vidpp refers to the peak-to-peak.
- The output Tx jitter is defined when applying the effect of a single-pole high-pass filter on the jitter. The high-pass filter 3 dB point is located at 4 MHz .
- mTC describes the insertion loss transmission magnitude relative to the maximal allowed fitted attenuation mask Amax over a predefined frequency range. Defined for test1. The value for test2 is 0.5 .
- The receiver tolerates noise at an amplitude specified under receiver interference tolerance test1.The value for test2 is 12 mV .
- Jdcdtx is included as a part of Jdtx.
- Defined for a 1010 pattern and includes the entire range of emphasis.
- The transmitter output waveform follows IEEE requirements as specified in section 72.7.1.10 Transmitter output waveform requirements.

Table 96: 10GBASE-KR Settings and Configuration

| Parameter | Setting/Configuration |
| :--- | :--- |
| Viddp | The Viddp is the input differential voltage. <br> The maximum single-ended voltage (common mode voltage and swing voltage) <br> must not exceed 1.8V. |
| Output <br> Equalization | The default as determined by the IEEE is 3 TAP FIR optimized per interconnect. <br> 3 TAP FIR capabilities comply with the IEEE 802.3 standard section 72.7.1.10 <br> Transmitter Output Waveform. <br> For FIR control information, refer to the Functional Specifications. |
| NOTE: For further information, refer to the Functional Specifications. |  |

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### 7.6.11.2 10GBASE-KR Interface Transmitter Output Voltage Limits and Definitions

Figure 51: 10GBASE-KR Interface Transmitter Output Voltage Limits and Definitions


Figure 52: 10GBASE-KR Transmitter Output Differential Amplitude and Eye Opening


### 7.7 Reference Clock

Table 97: Reference Clock
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{F}_{\text {CLK }}$ | Clock Frequency $^{1}$ |  | -100 ppm | 156.25 | +100 ppm | MHz |
| $\mathrm{T}_{\mathrm{R},} \mathrm{T}_{\mathrm{F}}$ | Rise and Fall Times | 20 to $80 \%$ of $\mathrm{V}_{\text {PPD }}$ | - | 0.5 | 0.8 | ns |
| $\mathrm{~V}_{\text {PPD }}$ | Peak-to-Peak Differential <br> Voltage |  | 0.4 | 0.8 | 1.2 | V |
| $\mathrm{Z}_{\text {IND }}$ | Input Impedance | Differential | 80 | 100 | 120 | $\Omega$ |
| $\mathrm{Z}_{\text {INC }}$ | Input Impedance | Common Mode | - | 100 K | - | $\Omega$ |
| $\mathrm{T}_{\text {DUTY }}$ | Duty Cycle |  | Integrated from <br> 12 KHz to $20 \mathrm{MHz}^{2}$ | - | 0.17 | 0.5 |
| $\mathrm{~J}_{\text {RMS }}$ | RMS Jitter |  |  | 50 | ps |  |

1. CLKP/N must have an external AC-counlina canacitor.
2. Specification assumes that there are no spurs in the phase noise plot.

Figure 53: Reference Clock Input Waveform


## 7.8 Output 25 MHz Clock

Table 98: Output 25 MHz Clock
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{F}_{\text {CLK }}$ | Clock Frequency | - | - | 25 | - | MHz |
| JRMS | RMS Jitter | - | - | 500 | - | $\mathrm{ps}, \mathrm{rms}$ |
| $\mathrm{V}_{\text {DIFF }}$ | Differential Amplitude <br> Peak-to-Peak | - | 760 | 780 | 800 | mV |
| $\mathrm{T}_{\mathrm{R}} / \mathrm{T}_{\mathrm{F}}$ | Rise/Fall Time | $2 \mathrm{pF}, 50 \Omega$ <br> termination/load | 100 | 115 | 130 | ps |

### 7.9 Latency

The transmit latency is measured from the input of the PPM FIFO to the SERDES transmit pin.
The receive latency is measured from the SERDES receive pin to the input of the PPM FIFO.
The total latency in each direction is the sum of receive and transmit latency in the path.

Table 99: Chip Pin-to-pin Latency ( $\mathrm{Rx}+\mathrm{Tx}$ )

| Parameter | Latency Variation | (Dynamic) <br> Latency Jitter | Min | Typ | Max |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1G PCS (1 lane) | - | - | - | 194.96 | - |
| 2.5G PCS (1 lane) | - | - | - | 74.95 | - |
| 5G PCS (1 lane) | - | - | - | 313.36 | - |
| 10G PCS - No FEC (1 lane) | - | _ | - | 144.52 | - |
| 10G PCS - KR FEC (1 lane) | - | - | - | 434.07 | - |
| 25G PCS - No FEC (1 lane) | 22 | 3.8 | 57 | 70 | 79 |
| 25G PCS - KR FEC (1 lane) | 22 | 3.8 | 172 | 186 | 194 |
| 25G PCS - RS FEC (1 lane) | 46 | 24.3 | 456 | 484.6 | 502 |
| 40G PCS - No FEC (4 lane) | 33 | 17.6 | 167 | 180 | 200 |
| 40G PCS - KR FEC (4 lane) | 32 | 17.6 | 455 | 468 | 487 |
| 50G PCS - No FEC (4 lane) | 0 | 14.08 | - | 143.6 | - |
| 50G PCS - KR FEC (4 lane) | 0 | 14.08 | - | 374.5 | - |
| 50G PCS - No FEC (2 lane) | 0 | 14.08 | - | 139.89 | - |
| 50G PCS - KR FEC (2 lane) | 0 | 14.08 | - | 372.02 | - |
| 50G PCS - RS FEC (2 lane) | 0 | 14.08 | - | 360.85 | - |
| 100G PCS - No FEC (4 lane) | 39 | 4.5 | 134 | 151 | 173 |
| 100G PCS - RS FEC (4 lane) | 44 | 4.5 | 215 | 246 | 259 |

## 8 <br> Mechanical Drawings

### 8.1 Package Mechanical Drawings

Figure 54: 169-pin FCBGA $14 \times 14$ Package Mechanical Drawings - Top and Side View



DETAIL A'

Figure 55: 169-pin FCBGA $14 \times 14$ Package Mechanical Drawings - Bottom View


$$
\underline{\underline{\text { DETAIL B' }}}
$$

Table 100: 169-pin FCBGA (14 mm $\times 14 \mathrm{~mm}$ ) Package Dimensions

|  | Symbol | Dimension in mm |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max |
| Total Thickness | A | 2.770 | 2.890 | 3.010 |
| Stand Off | A1 | 0.400 | -- | 0.600 |
| Substrate Thickness | A2 | 0.940 REF |  |  |
| Thickness from Substrate Surface to Die Backside | A3 | --- REF |  |  |
| Body Size | D | 14.000 BSC |  |  |
|  | E | 14.000 BSC |  |  |
| Ball Diameter |  | 0.600 |  |  |
| Ball Width | b | 0.500 | --- | 0.700 |
| Ball Pitch | e | 1.000 BSC |  |  |
| Ball Count | n | 169 |  |  |
| Edge Ball Center to Center | D1 | 12.000 BSC |  |  |
|  | E1 | 12.000 BSC |  |  |
| Expose Die Size | D2 | --- |  |  |
|  | E2 | --- |  |  |
| Package Edge Tolerance | aaa | 0.100 |  |  |
| Substrate Parallelism | bbb | --- |  |  |
| Top Parallelism | ccc | 0.200 |  |  |
| Coplanarity | ddd | 0.150 |  |  |
| Ball Offset <Package> | eee | 0.250 |  |  |
| Ball Offset <Ball> | fff | 0.100 |  |  |

## 9 <br> Order Information

### 9.1 Ordering Part Numbers and Package Markings

Figure 56 shows the ordering part numbering scheme for the 88X5113 device.
Figure 56: Sample Part Number


Table 101: 88X5113 Part Order Option

| Package Type | Part Order Number |
| :--- | :--- |
| $88 \times 5113$ 169-pin FCBGA $14 \times 14$ - Commercial | $88 \times 5113-$ XX-BVW4C000 |
| $88 \times 5113$ 169-pin FCBGA $14 \times 14$ - Industrial | $88 \times 5113-X X-$ BVW4I000 |

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### 9.1.1 Marking Example

Figure 57 and Figure 58 are examples of the package marking and pin 1 locations for the 88 X 5113 169-pin FCBGA $14 \times 14$ commercial and industrial Green package.

Figure 57: 88X5113 169-pin FCBGA Commercial Green Package Marking and Pin 1 Location


Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 58: 88×5113 169-pin FCBGA Industrial Green Package Marking and Pin 1 Location


Note: The above example is not drawn to scale. Location of markings is approximate.

## A <br> Revision History

## Table 102: Revision History

| Revision | Date | Section | Detail |
| :--- | :--- | :--- | :--- |
| Rev. B | July 30,2018 | All applicable | Initial release |



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[^0]:    The SERDES receiver is AC coupled on-chip. There is no off-chip AC-coupling capacitor required as long as the $R x$ input common mode is between AGND and AVDD (1.0V) and Rx amplitude is less than 1200 mVpp differential.

