SWITCHMODE

NPN Bipolar Power Transistor For Switching Power Supply Applications

The MJE13007G is designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- V_{CEO(sus)} 400 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100$ °C
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Standard TO-220
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

	Symbol	Value	Unit	
Collector-Emitter Sustaining Voltage		V _{CEO}	400	Vdc
Collector-Base Breakdown Voltage		V _{CES}	700	Vdc
Emitter-Base Voltage		V _{EBO}	9.0	Vdc
Collector Current	ContinuousPeak (Note 1)	I _C I _{CM}	8.0 16	Adc
Base Current	ContinuousPeak (Note 1)	I _B I _{BM}	4.0 8.0	Adc
Emitter Current	ContinuousPeak (Note 1)	I _E I _{EM}	12 24	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C		P _D	80 0.64	W W/°C
Operating and Storage Temperature		T _J , T _{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

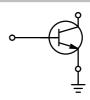
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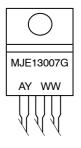
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POWER TRANSISTOR 8.0 AMPERES 400 VOLTS – 80 WATTS





MARKING DIAGRAM



A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13007G	TO-220 (Pb-Free)	50 Units / Rail

^{*}Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8lbs.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

		•		
V _{CEO(sus)}	400	_	-	Vdc
I _{CES}	<u>-</u>	- -	0.1 1.0	mAdc
I _{EBO}	-	_	100	μAdc
,		•	•	
I _{S/b}	See Figure 6			
-	See Figure 7			
•				
h _{FE}	8.0 5.0	- -	40 30	-
V _{CE(sat)}	- - -	- - - -	1.0 2.0 3.0 3.0	Vdc
V _{BE(sat)}		- - -	1.2 1.6 1.5	Vdc
f _T	4.0	14	-	MHz
C _{ob}	-	80	-	pF
t _d	-	0.025	0.1	μs
t _r	-	0.5	1.5	
t _s	-	1.8	3.0	1
t _f	-	0.23	0.7]
1	1	1		
t _{sv}	- -	1.2 1.6	2.0 3.0	μs
t _c	-	0.15	0.30 0.50	μS
	-	0.21	0.50	
	I _{CES}	ICES	ICES	ICES

^{2.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

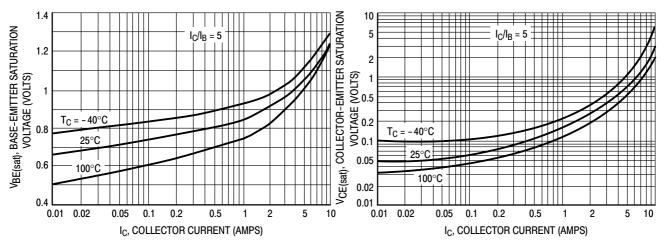


Figure 1. Base-Emitter Saturation Voltage

Figure 2. Collector-Emitter Saturation Voltage

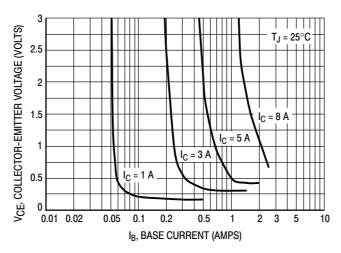


Figure 3. Collector Saturation Region

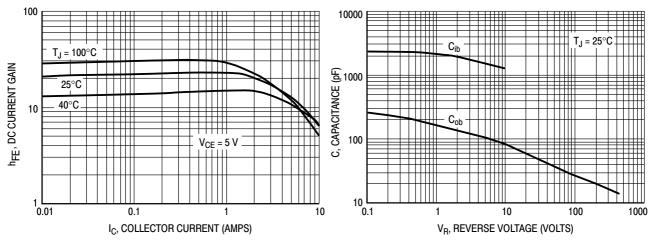
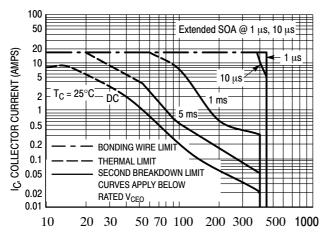


Figure 4. DC Current Gain

Figure 5. Capacitance



VCE, COLLECTOR-EMITTER VOLTAGE (VOLTS)



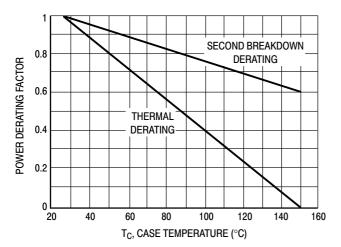


Figure 8. Forward Bias Power Derating

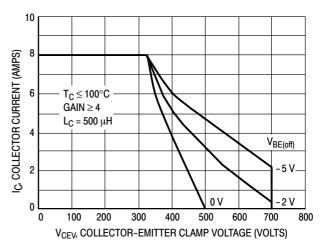


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25$ °C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

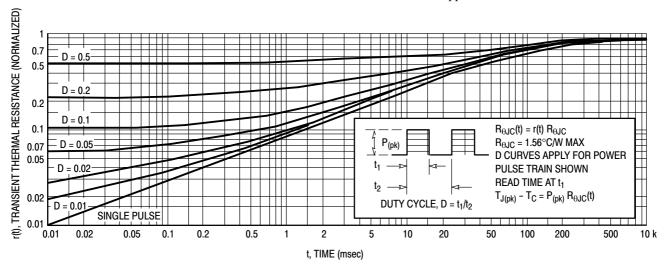


Figure 9. Typical Thermal Response for MJE13007

SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2. (Note 1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both

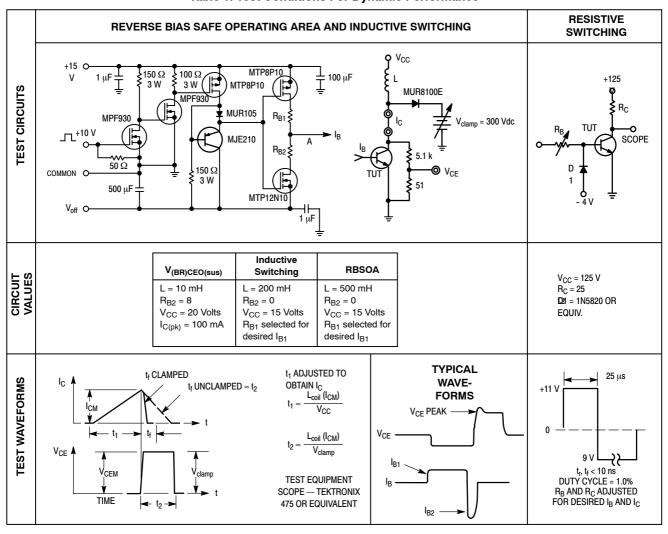
at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn—on and turn—off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn—on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage—current conditions that can be sustained during reverse biased turn—off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

NOTE: 1. For detailed information on specific switching applications, see ON Semiconductor Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance



VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

- 1. The device thermal limitations are not exceeded.
- 2. The turn–on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 6).
- 3. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{\text{CE(sat)}}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time ($t_{\rm fi}$). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are shown in Figures 12 and 13 and resistive loads in Figures 10 and 11. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

 t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

 t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

 t_{fi} = Current Fall Time, 90–10% I_{C}

 t_{ti} = Current Tail, 10–2% I_{C}

 t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 12 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

 $P_{SWT} = 1/2 V_{CC}I_{C}(t_{c}) f$

Typical inductive switching times are shown in Figure 13. In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

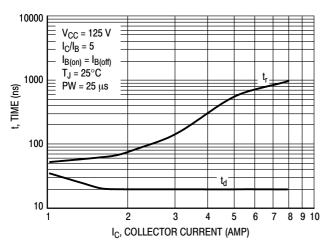


Figure 10. Turn-On Time (Resistive Load)

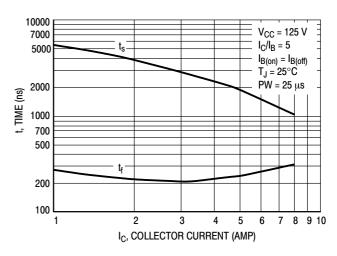


Figure 11. Turn-Off Time (Resistive Load)

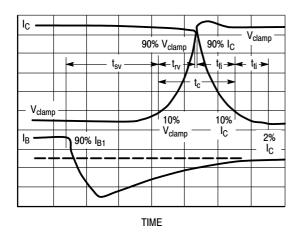


Figure 12. Inductive Switching Measurements

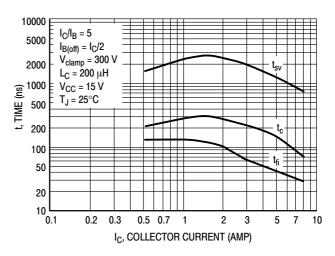
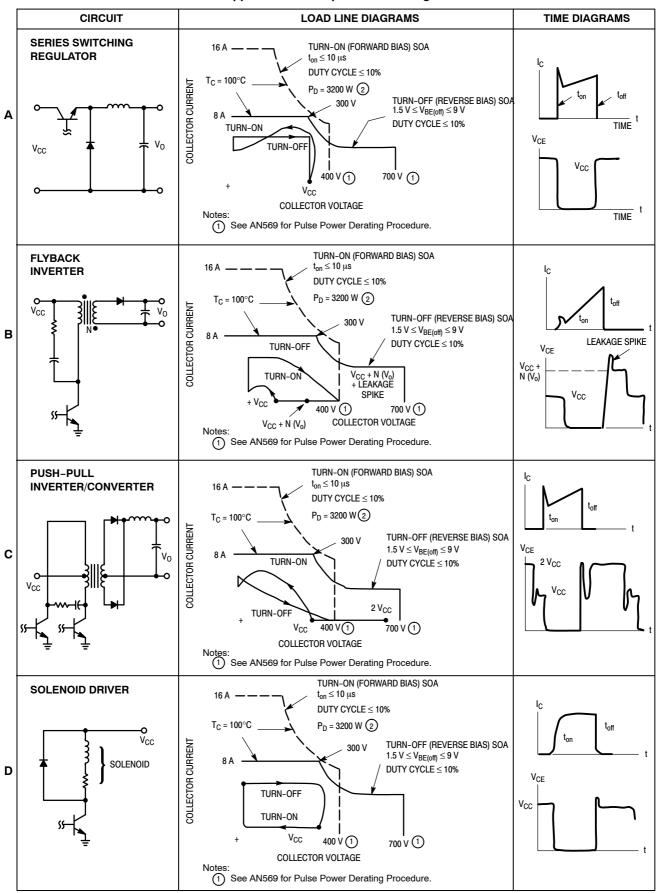


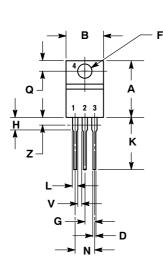
Figure 13. Typical Inductive Switching Times

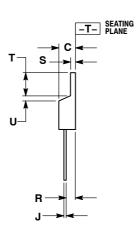
Table 2. Applications Examples of Switching Circuits



PACKAGE DIMENSIONS

TO-220 CASE 221A-09 ISSUE AG





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M. 1982.
- 2. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

STYLE 1:

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