

# 74VHC393FT

## 1. Functional Description

- Dual Binary Counter

## 2. General

The 74VHC393FT is an advanced high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the  $\overline{CK}$  pulse. The counter can be reset to "0" (QA to QD = "L") by a high at the CLR input regardless of other inputs.

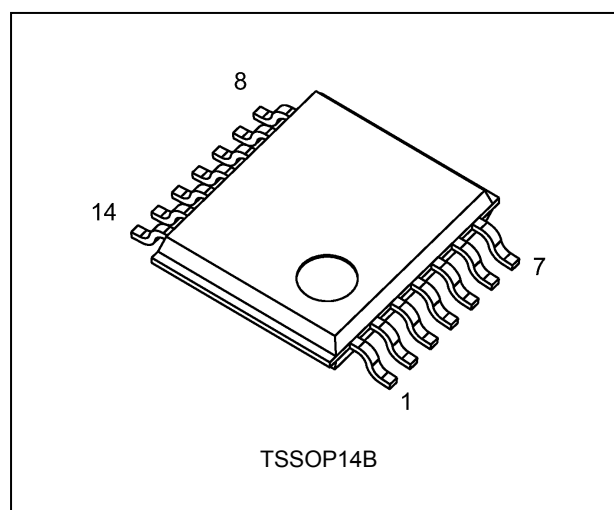
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed:  $f_{MAX} = 170$  MHz (typ.) at  $V_{CC} = 5.0$  V
- (4) Low power dissipation:  $I_{CC} = 4.0$   $\mu$ A (max) at  $T_a = 25$  °C
- (5) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (6) Power-down protection is provided on all inputs.
- (7) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (8) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to  $5.5$  V
- (9) Low noise:  $V_{OLP} = 0.8$  V (max)
- (10) Pin and function compatible with the 74 series (74AC/HC/AHC etc.) 393 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

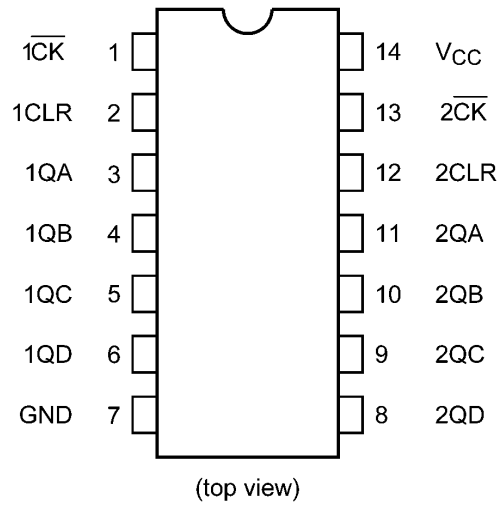
## 4. Packaging



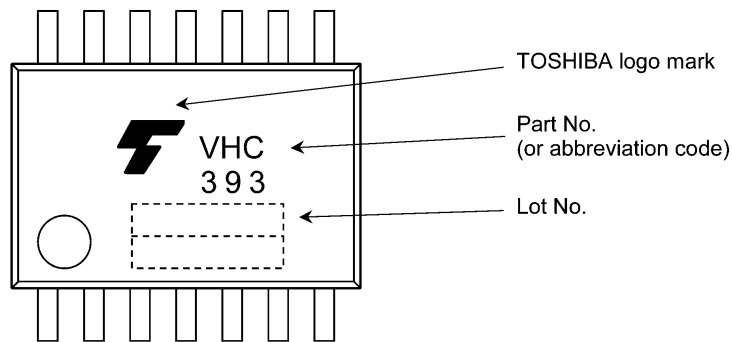
Start of commercial production

2014-12

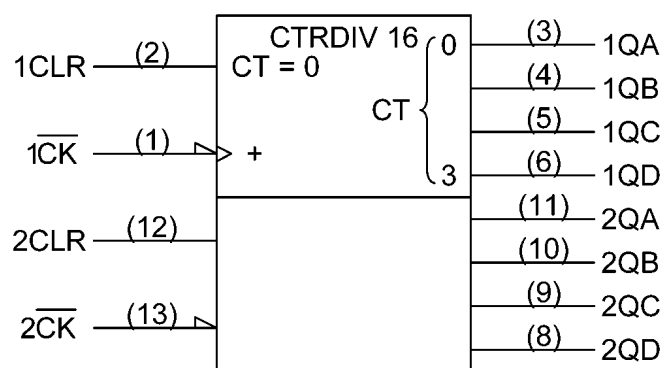
**5. Pin Assignment**



**6. Marking**



**7. IEC Logic Symbol**

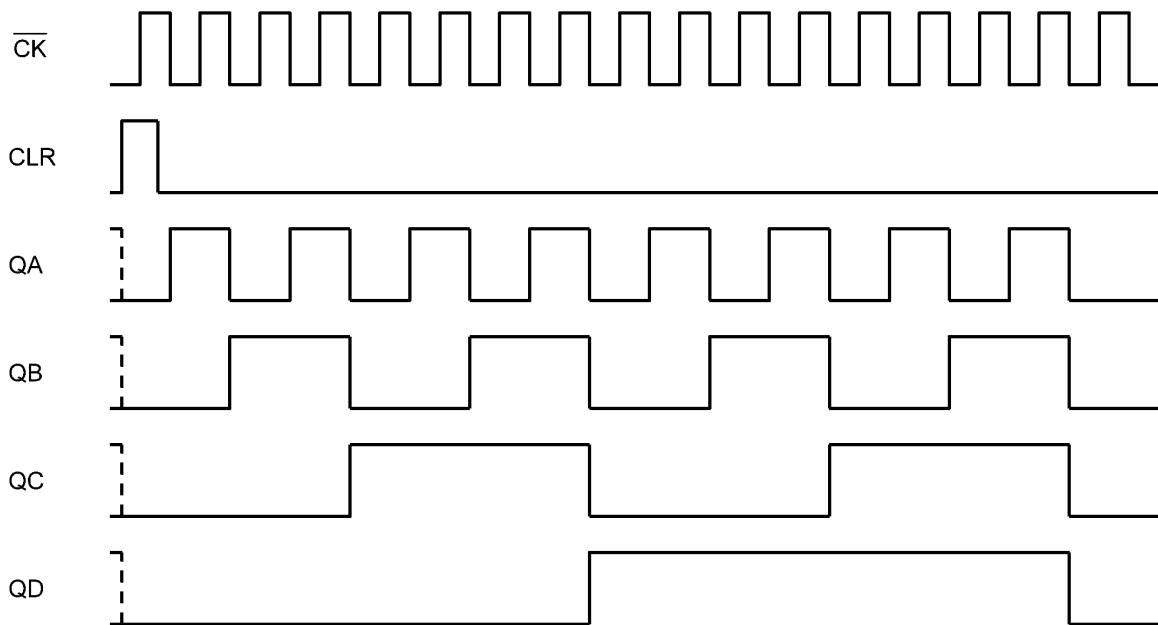


**8. Truth Table**

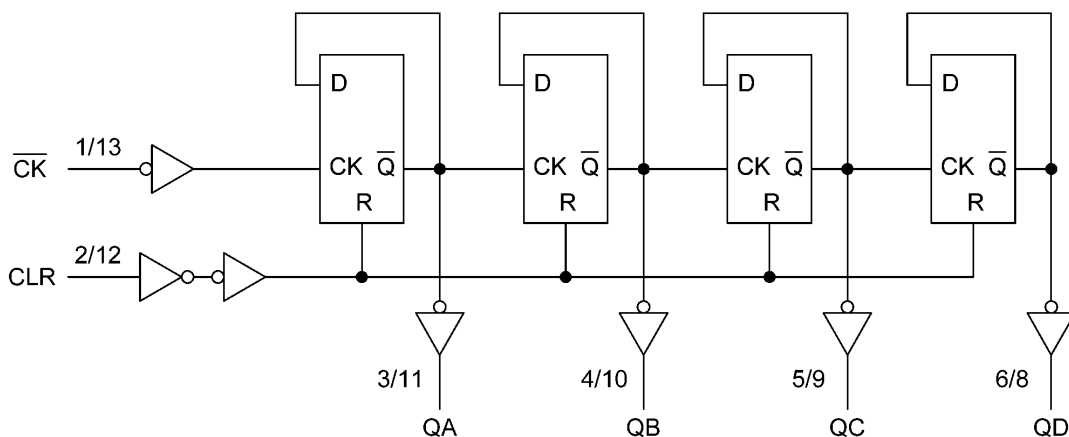
Inputs		Outputs			
$\overline{\text{CK}}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
	L	Count up			
	L	No change			

X: Don't care

**9. Timing Diagrams**



**10. System Diagram**



**11. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 75$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85$  °C. From  $T_a = 85$  to  $125$  °C a derating factor of  $-3.25$  mW/°C shall be applied until 50 mW.

**12. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$	—	2.0 to 5.5	V
Input voltage	$V_{IN}$	—	0 to 5.5	V
Output voltage	$V_{OUT}$	—	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	—	-40 to 125	°C
Input rise and fall times	$dt/dv$	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5.0 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**13. Electrical Characteristics**

**13.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
$I_{OH} = -8\text{ mA}$	4.5	3.94		—	—			
	Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1
3.0					—	0.0	0.1	
4.5					—	0.0	0.1	
$I_{OL} = 4\text{ mA}$				3.0	—	—	0.36	
				$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5		—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	

**13.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
				$I_{OH} = -8\text{ mA}$	4.5	3.80	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$		2.0	—	0.1
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
				$I_{OL} = 8\text{ mA}$	4.5	—	0.44
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5		—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	$\mu\text{A}$	

**13.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4$ mA	3.0	2.40	—	
			$I_{OH} = -8$ mA	4.5	3.70	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4$ mA	3.0	—	0.55	
			$I_{OL} = 8$ mA	4.5	—	0.55	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	$\pm 2.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	80.0	$\mu A$

**13.4. Timing Requirements (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Minimum pulse width ( $\overline{CK}$ )	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	—	5.0	ns
			$5.0 \pm 0.5$	—	5.0	
Minimum pulse width (CLR)	$t_{w(H)}$	—	$3.3 \pm 0.3$	—	5.0	ns
			$5.0 \pm 0.5$	—	5.0	
Minimum removal time	$t_{rem}$	—	$3.3 \pm 0.3$	—	5.0	ns
			$5.0 \pm 0.5$	—	4.0	

**13.5. Timing Requirements (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width ( $\overline{CK}$ )	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum pulse width (CLR)	$t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum removal time	$t_{rem}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	4.0	

**13.6. Timing Requirements (Unless otherwise specified,  $T_a = -40\text{ to }125\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width ( $\overline{CK}$ )	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum pulse width (CLR)	$t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum removal time	$t_{rem}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	4.0	

**13.7. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK-QA)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	8.6	13.2	ns
					50	—	11.1	16.7	
				$5.0 \pm 0.5$	15	—	5.8	8.5	
					50	—	7.3	10.5	
Propagation delay time (CK-QB)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	10.2	15.8	ns
					50	—	12.7	19.3	
				$5.0 \pm 0.5$	15	—	6.8	9.8	
					50	—	8.3	11.8	
Propagation delay time (CK-QC)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	11.7	18.0	ns
					50	—	14.2	21.5	
				$5.0 \pm 0.5$	15	—	7.7	11.2	
					50	—	9.2	13.2	
Propagation delay time (CK-QD)	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	13.0	19.7	ns
					50	—	15.5	23.2	
				$5.0 \pm 0.5$	15	—	8.5	12.5	
					50	—	10.0	14.5	
Propagation delay time (CLR-Qn)	$t_{PHL}$		—	$3.3 \pm 0.3$	15	—	7.9	12.3	ns
					50	—	10.4	15.8	
				$5.0 \pm 0.5$	15	—	5.4	8.1	
					50	—	6.9	10.1	
Maximum clock frequency	$f_{MAX}$		—	$3.3 \pm 0.3$	15	75	120	—	MHz
					50	45	65	—	
				$5.0 \pm 0.5$	15	125	170	—	
					50	85	115	—	
Input capacitance	$C_{IN}$		—			—	4	10	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—			—	23	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per circuit)}$$



**13.8. AC Characteristics**  
 (Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (CK-QA)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	15.5	ns
				50	1.0	19.0	
			$5.0 \pm 0.5$	15	1.0	10.0	
				50	1.0	12.0	
Propagation delay time (CK-QB)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	18.5	ns
				50	1.0	22.0	
			$5.0 \pm 0.5$	15	1.0	11.5	
				50	1.0	13.5	
Propagation delay time (CK-QC)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	21.0	ns
				50	1.0	24.5	
			$5.0 \pm 0.5$	15	1.0	13.0	
				50	1.0	15.0	
Propagation delay time (CK-QD)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	23.0	ns
				50	1.0	26.5	
			$5.0 \pm 0.5$	15	1.0	14.5	
				50	1.0	16.5	
Propagation delay time (CLR-Qn)	$t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	14.5	ns
				50	1.0	18.0	
			$5.0 \pm 0.5$	15	1.0	9.5	
				50	1.0	11.5	
Maximum clock frequency	$f_{MAX}$	—	$3.3 \pm 0.3$	15	65	—	MHz
				50	35	—	
			$5.0 \pm 0.5$	15	105	—	
				50	75	—	
Input capacitance	$C_{IN}$	—			—	10	pF

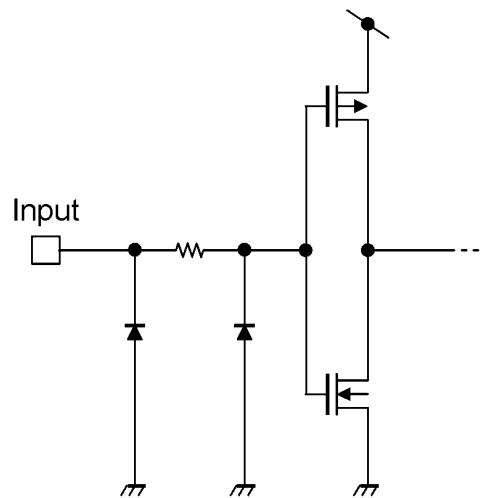
**13.9. AC Characteristics**  
 (Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (CK-QA)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	17.5	ns
				50	1.0	21.0	
			$5.0 \pm 0.5$	15	1.0	11.5	
				50	1.0	13.5	
Propagation delay time (CK-QB)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	21.0	ns
				50	1.0	24.5	
			$5.0 \pm 0.5$	15	1.0	13.0	
				50	1.0	15.0	
Propagation delay time (CK-QC)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	23.5	ns
				50	1.0	27.0	
			$5.0 \pm 0.5$	15	1.0	14.5	
				50	1.0	16.5	
Propagation delay time (CK-QD)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	25.5	ns
				50	1.0	29.0	
			$5.0 \pm 0.5$	15	1.0	16.5	
				50	1.0	18.5	
Propagation delay time (CLR-Qn)	$t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	16.5	ns
				50	1.0	20.0	
			$5.0 \pm 0.5$	15	1.0	11.0	
				50	1.0	13.0	
Maximum clock frequency	$f_{MAX}$	—	$3.3 \pm 0.3$	15	60	—	MHz
				50	35	—	
			$5.0 \pm 0.5$	15	100	—	
				50	65	—	
Input capacitance	$C_{IN}$	—			—	10	pF

**13.10. Noise Characteristics** (Unless otherwise specified,  $T_a = 25$  °C, Input:  $t_r = t_f = 3$  ns)

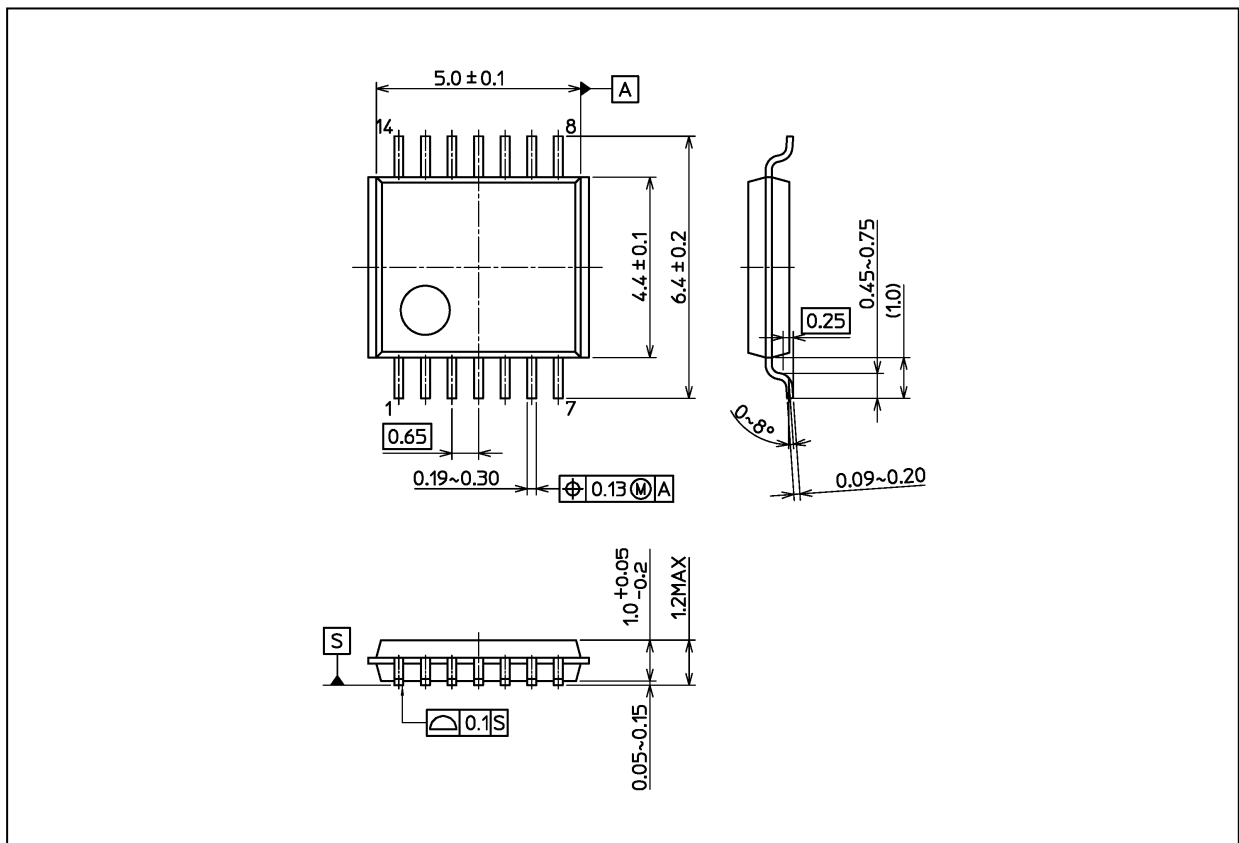
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50$ pF	5.0	0.5	0.8	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50$ pF	5.0	-0.5	-0.8	V
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50$ pF	5.0	—	3.5	V
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50$ pF	5.0	—	1.5	V

14. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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