

## 25 A standard and Snubberless™ triacs

### Features

- High current triac
- Low thermal resistance with clip bonding
- High commutation (4 quadrant) or very high commutation (3 quadrant) capability
- BTA series UL1557 certified (File ref: 81734)
- Packages are RoHS (2002/95/EC) compliant

### Applications

Applications include the ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits, etc., or for phase control operation in light dimmers, motor speed controllers, and similar.

The snubberless versions (BTA/BTB...W and T25 series) are especially recommended for use on inductive loads, due to their high commutation performances. The BTA series provides an insulated tab (rated at 2500 V<sub>RMS</sub>).

### Description

Available either in through-hole or surface-mount packages, the **BTA24**, **BTB24**, **BTA25**, **BTA26**, **BTB26** and **T25** triac series is suitable for general purpose mains power AC switching.



**Table 1. Device summary**

Symbol	Parameter	BTA24 <sup>(1)</sup>	BTB24	BTA25 <sup>(1)</sup>	BTA26 <sup>(1)</sup>	BTB26	T25	Unit
$I_{T(RMS)}$	RMS on-state current	25	25	25	25	25	25	A
$V_{DRM}/V_{RRM}$	Repetitive peak off-state voltage	600 / 800	600 / 800	600 / 800	600 <sup>(2)</sup> / 800	600	600 / 800	V
$I_{GT}$ (Snubberless)	Triggering gate current	35 / 50	35 / 50	50	35 / 50	-	35	mA
$I_{GT}$ (Standard)	Triggering gate current	-	50	50	50	50	-	mA

1. Insulated packages

2. 600 V version available only with  $I_{GT} = 50$  mA (Snubberless and Standard)

TM: Snubberless is a trademark of STMicroelectronics

# 1 Characteristics

**Table 2. Absolute maximum ratings**

Symbol	Parameter		Value	Unit		
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TOP3	$T_c = 105^\circ C$	25	A	
		D <sup>2</sup> PAK / TO-220AB	$T_c = 100^\circ C$			
		RD91 Ins/ TOP3 Ins.	$T_c = 100^\circ C$			
		TO-220AB Ins.	$T_c = 75^\circ C$			
$I_{TSM}$	Non repetitive surge peak on-state current (full cycle, $T_j$ initial = $25^\circ C$ )	F = 50 Hz	t = 20 ms	250	A	
		F = 60 Hz	t = 16.7 ms	260		
$I^2t$	$I^2t$ Value for fusing	$t_p = 10$ ms		340	A <sup>2</sup> s	
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \leq 100$ ns	F = 120 Hz	$T_j = 125^\circ C$	50	A/ $\mu$ s	
$V_{DSM}/V_{RSM}$	Non repetitive surge peak off-state voltage	$t_p = 10$ ms	$T_j = 25^\circ C$	$V_{DRM}/V_{RRM} + 100$	V	
$I_{GM}$	Peak gate current	$t_p = 20$ $\mu$ s	$T_j = 125^\circ C$	4	A	
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ C$	1	W	
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range				- 40 to + 150 - 40 to + 125	$^\circ C$

**Table 3. Electrical characteristics ( $T_j = 25^\circ C$ , unless otherwise specified), Snubberless and logic level (3 quadrants) T25, BTA/BTB24...W, BTA25...W, BTA26...W**

Symbol	Test Conditions	Quadrant		T25	BTA/BTB		Unit
				T2535	CW	BW	
$I_{GT}^{(1)}$	$V_D = 12$ V $R_L = 33$ $\Omega$	I - II - III	MAX.	35	35	50	mA
$V_{GT}$		I - II - III	MAX.	1.3			V
$V_{GD}$	$V_D = V_{DRM}$ $R_L = 3.3$ k $\Omega$ $T_j = 125^\circ C$	I - II - III	MIN.	0.2			V
$I_H^{(2)}$	$I_T = 500$ mA		MAX.	50	50	75	mA
$I_L$	$I_G = 1.2$ $I_{GT}$	I - III	MAX.	70	70	80	mA
		II		80	80	100	
dV/dt <sup>(2)</sup>	$V_D = 67\%$ $V_{DRM}$ gate open	$T_j = 125^\circ C$	MIN.	500	500	1000	V/ $\mu$ s
(dI/dt) <sub>c</sub> <sup>(2)</sup>	Without snubber	$T_j = 125^\circ C$	MIN.	13	13	22	A/ms

1. minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.
2. for both polarities of A2 referenced to A1.

**Table 4. Electrical characteristics ( $T_j = 25^\circ\text{C}$ , unless otherwise specified), standard (4 quadrants), BTB24...B, BTA25...B, BTA26...B, BTB26...B**

Symbol	Test Conditions	Quadrant		Value	Unit
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$ $R_L = 33\ \Omega$	I - II - III	MAX.	50	mA
		IV		100	
$V_{GT}$		ALL	MAX.	1.3	V
$V_{GD}$	$V_D = V_{DRM}$ $R_L = 3.3\ \text{k}\Omega$ $T_j = 125^\circ\text{C}$	ALL	MIN.	0.2	V
$I_H^{(2)}$	$I_T = 500\ \text{mA}$		MAX.	80	mA
$I_L$	$I_G = 1.2 I_{GT}$	I - III - IV	MAX.	70	mA
		II		160	
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$ gate open	$T_j = 125^\circ\text{C}$	MIN.	500	V/ $\mu\text{s}$
$(dV/dt)_c^{(2)}$	$(dI/dt)_c = 13.3\ \text{A/ms}$	$T_j = 125^\circ\text{C}$	MIN.	10	V/ $\mu\text{s}$

1. minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.
2. for both polarities of A2 referenced to A1.

**Table 5. Static characteristics**

Symbol	Test Conditions		Value	Unit	
$V_{TM}^{(1)}$	$I_{TM} = 35\ \text{A}$ $t_p = 380\ \mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.55	V
$V_{t0}^{(1)}$	Threshold voltage	$T_j = 125^\circ\text{C}$	MAX.	0.85	V
$R_d^{(1)}$	Dynamic resistance	$T_j = 125^\circ\text{C}$	MAX.	16	m $\Omega$
$I_{DRM}$ $I_{RRM}$	$V_{DRM} = V_{RRM}$	$T_j = 25^\circ\text{C}$	MAX.	5	$\mu\text{A}$
		$T_j = 125^\circ\text{C}$		3	mA

1. for both polarities of A2 referenced to A1.

**Table 6. Thermal resistance**

Symbol	Parameter	Value	Unit	
$R_{th(j-c)}$	Junction to case (AC)	TOP 3	0.6	$^\circ\text{C/W}$
		D <sup>2</sup> PAK / TO-220AB	0.8	
		RD91 Insulated / TOP3 Insulated	0.9	
		TO-220AB Insulated	1.7	
$R_{th(j-a)}$	Junction to ambient	<sup>(1)</sup> S = 1 cm <sup>2</sup> D <sup>2</sup> PAK	45	$^\circ\text{C/W}$
		TOP3 / TOP3 Insulated	50	
		TO-220AB / TO-220AB Insulated	60	

1. S = Copper surface under tab.

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)



Figure 2. RMS on-state current versus case temperature (full cycle)



Figure 3. D<sup>2</sup>PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)



Figure 4. Relative variation of thermal impedance versus pulse duration



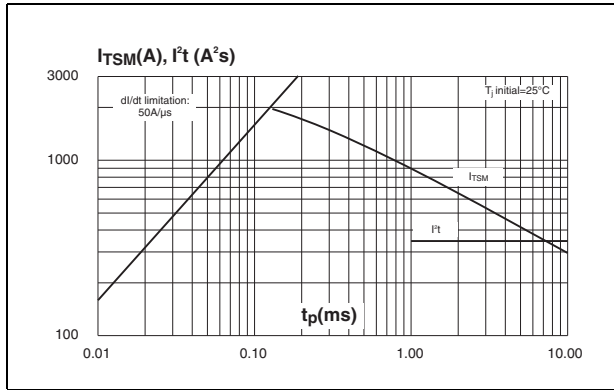
Figure 5. On-state characteristics (maximum values)



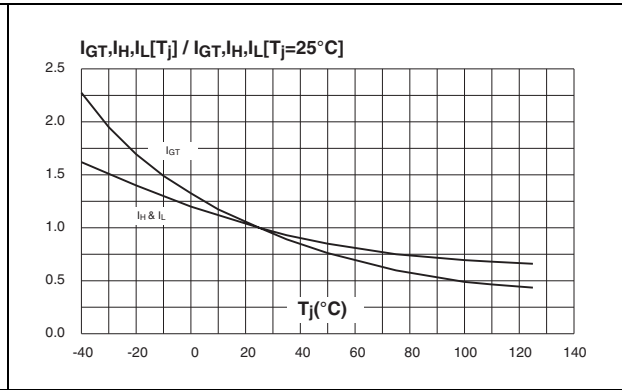
Figure 6. Surge peak on-state current versus number of cycles



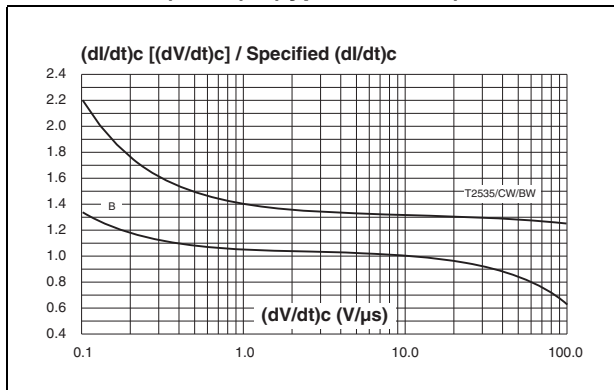
**Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10$  ms and corresponding value of  $I^2t$**



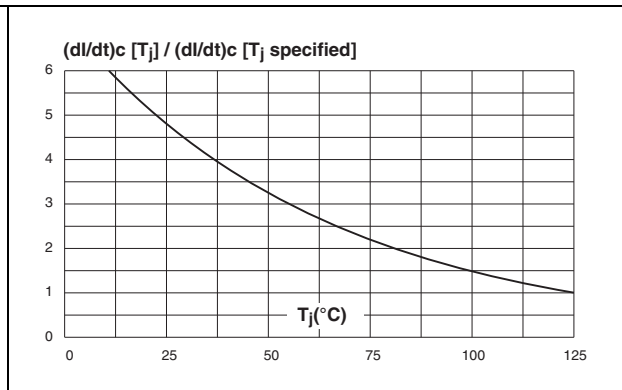
**Figure 8. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)**



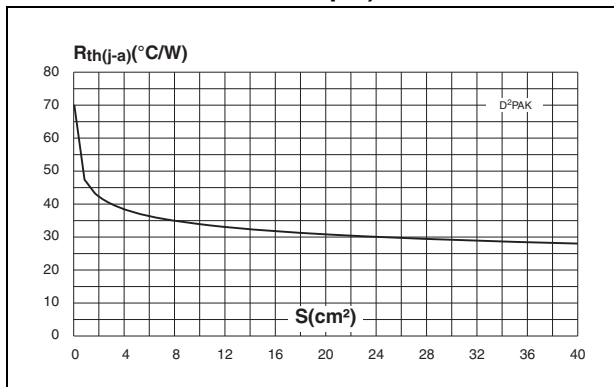
**Figure 9. Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$  (typical values)**



**Figure 10. Relative variation of critical rate of decrease of main current versus  $T_j$**



**Figure 11. D<sup>2</sup>PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35  $\mu$ m)**



## 2 Ordering information scheme

Figure 12. BTA and BTB series



Figure 13. T25 series



### 3 Package information

- Epoxy meets UL94,V0
- Cooling method: C
- Recommended torque value: 0.4 - 0.5 Nm (TO-220AB), 0.9 - 1.2 Nm (TOP3 and RD91)
- Maximum torque value for BTB24 is 0.5 Nm

Table 7. D<sup>2</sup>PAK dimensions

REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.169		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.70		0.93	0.027		0.037
B2	1.25	1.40		0.048	0.055	
C	0.45		0.60	0.017		0.024
C2	1.21		1.36	0.047		0.054
D	8.95		9.35	0.352		0.368
E	10.00		10.28	0.393		0.405
G	4.88		5.28	0.192		0.208
L	15.00		15.85	0.590		0.624
L2	1.27		1.40	0.050		0.055
L3	1.40		1.75	0.055		0.069
R		0.40			0.016	
V2	0°		8°	0°		8°

Figure 14. D<sup>2</sup>PAK footprint dimensions (in millimeters)



Table 8. RD91 dimensions

REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		40.00		1.575
A1	29.90	30.30	1.177	1.193
A2		22.00		0.867
B		27.00		1.063
B1	13.50	16.50	0.531	0.650
B2		24.00		0.945
C		14.00		0.551
C1		3.50		0.138
C2	1.95	3.00	0.077	0.118
E3	0.70	0.90	0.027	0.035
F	4.00	4.50	0.157	0.177
I	11.20	13.60	0.441	0.535
L1	3.10	3.50	0.122	0.138
L2	1.70	1.90	0.067	0.075
N1	33°	43°	33°	43°
N2	28°	38°	28°	38°





Table 9. TOP3 (insulated and non\_insulated) dimensions

REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.4		4.6	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.5		0.7	0.020		0.028
E	2.7		2.9	0.106		0.114
F	15.8		16.5	0.622		0.650
G	20.4		21.1	0.815		0.831
H	15.1		15.5	0.594		0.610
J	5.4		5.65	0.213		0.222
K	3.4		3.65	0.134		0.144
ØL	4.08		4.17	0.161		0.164
P	1.20		1.40	0.047		0.055
R		4.60			0.181	



Table 10. TO-220AB (insulated and non-insulated) dimensions



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
ØI	3.75		3.85	0.147		0.151
I4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
I2	1.14		1.70	0.044		0.066
I3	1.14		1.70	0.044		0.066
M		2.60			0.102	

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 4 Ordering information

**Table 11. Ordering information**

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
BTA/BTB24-xxxxyzRG	BTA/BTB24 xxxyz	TO-220AB	2.3 g	50	Tube
BTA25-xxxxyz	BTA25xxxxyz	RD91	20 g	25	Bulk
BTA26-xxxxyzRG	BTA26xxxxyz	TOP3 Ins.	4.5 g	30	Tube
BTB26-600BRG	BTB26600B	TOP3	4.5 g	30	Tube
T2535-xxxG	T2535 xxxG	D <sup>2</sup> PAK	1.5 g	50	Tube
T2535-xxxG-TR	T2535 xxxG			1000	Tape and reel

**Note:** xxx = voltage, y = sensitivity, z = type

## 5 Revision history

**Table 12. Revision history**

Date	Revision	Description of changes
Oct-2002	6A	Previous update.
13-Feb-2006	7	TO-220AB delivery mode changed from bulk to tube. ECOPACK statement added.
31-May-2006	8	Reformatted to current standard. $T_c$ in figure 3 changed to $T_{amb}$
31-Jul-2006	9	Typing error corrected on page 1 (BTB124 instead of BTB24)
05-Jul-2007	10	Added BTB26-600BRG. Restructured cover page and section 2: <a href="#">Ordering information scheme on page 6</a> to simplify product selection. Thermal resistance values updated in <a href="#">Table 6</a> and <a href="#">Figure 2</a> . Graphic for $I^2t$ updated in <a href="#">Figure 7</a> .

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

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