Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range T_i = 175 °C
- · Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- · High-speed line driver
- · Low-side load switch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C	-	-	40	V
V_{GS}	gate-source voltage		-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C	-	-	19	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C	-	-	15	W
Static charact	teristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	18	25	mΩ



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	1 6	D
2	D	drain		
3	G	gate	2 5	G—(F)
4	S	source	3 8 4	mbb076 S
5	D	drain	Transparent top view	
6	D	drain	DFN2020MD-6 (SOT1220)	
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK7D25-40E	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220		

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7D25-40E	4C

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	40	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C		-	19	Α
		V _{GS} = 10 V; T _{sp} = 100 °C		-	12	Α
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	8	Α
I _{DM}	peak drain current	T_{sp} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	76	Α
P _{tot}	total power dissipation	T _{sp} = 25 °C		-	15	W
		T _{amb} = 25 °C	[1]	-	2.3	W
Tj	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drai	in diode					,
Is	source current	T _{sp} = 25 °C		-	15	Α
		T _{amb} = 25 °C	[1]	-	2.3	Α
I _{SM}	peak source current	single pulse; t_p = 10 μ s; T_{sp} = 25 °C		-	62	Α
ESD maxim	um rating					,
V_{ESD}	electrostatic discharge voltage	НВМ	[2]	-	500	V
Avalanche ı	ruggedness			,		
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = 1.35 A; DUT in avalanche (unclamped)		-	28.4	mJ

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

^[2] Measured between all pins.

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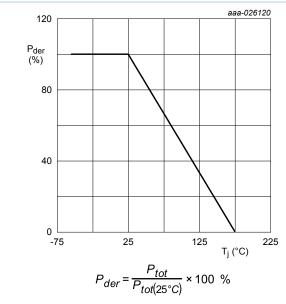


Fig. 1. Normalized total power dissipation as a function of junction temperature

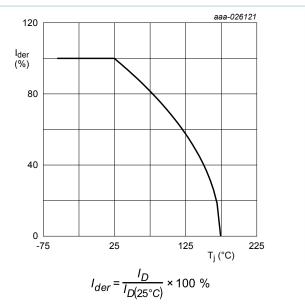


Fig. 2. Normalized continuous drain current as a function of junction temperature

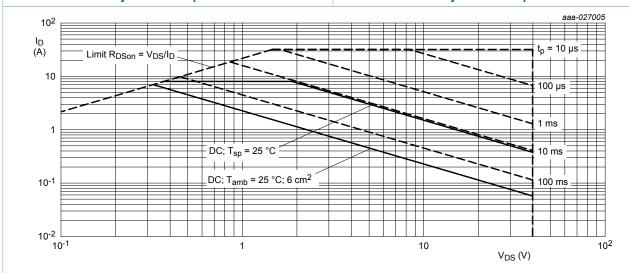


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	57	66	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

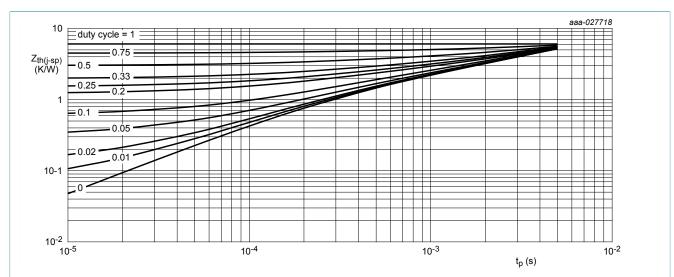


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

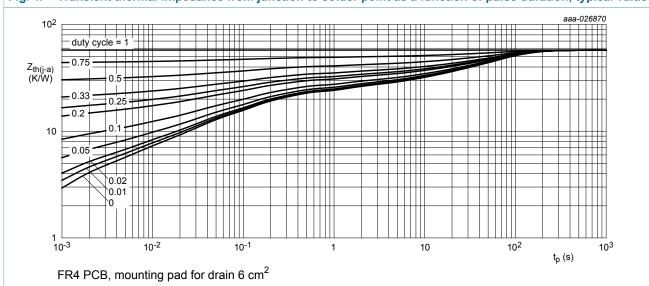


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics			,		
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 °C$	2.4	3	4	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
R _{DSon}	drain-source on-state	V _{GS} = 10 V; I _D = 8 A; T _j = 25 °C	-	18	25	mΩ
	resistance	V _{GS} = 10 V; I _D = 8 A; T _j = 175 °C	-	33	46	mΩ
9 _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	26	-	S
R _G	gate resistance	f = 1 MHz	-	1.7	-	Ω
Dynamic c	haracteristics					
Q _{G(tot)}	total gate charge	V _{DS} = 20 V; I _D = 7 A; V _{GS} = 10 V;	-	8.6	13	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.8	-	nC
Q _{GD}	gate-drain charge		-	2.6	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; f = 1 MHz; V _{GS} = 0 V;	-	460	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	105	-	pF
C _{rss}	reverse transfer capacitance		-	64	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; I _D = 7 A; V _{GS} = 10 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	6	-	ns
t _{d(off)}	turn-off delay time		-	8	-	ns
t _f	fall time		-	4	-	ns
Source-dra	in diode					,
V_{SD}	source-drain voltage	$I_S = 2.3 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	8.0	1.2	V
t _{rr}	reverse recovery time	$I_S = 2.3 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	14.3	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	6.1	-	nC

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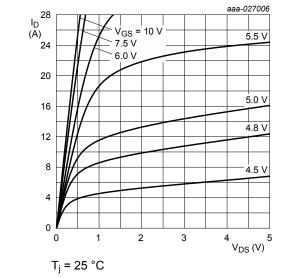


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

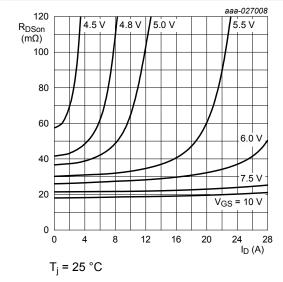


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

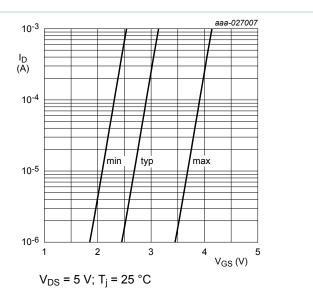


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

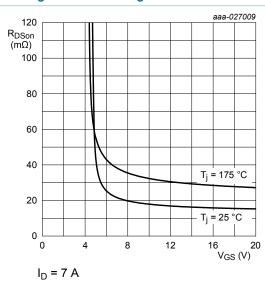


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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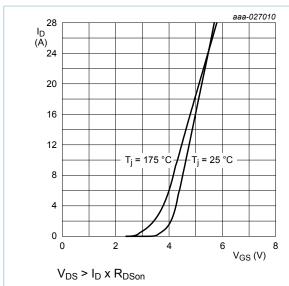


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

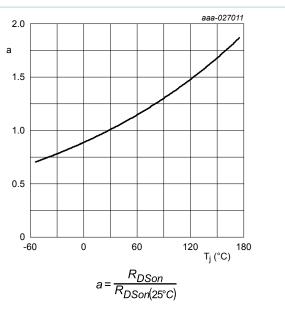


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

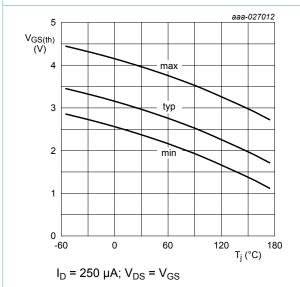


Fig. 12. Gate-source threshold voltage as a function of junction temperature

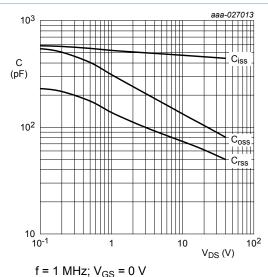


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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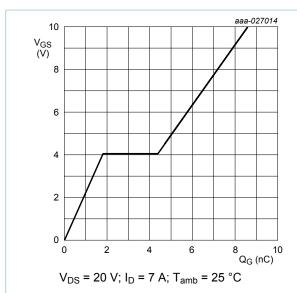


Fig. 14. Gate-source voltage as a function of gate charge; typical values

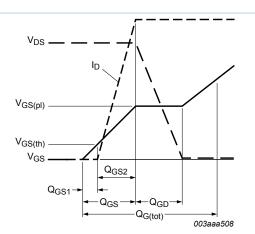


Fig. 15. Gate charge waveform definitions

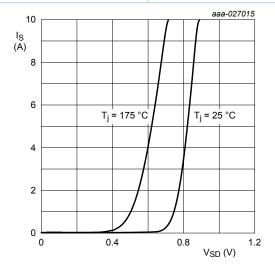
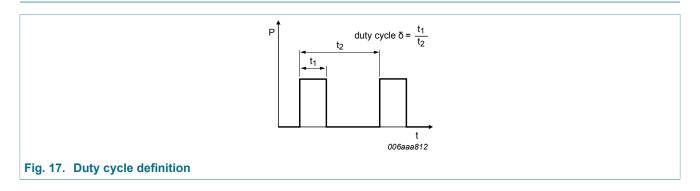


Fig. 16. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0 V$

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11. Test information

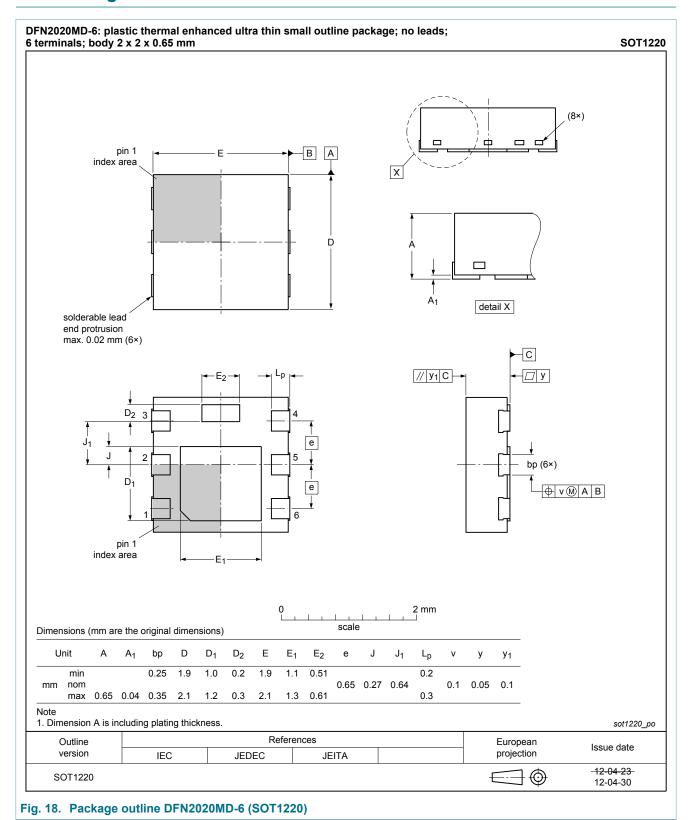


Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

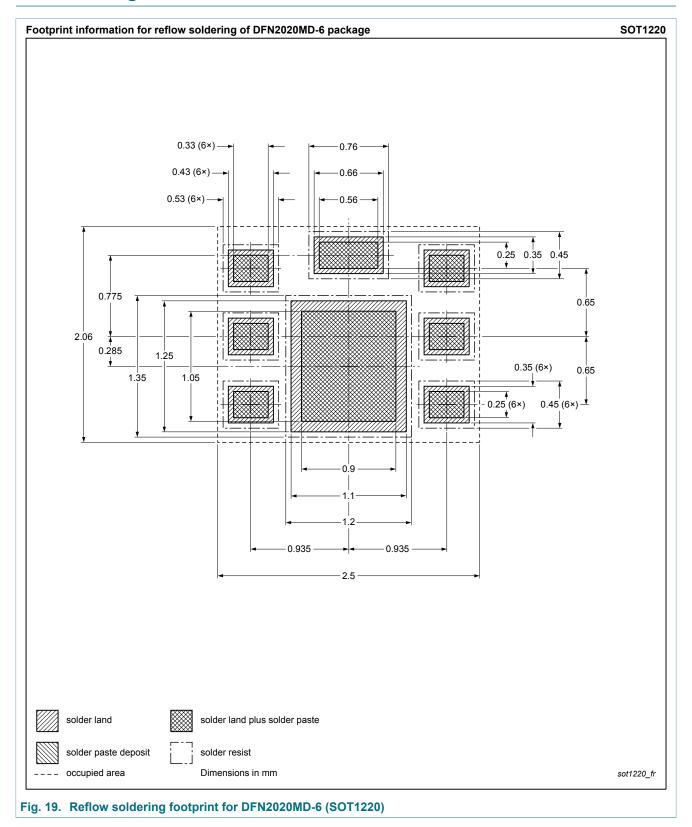
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12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK7D25-40E v.1	20171213	Product data sheet	-	-

40 V, N-channel Trench MOSFET

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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