

74LVC06A

Hex inverter with open-drain outputs

Rev. 7 — 2 October 2019

Product data sheet

1. General description

The 74LVC06A provides six inverting buffers. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVC06AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1
74LVC06APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink outline package; 14 leads; body width 4.4 mm		SOT402-1
74LVC06ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm		SOT762-1

4. Functional diagram

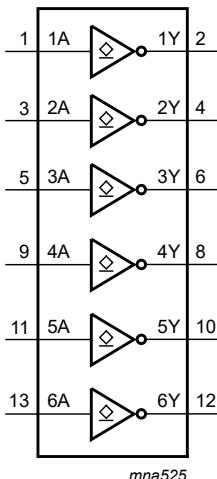


Fig. 1. Logic symbol

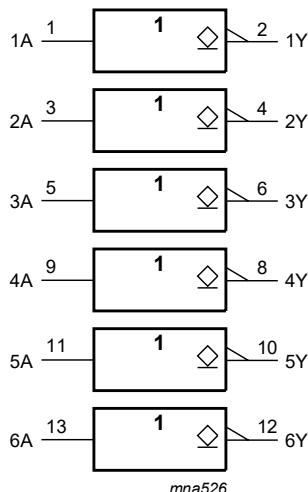


Fig. 2. IEC logic symbol

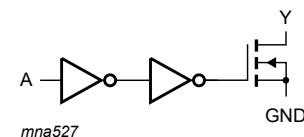


Fig. 3. Logic diagram for one gate

5. Pinning information

5.1. Pinning

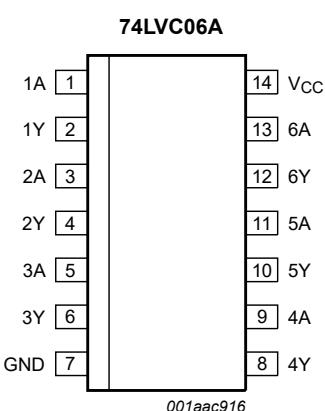
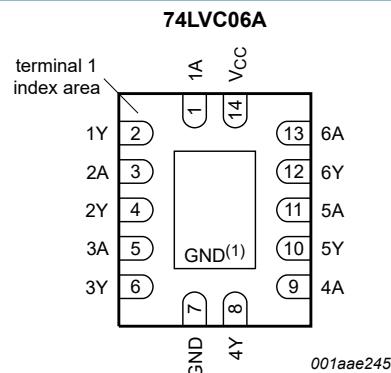


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	Z
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{CC}	supply voltage		-0.5	+6.5	V	
I _{IK}	input clamping current	V _I < 0	-50	-	mA	
V _I	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0	-50	-	mA	
V _O	output voltage	active mode	[2]	-0.5	+6.5	V
		high-impedance mode	[2]	-0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	50	mA	
I _{CC}	supply current		-	100	mA	
I _{GND}	ground current		-100	-	mA	
T _{stg}	storage temperature		-65	+150	°C	
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	500 mW	

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT108-1 (SO14) packages: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) packages: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) packages: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	active mode	0	-	5.5	V
		high-impedance mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$	-	-	$0.7 \times V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	$0.30 \times V_{CC}$	-	$0.30 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	-	-	-	-	-	-
		$I_O = 100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.20	-	0.3	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.6	V
		$I_O = 8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	-	-	0.3	-	0.75	V
		$I_O = 12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
		$I_O = 32 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	± 0.1	± 5	-	± 20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	± 0.1	± 10	-	± 20	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	± 0.1	± 10	-	± 20	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0 \text{ V to } 5.5 \text{ V}$; $V_I = \text{GND to } V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{amb} = 25 \text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 1.2 V	-	9	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	0.5	2.8	5.7	0.5	6.7	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.9	3.1	0.5	4.0	ns
		V _{CC} = 2.7 V	0.5	1.8	3.9	0.5	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.8	3.7	0.5	5.0	ns
		V _{CC} = 4.5 V to 5.5 V	0.7	1.5	2.5	0.7	3.5	ns
t _{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 1.2 V	-	10	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	0.5	2.6	5.7	0.5	6.7	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.4	3.1	0.5	4.0	ns
		V _{CC} = 2.7 V	0.5	2.6	3.9	0.5	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.2	3.7	0.5	5.0	ns
		V _{CC} = 4.5 V to 5.5 V	0.6	1.5	2.6	0.6	3.5	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [2]						
		V _{CC} = 1.65 V to 1.95 V	-	6.5	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	6.9	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	7.2	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$

f_i = input frequency in MHz; f_o = output frequency in MHz

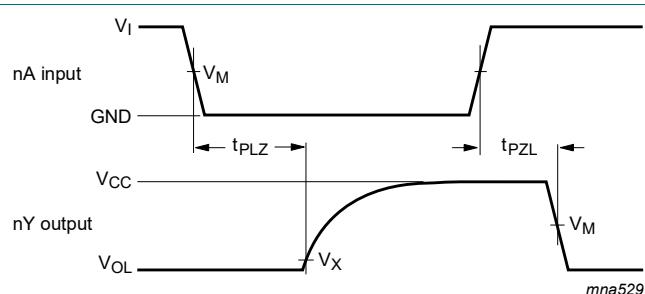
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of the outputs}$$

10.1. Waveforms



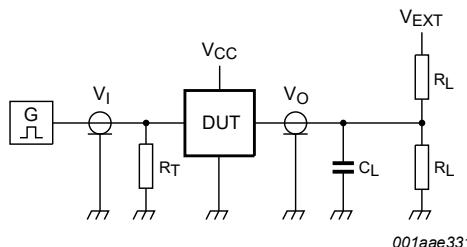
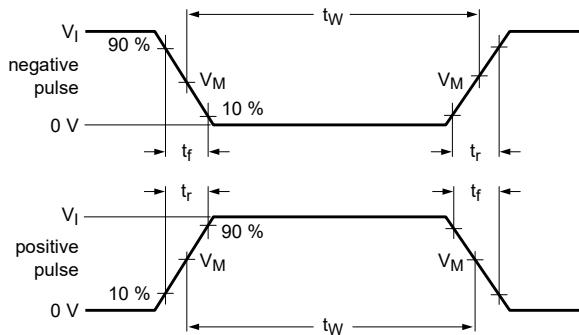
Measurement points are given in [Table 8](#)

Logic level: V_{OL} is a typical output voltage level that occurs with the output load.

Fig. 6. The input nA to output nY propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
< 2.7 V	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$
≥ 2.7 V to 3.6 V	1.5 V	$V_{OL} + 0.3 \text{ V}$
≥ 4.5 V to 5.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

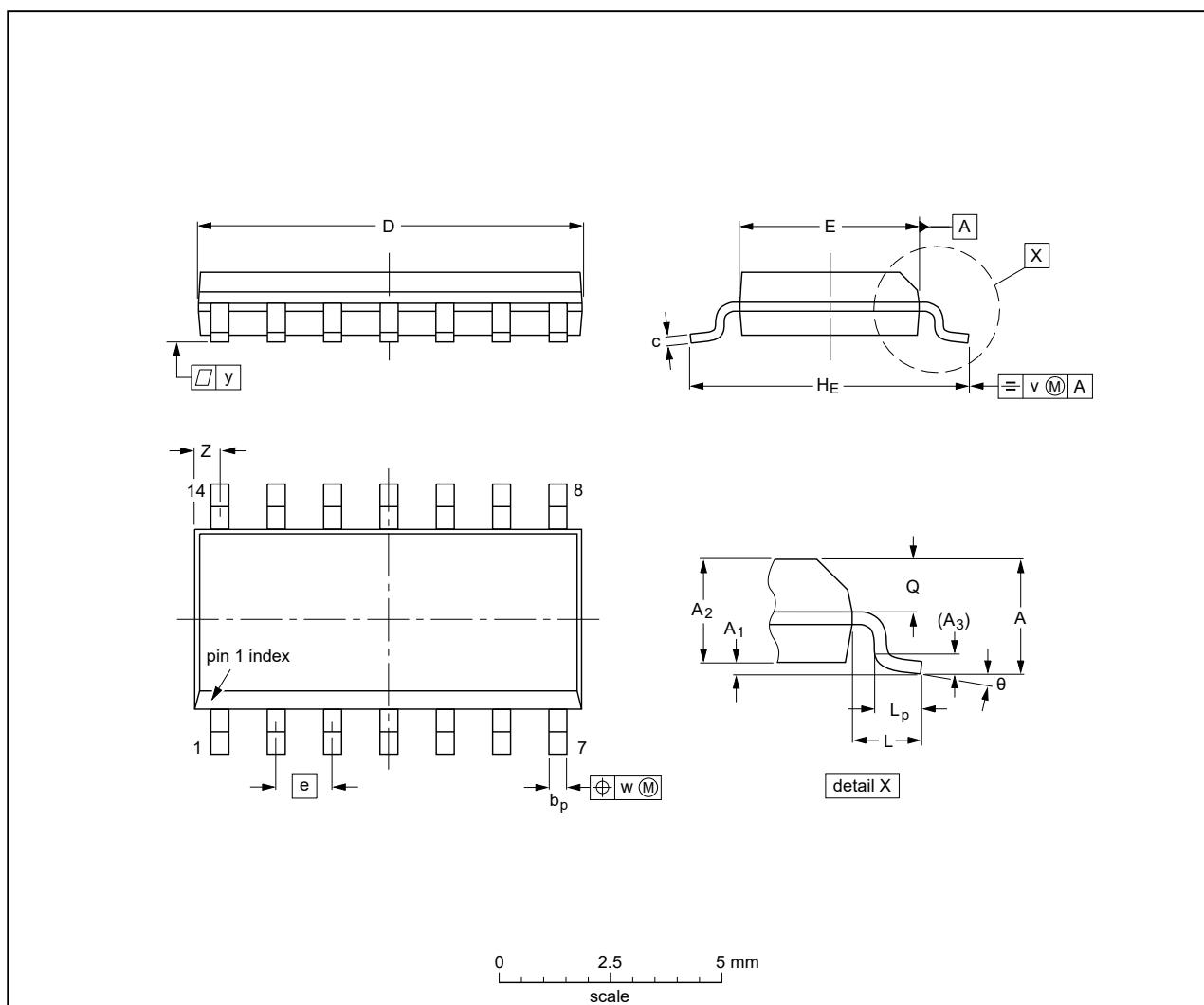
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L		t_{PLH}, t_{PHL}	t_{PZL}, t_{PZL}
1.2 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
4.5 V to 5.5 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.45	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0° 0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

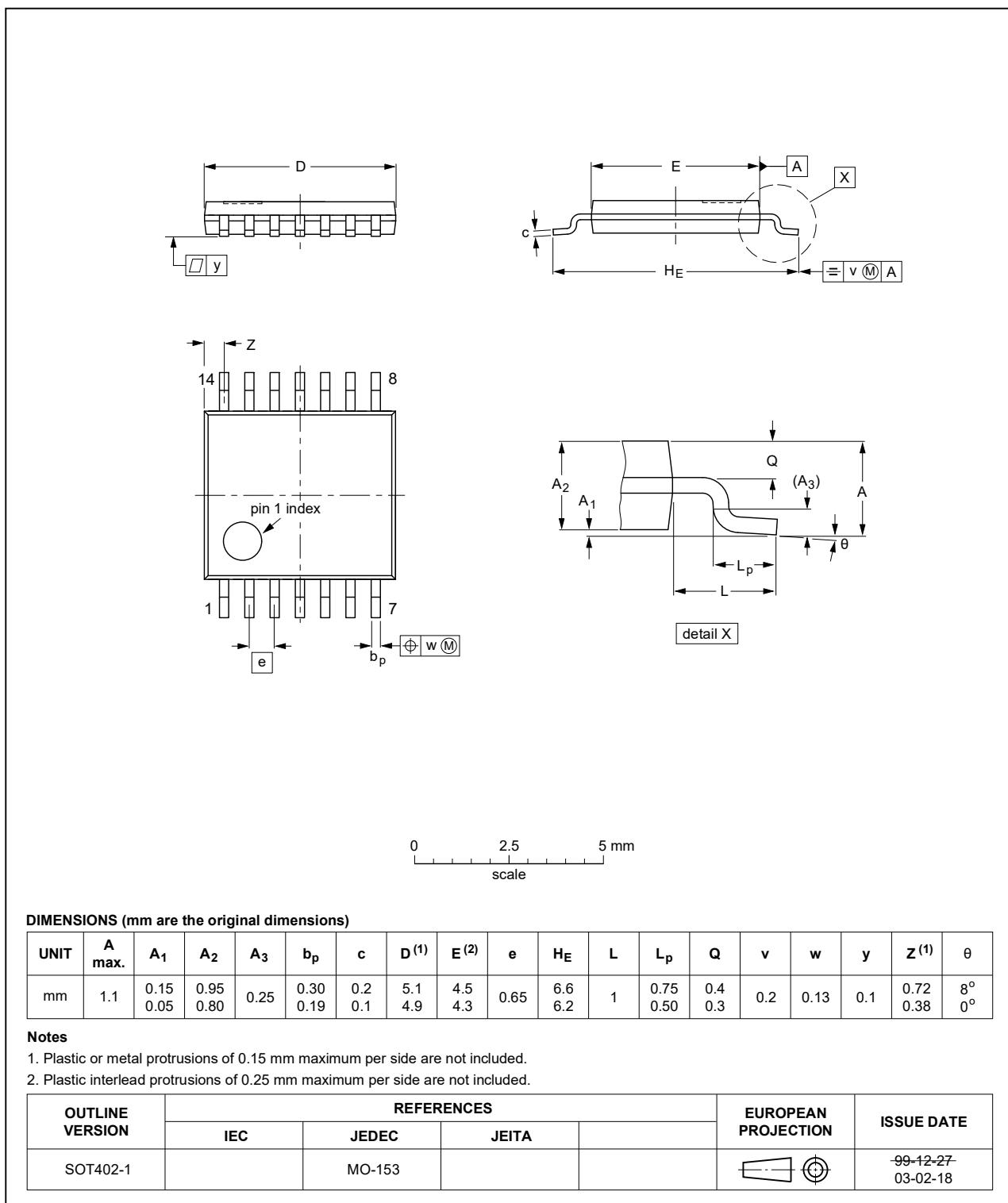
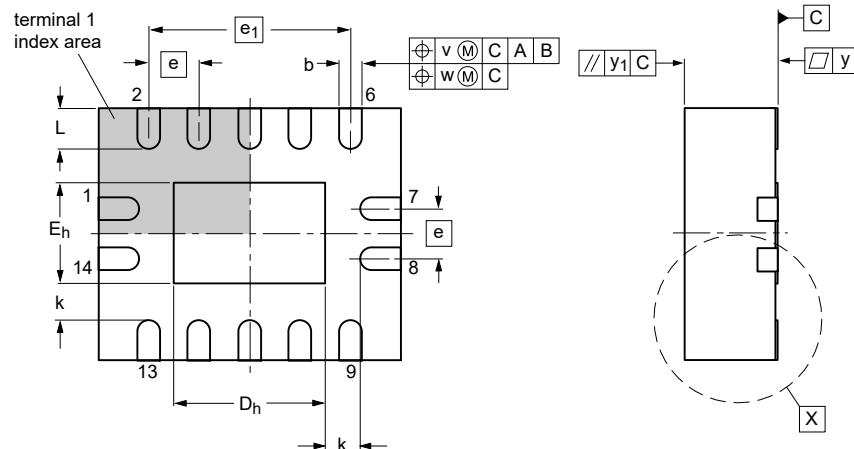
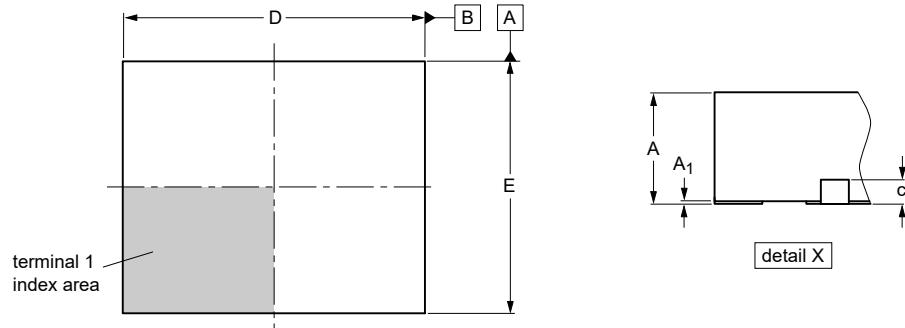


Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



0 2 4 mm
scale

Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30	3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2	0.4	0.1	0.05	0.05	0.1
mm	min		0.00	0.18	2.9	1.35	2.4	0.85				0.2	0.3			

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1	MO-241					15-04-10 15-05-05

Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC06A v.7	20191002	Product data sheet	-	74LVC06A v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation updated. Package outline drawing SOT762-1 (DHVQFN14) updated. 			
74LVC06A v.6	20111110	Product data sheet	-	74LVC06A v.5
Modifications:	<ul style="list-style-type: none"> Table 6: Conditions column, additional supply current V_{CC} range updated 			
74LVC06A v.5	20111024	Product data sheet	-	74LVC06A v.4
Modifications:	<ul style="list-style-type: none"> Table 7: values added for lower voltage ranges 			
74LVC06A v.4	20110810	Product data sheet	-	74LVC06A v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. 			
74LVC06A v.3	20031127	Product specification	-	74LVC06A v.2
74LVC06A v.2	20030828	Product specification	-	74LVC06A v.1
74LVC06A v.1	20000307	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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