

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM6J503NU

Power Management Switch Applications

- 1.5V drive
- Low ON-resistance: $R_{DS(ON)} = 89.6 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.5 \text{ V}$)
 $R_{DS(ON)} = 57.9 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.8 \text{ V}$)
 $R_{DS(ON)} = 41.7 \text{ m}\Omega$ (max) (@ $V_{GS} = -2.5 \text{ V}$)
 $R_{DS(ON)} = 32.4 \text{ m}\Omega$ (max) (@ $V_{GS} = -4.5 \text{ V}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-6.0	A
	Pulse	I_{DP} (Note 1)	-24.0	
Power Dissipation		P_D (Note 2)	1	W
		$t \leq 10\text{s}$	2	
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature		T_{stg}	-55 to 150	$^\circ\text{C}$

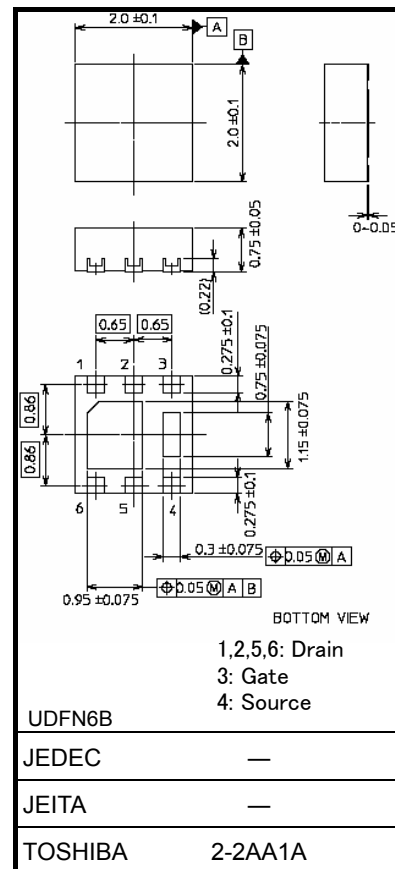
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

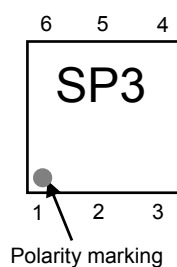
Note 1: The pulse width limited by max channel temperature.

Note 2: Mounted on an FR4 board.
(25.4 mm $\times$ 25.4 mm $\times$ 1.6 mm, Cu Pad: 645 mm²)

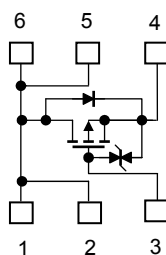
Unit: mm



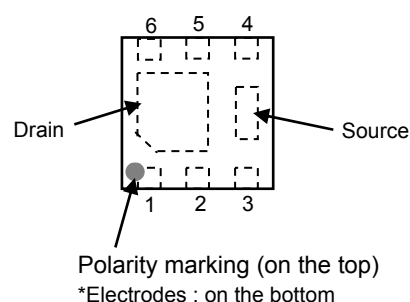
Marking(Top View)



Equivalent Circuit(Top View)



Pin Condition(Top View)



Start of commercial production
2010-11

Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}$, $V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}$, $V_{GS} = 5 \text{ V}$ (Note 4)	-15	—	—	
Drain cut-off current	I_{DSS}	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$	—	—	-1	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}$, $I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}$, $I_D = -1.0 \text{ A}$ (Note 3)	4.5	9.1	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -3.0 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ (Note 3)	—	27.7	32.4	m Ω
		$I_D = -2.5 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ (Note 3)	—	33.1	41.7	
		$I_D = -1.5 \text{ A}$, $V_{GS} = -1.8 \text{ V}$ (Note 3)	—	40.6	57.9	
		$I_D = -0.5 \text{ A}$, $V_{GS} = -1.5 \text{ V}$ (Note 3)	—	48.6	89.6	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	840	—	pF
Output capacitance	C_{oss}		—	118	—	
Reverse transfer capacitance	C_{rss}		—	99	—	
Total Gate Charge	Q_g	$V_{DD} = -10 \text{ V}$, $I_D = -4.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$	—	12.8	—	nC
Gate-Source Charge	Q_{gs1}		—	1.4	—	
Gate-Drain Charge	Q_{gd}		—	3.0	—	
Switching time	Turn-on time	$V_{DD} = -10 \text{ V}$, $I_D = -2.0 \text{ A}$, $V_{GS} = 0 \text{ to } -2.5 \text{ V}$, $R_G = 4.7 \text{ }\Omega$	—	32	—	ns
	Turn-off time		—	107	—	
Drain-Source forward voltage	V_{DSF}	$I_D = 4.0 \text{ A}$, $V_{GS} = 0 \text{ V}$ (Note 3)	—	0.78	1.2	V

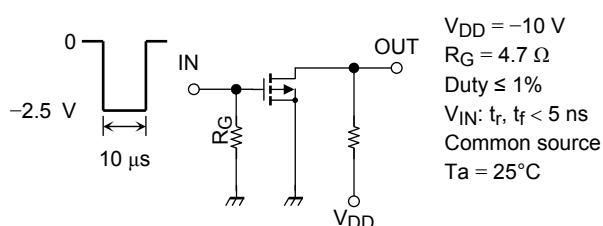
Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.

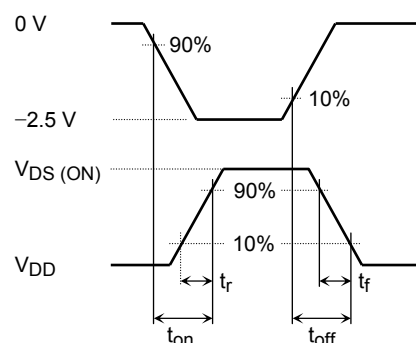
Note that the drain-source breakdown voltage is lowered in this mode

Switching Time Test Circuit

(a) Test circuit



(b) V_{IN}



(c) V_{OUT}

Precaution

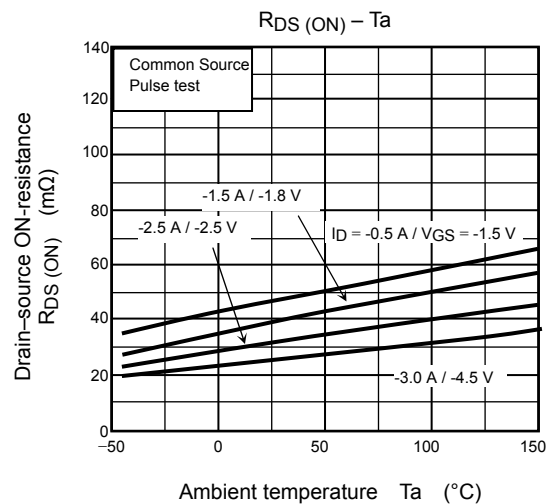
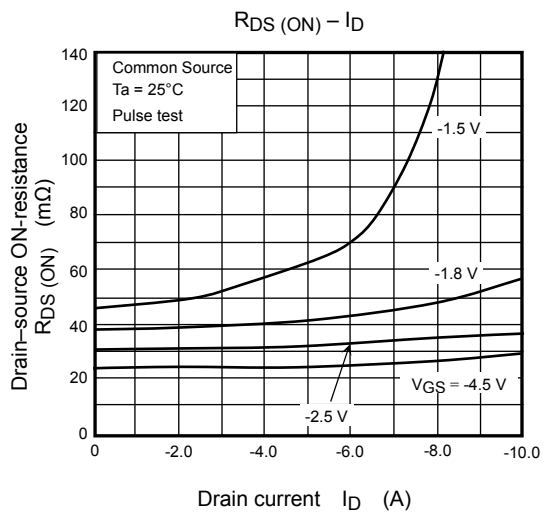
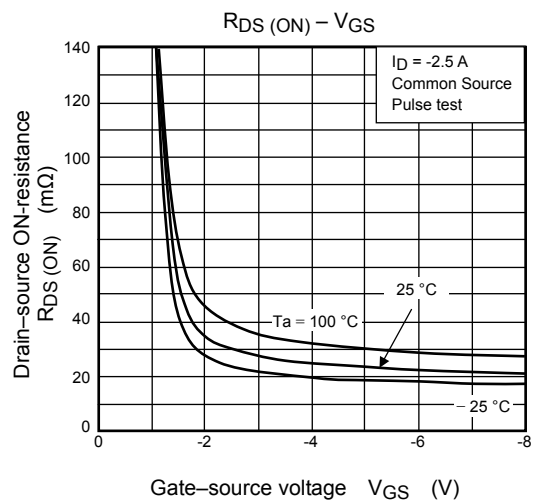
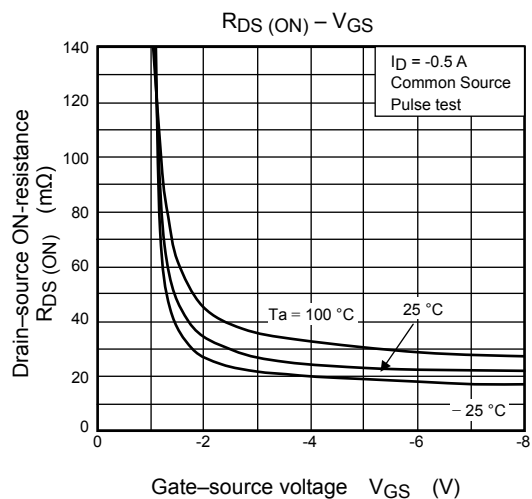
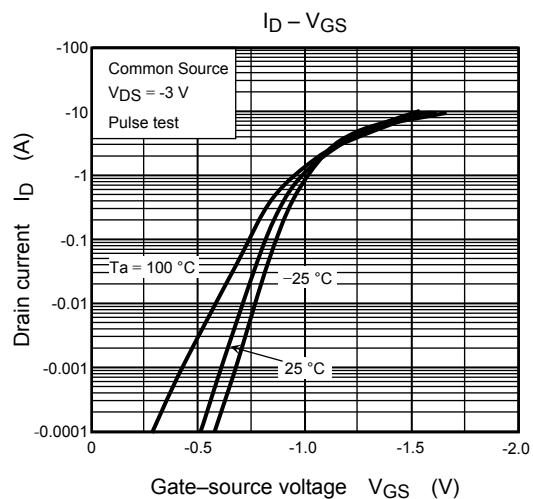
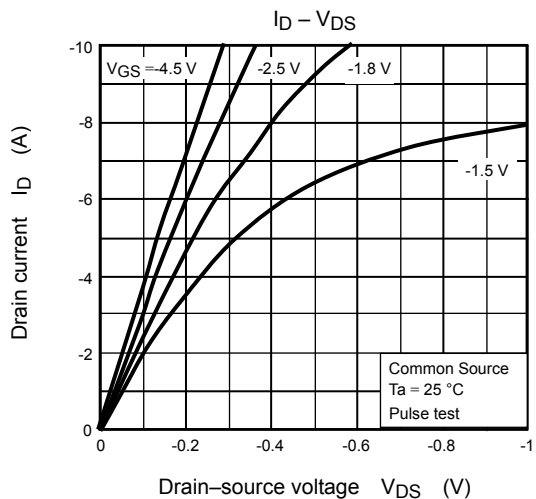
V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = -1 \text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

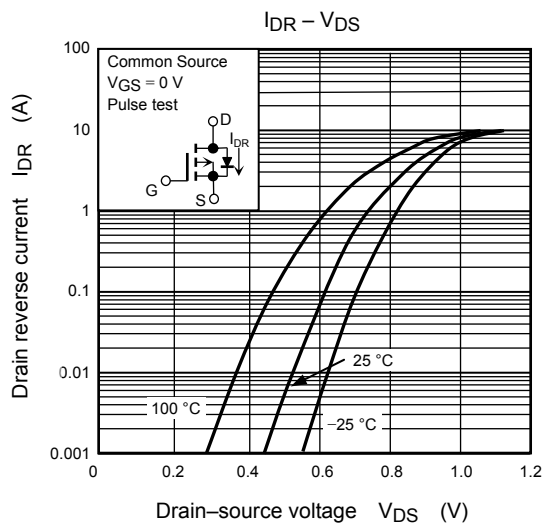
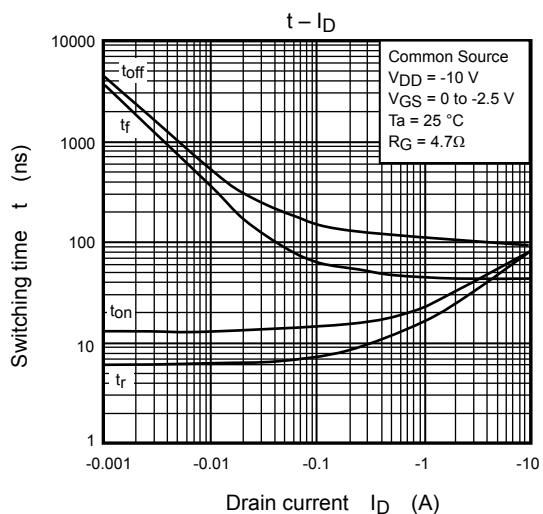
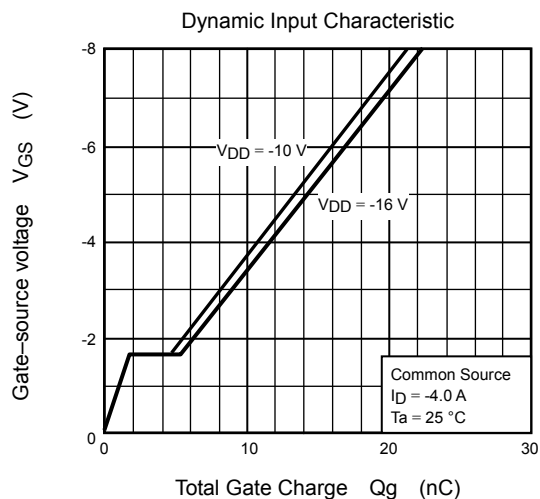
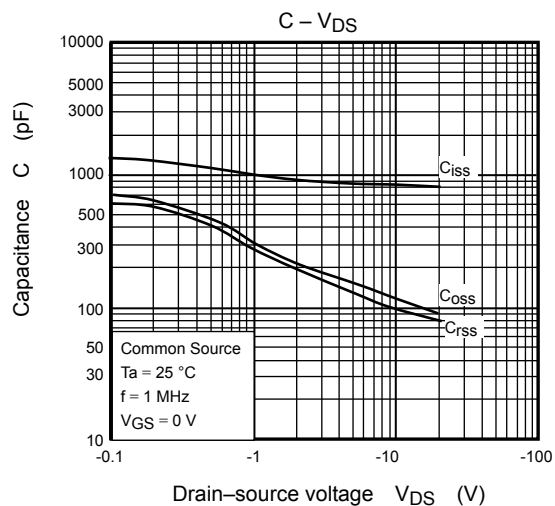
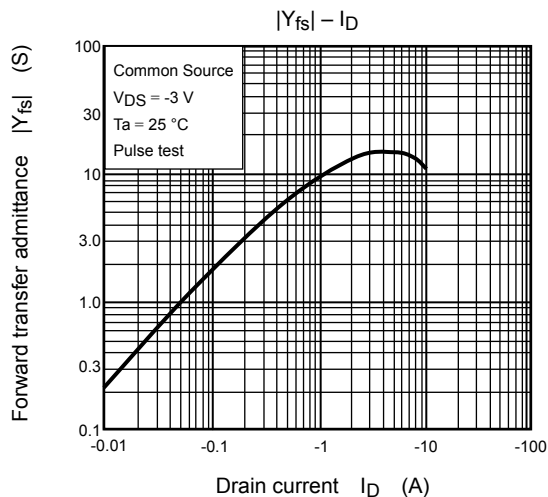
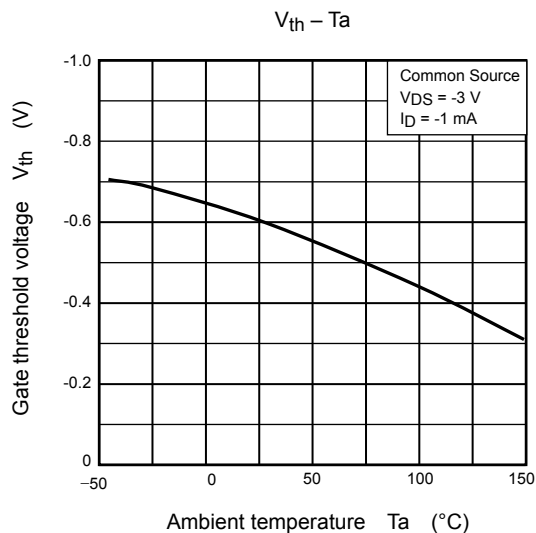
Please take this into consideration for using the device.

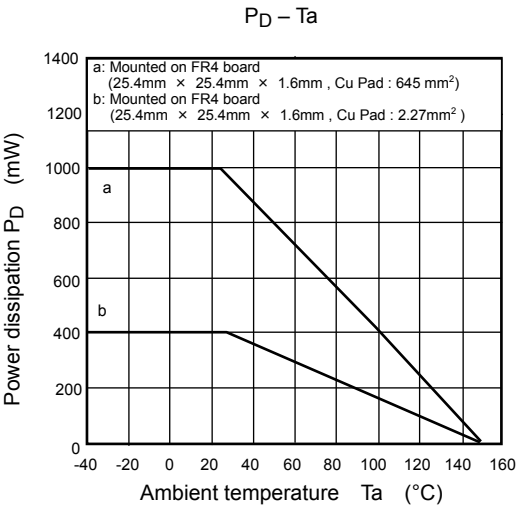
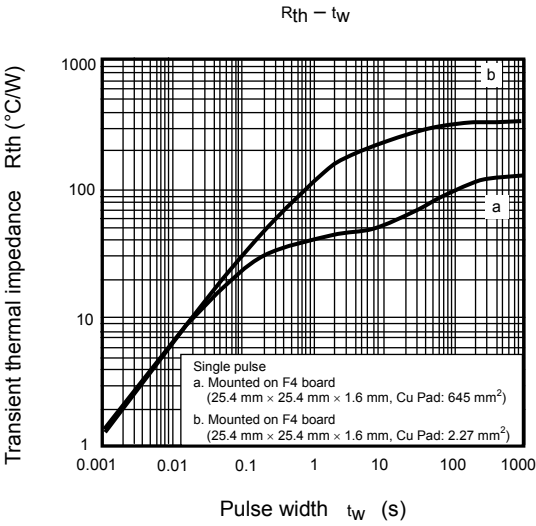
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th(ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration







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