



HIGH SPEED 2K X 16 DUAL-PORT SRAM

**IDT7133SA/LA
IDT7143SA/LA**

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- ◆ **High-speed access**
 - Military: 35/55/70/90ns (max.)
 - Industrial: 25/55ns (max.)
 - Commercial: 20/25/35/45/55/70/90ns (max.)
- ◆ **Low-power operation**
 - IDT7133/43SA
Active: 1150mW (typ.)
Standby: 5mW (typ.)
 - IDT7133/43LA
Active: 1050mW (typ.)
Standby: 1mW (typ.)
- ◆ **Versatile control for write: separate write control for lower and upper byte of each port**
- ◆ MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- ◆ On-chip port arbitration logic (IDT7133 only)
- ◆ **BUSY** output flag on IDT7133; **BUSY** input on IDT7143
- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation-2V data retention
- ◆ TTL-compatible; single 5V (±10%) power supply
- ◆ Available in 68-pin ceramic PGA, Flatpack, PLCC and 100-pin TQFP
- ◆ Military product compliant to MIL-PRF-38535 QML
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

Functional Block Diagram



NOTE:

1. IDT7133 (MASTER): **BUSY** is open drain output and requires pull-up resistor.
IDT7143 (SLAVE): **BUSY** is input.

JUNE 2018

Pin Configurations^(1,2,3) (con't.)



2746 drw 04

NOTES:

1. Both Vcc pins must be connected to the power supply to ensure reliable operation.
2. Both GND pins must be connected to the ground supply to ensure reliable operation.
3. Package body is approximately 1.18 in x 1.18 in x 0.16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

| Left Port | Right Port | Names |
|------------------------------------------|------------------------------------------|------------------------------|
| $\overline{\text{CE}}\text{L}$ | $\overline{\text{CE}}\text{R}$ | Chip Enable |
| $\text{R}/\overline{\text{W}}\text{LUB}$ | $\text{R}/\overline{\text{W}}\text{RUB}$ | Upper Byte Read/Write Enable |
| $\text{R}/\overline{\text{W}}\text{LLB}$ | $\text{R}/\overline{\text{W}}\text{RLB}$ | Lower Byte Read/Write Enable |
| $\overline{\text{OE}}\text{L}$ | $\overline{\text{OE}}\text{R}$ | Output Enable |
| A0L - A10L | A0R - A10R | Address |
| I/O0L - I/O15L | I/O0R - I/O15R | Data Input/Output |
| $\overline{\text{BUSY}}\text{L}$ | $\overline{\text{BUSY}}\text{R}$ | Busy Flag |
| VCC | | Power |
| GND | | Ground |

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Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Military | Unit |
|----------------------------------|--------------------------------------|-------------------------|--------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | -65 to +150 | °C |
| P _T | Power Dissipation | 2.0 | 2.0 | W |
| I _{OUT} | DC Output Current | 50 | 50 | mA |

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{CC} + 10%.

Maximum Operating Temperature and Supply Voltage^(1,2)

| Grade | Ambient Temperature | GND | V _{CC} |
|------------|---------------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

2746 tbl 04

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | 6.0 ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

2746 tbl 05

NOTES:

- V_{IL} (min.) = -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{CC} + 10%.

Capacitance (T_A = +25°C, f = 1.0mhz)

| Symbol | Parameter ⁽¹⁾ | Conditions ⁽²⁾ | Max. | Unit |
|------------------|--------------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 11 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 3dV | 11 | pF |

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NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Either port, V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | 7133SA 7143SA | | 7133LA 7143LA | | Unit |
|-----------------|---------------------------------------------------------|---------------------------------------------------------------------|------------------|------|------------------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| I _L | Input Leakage Current ⁽¹⁾ | V _{CC} = 5.5V, V _{IN} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| I _O | Output Leakage Current | $\overline{CE} = V_{IH}$, V _{OUT} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| V _{OL} | Output Low Voltage (I _{O0} -I _{O15}) | I _{OL} = 4mA | — | 0.4 | — | 0.4 | V |
| V _{OL} | Open Drain Output Low Voltage (BUSY) | I _{OL} = 16mA | — | 0.5 | — | 0.5 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4mA | 2.4 | — | 2.4 | — | V |

2746 tbl 06

NOTE:

- At V_{CC} ≤ 2.0V, input leakages are undefined.

DC Electrical Characteristics Operating Temperature and Supply Voltage Range⁽²⁾ (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Condition | Version | 7133X20 7143X20 Com'l Only | | 7133X25 7143X25 Com'l & Ind | | 7133X35 7143X35 Com'l & Military | | Unit |
|------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|----------------------------------|------|-----------------------------------|------|-------------------------------------------|------|------|
| | | | | Typ. ⁽¹⁾ | Max. | Typ. ⁽¹⁾ | Max. | Typ. ⁽¹⁾ | Max. | |
| I _{CC} | Dynamic Operating Current (Both Ports Active) | $\overline{CE} = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(3)}$ | COM'L S L | 250 | 310 | 250 | 300 | 240 | 295 | mA |
| | | | | 230 | 280 | 230 | 270 | 210 | 250 | |
| | | | MIL & IND S L | — | — | 250 | 330 | 240 | 325 | |
| | | | | — | — | 230 | 300 | 220 | 295 | |
| I _{SB1} | Standby Current (Both Ports - TTL Level Inputs) | \overline{CE}_L and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L S L | 25 | 80 | 25 | 80 | 25 | 70 | mA |
| | | | | 25 | 70 | 25 | 70 | 25 | 60 | |
| | | | MIL & IND S L | — | — | 25 | 90 | 25 | 75 | |
| | | | | — | — | 25 | 80 | 25 | 65 | |
| I _{SB2} | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(4)}$ $f = f_{MAX}^{(3)}$ Active Port Outputs Disabled | COM'L S L | 140 | 200 | 140 | 200 | 120 | 180 | mA |
| | | | | 120 | 180 | 100 | 170 | 100 | 160 | |
| | | | MIL & IND S L | — | — | 140 | 230 | 120 | 200 | |
| | | | | — | — | 100 | 190 | 100 | 180 | |
| I _{SB3} | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports \overline{CE}_L and $\overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$, $f = 0^{(4)}$ | COM'L S L | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | mA |
| | | | | 0.2 | 5 | 0.2 | 4 | 0.2 | 4 | |
| | | | MIL & IND S L | — | — | 1.0 | 30 | 1.0 | 30 | |
| | | | | — | — | 0.2 | 10 | 0.2 | 10 | |
| I _{SB4} | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}^*A < 0.2V$ and $\overline{CE}^*B > V_{CC} - 0.2V^{(5)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Disabled $f = f_{MAX}^{(3)}$ | COM'L S L | 140 | 190 | 140 | 190 | 120 | 170 | mA |
| | | | | 120 | 170 | 120 | 170 | 100 | 150 | |
| | | | MIL & IND S L | — | — | 140 | 220 | 120 | 190 | |
| | | | | — | — | 120 | 200 | 100 | 170 | |

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| Symbol | Parameter | Test Condition | Version | 7133X45 7143X45 Com'l Only | | 7133X55 7143X55 Com'l, Ind & Military | | 7133X70/90 7143X70/90 Com'l & Military | | Unit |
|------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|----------------------------------|------|------------------------------------------------|------|-------------------------------------------------|------|------|
| | | | | Typ. ⁽¹⁾ | Max. | Typ. ⁽¹⁾ | Max. | Typ. ⁽¹⁾ | Max. | |
| I _{CC} | Dynamic Operating Current (Both Ports Active) | $\overline{CE} = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(3)}$ | COM'L S L | 230 | 290 | 230 | 285 | 230 | 280 | mA |
| | | | | 210 | 250 | 210 | 250 | 210 | 250 | |
| | | | MIL & IND S L | — | — | 230 | 315 | 230 | 310 | |
| | | | | — | — | 210 | 285 | 210 | 280 | |
| I _{SB1} | Standby Current (Both Ports - TTL Level Inputs) | \overline{CE}_L and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L S L | 25 | 75 | 25 | 70 | 25 | 70 | mA |
| | | | | 25 | 65 | 25 | 60 | 25 | 60 | |
| | | | MIL & IND S L | — | — | 25 | 80 | 25 | 75 | |
| | | | | — | — | 25 | 70 | 25 | 65 | |
| I _{SB2} | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(4)}$ $f = f_{MAX}^{(3)}$ Active Port Outputs Disabled | COM'L S L | 120 | 190 | 120 | 180 | 120 | 180 | mA |
| | | | | 100 | 170 | 100 | 160 | 100 | 160 | |
| | | | MIL & IND S L | — | — | 120 | 210 | 120 | 200 | |
| | | | | — | — | 100 | 190 | 100 | 180 | |
| I _{SB3} | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports \overline{CE}_L and $\overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$, $f = 0^{(4)}$ | COM'L S L | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | mA |
| | | | | 0.2 | 4 | 0.2 | 4 | 0.2 | 4 | |
| | | | MIL & IND S L | — | — | 1.0 | 30 | 1.0 | 30 | |
| | | | | — | — | 0.2 | 10 | 0.2 | 10 | |
| I _{SB4} | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}^*A < 0.2V$ and $\overline{CE}^*B > V_{CC} - 0.2V^{(5)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Disabled $f = f_{MAX}^{(3)}$ | COM'L S L | 120 | 180 | 120 | 170 | 120 | 170 | mA |
| | | | | 100 | 160 | 100 | 150 | 100 | 150 | |
| | | | MIL & IND S L | — | — | 120 | 200 | 120 | 190 | |
| | | | | — | — | 100 | 180 | 100 | 170 | |

2746 tbl 07b

NOTES:

- V_{CC} = 5V, T_A = +25°C for Typ., and are not production tested. I_{CCDC} = 180mA (typ.)
- 'X' in part number indicates power rating (SA or LA)
- At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ t_{rc}, and using "AC Test Conditions" of input levels of GND to 3V.
- f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Data Retention Characteristics

(LA Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

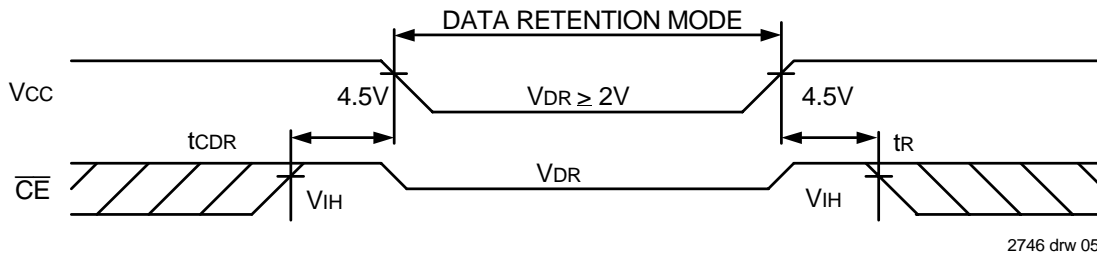
| Symbol | Parameter | Test Condition | 7133LA/7143LA | | | Unit |
|---------------------------------|--------------------------------------|----------------------------------------------------------------------|--------------------------------|---------------------|------|------|
| | | | Min. | Typ. ⁽¹⁾ | Max. | |
| V _{DR} | V _{CC} for Data Retention | V _{CC} = 2V | 2.0 | — | — | V |
| I _{CCDR} | Data Retention Current | $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | MIL. & IND. — | 100 | 4000 | μA |
| | | | COM'L. — | 100 | 1500 | |
| t _{CDR} ⁽³⁾ | Chip Deselect to Data Retention Time | | 0 | — | — | V |
| t _r ⁽³⁾ | Operation Recovery Time | | t _{rc} ⁽²⁾ | — | — | V |

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NOTES:

- V_{CC} = 2V, T_A = +25°C, and are not production tested.
- t_{rc} = Read Cycle Time
- This parameter is guaranteed by device characterization but is not production tested.

Data Retention Waveform



2746 drw 05

AC Test Conditions

| | |
|-------------------------------|--------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1, 2 and 3 |

2746 tbl 09

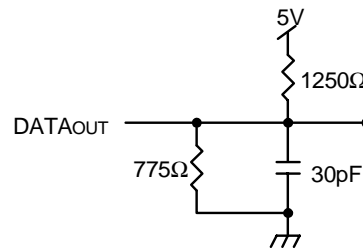


Figure 1. AC Output Test Load

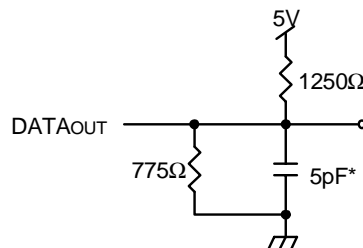


Figure 2. Output Load
(for t_{LZ}, t_{HZ}, t_{wz}, t_{ow})
*Including scope and jig

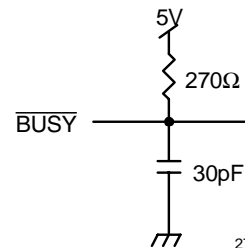


Figure 3. \overline{BUSY} Output Load
(IDT7133 only)

2746 drw 06

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽³⁾

| Symbol | Parameter | 7133X20 7143X20 Com'l Only | | 7133X25 7143X25 Com'l & Ind | | 7133X35 7143X35 Com'l & Military | | Unit |
|-------------------|------------------------------------------------|----------------------------------|------|-----------------------------------|------|-------------------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{ACE} | Chip Enable Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{AOE} | Output Enable Access Time | — | 12 | — | 15 | — | 20 | ns |
| t _{OH} | Output Hold from Address Change | 0 | — | 0 | — | 0 | — | ns |
| t _{LZ} | Output Low-Z Time ^(1,2) | 0 | — | 0 | — | 0 | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 12 | — | 15 | — | 20 | ns |
| t _{PU} | Chip Enable to Power Up Time ⁽²⁾ | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Chip Disable to Power Down Time ⁽²⁾ | — | 20 | — | 50 | — | 50 | ns |

2746 tbl 10a

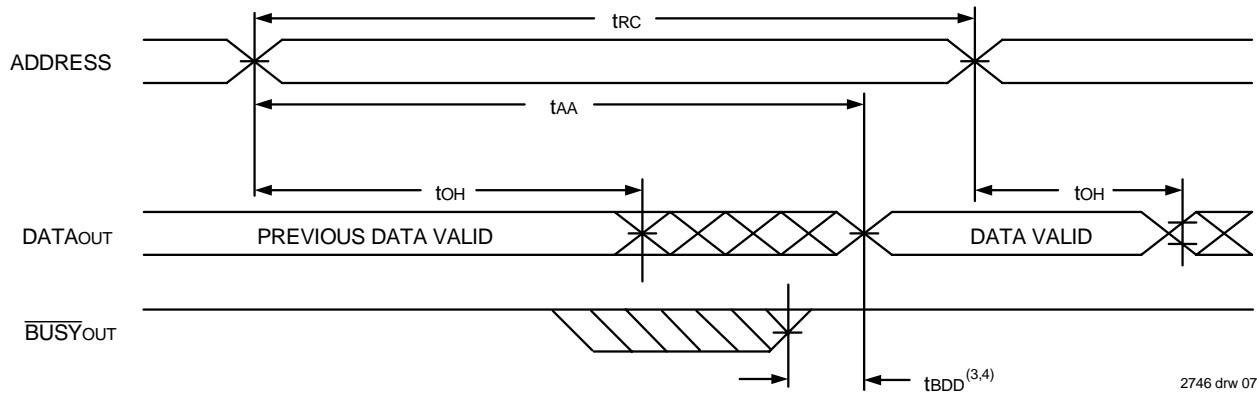
| Symbol | Parameter | 7133X45 7143X45 Com'l Only | | 7133X55 7143X55 Com'l, Ind & Military | | 7133X70/90 7143X70/90 Com'l & Military | | Unit |
|-------------------|------------------------------------------------|----------------------------------|------|------------------------------------------------|------|-------------------------------------------------|-------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 45 | — | 55 | — | 70/90 | — | ns |
| t _{AA} | Address Access Time | — | 45 | — | 55 | — | 70/90 | ns |
| t _{ACE} | Chip Enable Access Time | — | 45 | — | 55 | — | 70/90 | ns |
| t _{AOE} | Output Enable Access Time | — | 25 | — | 30 | — | 40/40 | ns |
| t _{OH} | Output Hold from Address Change | 0 | — | 0 | — | 0/0 | — | ns |
| t _{LZ} | Output Low-Z Time ^(1,2) | 0 | — | 5 | — | 5/5 | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 20 | — | 20 | — | 25/25 | ns |
| t _{PU} | Chip Enable to Power Up Time ⁽²⁾ | 0 | — | 0 | — | 0/0 | — | ns |
| t _{PD} | Chip Disable to Power Down Time ⁽²⁾ | — | 50 | — | 50 | — | 50/50 | ns |

2746 tbl 10b

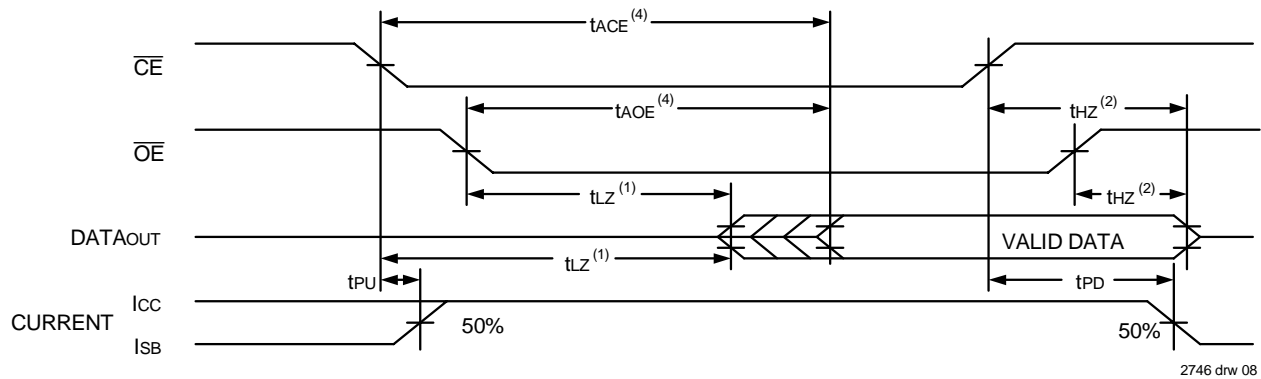
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE⁽⁵⁾



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE⁽⁵⁾



NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
2. Timing depends on which signal is deasserted first, \overline{OE} or \overline{CE} .
3. t_{BDD} delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, \overline{BUSY} has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, t_{AOE} , t_{ACE} , t_{AA} , or t_{BDD} .
5. $R/\overline{W} = V_{IH}$, and the address is valid prior to or coincidental with \overline{CE} transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

| Symbol | Parameter | 7133X20 7143X20 Com'l Only | | 7133X25 7143X25 Com'l & Ind | | 7133X35 7143X35 Com'l & Military | | Unit |
|--------------------|----------------------------------------------------|----------------------------------|------|-----------------------------------|------|-------------------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | |
| t _{wc} | Write Cycle Time ⁽³⁾ | 20 | — | 25 | — | 35 | — | ns |
| t _{ew} | Chip Enable to End-of-Write | 15 | — | 20 | — | 25 | — | ns |
| t _{aw} | Address Valid to End-of-Write | 15 | — | 20 | — | 25 | — | ns |
| t _{as} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{wp} | Write Pulse Width | 15 | — | 20 | — | 25 | — | ns |
| t _{wr} | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| t _{dw} | Data Valid to End-of-Write | 15 | — | 15 | — | 20 | — | ns |
| t _{hz} | Output High-Z Time ^(1,2) | — | 12 | — | 15 | — | 20 | ns |
| t _{dh} | Data Hold Time ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | ns |
| t _{wz} | Write Enable to Output in High-Z ^(1,2) | — | 12 | — | 15 | — | 20 | ns |
| t _{ow} | Output Active from End-of-Write ^(1,2,4) | 0 | — | 0 | — | 0 | — | ns |

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| Symbol | Parameter | 7133X45 7143X45 Com'l Only | | 7133X55 7143X55 Com'l, Ind & Military | | 7133X70/90 7143X70/90 Com'l & Military | | Unit |
|--------------------|----------------------------------------------------|----------------------------------|------|------------------------------------------------|------|-------------------------------------------------|-------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | |
| t _{wc} | Write Cycle Time ⁽³⁾ | 45 | — | 55 | — | 70/90 | — | ns |
| t _{ew} | Chip Enable to End-of-Write | 30 | — | 40 | — | 50/50 | — | ns |
| t _{aw} | Address Valid to End-of-Write | 30 | — | 40 | — | 50/50 | — | ns |
| t _{as} | Address Set-up Time | 0 | — | 0 | — | 0/0 | — | ns |
| t _{wp} | Write Pulse Width | 30 | — | 40 | — | 50/50 | — | ns |
| t _{wr} | Write Recovery Time | 0 | — | 0 | — | 0/0 | — | ns |
| t _{dw} | Data Valid to End-of-Write | 20 | — | 25 | — | 30/30 | — | ns |
| t _{hz} | Output High-Z Time ^(1,2) | — | 20 | — | 20 | — | 25/25 | ns |
| t _{dh} | Data Hold Time ⁽⁴⁾ | 5 | — | 5 | — | 5/5 | — | ns |
| t _{wz} | Write Enable to Output in High-Z ^(1,2) | — | 20 | — | 20 | — | 25/25 | ns |
| t _{ow} | Output Active from End-of-Write ^(1,2,4) | 5 | — | 5 | — | 5/5 | — | ns |

2746 tbl 11b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage from the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but not production tested.
3. For MASTER/SLAVE combination, t_{wc} = t_{BAA} + t_{wr} + t_{wp}, since R_W = V_{IL} must occur after t_{BAA}.
4. The specification for t_{dh} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{dh} and t_{ow} values will vary over voltage and temperature, the actual t_{dh} will always be smaller than the actual t_{ow}.
5. 'X' in part number indicates power rating (SA or LA).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁶⁾

| Symbol | Parameter | 7133X20 7143X20 Com'l Only | | 7133X25 7143X25 Com'l & Ind | | 7133X35 7143X35 Com'l & Military | | Unit |
|--------------------------------------------|---------------------------------------------------------------|----------------------------------|------|-----------------------------------|------|-------------------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| BUSY TIMING (For MASTER 71V33) | | | | | | | | |
| t _{BAA} | $\overline{\text{BUSY}}$ Access Time from Address | — | 20 | — | 20 | — | 30 | ns |
| t _{BDA} | $\overline{\text{BUSY}}$ Disable Time from Address | — | 20 | — | 20 | — | 30 | ns |
| t _{BAC} | $\overline{\text{BUSY}}$ Access Time from Chip Enable | — | 20 | — | 20 | — | 25 | ns |
| t _{BDC} | $\overline{\text{BUSY}}$ Disable Time from Chip Enable | — | 17 | — | 20 | — | 25 | ns |
| t _{WDD} | Write Pulse to Data Delay ⁽¹⁾ | — | 40 | — | 50 | — | 60 | ns |
| t _{DDD} | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 30 | — | 35 | — | 45 | ns |
| t _{BDD} | $\overline{\text{BUSY}}$ Disable to Valid Data ⁽²⁾ | — | 25 | — | 30 | — | 35 | ns |
| t _{APS} | Arbitration Priority Set-up Time ⁽³⁾ | 5 | — | 5 | — | 5 | — | ns |
| t _{WH} | Write Hold After $\overline{\text{BUSY}}$ ⁽⁶⁾ | 20 | — | 20 | — | 25 | — | ns |
| BUSY INPUT TIMING (For SLAVE 71V43) | | | | | | | | |
| t _{WB} | $\overline{\text{BUSY}}$ Input to Write ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | ns |
| t _{WH} | Write Hold After $\overline{\text{BUSY}}$ ⁽⁶⁾ | 20 | — | 20 | — | 25 | — | ns |
| t _{WDD} | Write Pulse to Data Delay ⁽¹⁾ | — | 40 | — | 50 | — | 60 | ns |
| t _{DDD} | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 30 | — | 35 | — | 45 | ns |

2746 tbl 12a

| Symbol | Parameter | 7133X45 7143X45 Com'l Only | | 7133X55 7143X55 Com'l, Ind & Military | | 7133X70/90 7143X70/90 Com'l & Military | | Unit |
|--------------------------------------------|---------------------------------------------------------------|----------------------------------|------|------------------------------------------------|------|-------------------------------------------------|-------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| BUSY TIMING (For MASTER 71V33) | | | | | | | | |
| t _{BAA} | $\overline{\text{BUSY}}$ Access Time from Address | — | 40 | — | 40 | — | 45/45 | ns |
| t _{BDA} | $\overline{\text{BUSY}}$ Disable Time from Address | — | 40 | — | 40 | — | 45/45 | ns |
| t _{BAC} | $\overline{\text{BUSY}}$ Access Time from Chip Enable | — | 30 | — | 35 | — | 35/35 | ns |
| t _{BDC} | $\overline{\text{BUSY}}$ Disable Time from Chip Enable | — | 25 | — | 30 | — | 30/30 | ns |
| t _{WDD} | Write Pulse to Data Delay ⁽¹⁾ | — | 80 | — | 80 | — | 90/90 | ns |
| t _{DDD} | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 55 | — | 55 | — | 70/70 | ns |
| t _{BDD} | $\overline{\text{BUSY}}$ Disable to Valid Data ⁽²⁾ | — | 40 | — | 40 | — | 40/40 | ns |
| t _{APS} | Arbitration Priority Set-up Time ⁽³⁾ | 5 | — | 5 | — | 5/5 | — | ns |
| t _{WH} | Write Hold After $\overline{\text{BUSY}}$ ⁽⁶⁾ | 30 | — | 30 | — | 30/30 | — | ns |
| BUSY INPUT TIMING (For SLAVE 71V43) | | | | | | | | |
| t _{WB} | $\overline{\text{BUSY}}$ Input to Write ⁽⁴⁾ | 0 | — | 0 | — | 0/0 | — | ns |
| t _{WH} | Write Hold After $\overline{\text{BUSY}}$ ⁽⁶⁾ | 30 | — | 30 | — | 30/30 | — | ns |
| t _{WDD} | Write Pulse to Data Delay ⁽¹⁾ | — | 80 | — | 80 | — | 90/90 | ns |
| t _{DDD} | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 55 | — | 55 | — | 70/70 | ns |

2746 tbl 12b

NOTES:

- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
- t_{BDD} is calculated parameter and is greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{WR} (actual).
- To ensure that the earlier of the two ports wins.
- To ensure that the write cycle is inhibited on port "B" during contention on port "A".
- To ensure that a write cycle is completed on port "B" after contention on port "A".
- 'X' in part number indicates power rating (SA or LA).

Timing Waveform of Write Cycle No. 1 ($\overline{R/\overline{W}}$ Controlled Timing)^(1,5,8)



2746 drw 09

Write Cycle No. 2 (\overline{CE} Controlled Timing)^(1,5)

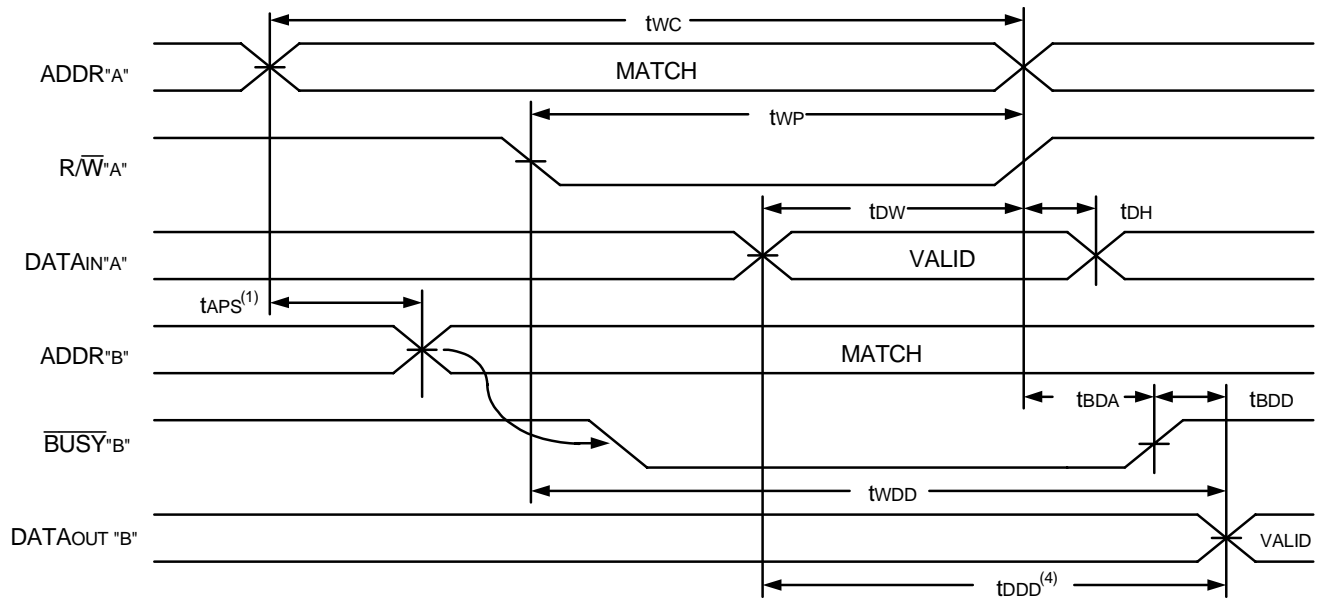


2746 drw 10

NOTES:

1. $\overline{R/\overline{W}}$ or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and a $\overline{R/\overline{W}} = V_{IL}$.
3. t_{WR} is measured from the earlier of \overline{CE} or $\overline{R/\overline{W}}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} LOW transition occurs simultaneously with or after the $\overline{R/\overline{W}}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (\overline{CE} or $\overline{R/\overline{W}}$) is asserted last.
7. Timing depends on which enable signal is de-asserted first, \overline{CE} or \overline{OE} .
8. If \overline{OE} is LOW during a $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
9. $\overline{R/\overline{W}}$ for either upper or lower byte.

Timing Waveform of Write with Port-to-Port Read and **BUSY**^(1,2,3)



NOTES:

1. To ensure that the earlier of the two ports wins, tAPs is ignored for Slave (IDT7143).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

2746 drw 11

Timing Waveform of Write with **BUSY**⁽³⁾



2746 drw 12

NOTES:

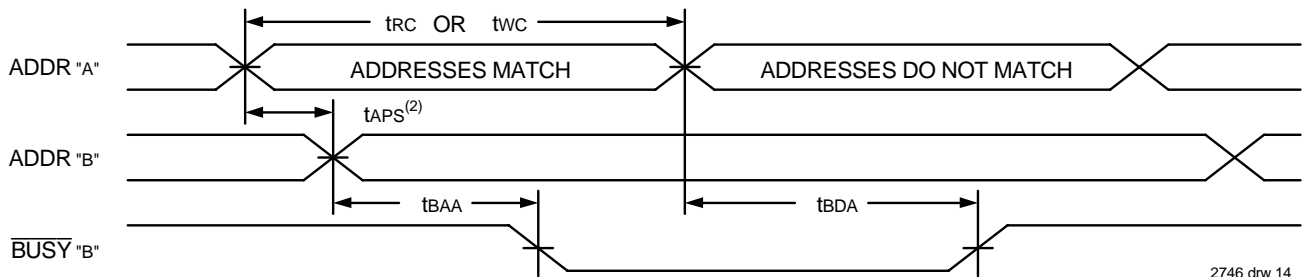
1. tWH must be met for both **BUSY** input (IDT7143, slave) and output (IDT7133, master).
2. **BUSY** is asserted on port "B" blocking R/W'B', until **BUSY**'B' goes HIGH.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Timing Waveform of **BUSY** Arbitration Controlled by **CE** Timing⁽¹⁾



2746 drw 13

Timing Waveform of **BUSY** Arbitration Controlled by Addresses⁽¹⁾



2746 drw 14

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the **BUSY** will be asserted on one side or the other, but there is no guarantee on which side **BUSY** will be asserted (IDT7133 only).

Functional Description

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (\overline{CE} HIGH). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table 1.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The \overline{BUSY} pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a \overline{BUSY} indication, the write signal is gated internally to prevent the write from proceeding.

The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of \overline{BUSY} logic is not desirable, the \overline{BUSY} logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. If desired, unintended write operations can be prevented to a port by tying the \overline{BUSY} pin for that port LOW. The \overline{BUSY} outputs on the IDT 7133 RAM are open drain and require pull-up resistors.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7133/43 RAM array in width while using \overline{BUSY} logic, one master part is used to decide which side of the RAM array will receive a \overline{BUSY} indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the \overline{BUSY} signal as a write inhibit signal. Thus on the IDT7133 RAM the \overline{BUSY} pin is an output and on the IDT7143 RAM, the \overline{BUSY} pin is an input (see Figure 3).



Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its \overline{BUSY}_L while another activates its \overline{BUSY}_R signal. Both sides are now \overline{BUSY} and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has \overline{BUSY} inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the \overline{BUSY} input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past \overline{BUSY} to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to \overline{BUSY} from the MASTER.

Truth Table I – Non-Contention Read/Write Control⁽⁴⁾

| LEFT OR RIGHT PORT ⁽¹⁾ | | | | | | Function |
|-----------------------------------|-------------------|-----------------|-----------------|---------------------|---------------------|------------------------------------------------------------------------------------------------------------|
| R/W _{LB} | R/W _{UB} | \overline{CE} | \overline{OE} | I/O ₀₋₇ | I/O ₈₋₁₅ | |
| X | X | H | X | Z | Z | Port Disabled and in Power Down Mode, ISB2, ISB4 |
| X | X | H | X | Z | Z | CE _R = CE _L = V _{IH} , Power Down Mode, ISB1 or ISB3 |
| L | L | L | X | DATA _{IN} | DATA _{IN} | Data on Lower Byte and Upper Byte Written into Memory ⁽²⁾ |
| L | H | L | L | DATA _{IN} | DATA _{OUT} | Data on Lower Byte Written into Memory ⁽²⁾ , Data in Memory Output on Upper Byte ⁽³⁾ |
| H | L | L | L | DATA _{OUT} | DATA _{IN} | Data in Memory Output on Lower Byte ⁽³⁾ , Data on Upper Byte Written into Memory ⁽²⁾ |
| L | H | L | H | DATA _{IN} | Z | Data on Lower Byte Written into Memory ⁽²⁾ |
| H | L | L | H | Z | DATA _{IN} | Data on Upper Byte Written into Memory ⁽²⁾ |
| H | H | L | L | DATA _{OUT} | DATA _{OUT} | Data in Memory Output on Lower Byte and Upper Byte |
| H | H | L | H | Z | Z | High Impedance Outputs |

2746 tbl 13

NOTES:

1. A_{0L} - A_{10L} ≠ A_{0R} - A_{10R}
2. If \overline{BUSY} = LOW, data is not written.
3. If \overline{BUSY} = LOW, data may not be valid, see twDD and tDD timing.
4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High-Impedance, "LB" = Lower Byte, "UB" = Upper Byte

Truth Table II — Address **BUSY** Arbitration

| Inputs | | | Outputs | | Function |
|-------------------|-------------------|------------------------------------------------------------------------|------------------------------------|------------------------------------|------------------------------|
| \overline{CE}_L | \overline{CE}_R | A _{0L} -A _{10L} A _{0R} -A _{10R} | \overline{BUSY}_L ⁽¹⁾ | \overline{BUSY}_R ⁽¹⁾ | |
| X | X | NO MATCH | H | H | Normal |
| H | X | MATCH | H | H | Normal |
| X | H | MATCH | H | H | Normal |
| L | L | MATCH | (2) | (2) | Write Inhibit ⁽³⁾ |

2746 tbl 14

NOTES:

1. Pins \overline{BUSY}_L and \overline{BUSY}_R are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the \overline{BUSY} input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either \overline{BUSY}_L or \overline{BUSY}_R = V_{IL} will result \overline{BUSY}_L and \overline{BUSY}_R outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when \overline{BUSY}_L outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when \overline{BUSY}_R outputs are driving LOW regardless of actual logic level on the pin.

Ordering Information



NOTES:

- Contact your local sales office for industrial temp. range for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

| | | |
|-----------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12/18/98: | | Initiated datasheet document history |
| | | Converted to new format |
| | | Cosmetic and typographical corrections |
| | | Added additional notes to pin configurations |
| | Page 2 | Corrected PN100 pinout |
| 02/17/99: | | Corrected PF ordering code |
| 03/09/99: | | Cosmetic and typographical corrections |
| 06/09/99: | | Changed drawing format |
| 10/01/99: | | Added Industrial Temperature Ranges and removed corresponding notes |
| 11/10/99: | | Replaced IDT logo |
| 04/01/00: | | Changed ±500mV to 0mV in notes |
| | Page 2 | Fixed overbar in pinout |
| 06/26/00: | Page 4 | Increased storage temperature parameters |
| | | Clarified TA parameter |
| | Page 5 | DC Electrical parameters—changed wording from "open" to "disabled" |
| 01/31/06: | Page 1 | Added green availability to features |
| | Page 16 | Added green indicator for ordering information |
| 10/21/08: | Page 16 | Removed "IDT" from orderable part number |
| 01/16/13: | Page 1, 5, 7, 9 & 10 | Removed Military 25ns & 45ns & Industrial 35ns speed grades from Features and from the headers of the MIL & IND of the DC Chars and AC Chars tables to indicate this change |
| | Page 5 | Removed the Typ & Max values for the MIL & IND temp range from the 7133x45 and 7143x45 speed grade offering from the DC Chars tables to indicate this change, see table 07b |

Datasheet Document History (con't.).

| | |
|------------|------------------------------------------------------------------------------------------------------------------------|
| Page 4 | Removed annotation for footnote 3 in the Absolute Maximum Ratings table |
| Page 8 & 9 | Typo/correction |
| Page 16 | Added T & R indicator to and removed Military 25ns & 45ns & Industrial 35ns speed grades from the ordering information |
| 06/19/18: | Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018 |



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