MIC23099

Single AA/AAA Cell Step-Up/Step-Down Regulators with Battery Monitoring

General Description

The MIC23099 is a high-efficiency, low-noise, dual-output, integrated power-management solution for single-cell alkaline or NiMH battery applications. The synchronous boost output voltage (V_{OUT1}) is enabled first and is powered from the battery. Next the synchronous buck output (V_{OUT2}), which is powered from the boost output voltage, is enabled. This configuration allows V_{OUT2} to be independent of battery voltage, thereby allowing the buck output voltage to be higher or lower than the battery voltage.

To minimize switching artifacts in the audio band, both the converters are design to operate with a minimum switching frequency of 80kHz for the buck and 100kHz for the boost. The high current boost has a maximum switching frequency of 1MHz, minimizing the solution footprint.

The MIC23099 incorporates both battery-management functions and fault protection. The low-battery level is indicated by an external LED connected to the LED pin. In addition, a supervisory circuit monitors each output and asserts a power-good (PG) signal when the sequencing is done or de-asserted when a fault condition occurs.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

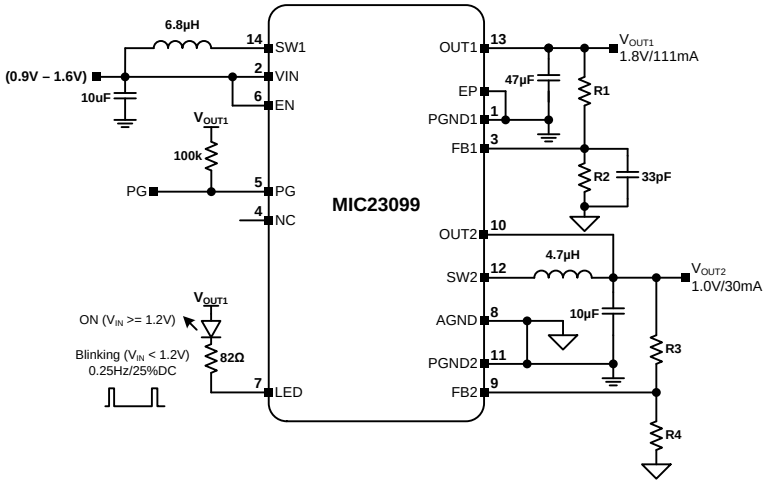
Features

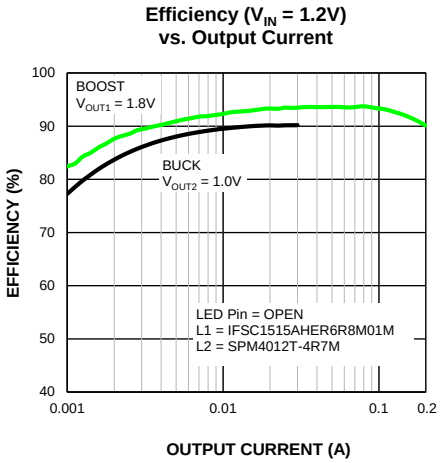
- V_{IN} range from 0.85V to 1.6V
- V_{OUT1} (step-up) adjustable from 1.8V to 3.3V
- V_{OUT2} (step-down) adjustable from 1.0V to V_{OUT1}
- V_{OUT1}/400mW and V_{OUT2}/30mA from a single cell
- Minimizes switching noise in the audio band
- Step-up regulator with output disconnect in shutdown
- V_{OUT1}, above 90% efficiency for 5mA to 200mA
- Anti-ringing control circuit to minimize EMI
- Turn-on inrush current limiting and soft-start
- Automatic output discharge
- Low-battery indicator
- Power Good (PG) output
- Low output ripple < 10mV
- Short-circuit and thermal protection
- 14-pin 2.5mm × 2.5mm × 0.55mm thin QFN (TQFN) package
- –40°C to +125°C junction temperature range

Applications

- Audio headsets
- Portable applications

Typical Application





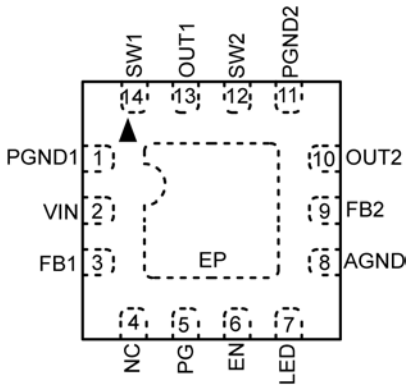
Ordering Information

Part Number	Output Voltages	Marking[1]	Junction Temperature Range	Package[2]	Lead Finish
MIC23099YFT	Adjustable	23099	–40°C to +125°C	14-Pin 2.5mm × 2.5mm × 0.55mm Thin QFN	Pb-Free

Notes:

1. Pin 1 identifier = "▲".
2. Thin QFN is a Green RoHs-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



14-Pin 2.5mm × 2.5mm QFN (FT)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND1	Power Ground 1: The power ground for the synchronous boost DC/DC converter power stage.
2	VIN	Battery Voltage Supply (Input): The internal circuitry operates from the battery voltage during start up. Once V_{OUT1} exceeds V_{IN}, the bias current comes from V_{OUT1}. The start-up sequence is initiated once the battery voltage is above 0.9V. The boost output (V_{OUT1}) is power-up first, then the buck output (V_{OUT2}) follows. If the battery voltage falls below 0.85V for more than 15 cool-off cycles, both outputs are simultaneously turned off and an internal resistor discharges the output capacitors to 0V.
3	FB1	Feedback 1 (Input): Connect a resistor divider network to this pin to set the output voltage for the synchronous boost regulator. Resistors should be selected based on a nominal V_{FB1} = 0.6V.
4	NC	No Connect Pin (NC): Leave open, do not connect to ground.
5	PG	Power Good (Output): This is an open drain, active high output. When V_{IN}, V_{FB1} or V_{FB2} are below their nominal voltages the Power Good output gets pulled low after a de-glitch period. The PG pin will be pulled low without delay when the enable is set low.
6	EN	Enable (input): A logic level control of both outputs. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 1µA). When the EN pin goes high, the start-up sequence is initiated. The boost output (V_{OUT1}) is powered up first then the buck output (V_{OUT2}) follows. When EN goes low, both outputs are immediately turned off and the boost output (V_{OUT1}) is completely disconnected from the input voltage. Then both converters output capacitors are discharged to ground through an internal pull down circuit. The EN pin has a 4MΩ resistance to AGND.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
7	LED	LED (Output): This is an open drain output that is used for a low battery indicator. Under normal conditions, the LED is always ON. If the battery voltage is between 1.2V to 0.85V, the external LED will blink with a duty cycle of 25% at 0.25Hz. The LED will be OFF if the battery voltage falls below 0.85V for more than 15 cool-off cycles or the EN pin is low.
8	AGND	Analog Ground: The analog ground for both regulator control loops.
9	FB2	Feedback 2 (Input): Connect a resistor divider network to this pin to set the output voltage for the synchronous buck regulator. Resistors should be selected based on a nominal V_{FB2} = 0.6V.
10	OUT2	Output Voltage 2 (Input): If the EN is low or the power good output is pulled low, an internal resistor discharges V_{OUT2} output capacitance to 0V. Also, if the inductor current falls to zero an internal anti-ringing switch is connected between the SW2 and OUT2 pins to minimize the switch node ringing.
11	PGND2	Power Ground 2: The power ground for the synchronous buck DC/DC converter power stage.
12	SW2	Switch Pin 2 (Input): Inductor connection for the synchronous step-down regulator. Connect the inductor between V_{OUT2} and the SW2 pin. Due to the high-speed switching on this pin, the SW2 pin should be routed away from sensitive nodes and trace length should be kept as short and wide as possible to reduce EMI. If the inductor current falls to zero or EN is low, then an internal anti-ringing switch is connected between the SW2 and VOUT2 pins to minimize the switch node ringing.
13	OUT1	Output 1 (Output): Output of the synchronous boost regulator and is the bias supply once V_{OUT1} is greater than V_{IN}. The boost output also serves as the supply input for the buck converter (V_{OUT2}). If the EN is low or the power good output is pulled low, an internal resistor discharges V_{OUT1} output capacitance to 0V.
14	SW1	Switch Pin 1 (Input): Inductor connection for the synchronous boost regulator. Connect the inductor between V_{IN} and SW1. Due to the high-speed switching on this pin, the SW1 pin should be routed away from sensitive nodes and trace length should be kept as short and wide as possible to reduce EMI. If the inductor current falls to zero, an internal anti-ringing switch is connected between the SW1 and VIN pins to minimize the switch node ringing.
EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane.

Absolute Maximum Ratings[3]

Supply Voltage (V_{IN}) ..... –0.3V to +6.0V
Switch Voltage (V_{SW1}) ..... –0.3V to +6.0V
Switch Voltage (V_{SW2}) ..... –0.8V to +6.0V
Enable Voltage (V_{EN}) ..... –0.3V to V_{IN}
Feedback Voltage (V_{FB}) ..... –0.3V to +6.0V
LED Output (V_{LED}) ..... –0.3V to +6.0V
Power Good (V_{PG}) ..... –0.3V to +6.0V
AGND to PGND1, PGND2 ..... –0.3V to +0.3V
Ambient Storage Temperature (Ts) ..... –65°C to +150°C
ESD HBM Rating[6] 2kV
ESD MM Rating 200V

Operating Ratings[4]

Input Voltage after Start-Up (V_{IN}) ..... +0.875V to +1.6V
Enable Voltage (V_{EN}) ..... 0V to V_{IN}
LED Output (V_{LED}) ..... 0V to V_{OUT1}
Output Voltage Range (V_{OUT1}) ..... +1.8V to +3.3V
Output Voltage Range (V_{OUT2}) ..... +1.0V to V_{OUT1}
Junction Temperature (T_J)[5] ..... –40°C to +125°C
Junction Thermal Resistance
2.5mm × 2.5mm Thin QFN-14 (θ_{JA}) ..... +70°C/W
2.5mm × 2.5mm Thin QFN-14 (θ_{JC}) ..... +25°C/W

Electrical Characteristics[7]

$V_{IN} = V_{EN}$ = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = 1.0V; L_{OUT1} = 6.8µH; L_{OUT2} = 4.7µH; C_{OUT1} = 47µF; C_{OUT2} = 10µF
T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Input Supply (VIN)					
Minimum Start Up Voltage	V_{IN} Rising; R_{LOAD} ≥ 500Ω, I_{OUT2} = 0mA		0.75	**0.9**	V
Quiescent Current - PFM Mode	I_{OUT1} , I_{OUT2} = 0mA (Switching, Closed Loop) Measured at V_{IN} with LED pin open		200	**270**	µA
Quiescent Current - PFM Mode	I_{OUT1} , = 2mA; I_{OUT2} = 10mA (Switching, Closed Loop) Measured at V_{IN}		12.6		mA
Shutdown Current	V_{EN} = 0V; V_{IN} = 1.6V Measured at V_{IN}		0.02	**2**	µA
Enable Input (EN)					
EN Logic Level High to Start Up	V_{EN} Rising, Regulator Enabled	**0.8**	0.58		V
EN Logic Level Low	V_{EN} Falling, Regulator Shutdown		0.5	**0.2**	V
EN Bias Current	V_{EN} = 0V (Regulator Shutdown)		0.3	**1**	µA
EN Pull-Down Resistance	I_{EN} = 0.5µA into Pin	**3.0**	4.0	**5.0**	MΩ
Solution Efficiency					
System Efficiency	V_{IN} = 1.25V; V_{OUT1} = 1.8V; V_{OUT2} = 1.0V P_{OUT1} = 8mW; P_{OUT2} = 20mW		88		%
System Efficiency	V_{IN} = 1.25V; V_{OUT1} = 1.8V; V_{OUT2} = 1.0V P_{OUT1} = 80mW; P_{OUT2} = 20mW		92		%

Notes:

3. Absolute maximum ratings indicate limits beyond which damage to the component may occur.
4. The device is not guaranteed to function outside its operating ratings.
5. The maximum allowable power dissipation is a function of the maximum junction temperature ($T_{J(MAX)}$), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
6. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
7. Specification for packaged product only.
8. Guaranteed by design.

Electrical Characteristics[7] (Continued)

$V_{IN} = V_{EN}$ = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = 1.0V; L_{OUT1} = 6.8µH; L_{OUT2} = 4.7µH; C_{OUT1} = 47µF; C_{OUT2} = 10µF;
T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Fault Conditions					
V_{IN} and $V_{OUT1, 2}$ Fault Conditions					
V_{IN} Turn Off Threshold Voltage	V_{IN} Falling; after Start Up	0.825	0.85	0.875	V
PG Deglitch Delay, V_{IN} Fault	V_{IN} Falling below 0.85V to V_{PG} = LOW	120		180	ms
PG Deglitch Delay, $V_{OUT1, 2}$ Fault	V_{OUT1} or V_{OUT2} falling below 90% of target value to V_{PG} = LOW	60		120	ms
Cool OFF Delay Time	V_{PG} = Low to V_{OUT1} Enabled C_{OUT1} = 47µF; C_{OUT2} = 10µF	750	1300	2250	ms
Hiccup Cycles before Latch OFF	Counts Cool OFF cycles		15		Cycles
OUT1 Active Discharge Resistance	V_{EN} = 0V		500	700	Ω
OUT2 Active Discharge Resistance	V_{EN} = 0V		500	700	Ω
Power Good Output (PG)					
PG Threshold Voltage	V_{REF1} Rising or Falling	90	92.5	95	$\%V_{REF1}$
PG Threshold Voltage	V_{REF2} Rising or Falling	90	92.5	95	$\%V_{REF2}$
PG Output Low Voltage	I_{PG} = 1mA (sinking), V_{EN} = 0V		0.1	**0.5**	V
PG Leakage Current	V_{PG} = 1.8V; V_{EN} = 1.8V	**–1**	0.01	**1**	µA
PG Turn-On Delay		10		50	ms
LED Low-Battery Indicator Output (LED)					
Low-Battery Threshold	V_{IN} Falling	**1.15**	1.2	**1.25**	V
Low-Battery Hysteresis	V_{IN} Rising			31	mV
LED Flash Frequency	V_{IN} = 1.15V; V_{EN} = 1.15V	0.125	0.25	0.5	Hz
LED Flash Duty Cycle	V_{IN} = 1.15V; V_{EN} = 1.15V	22.5	25	27.5	%
LED Output Leakage Current	V_{LED} = 4.0V; V_{EN} = 0V		0.01	1	µA
LED Switch On-Resistance	$V_{IN} = V_{EN}$ = 1.25V; I_{LED} = 1.0mA			25	Ω
Thermal Protection					
Thermal Shutdown	T_J Rising		150		°C
Thermal Hysteresis	Temperature Decreasing		20		°C

Electrical Characteristics[7] (Continued)

V_{IN} = V_{EN} = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = 1.0V; L_{OUT1} = 6.8µH; L_{OUT2} = 4.7µH; C_{OUT1} = 47µF; C_{OUT2} = 10µF; T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

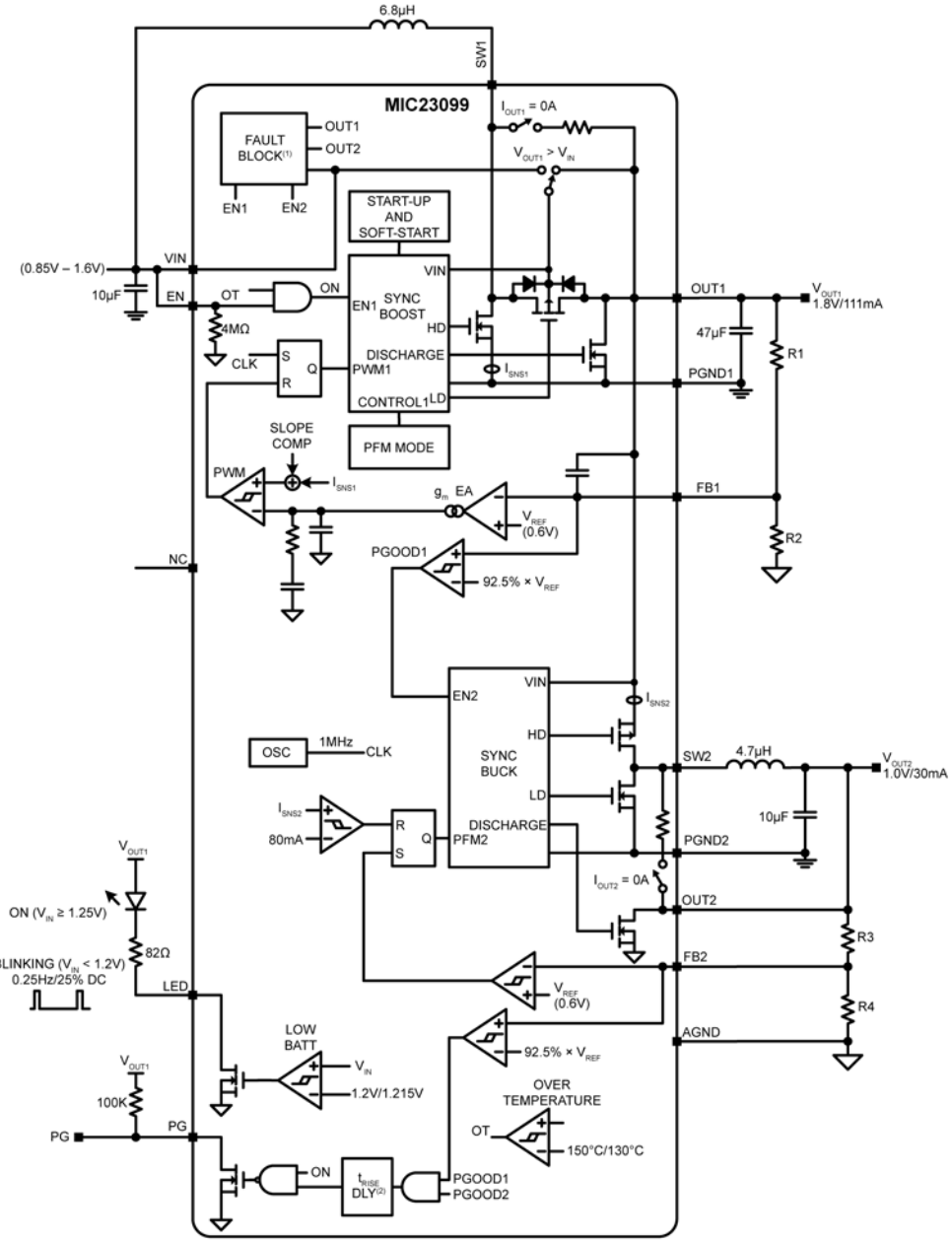
Parameter	Test Conditions	Min.	Typ.	Max.	Units
Boost					
Boost Reference (FB1)					
Feedback Regulation Voltage	V_{IN} = 0.9V to 1.5V PWM Mode	**0.579**	0.6	**0.621**	V
FB Bias Current	V_{FB1} = 0.6V		1	500	nA
Soft-Start Time	V_{OUT1}: 10% to 90% of target value R_{LOAD} = 500Ω; C_{OUT1} = 47µF		5		ms
Boost Internal MOSFETs					
High-Side On-Resistance	I_{SW1} = 100mA; V_{IN} = 1.25V		200		mΩ
Low-Side On-Resistance	I_{SW1} = -100mA; V_{IN} = 1.25V		140		mΩ
Leakage Current into SW1	V_{SW} = 4.0V, V_{OUT1} = 0V, V_{EN} = 0V, V_{IN} = 4.0V		0.01	**2**	µA
Anti-Ringing Resistance			80	140	Ω
Boost Switching Frequency					
Switching Frequency	PWM Mode	0.9	1.0	1.1	MHz
Minimum Switching Frequency[8]	P_{OUT1} = 20mW (PFM Mode)	100			kHz
Minimum Duty Cycle	V_{FB1} = 0.7V		15		%
Maximum Duty Cycle	V_{FB1} = 0.5V		85		%
Boost Current Limit					
Maximum Output Power	V_{OUT1}>1.8V; I_{OUT2} = 0mA		450		mW
Current-Limit Threshold (NMOS)	V_{FB1} = 0.5V	**1.0**	1.5	**2.0**	A
Current-Limit Threshold (PMOS)	V_{FB1} = 0.5V	1.5	2.5	3.0	A
Linear Mode Current Limit (PMOS)	V_{IN}=1.25V, V_{OUT1} = 0V	56	80	180	mA
Boost Power Supply Rejection					
PSRR ($\Delta V_{IN}/\Delta_{VOUT1}$)	ΔV_{IN} = 200mVp-p, f = 217Hz, I_{OUT1} = PFM		50		dB
PSRR ($\Delta V_{IN}/\Delta_{VOUT1}$)	ΔV_{IN} = 200mVp-p, f = 1.0kHz, I_{OUT1} = PFM		50		dB
PSRR ($\Delta V_{IN}/\Delta_{VOUT1}$)	ΔV_{IN} = 200mVp-p, f = 20kHz, I_{OUT1} = PFM		42		dB

Electrical Characteristics[7] (Continued)

V_{IN} = V_{EN} = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = 1.0V; L_{OUT1} = 6.8µH; L_{OUT2} = 4.7µH; C_{OUT1} = 47µF; C_{OUT2} = 10µF; T_A = 25°C, unless otherwise noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

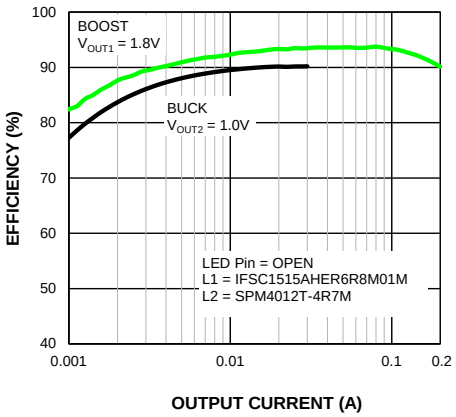
Parameter	Test Conditions	Min.	Typ.	Max.	Units
Buck					
Buck Reference (FB2)					
Feedback Regulation Voltage	V_{out1} = 1.8V to 3.3V I_{OUT2} = 6mA to 30mA; (±3.5%)	**0.579**	0.6	**0.621**	V
FB Bias Current	V_{FB2} = 0.6V		1	500	nA
Soft-Start Time	V_{OUT2}: 10% to 90% of target value I_{OUT2} = 0mA; C_{OUT2} = 10µF		0.1		ms
Buck Internal MOSFETs					
High-Side On-Resistance	I_{SW2} = 100mA; V_{OUT1} = 1.8V		560		mΩ
Low-Side On-Resistance	I_{SW2} = -100mA; V_{OUT1} = 1.8V		380		mΩ
Leakage Current into SW2	V_{OUT1} = 3.3V, V_{SW2} = 3.3V, V_{EN} = 0V, V_{OUT2} = 3.3V		0.01	2	µA
Leakage Current out of SW2	V_{OUT1} = 3.3V, V_{SW2} = 0V, V_{EN} = 0V, V_{OUT2}=0V		0.01	0.5	µA
Anti-Ringing Resistance			80	140	Ω
Buck Switching Frequency					
Minimum Switching Frequency[8]	P_{OUT2} = 8mW (PFM Mode)	80			kHz
Maximum Duty Cycle	V_{FB2} = 0.5V		100		%
Buck Current Limit					
Maximum Output Current			30		mA
Current-Limit Threshold (PMOS)	V_{FB2} = 0.5V		80	120	mA
Buck Power Supply Rejection					
PSRR ($\Delta V_{OUT1}/\Delta_{VOUT2}$)	ΔV_{OUT1} = 200mVp-p, f = 217Hz, I_{OUT2} = 10mA		50		dB
PSRR ($\Delta V_{OUT1}/\Delta_{VOUT2}$)	ΔV_{OUT1} = 200mVp-p, f = 1.0kHz, I_{OUT2} = 10mA		50		dB
PSRR ($\Delta V_{OUT1}/\Delta_{VOUT2}$)	ΔV_{OUT1} = 200mVp-p, f = 20kHz, I_{OUT2} = 10mA		42		dB

Block Diagram

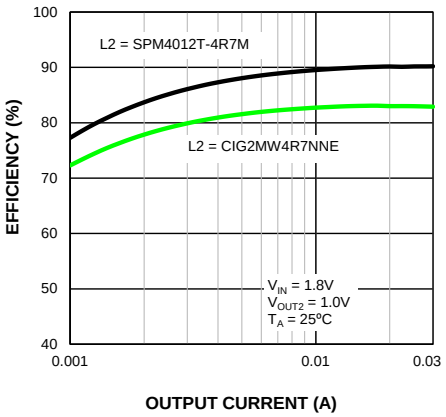


Typical Characteristics

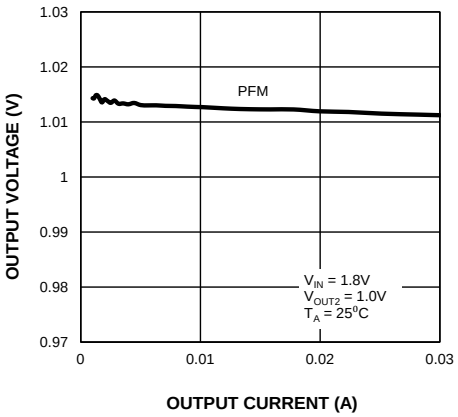
Efficiency (V_{IN} = 1.2V) vs. Output Current



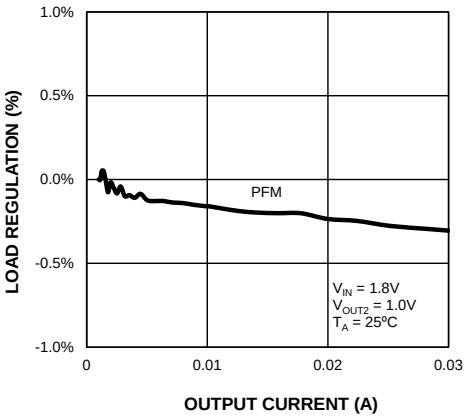
Buck Efficiency (V_{IN} = 1.8V) vs. Output Current



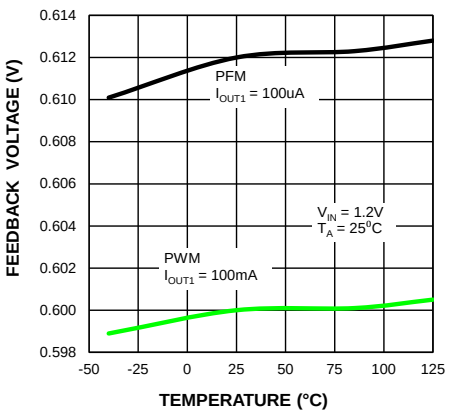
Buck Output Voltage vs. Output Current



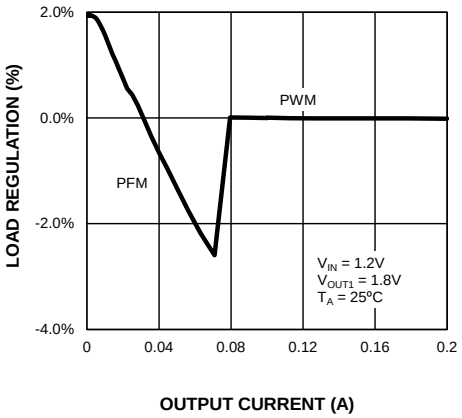
Buck Load Regulation vs. Output Current



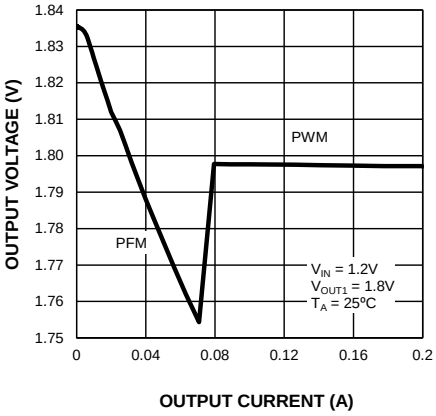
Boost Feeback Voltage vs. Temperature



Boost Output Voltage vs. Output Current

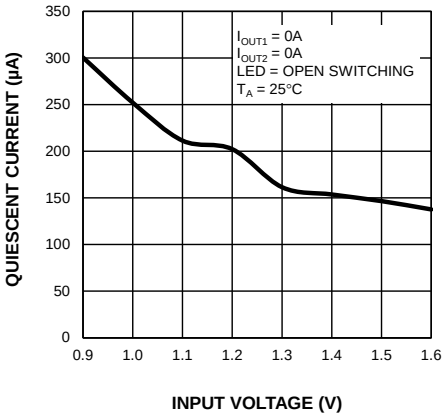


Boost Output Voltage vs. Output Current

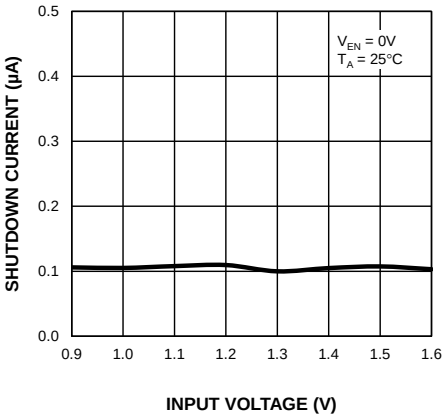


Typical Characteristics (Continued)

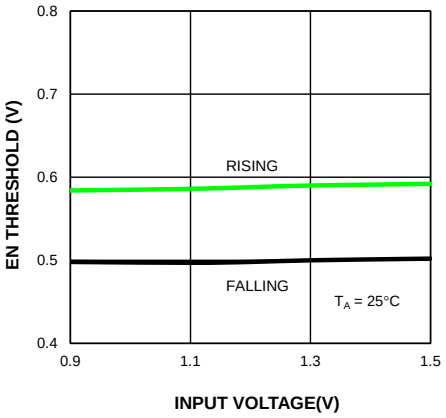
V_{IN} Quiescent Current (Switching) vs. Input Voltage



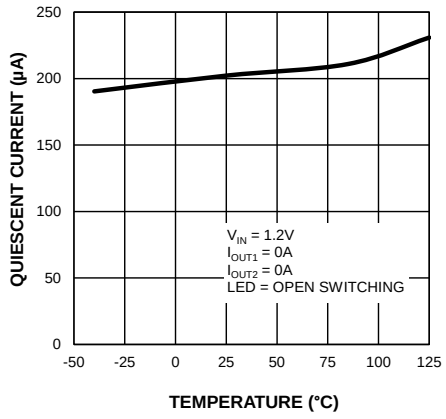
V_{IN} Shutdown Current vs. Input Voltage



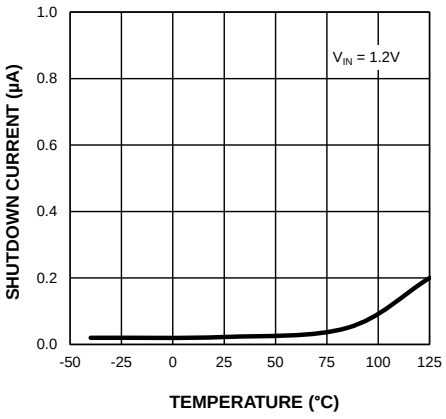
Enable Threshold vs. Input Voltage



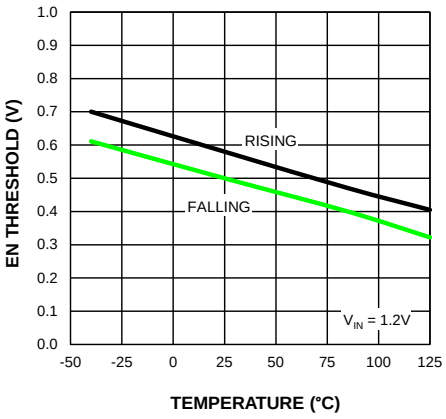
V_{IN} Quiescent Current (Switching) vs. Temperature



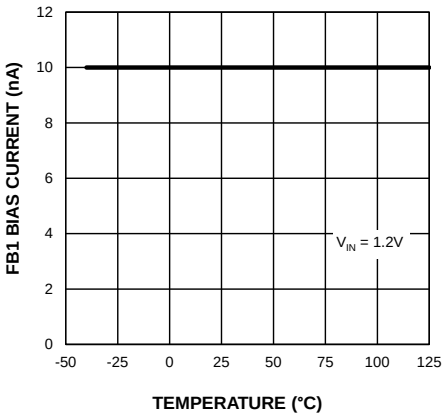
V_{IN} Shutdown Supply Current vs. Temperature



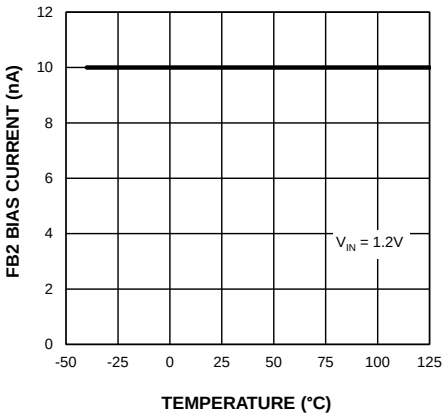
Enable Threshold vs. Temperature



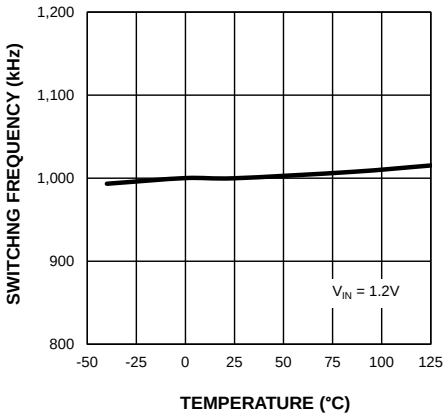
FB1 BIAS Current vs. Temperature



FB2 BIAS Current vs. Temperature

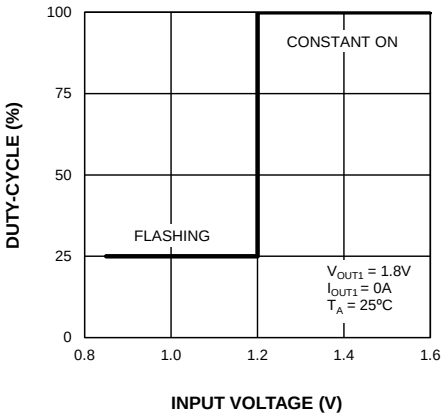


Boost Switching Frequency (PWM) vs. Temperature

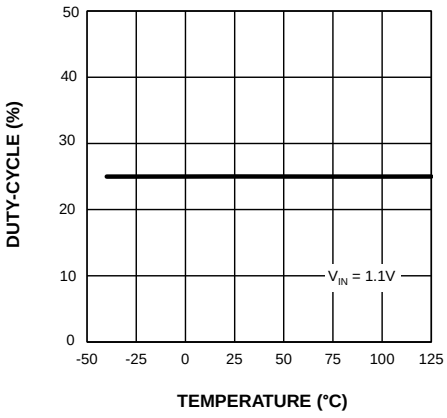


Typical Characteristics (Continued)

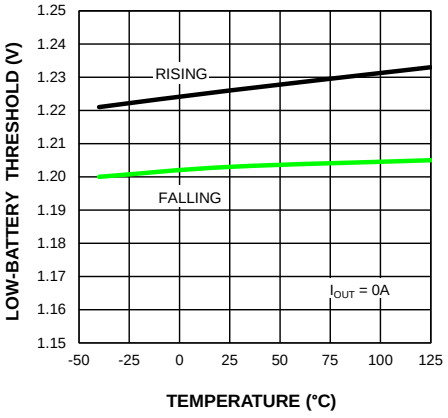
LED Flash Duty-Cycle vs. Input Voltage



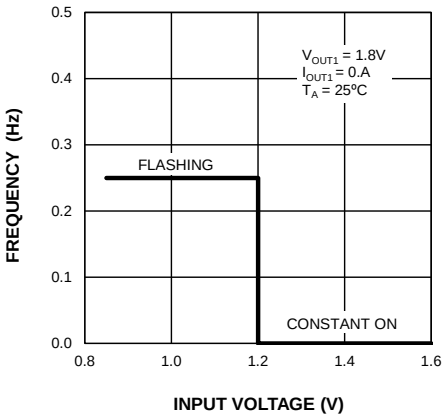
LED Flash Duty-Cycle vs. Temperature



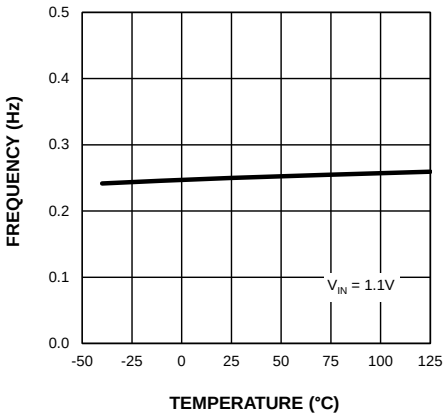
Low-BatteryThreshold vs. Temperature



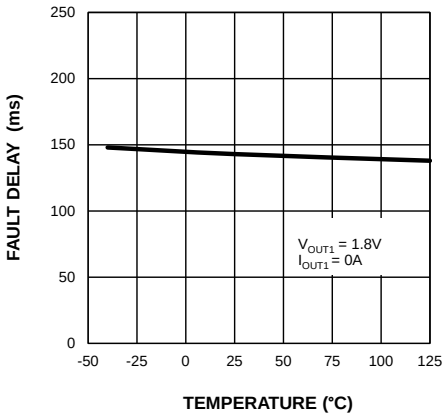
LED Flash Frequency vs. Input Voltage



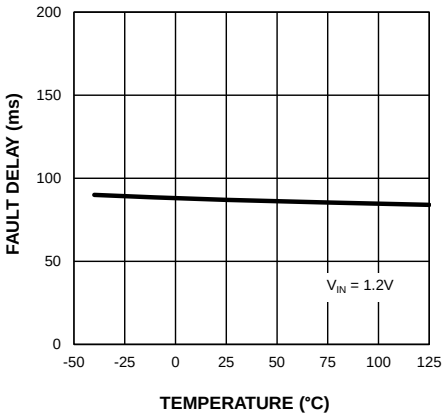
LED Flash Frequency vs. Temperature



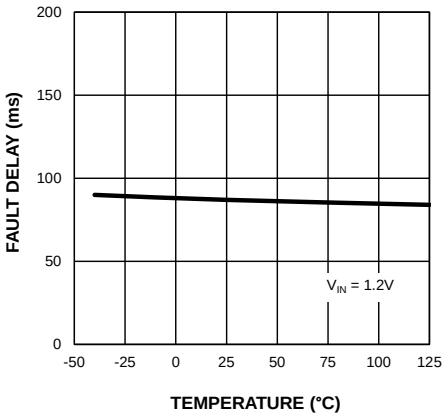
V_{IN} Fault Delay vs. Temperature



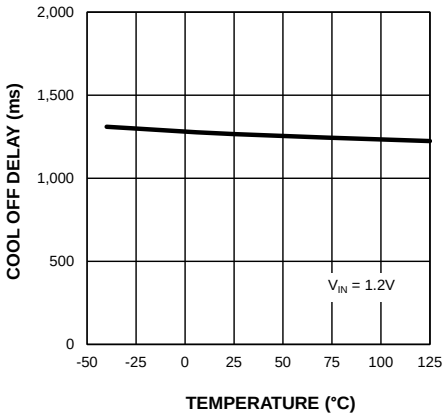
V_{OUT1} Fault Delay vs. Temperature



V_{OUT2} Fault Delay vs. Temperature

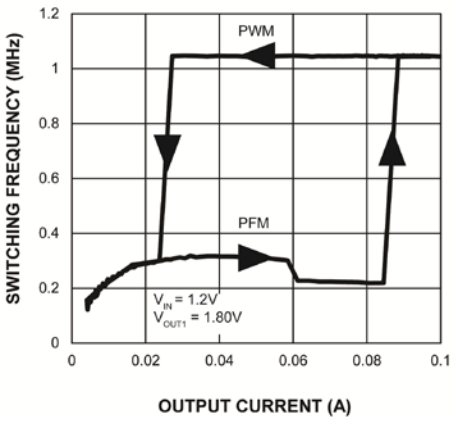


Cool OFF Delay vs. Temperature

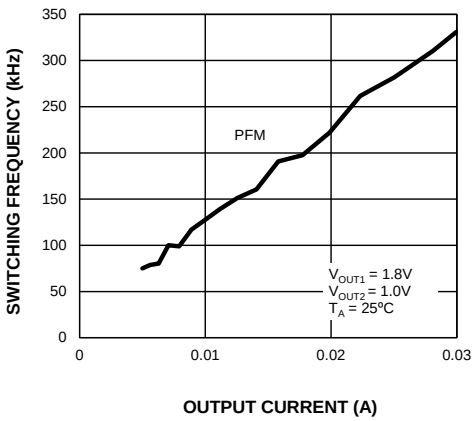


Typical Characteristics (Continued)

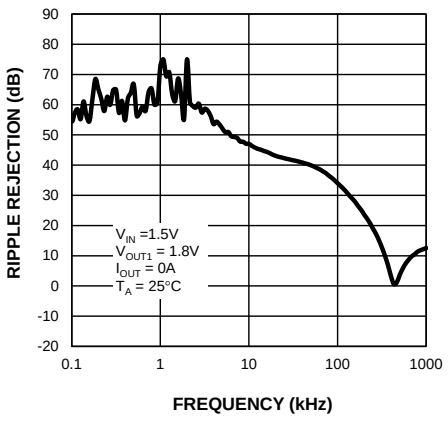
Boost Switching Frequency vs. Output Current



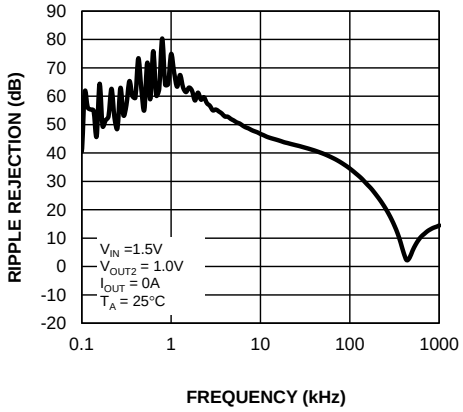
Buck Switching Frequency vs. Output Current



Boost Ripple Rejection

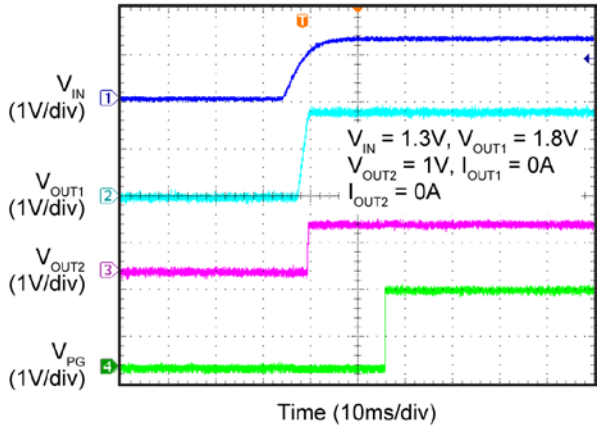


Buck Ripple Rejection

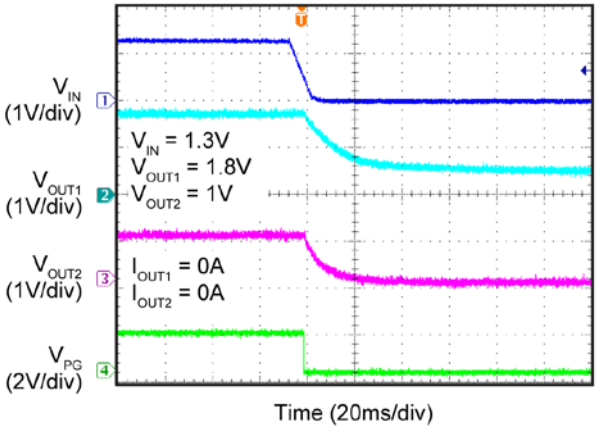


Functional Characteristics

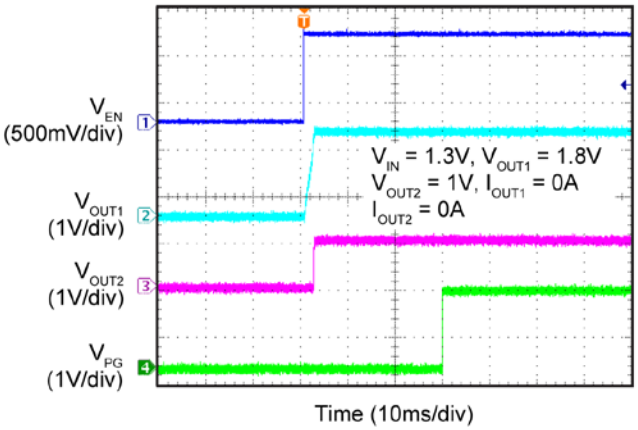
Power-Up Waveforms



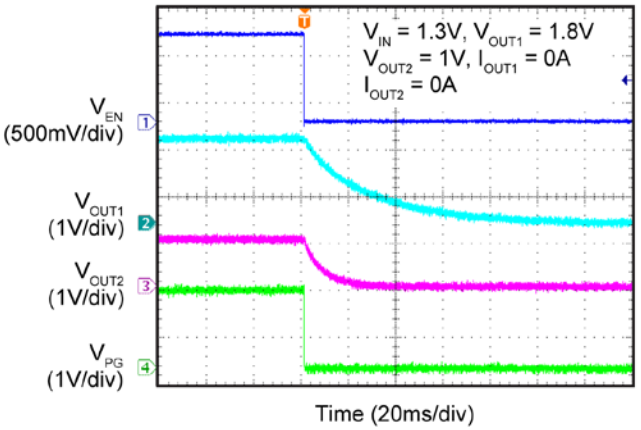
Power-Down Waveforms



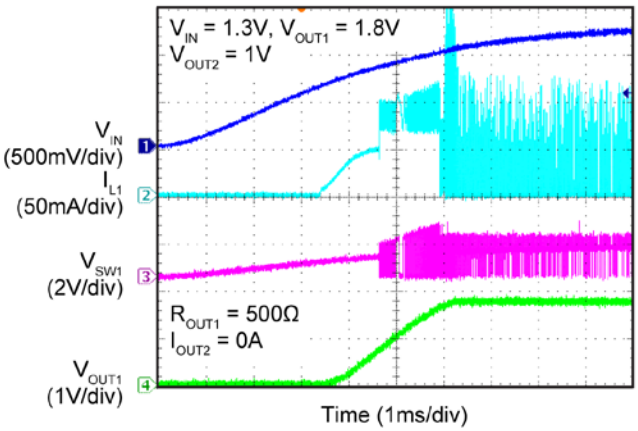
Enable Turn-On



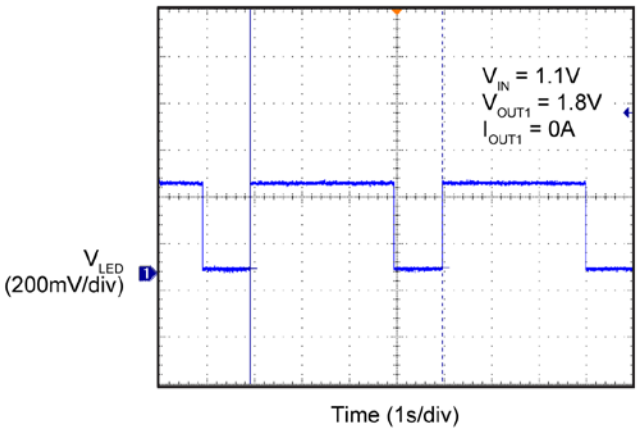
Enable Turn-Off



Power-Up with 500Ω Load

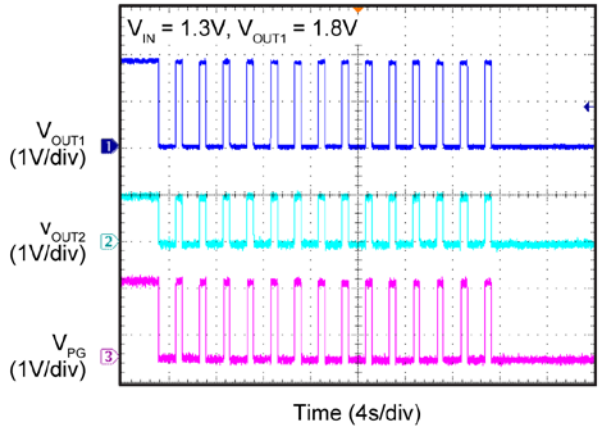


LED Flash Frequency and Duty Cycle

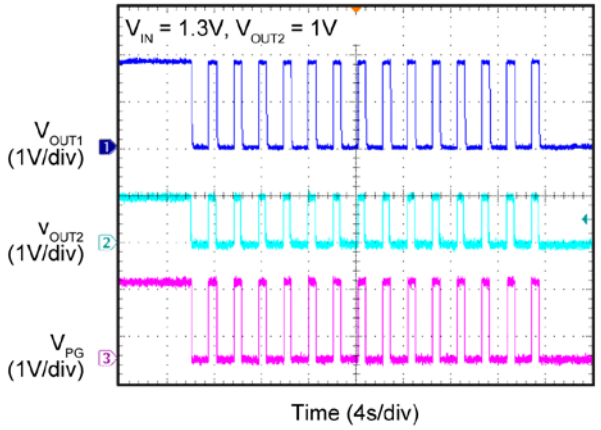


Functional Characteristics (Continued)

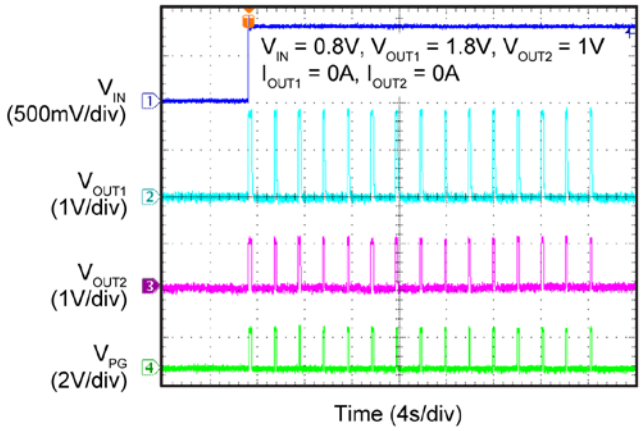
Short-Circuit Cycles – V_{OUT1}



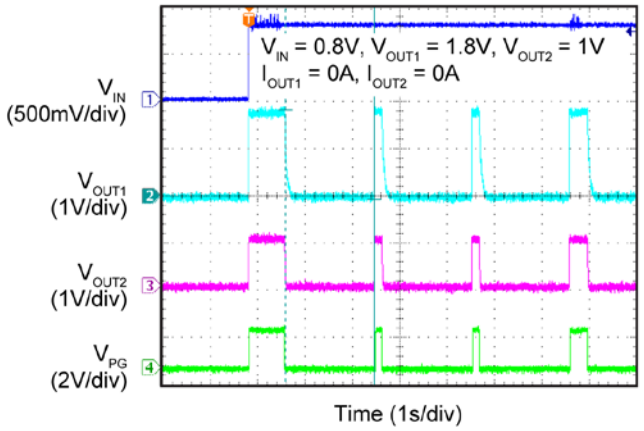
Short-Circuit Cycles – V_{OUT2}



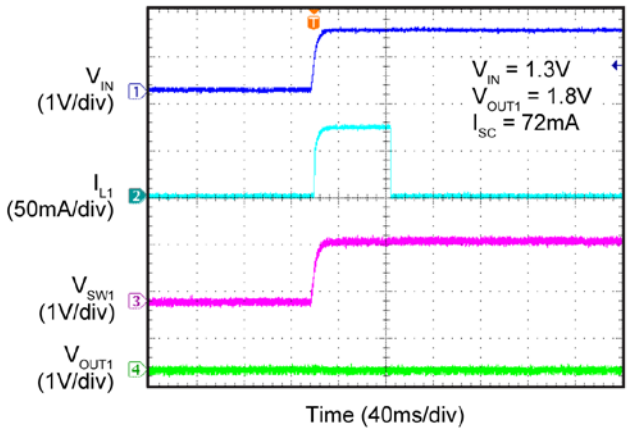
Hiccup Cycles – V_{IN} Fault



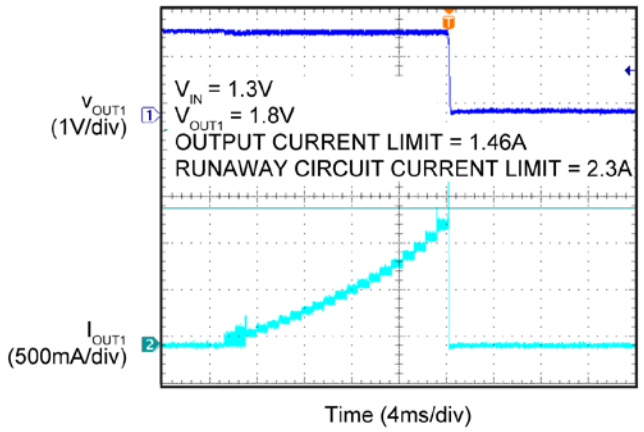
Cool Off Delay – V_{IN} Fault



Power-Up into Short Circuit – V_{OUT1}

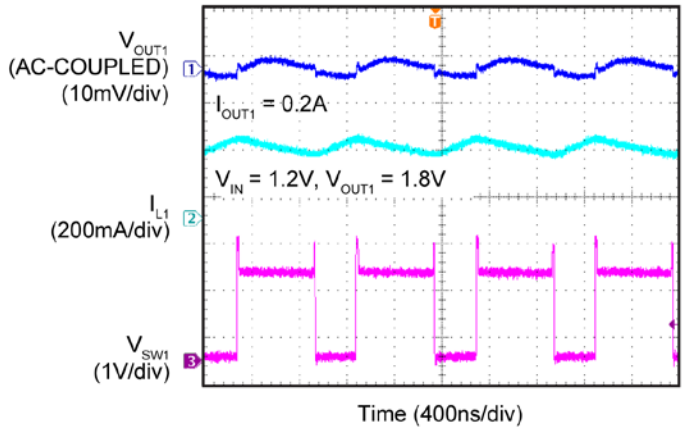


Boost Output Current Limit – V_{OUT1}

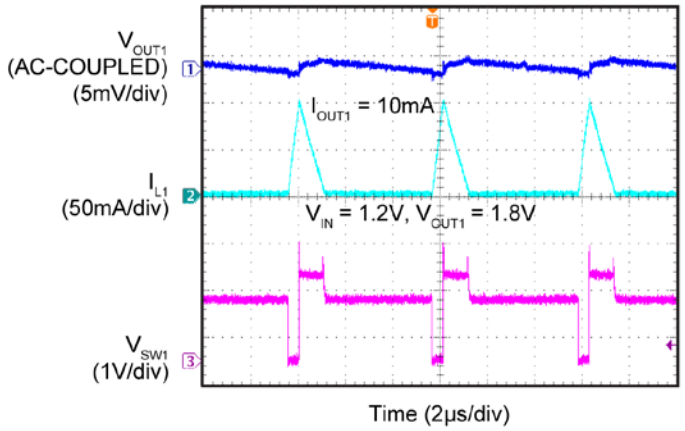


Functional Characteristics (Continued)

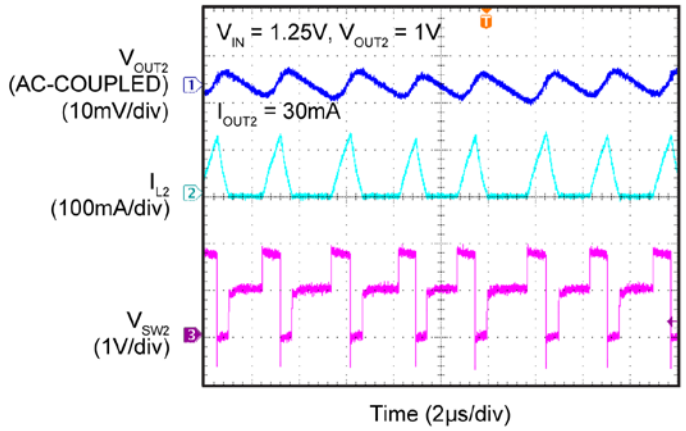
Boost Switching Waveforms – 200mA



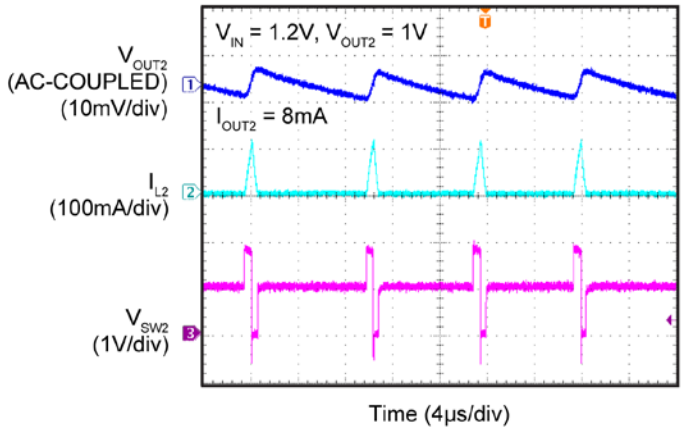
Boost Switching Waveforms – 10mA



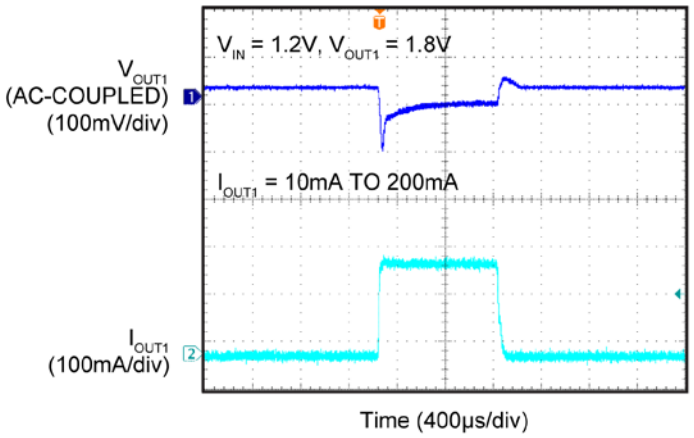
Buck Switching Waveforms – 30mA



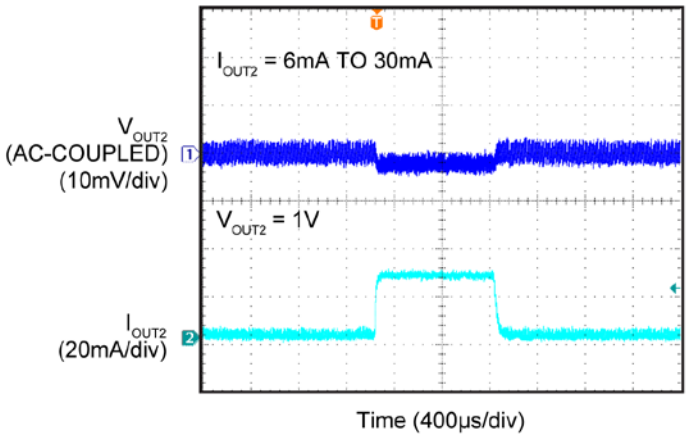
Buck Switching Waveforms – 8mA



Boost Transient Response



Buck Transient Response



Application Information

Overview

The MIC23099 is a dual output voltage, power-management IC (PMIC) that has excellent light load efficiency that operates from a single cell battery. The PMIC has a synchronous boost regulator, a synchronous buck regulator, inrush current limiting, fault detection, a low battery monitor and warning circuitry. The synchronous boost output voltage (V_{OUT1}) is enabled first and is powered from the battery. Next the synchronous buck output (V_{OUT2}), which is powered from the boost output voltage, is enabled. This configuration allows V_{OUT2} to be independent of battery voltage, thereby allowing the buck output voltage to be higher or lower than the battery voltage.

The boost regulator is a current-mode PWM design that incorporates a high-efficiency PFM light-load mode, while the buck operates in PFM mode with constant peak current control. The boost employs adaptive pulse width control that minimizes output ripple and avoids output ripple chatter commonly found in conventional micro power boost regulators. In addition, the MIC23099 incorporates a frequency control scheme that minimizes switching noise in the audio band.

The MIC23099 has an integrated low-battery monitor function. The low-battery level is indicated by an external LED connected to the LED pin. The LED is on when the battery voltage is above the 1.2V threshold and flashes when the battery voltage falls below the threshold. In addition, a supervisor circuit monitors each output and asserts a power good signal when the sequencing is done or the power good output is pulled low when a fault condition occurs.

Boost Regulator

The high-efficiency, micro-power synchronous boost regulator operates from one alkaline or NiMH battery. It offers true output disconnect to achieve a shutdown quiescent current of less than 1.0µA, extending battery life.

The boost regulator achieves high efficiency over a wide output current range by operating in either PWM or PFM mode. PFM mode provides the best efficiency at light loads and PWM mode at heavy loads. Operating mode is automatically selected according to output load conditions. In PWM mode, the switching frequency is 1.0MHz, minimizing the solution foot-print.

The current-mode PWM design is internally compensated, simplifying the design. Current mode provides excellent line and load regulation as well as cycle-by-cycle current limiting.

Also, an inrush current limiting feature is provided to reduce the inrush current which minimizes the voltage droop on the battery when the device is turned on.

Buck Regulator

The buck converter is designed to operate in PFM mode with constant peak current control. When the buck regulator high-side switch turns on, the inductor current starts to rise. When the inductor current hits the current limit threshold, a RS flip-flop is reset, turning off high-side switch and on the low-side synchronous switch. The low-side switch will remain on until the inductor current falls to zero at which time it is turned off. Both switches will remain off until the cycle repeats itself when the buck feedback voltage falls below the internal 0.6V reference and the internal comparator sets the RS flip-flop Q output high.

Low-Battery Voltage Monitoring

The internal low input voltage monitor determines when the input voltage is below the internally set 1.2V (typical) threshold. When the input voltage falls below the internally set threshold, the external LED connected to the LED pin begins to blink at a frequency of 0.25Hz with a duty cycle of 25%. The low input voltage threshold of 1.2V has a ±50mV variation.

Anti-Ringing Control

Both the buck and boost converters have an anti-ringing control circuit that minimizes the ringing on the switching node caused by the inductor and the parasitic capacitance of the switch node when the synchronous MOSFET turns off. When the inductor current falls to zero an internal anti-ringing switch is connected across the inductor. This temporally shorts the inductor and eliminates the ringing on the switch node.

True Micro-Power Shutdown

This shutdown feature disconnects the boost output from the battery. This feature eliminates power draw from the battery through the synchronous switch during shutdown. In conventional boost regulators, there is a catch diode that provides a current path from the battery through the inductor to the output of the boost regulator that can draw current even when the regulator is shutdown.

Power-Up Sequencing

When the enable pin voltage rises above the enable threshold voltage, the MIC23099 enters its start-up sequence. Initially, the boost converter high-side PMOS switch operates in linear mode and emulates a current limited switch until the output voltage V_{OUT1} reaches V_{IN}. Then a fixed duty-cycle clock controls the boost converter until V_{OUT1} reaches 1.6V. When V_{OUT1} is greater than 1.6V the boost PFM control circuitry takes over until the output reaches its regulated voltage value.

When V_{OUT1} reaches 92.5% of its nominal value, V_{OUT2} is enabled. The power good output goes high 10ms to 50ms after V_{OUT2} reaches the programmed value. Figure 1 waveforms detail the circuits operation.

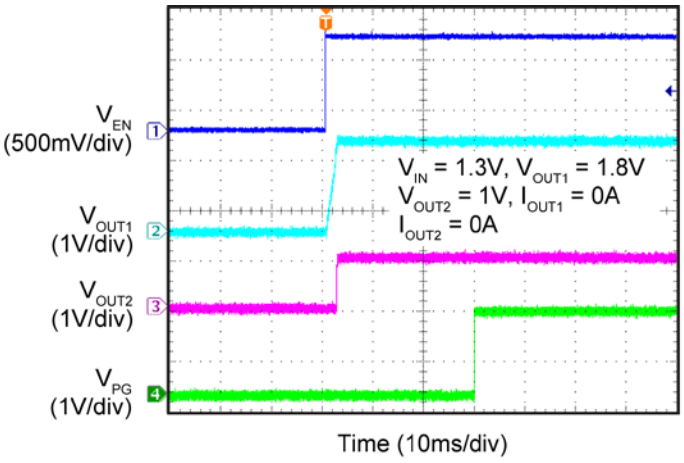


Figure 1. Power-Up Sequencing

Power Good

The power good (PG) circuitry monitors the battery voltage and feedback pin voltage of the boost and buck regulators. The PG pin output goes logic high when FB1 and FB2 pin voltages are both greater than 92.5% (typical) of the internal reference voltage and the input voltage is greater than 0.85V (typical). To minimize false triggering, the power good output has both a turn on delay and a falling deglitch delay.

Boost Switching Frequency

To reduce switching artifacts in the audio band, the buck and boost regulators switching frequency are controlled to minimize overlap. Figure 2 shows the boost switching frequency versus output load current and Figure 3 shows the buck. switching frequency versus output load current.

The boost regulator operates in either PWM or PFM mode. To avoid PWM to PFM chatter, the PWM entry and exit points are not the same. When in PFM mode the output current needs to reach 90mA to enter into PWM mode and exits at 30mA. The boost switching frequency is greater than 100kHz with loads greater than 20mW.

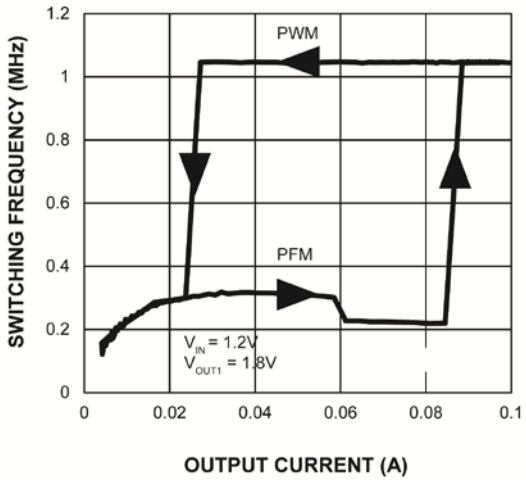


Figure 2. Boost Switching Frequency vs. Output Current

Buck Switching Frequency

The buck converter is designed to operate in PFM mode only. It has peak current control, which turns off the high-side switch when the inductor current hits the current limit threshold. The cycle repeats itself when the output voltage falls below its regulated value. As a result, the switching frequency varies linearly with output current as shown in Figure 3. The buck switching frequency is greater than 80kHz with loads greater than 8mW.

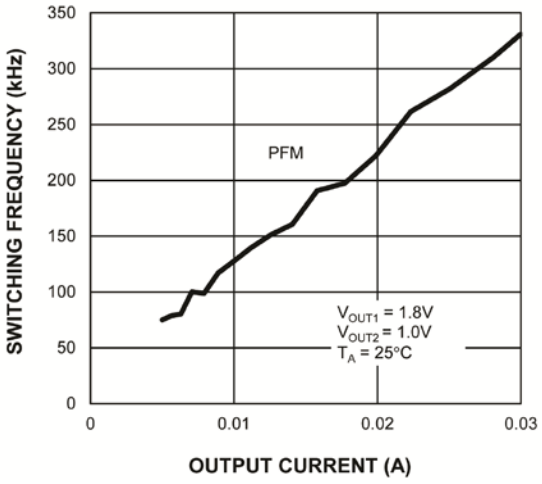


Figure 3. Buck Switching Frequency vs. Output Current

Low-Battery Detection and Output Latch-Off

Figure 4 shows the low-battery power cycling operation. If the battery voltage (V_{IN}) drops below 0.85V for more than 100ms to 150ms, the PG de-asserts (goes low) and outputs V_{OUT1} and V_{OUT2} are disabled. Then the 500Ω active discharges resistors are enabled and discharges V_{OUT1} and V_{OUT2} to ground, finally the MIC23099 enters a cool off or sleep period. After a cool off period of about 1.3 sec, if the battery voltage is above the 0.85V threshold, then the outputs will power up again. This cycle repeats itself until the end of the 15th cycle when both outputs are latched off for the last time.

The outputs can be turned back on by recycling the input power or by toggling the enable pin. If the battery voltage is still low, the MIC23099 will turn itself off again after 15 power-up cycles.

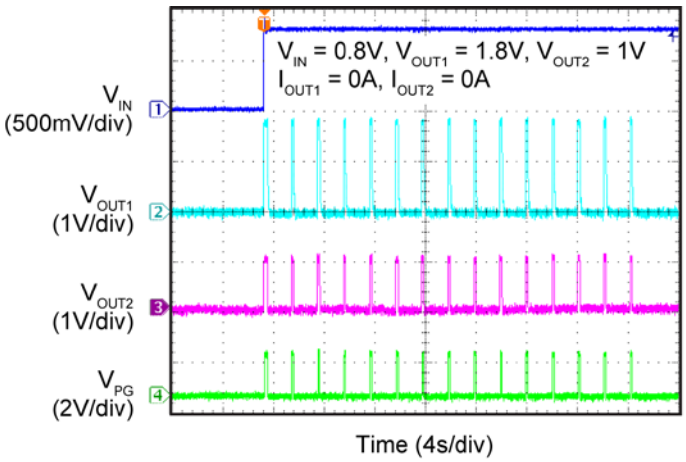


Figure 4. Low-Battery Power Cycling

Output Fault and Power Cycling

If either V_{OUT1} or V_{OUT2} outputs are out of tolerance for longer than the power good deglitch delay of between 60ms to 120ms, both outputs are disabled. The power down procedure is the same as the low-battery fault detection, as shown in Figure 5. The outputs can be turned back on by recycling the input power or by toggling the enable pin. The latch-off feature eliminates the thermal stress on the MIC23099 and the external inductors during a fault event.

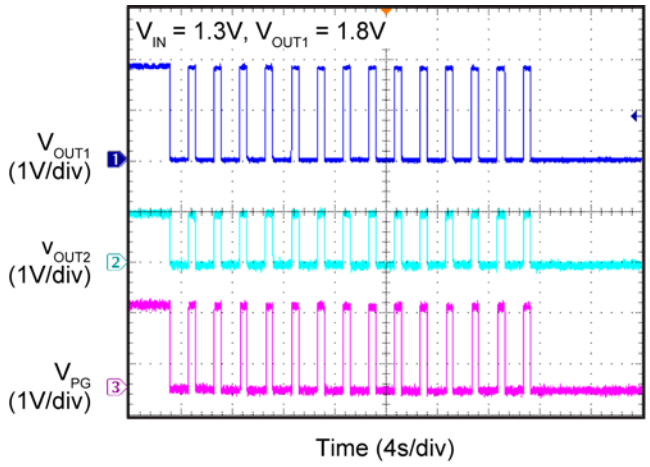


Figure 5. Output Fault Power Cycling

Boost Short-Circuit Protection

The low-side current limit protects the IC from transient overload conditions, but not from a direct short to ground. The high-side MOSFET current limit provides the protection from a short to ground. In this fault condition, the high-side PMOS switch operates in linear mode and limits the current to approximately 80mA. If the short circuit condition last for more than 30ms, the PMOS switch is latched off as shown in Figure 6. The outputs are not re-enabled until the input power is recycled or the enable pin is toggled.

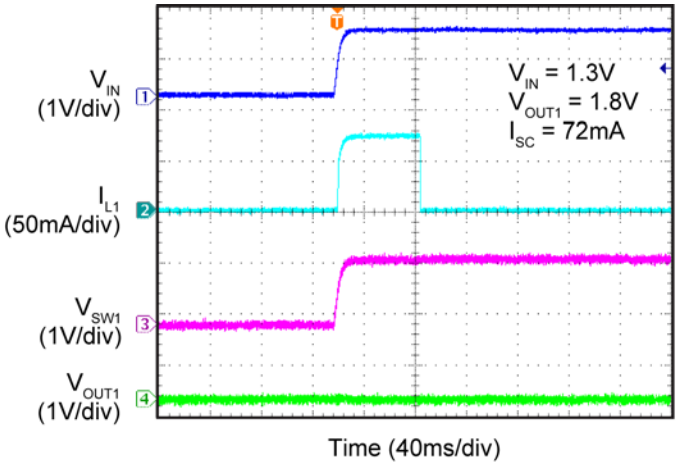


Figure 6. Power-Up into Short Circuit

Boost Overcurrent Protection

The boost converter has current-limit protection on both the high-side and low-side MOSFETs. The low-side MOSFET provides cycle-by-cycle current limiting. When the peak switch current exceeds the NMOS current limit threshold, the low-side switch is immediately turned off and the high-side switch is turned on. Peak switch current is limited to approximately 1.5A. The low-side switch is allowed to turn on again on the next clock cycle. If the overload condition last more than 60ms to 120ms, both outputs are disabled and the IC enters its power cycling mode.

Component Selection

Resistors

An external resistive divider network (R1 and R2) with its center tap connected to the feedback pin sets the output voltage for each regulator. R1 is the top resistor and R2 is the bottom resistor in the divider string. The resistor values for the desired output voltage are calculated as illustrated in Equation 1. Large resistor values are recommended to reduce light load operating current, and improve efficiency. The recommended resistor value for R1 should be around, R1 ≈ 150kΩ.

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{0.6V} - 1\right)} \qquad \text{Eq. 1}$$

In the case of the boost converter, Equation 1 sets the output voltage to its PWM value as shown in Figure 7. The no-load PFM output voltage is 2% higher than the PWM value. This higher PFM output voltage value is necessary to prevent PFM to PWM mode skipping which can introduce noise into the audio band.

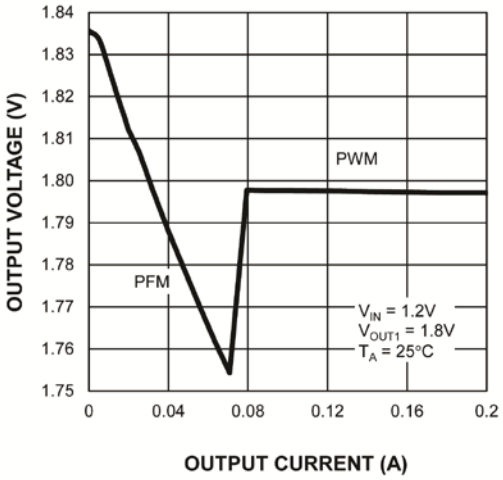


Figure 7. Boost Load Regulation

Figure 8 shows the buck load regulation.

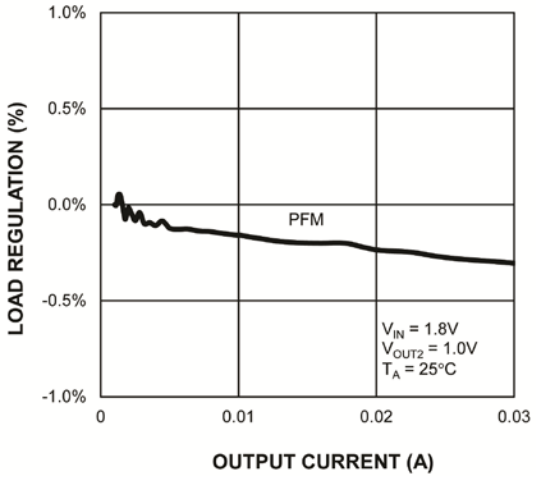


Figure 8. Buck Load Regulation

Inductor

Inductor selection is a balance between efficiency, cost, size, switching frequency and rated current. For most applications, inductors in the range 4.7µH to 6.8µH are recommended. Larger inductance values reduce the peak-to-peak ripple current, thereby reducing both the DC losses and AC losses for better efficiency. The inductor's DC resistance (DCR) also plays an important role. Since the majority of the input current (minus the MIC23099 operating current) is passed through the inductor, higher DCR inductors will reduce efficiency at higher load currents.

The switch current limit for the MIC23099 is typically 1.5A. The saturation current rating of the selected inductor should be 20 – 30% higher than the current limit specification for the respective regulator.

Input Capacitor

The step-up converter exhibits a triangular, or sawtooth, current waveform at its input, so an input capacitor is required to decouple this waveform and thereby reduce the input voltage ripple. A 4.7µF to 10µF ceramic capacitor should be sufficient for most applications. A minimum input capacitance of 1µF is recommended. The input capacitor should be as close as possible to the inductor, VIN pin, and PGND1 pin of the MIC23099. Short, and wide, PCB traces are good for noise performance.

Output Capacitor

Output capacitor selection is also a trade-off between performance, size, and cost. Increasing the output capacitor will lead to an improved transient response performance. X5R and X7R ceramic capacitors are recommended. For most applications, 10µF to 47µF should be sufficient.

PCB Layout Guidelines

WARNING! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC23099 converter.

IC

- The 4.7µF ceramic capacitor, which is connected between OUT1 and PGND1, must be located as close as possible to the IC.
- The analog ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND Pad on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines to minimize EMI.
- Signal and power grounds should be kept separate and connected at only one location.
- The exposed pad (EP) must be soldered to the ground plane (layer 2). It serves as an additional ground connection and a way to conduct heat away from the package.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply when power is suddenly applied.

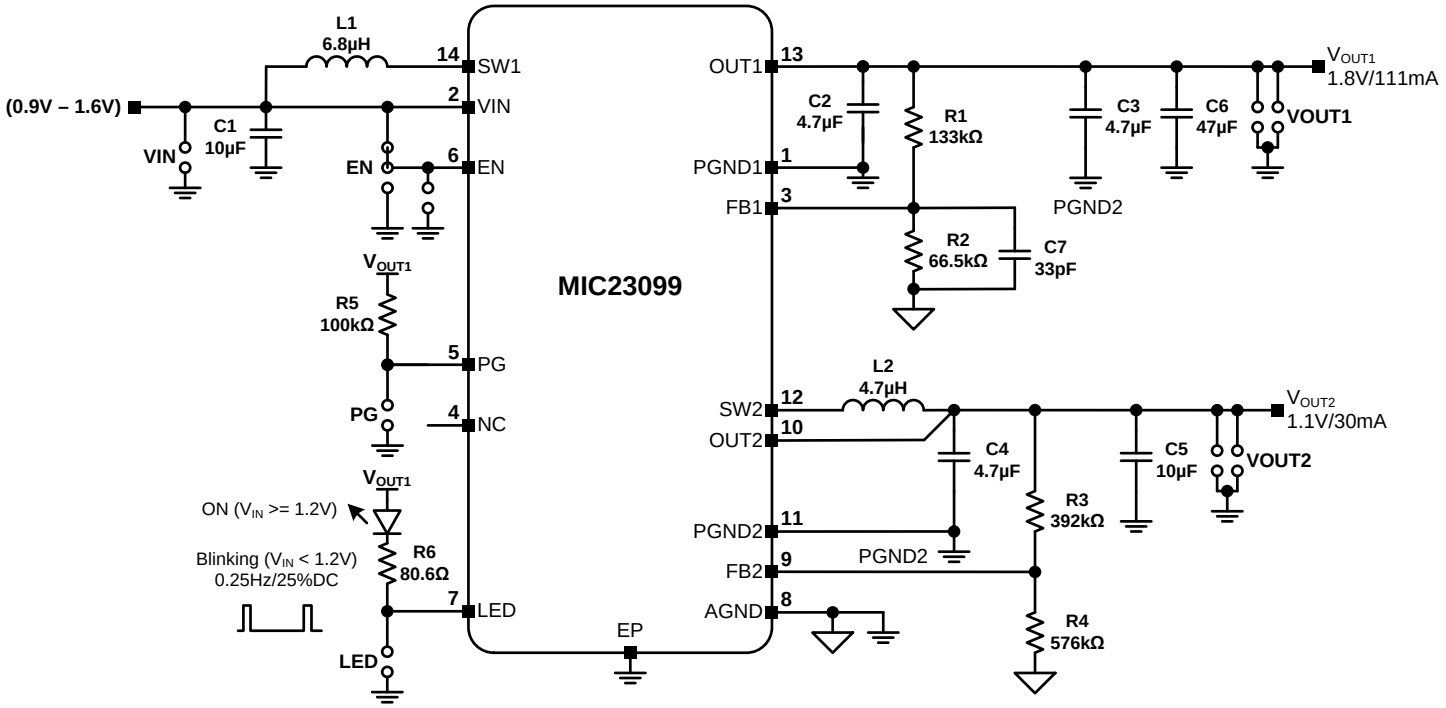
Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Typical Application Schematic



Note:
C5 AND C6 ARE SOC BYPASS CAPACITORS

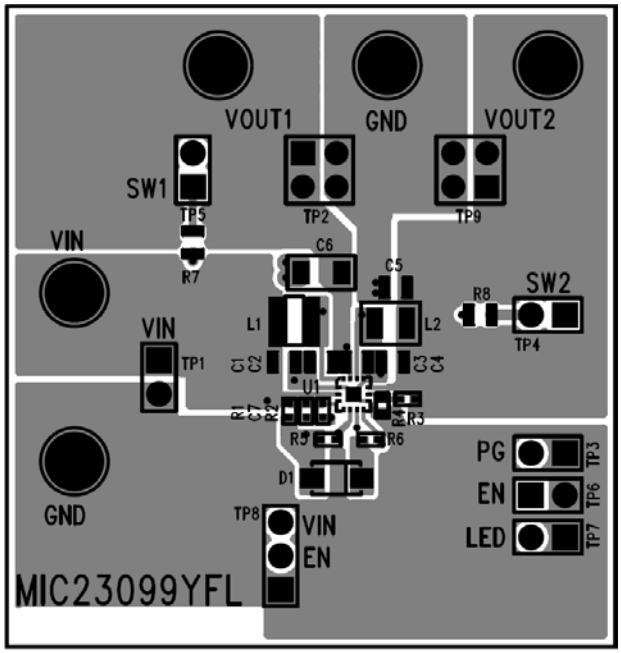
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C5	GRM188R60J106ME47D	Murata[9]	10µF/6.3V, Ceramic Capacitor, X5R, 0603, ±20%	2
	CL10A106MQ8NNNC	Samsung[10]		
C2, C3, C4	GRM188R60J475ME19D	Murata	4.7µF/6.3V, Ceramic Capacitor, X5R, 0603, ±20%	3
	CL10A475MQ8NNNC	Samsung		
C6	GRM31CR60J476ME19L	Murata	47µF/6.3V, Ceramic Capacitor, X5R, 1206, ±20%	1
	CL31A476MQHNNNE	Samsung		
C7	CL05C330JB5NNNC	Samsung	33pF/50V, Ceramic Capacitor, C0G, 0402, ±5%	1
D1	SML-LXT1206SRC	Lumex[11]	1.7V/20mA, LED, 660NM RED WTR CLR, 1206	1
L1	IFSC1515AHER6R8M01	Vishay Dale[12]	6.8µH, 1.5A Inductor, 90mΩ, 3.8mm × 3.8mm × 1.8mm	1
L2	CIG2MW4R7NNE	Samsung	4.7µH, 1.1A Inductor, 140mΩ, 2.0mm × 1.6mm × 1.0mm	1
R1	RC1005F1333CS	Samsung	133kΩ Resistor, 0402, 1%	1
R2	RC1005F6652CS	Samsung	66.5kΩ Resistor, 0402, 1%	1
R3	RC1005F3923CS	Samsung	392kΩ Resistor, 0402, 1%	1
R4	RC1005F5763CS	Samsung	576kΩ Resistor, 0402, 1%	1
R5	RC1005F1003CS	Samsung	100kΩ Resistor, 0402, 1%	1
R6	RC1005F80R6CS	Samsung	80.6Ω Resistor, 0402, 1%	1
U1	**MIC23099YFT**	**Micrel[13]**	**Single AA/AAA Cell Step-Up/Step-Down Regulators with Battery Monitoring**	**1**

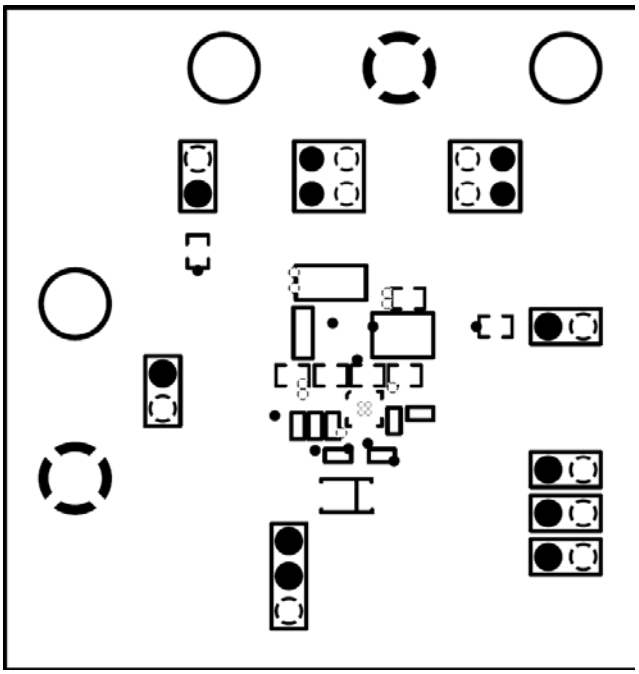
Notes:

9. Murata: www.murata.com.
10. Samsung: www.samsung.com.
11. Lumex: www.lumex.com.
12. Vishay Dale: www.vishay.com.
13. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

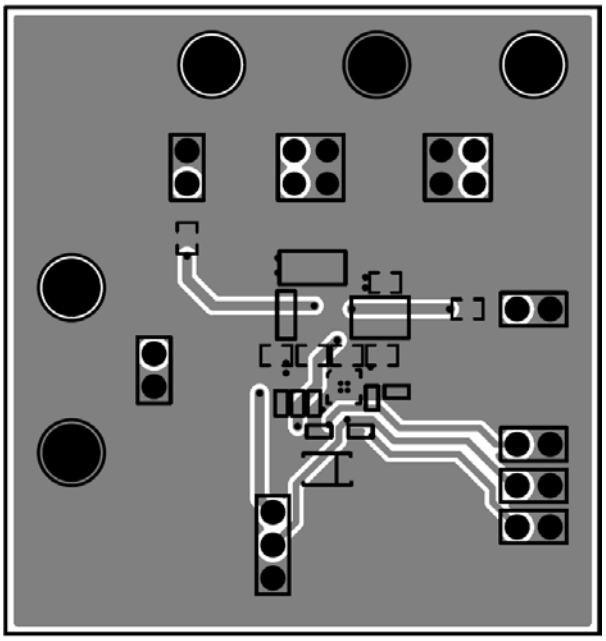


Top Layer (Power Trace Layer)

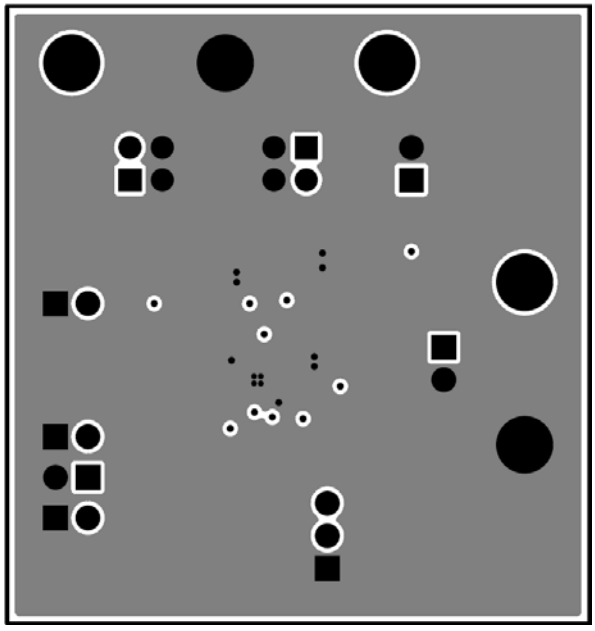


Layer 2 (Ground Plane)

PCB Layout Recommendations (Continued)

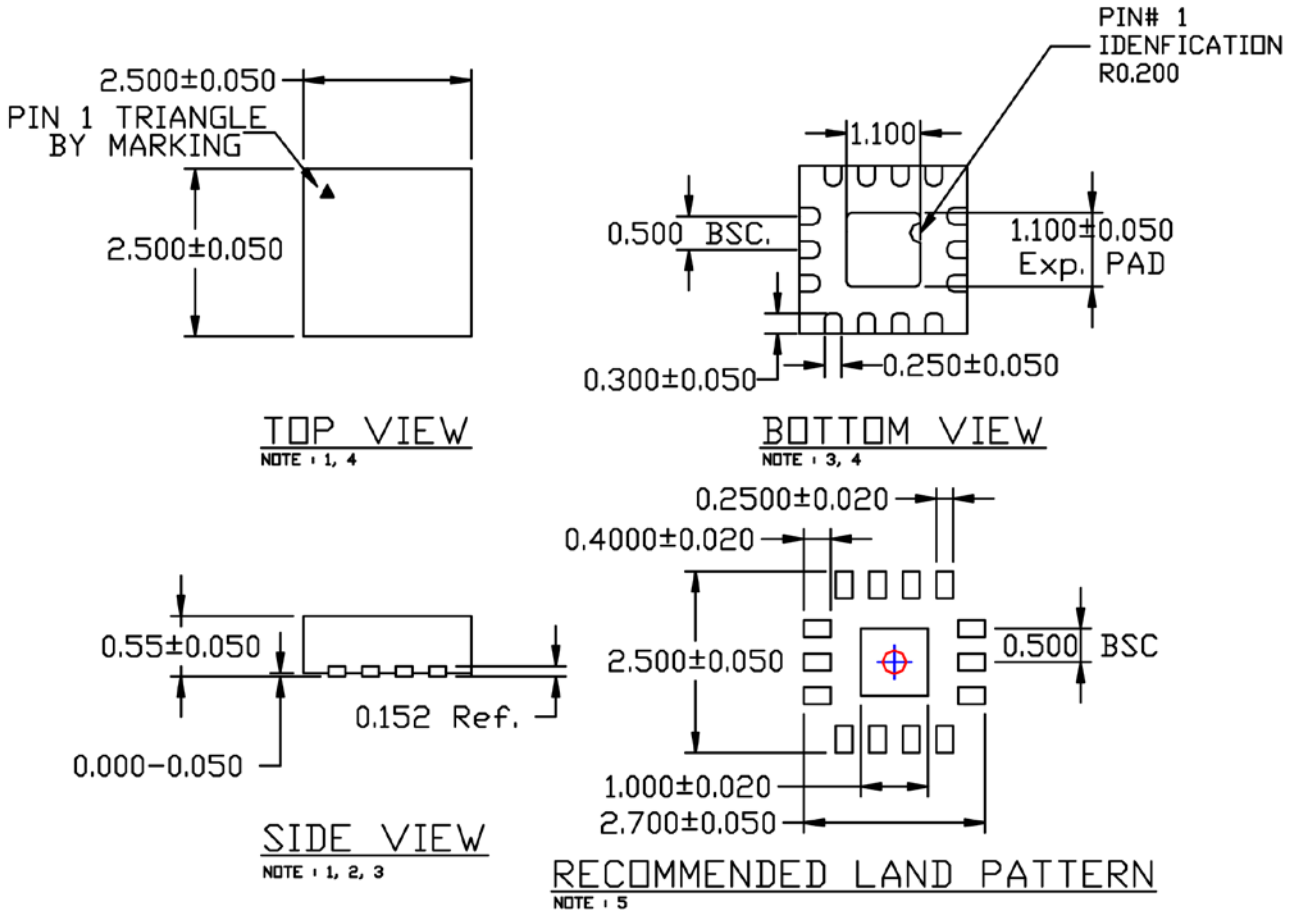


Layer 3 (Routing Layer)



Bottom Layer (Ground Plane)

Package Information[14]



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.08 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID WILL BE LASER MARKED.
5. RED CIRCLE INDICATE THERMAL VIA. SIZE IS 0.300-0.350 mm IN DIAMETER AND SHOULD BE CONNECTED TO GND PLANE FOR MAXIMUM THERMAL PERFORMANCE.

14-Pin 2.5mm × 2.5mm Thin QFN (FT)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Micrel:

MIC23099YFT T5 MIC23099YFT-TR MIC23099YFT-T5

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9