

2.7V to 5.5V Input, 3.0A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9B300MUV

General Description

BD9B300MUV is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. This IC, which is capable of providing current up to 3A, features fast transient response by employing constant on-time control system. It offers high oscillating frequency at low inductance. With its original constant on-time control method which operates low consumption at light load, this product is ideal for equipment and devices that demand minimal standby power consumption.

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.8 V to $V_{PVIN} \times 0.8$ V
- Maximum Operating Current: 3A (Max)
- Switching Frequency: 2MHz/1MHz (Typ)
- High-Side MOSFET ON Resistance: 35mΩ (Typ)
- Low-Side MOSFET ON Resistance: 35mΩ (Typ)
- Standby Current: 0μA (Typ)

Package

VQFN016V3030

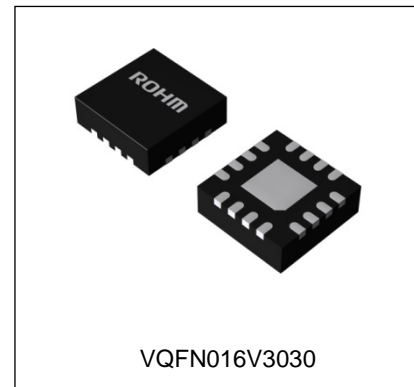
W (Typ) x D (Typ) x H (Max)
 3.00 mm x 3.00 mm x 1.00 mm

Features

- Synchronous Single DC/DC Converter
- Constant on-time control suitable to Deep-SLLM
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Adjustable Soft Start
- Power Good Output
- VQFN016V3030 Package (backside heat dissipation)

Applications

- Step-down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Laptop PCs/Tablet PCs/Servers
- LCD TVs
- Storage Devices (HDDs/SSDs)
- Printers, OA Equipment
- Entertainment Devices
- Distributed Power Supply, Secondary Power Supply



Typical Application Circuit

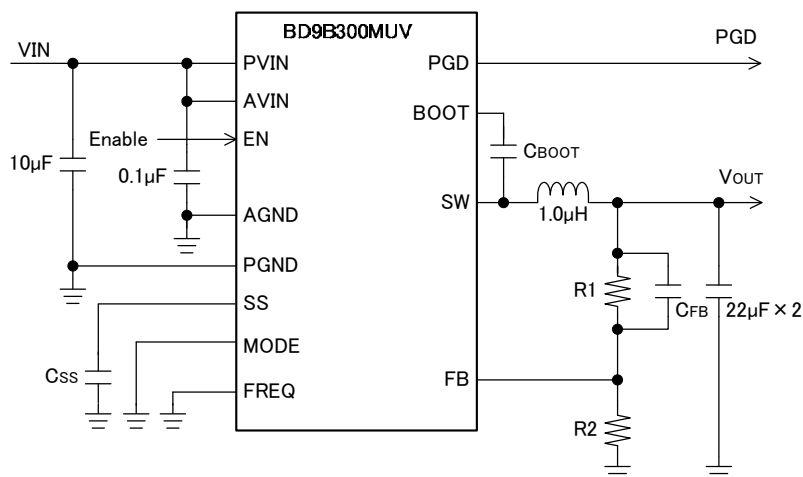


Figure 1. Application Circuit

Pin Configuration

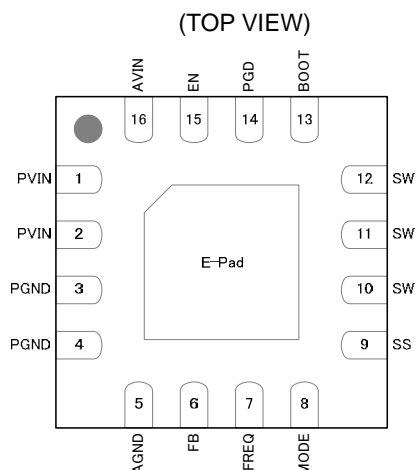


Figure 2. Pin Assignment

Pin Descriptions

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply terminals for the switching regulator. These terminals supply power to the output stage of the switching regulator. Connecting a 10 μ F ceramic capacitor is recommended.
3, 4	PGND	Ground terminals for the output stage of the switching regulator.
5	AGND	Ground terminal for the control circuit.
6	FB	An inverting input node for the error amplifier and main comparator. See page 22 for how to calculate the resistance of the output voltage setting.
7	FREQ	Terminal for setting switching frequency. Connecting this terminal to ground makes switching to operate constant on-time corresponding to 2.0MHz. Connecting this terminal to AVIN makes switching to operate constant on-time corresponding to 1.0MHz. This terminal needs to be terminated.
8	MODE	Terminal for setting switching control mode. Connecting this terminal to AVIN forces the device to operate in the fixed frequency PWM mode. Connecting this terminal to ground enables the Deep-SLLM control and the mode is automatically switched between the Deep-SLLM control and fixed frequency PWM mode.
9	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. See page 23 for how to calculate the capacitance.
10, 11, 12	SW	Switch nodes. These terminals are connected to the source of the High-Side MOSFET and drain of the Low-Side MOSFET. Connect a bootstrap capacitor of 0.1 μ F between these terminals and BOOT terminal. In addition, connect an inductor of 0.47 μ H to 1 μ H (FREQ=L), 1 μ H to 1.5 μ H (FREQ=H) considering the direct current superimposition characteristic.
13	BOOT	Terminal for bootstrap. Connect a bootstrap capacitor of 0.1 μ F between this terminal and SW terminals. The voltage of this capacitor is the gate drive voltage of the High-Side MOSFET.
14	PGD	A "Power Good" terminal, an open drain output. Use of pull up resistor is needed. See page 17 for how to specify the resistance. When the FB terminal voltage reaches more than 80% of 0.8 V, the internal Nch MOSFET turns off and the output turns High.
15	EN	Enable terminal. Turning this terminal signal Low (0.3V or lower) forces the device to enter the shutdown mode. Turning this terminal signal High (2.0V or higher) enables the device. This terminal must be terminated.
16	AVIN	Terminal for supplying power to the control circuit of the switching regulator. Connecting a 0.1 μ F ceramic capacitor is recommended.
-	E-Pad	A backside heat dissipation exposed pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.

Block Diagram

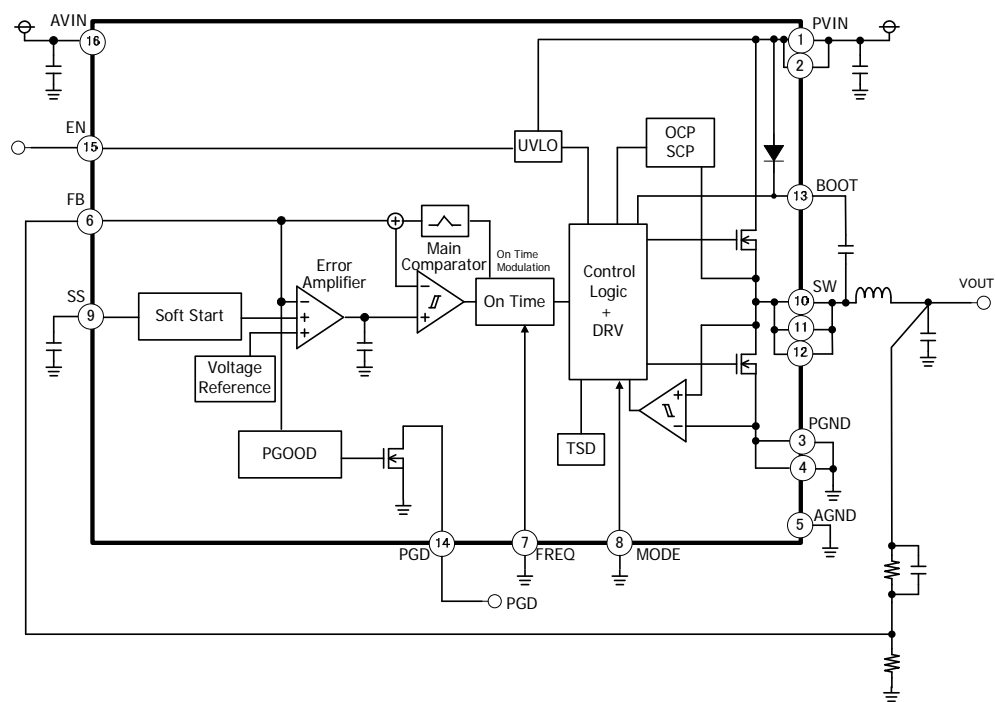


Figure 3. Block Diagram

Description of Blocks

- **VREF**
The VREF block generates the internal reference voltage.
- **UVLO**
The UVLO block is for Under Voltage lockout protection. It will shut down the IC when VIN falls to 2.45 V (Typ) or lower. The threshold voltage has a hysteresis of 100mV (Typ).
- **TSD**
The TSD block is for thermal protection. The thermal protection circuit shuts down the device when the internal temperature of IC rises to 175°C (Typ) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (Typ).
- **Soft Start**
The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. A built-in soft start function is provided and a soft start is initiated in 1msec (Typ) when the SS terminal is open.
- **Control Logic + DRV**
This block is a DC/DC driver. A signal from On Time is applied to drive the MOSFETs.
- **PGOOD**
When the FB terminal voltage reaches more than 80% of 0.8 V, the Nch MOSFET of the built-in open drain output turns off and the output turns High.
- **OCP/SCP**
After soft start is completed and in condition where output voltage is below 70% (typ) of voltage setting, it counts the number of times of which current flowing in High side FET reaches over current limit. When 1024 times is counted it stops operation for 1m sec (typ.) and re-operates. Counting is reset when output voltage is above 80% (typ.) of voltage setting or when EN, UVLO, SCP function is re-operated.
- **Error Amplifier**
Adjusts Main Comparator input to make internal reference voltage equal to FB terminal voltage.
- **Main Comparator**
Main comparator compares Error Amplifier output and FB terminal voltage. When FB terminal voltage becomes low it outputs High and reports to the On Time block that the output voltage has dropped below control voltage.
- **On Time**
This is a block which creates On Time. Requested On Time is created when Main Comparator output becomes High. On Time is adjusted to restrict frequency change even with I/O voltage change.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VPVIN, VAVIN	-0.3 to +7	V
EN Terminal Voltage	VEN	-0.3 to +7	V
MODE Terminal Voltage	VMODE	-0.3 to +7	V
FREQ Terminal Voltage	VFREQ	-0.3 to +7	V
PGD Terminal Voltage	VPGD	-0.3 to +7	V
Voltage from GND to BOOT	VBOOT	-0.3 to +14	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Terminal Voltage	VFB	-0.3 to +7	V
SW Terminal Voltage	VSW	-0.3 to VPVIN + 0.3	V
Output Current	IOUT	3.5	A
Allowable Power Dissipation ^(Note 1)	Pd	2.66	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

(Note 1) When mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board (copper foil area: 70 mm x 70 mm)

Derate by 21.3mW when operating above 25°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VPVIN, VAVIN	2.7	-	5.5	V
Output Current ^(Note 2)	IOUT	-	-	3	A
Output Voltage Range	VRANGE	0.8	-	VPVIN × 0.8	V

(Note 3) Pd, ASO should not be exceeded

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{AVIN} = V_{PVIN} = 5V, V_{EN} = 5V, V_{MODE} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN pin						
Standby Supply Current	ISTB	-	0	10	μA	EN=GND
Operating Supply Current	I _{CC}	-	35	50	μA	FREQ=AVIN, I _{OUT} =0mA Non switching
UVLO Detection Threshold	V _{UVLO1}	2.35	2.45	2.55	V	V _{IN} falling
UVLO Release Threshold	V _{UVLO2}	2.425	2.55	2.7	V	V _{IN} rising
UVLO Hysteresis	V _{UVLOHYS}	50	100	200	mV	
Enable						
EN Input High Level Voltage	V _{ENH}	2.0	-	-	V	
EN Input Low Level Voltage	V _{ENL}	-	-	0.3	V	
EN Input Current	I _{EN}	-	0	10	μA	EN=5V
Reference Voltage, Error Amplifier						
FB Terminal Voltage	V _{FB}	0.792	0.8	0.808	V	
FB Input Bias Current	I _{FB}	-	-	1	μA	FB=0.8V
Internal Soft Start Time	T _{SS}	0.5	1.0	2.0	ms	With internal constant
Soft Start Terminal Current	I _{SS}	0.5	1.0	2.0	μA	
Control						
FREQ Input High Level Voltage	V _{FREQH}	V _{AVIN} -0.3	-	-	V	
FREQ Input Low Level Voltage	V _{FREQL}	-	-	0.3	V	
MODE Input High Level Voltage	V _{MODEH}	V _{AVIN} -0.3	-	-	V	
MODE Input Low Level Voltage	V _{MODEL}	-	-	0.3	V	
On time1	ONT1	96	120	144	ns	V _{OUT} =1.2V, FREQ=GND
On time2	ONT2	192	240	288	ns	V _{OUT} =1.2V, FREQ=AVIN
Power Good						
Power Good Rising Threshold	V _{PGDH}	75	80	85	%	FB rising, V _{PGDH} =FB/V _{FB} ×100
Power Good Falling Threshold	V _{PGDL}	65	70	75	%	FB falling, V _{PGDL} =FB/V _{FB} ×100
Output Leakage Current	I _{LKPGD}	-	0	5	μA	PGD=5V
Power Good On Resistance	R _{PGD}	-	100	200	Ω	
Power Good Low Level Voltage	P _{GDV_L}	-	0.1	0.2	V	I _{PGD} =1mA
SW						
High Side FET On Resistance	R _{ONH}	-	35	70	mΩ	BOOT - SW = 5 V
Low Side FET On Resistance	R _{ONL}	-	35	70	mΩ	
High Side Output Leakage Current	R _{ILH}	-	0	10	μA	No switching
Low Side Output Leakage Current	R _{ILL}	-	0	10	μA	No switching

Typical Performance Curves

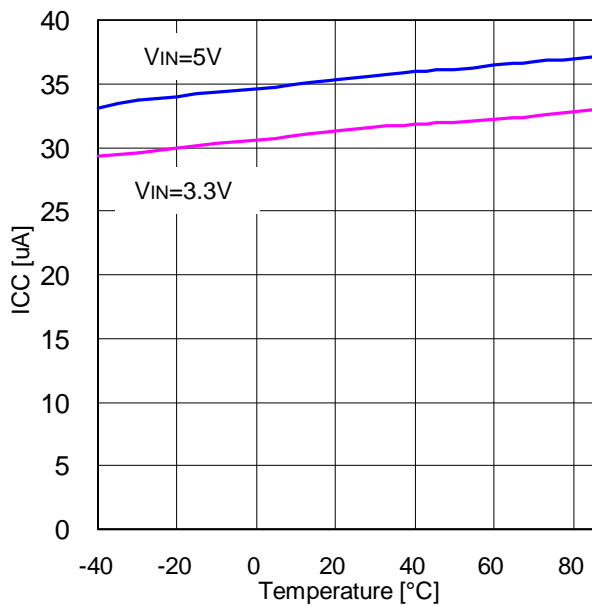


Figure 4. Operating Supply Current vs Temperature

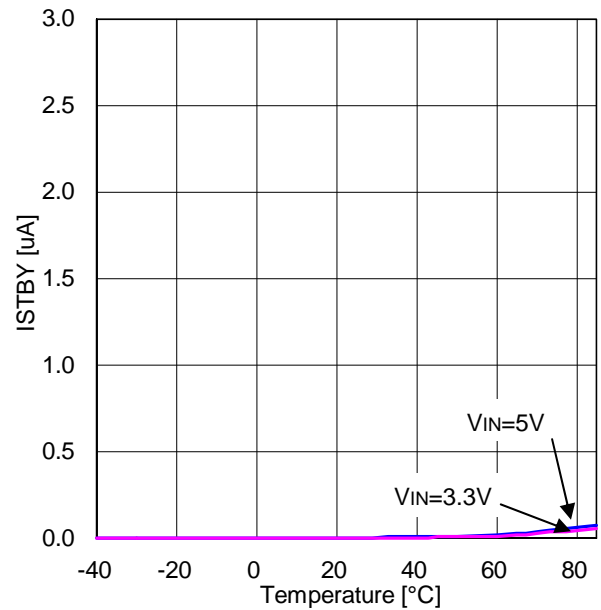
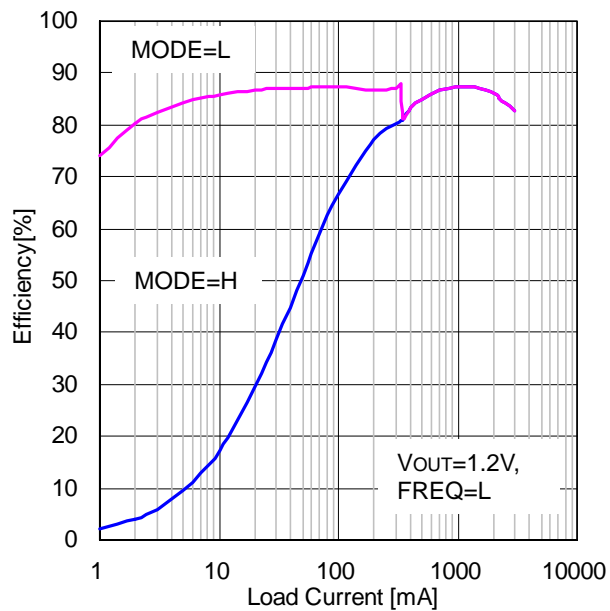
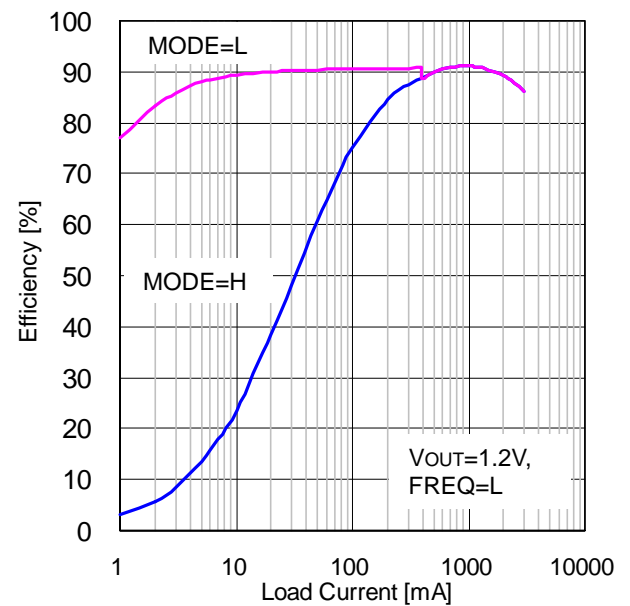


Figure 5. Stand-by Supply Current vs Temperature

Figure 6. Efficiency vs Load Current
(VIN=5V, VOUT=1.2V, L=1.0 μ H, FREQ=L)Figure 7. Efficiency vs Load Current
(VIN=5V, VOUT=1.2V, L=1.5 μ H, FREQ=H)

Typical Performance Curves - continued

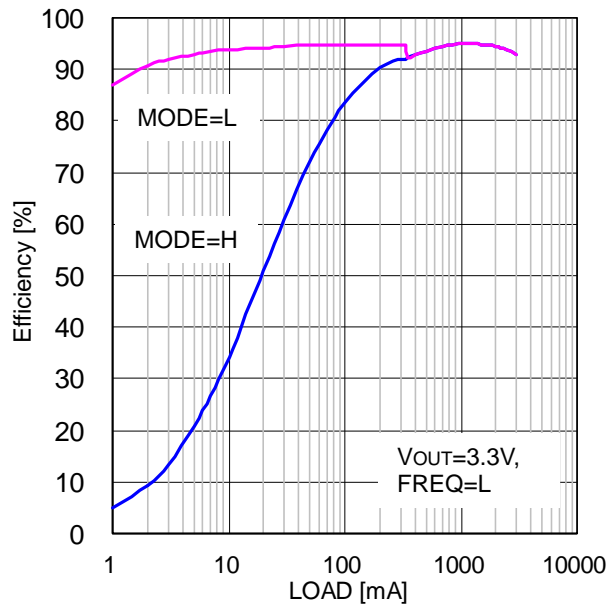


Figure 8. Efficiency vs Load Current
($V_{IN}=5V$, $V_{OUT}=3.3V$, $L=1.0\mu H$, $FREQ=L$)

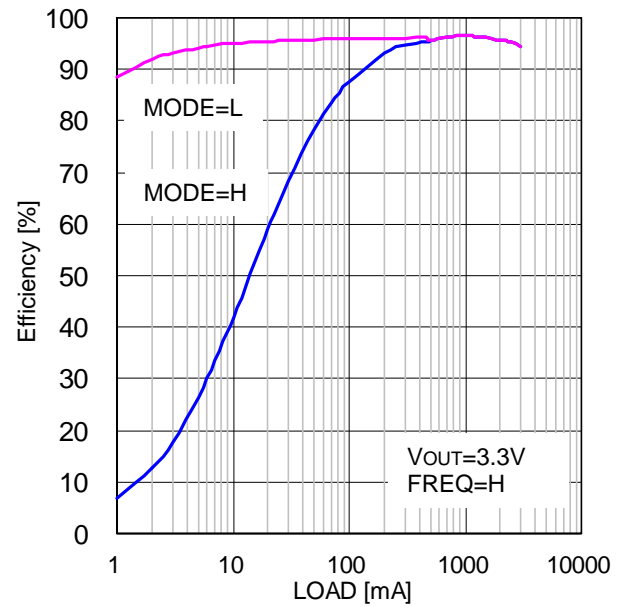


Figure 9. Efficiency vs Load Current
($V_{IN}=5V$, $V_{OUT}=3.3V$, $L=1.5\mu H$, $FREQ=H$)

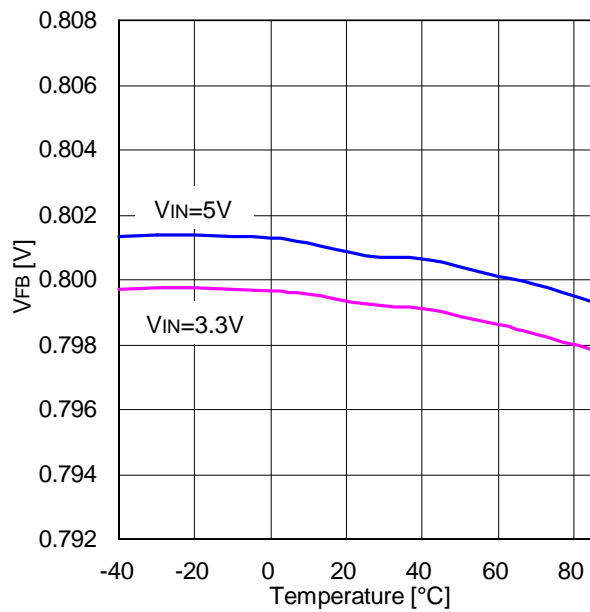


Figure 10. FB Voltage vs Temperature

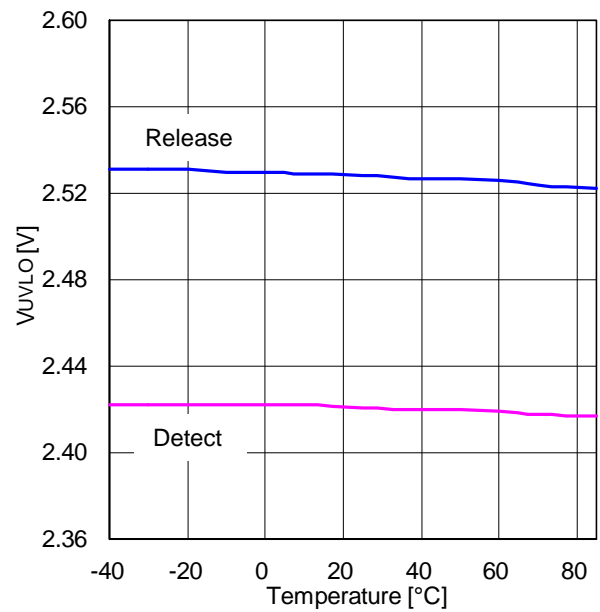


Figure 11. UVLO Threshold vs Temperature

Typical Performance Curves - continued

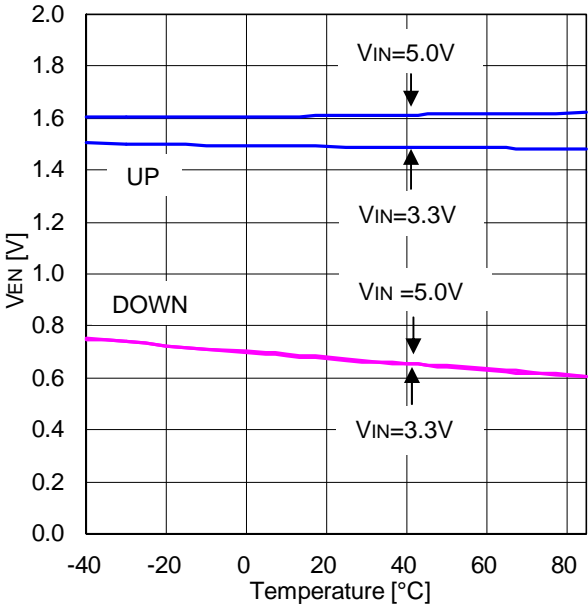


Figure 12. EN Threshold vs Temperature

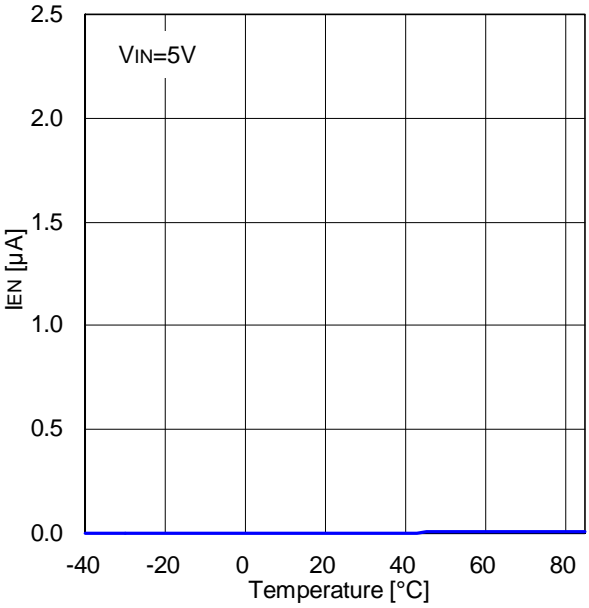


Figure 13. EN Input Current vs Temperature

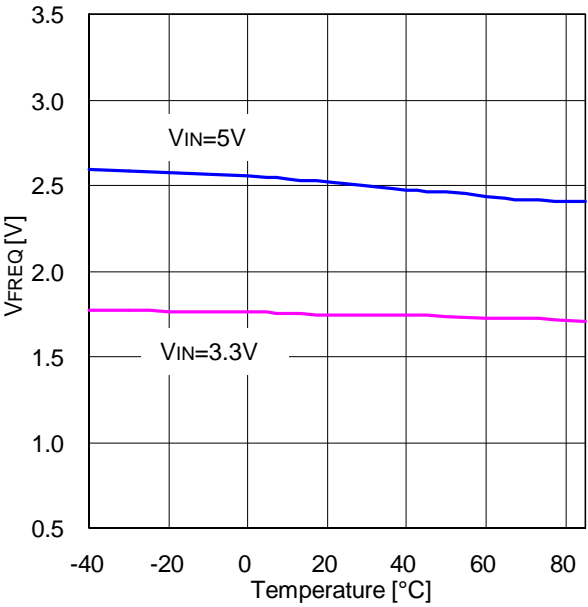


Figure 14. FREQ Threshold vs Temperature

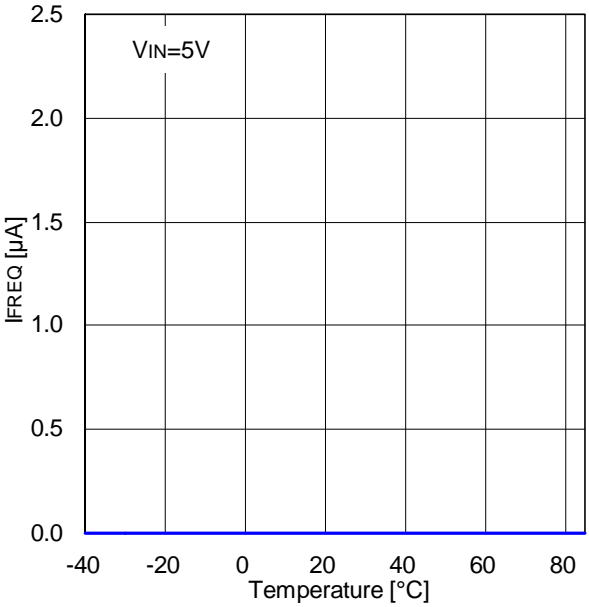


Figure 15. FREQ Input Current vs Temperature

Typical Performance Curves - continued

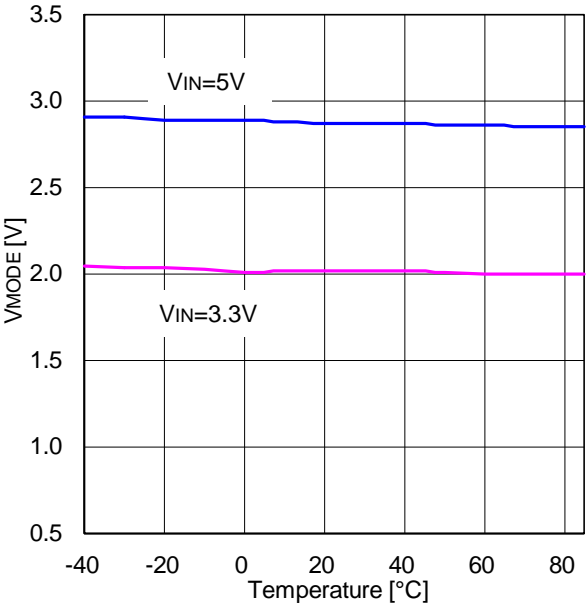


Figure 16. MODE Threshold Voltage vs Temperature

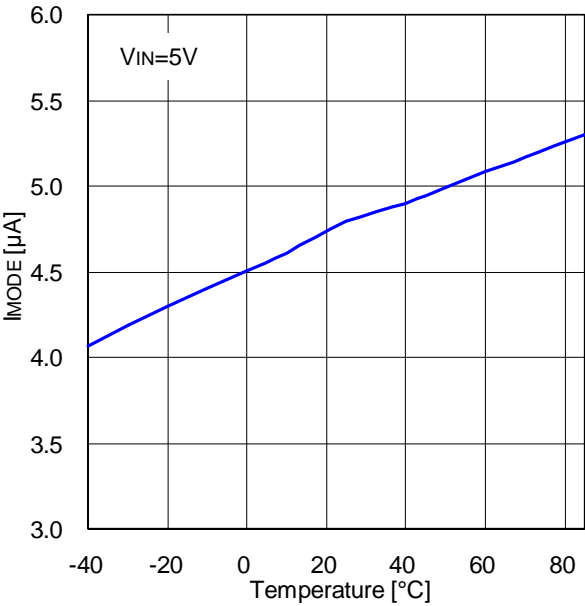


Figure 17. MODE Input Current vs Temperature

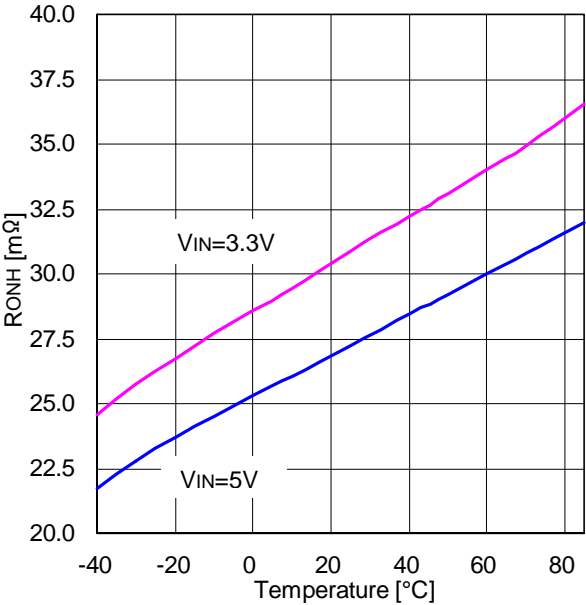


Figure 18. High Side ON-Resistance

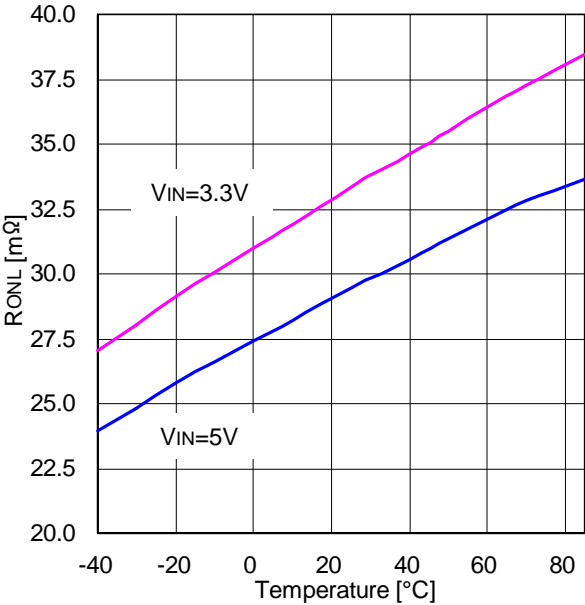


Figure 19. Low Side ON-Resistance

Typical Performance Curves - continued

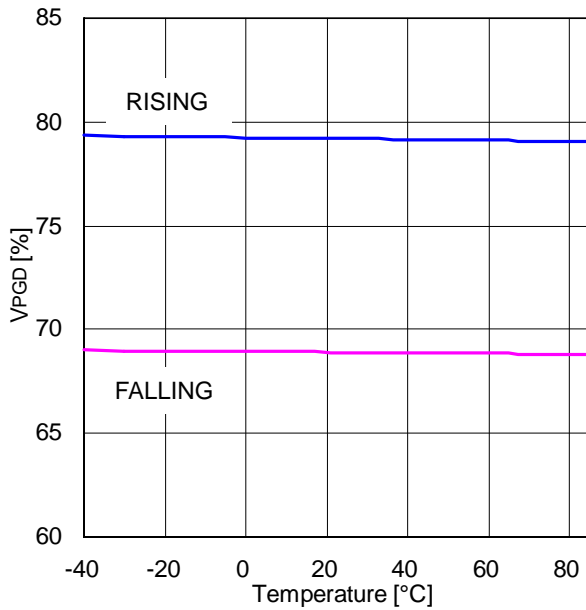


Figure 20. PGD Threshold vs Temperature

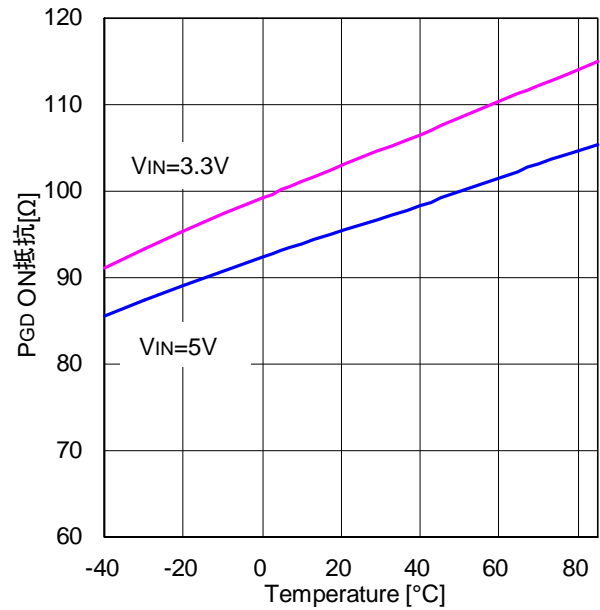


Figure 21. PGD ON ON-Resistance vs Temperature

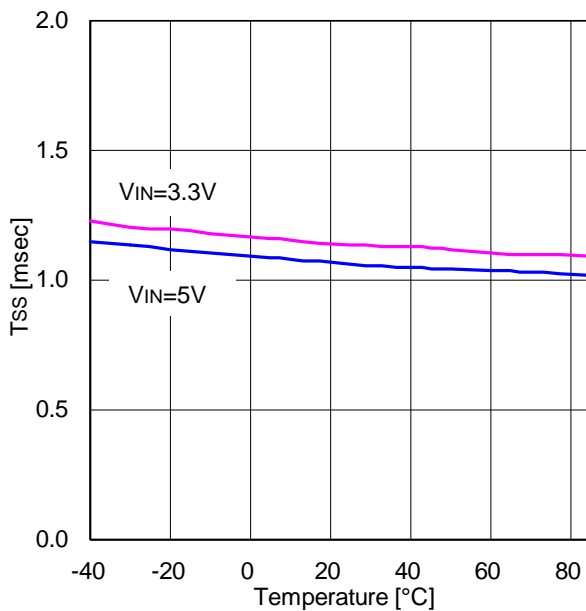


Figure 22. Soft Start Time vs Temperature

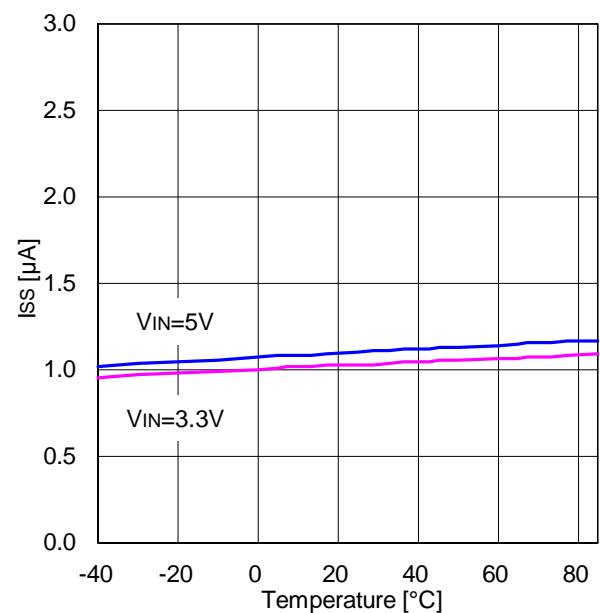


Figure 23. SS Terminal Current vs Temperature

Typical Performance Curves - continued

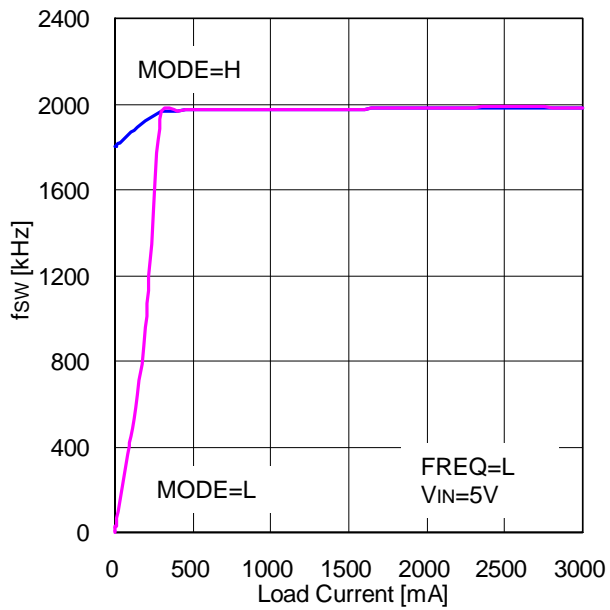


Figure 24. Switching Frequency vs Load Current

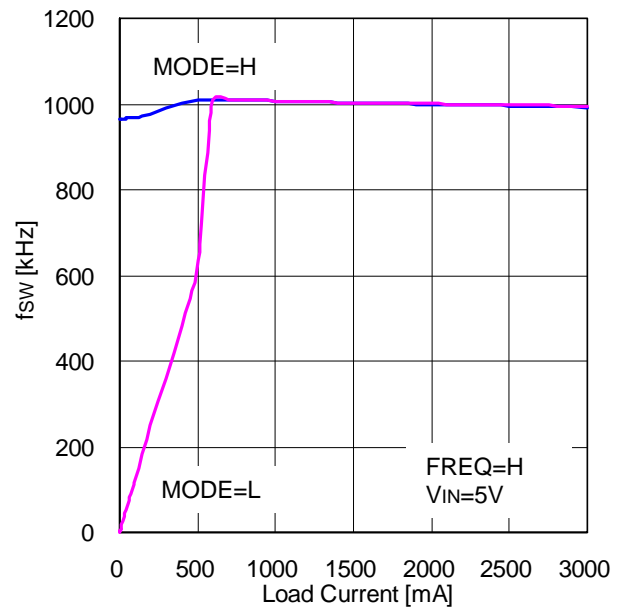


Figure 25. Switching Frequency vs Load Current

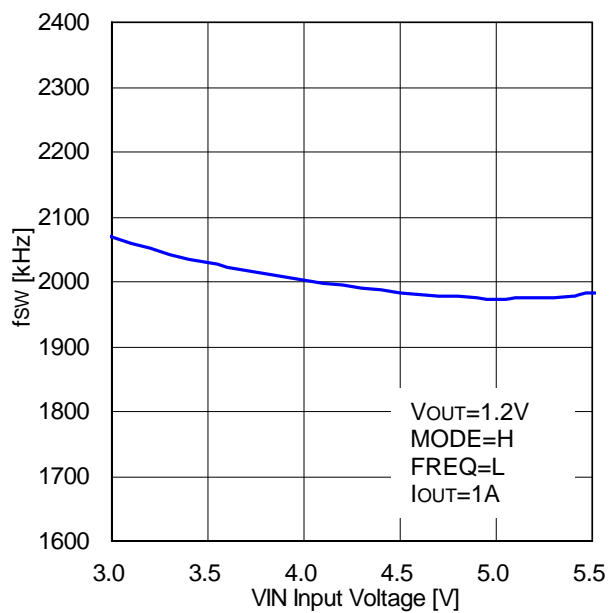


Figure 26. Switching Frequency vs Input Voltage

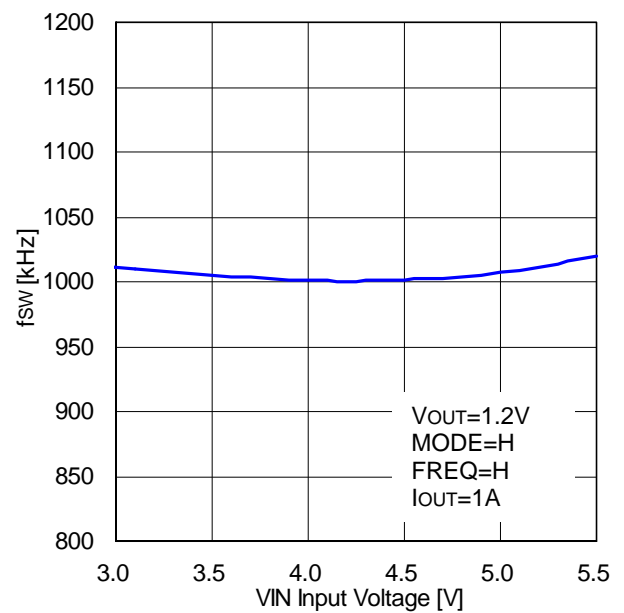


Figure 27. Switching Frequency vs Input Voltage

Typical Performance Curves - continued

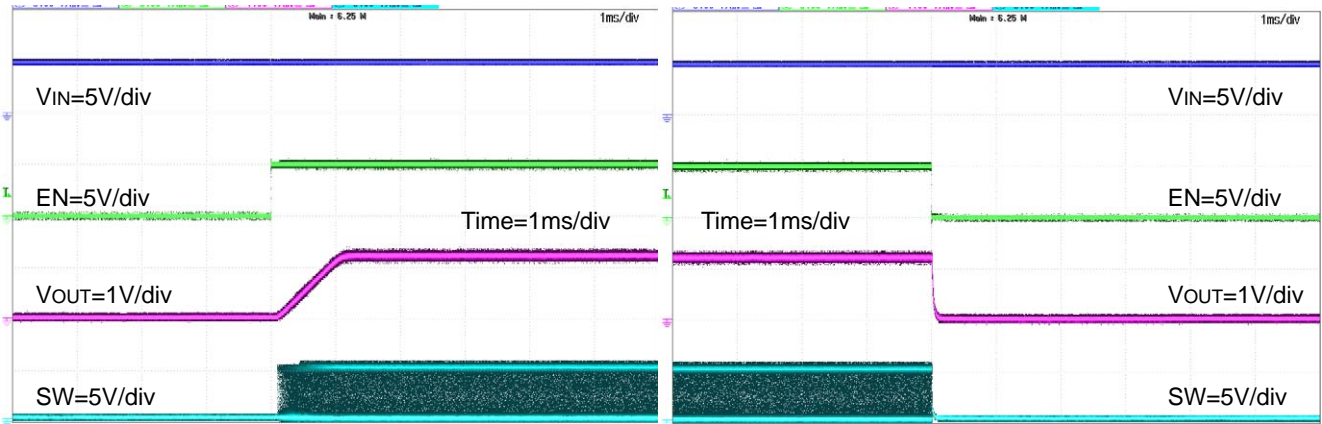


Figure 28. Power Up Waveform with EN
(FREQ=H, RLOAD=0.5Ω)

Figure 29. Power Down Waveform with EN
(FREQ=H, RLOAD=0.5Ω)

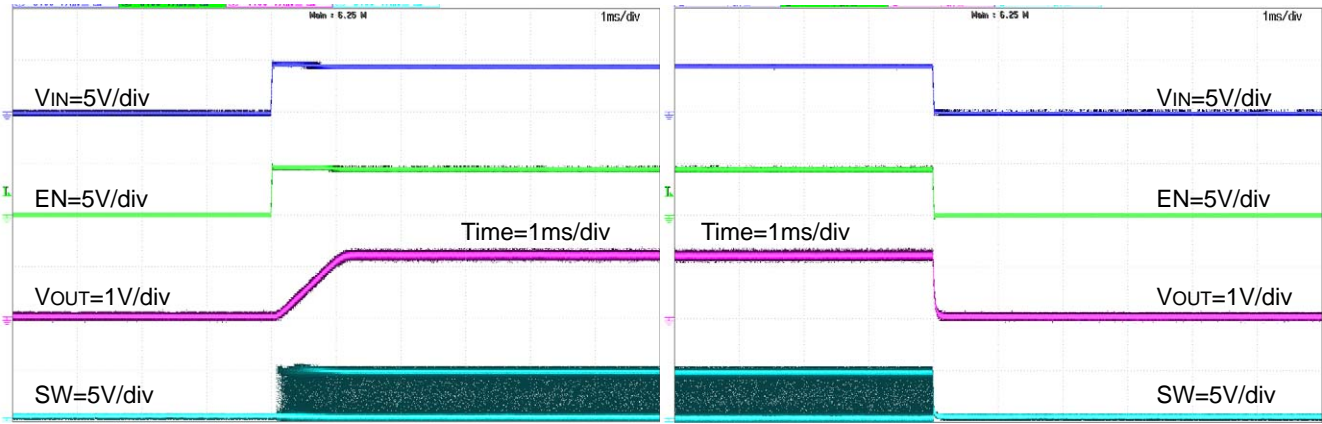


Figure 30. Power Up Waveform with VIN
(FREQ=H, RLOAD=0.5Ω)

Figure 31. Power Down Waveform with VIN
(FREQ=H, RLOAD=0.5Ω)

Typical Performance Curves - continued

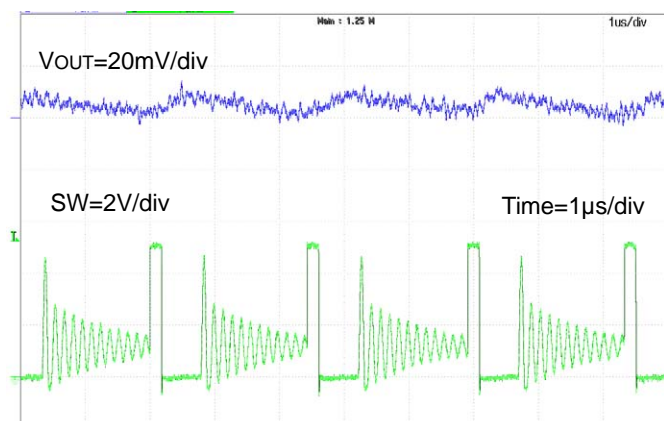


Figure 32. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=L, IOUT=0.1A)

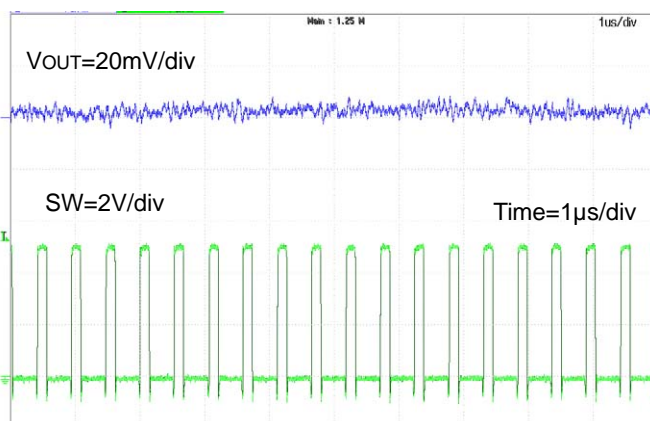


Figure 33. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=L, IOUT=3A)

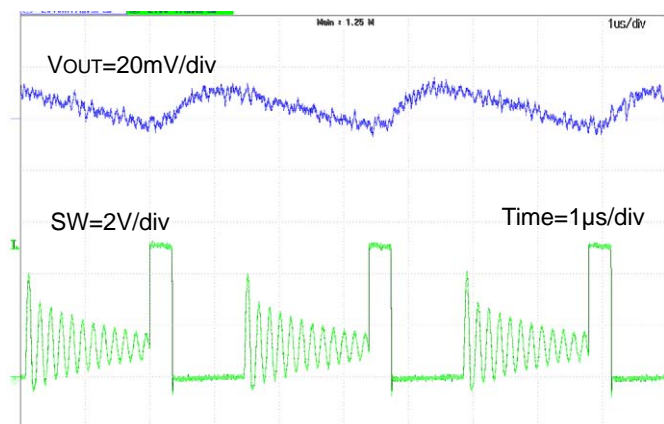


Figure 34. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=H, IOUT=0.2A)

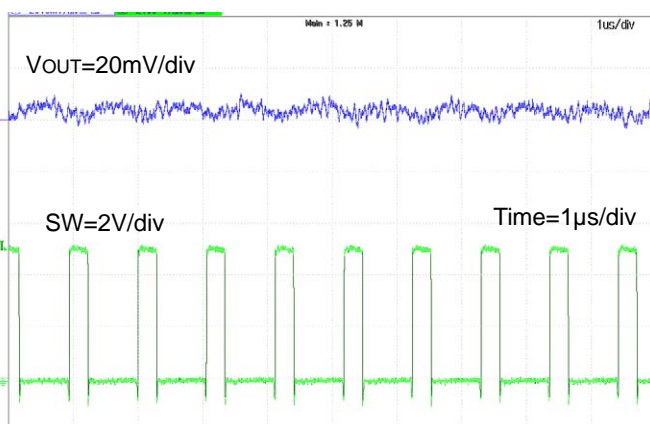


Figure 35. Switching Waveform
(VIN=5V, VOUT=1.2V, FREQ=H, IOUT=3A)

Typical Performance Curves - continued

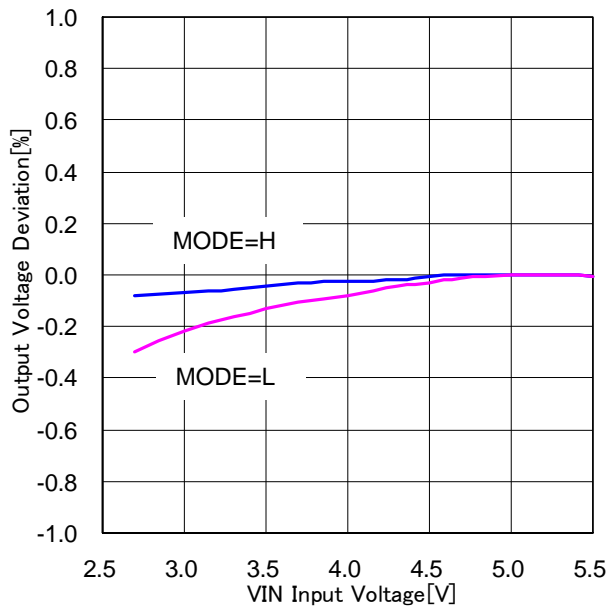


Figure 36. Line Regulation
($V_{OUT}=1.2V$, $L=1.5\mu H$, $FREQ=H$)

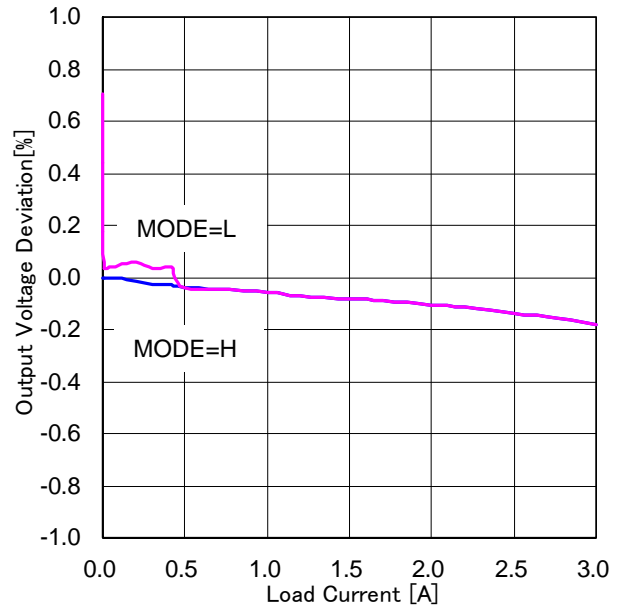


Figure 37. Load Regulation
($V_{IN}=5V$, $V_{OUT}=1.2V$, $L=1.5\mu H$, $FREQ=H$)

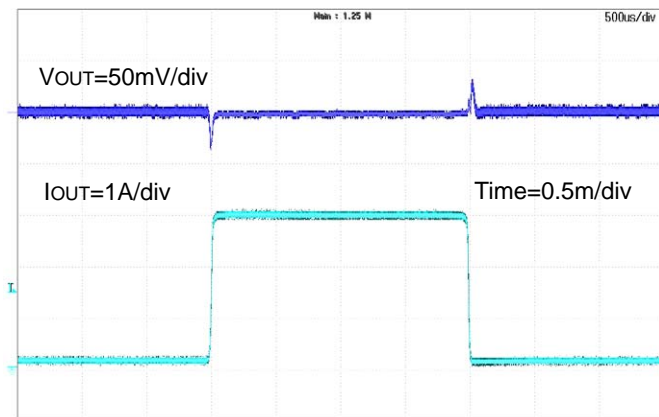


Figure 38. Load Transient Response $I_{OUT}=0.1A$ to $2A$
($V_{IN}=5V$, $V_{OUT}=1.2V$, $FREQ=L$, $MODE=L$, $C_{OUT}=\text{Ceramic } 44\mu F$)

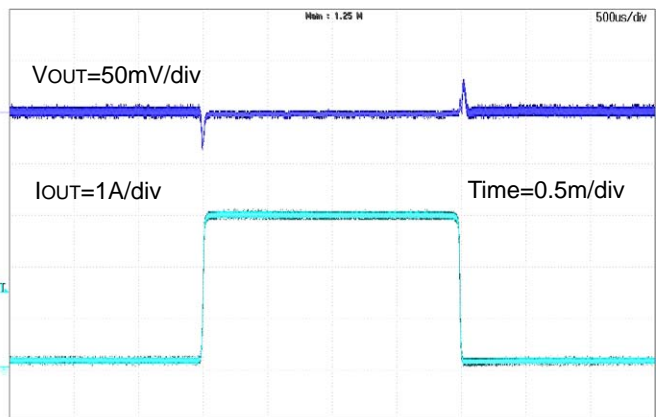


Figure 39. Load Transient Response $I_{OUT}=0A$ to $3A$
($V_{IN}=5V$, $V_{OUT}=1.2V$, $FREQ=L$, $MODE=H$, $C_{OUT}=\text{Ceramic } 44\mu F$)

Application Example(s)

1. Basic Operation

(1) DC/DC Converter operation

BD9B300MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing constant on-time control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes Deep-SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.

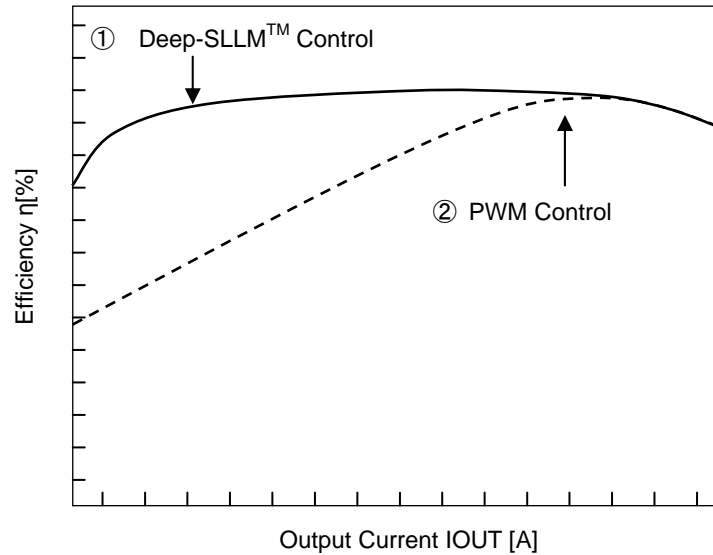
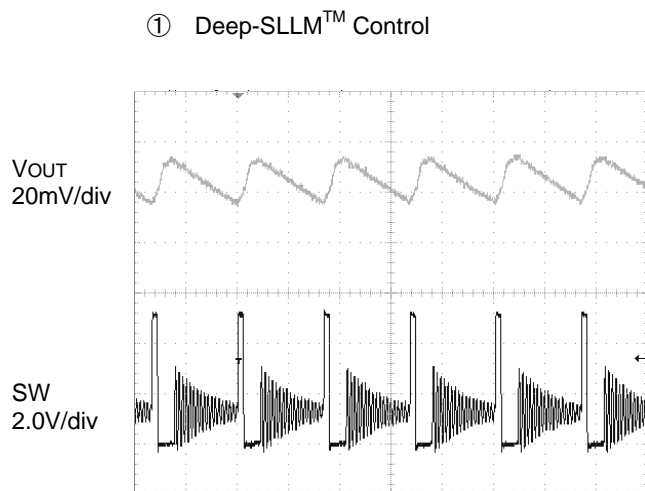
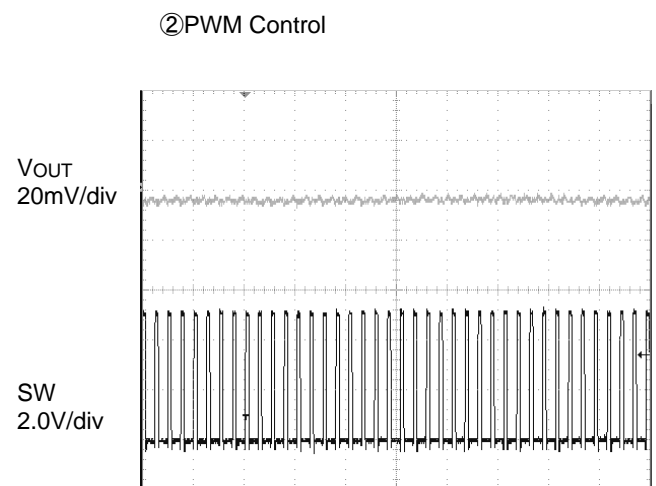


Figure 40. Efficiency (Deep-SLLM™ Control and PWM Control)

Figure 41. Switching Waveform at Deep-SLLM™ Control
(VIN=5.0V, VOUT=1.2V, IOUT=100mA)Figure 42. Switching Waveform at PWM Control
(VIN=5.0V, VOUT=1.2V, IOUT=3A)

(2) Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When VEN reaches 2.0 V(Typ), the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, the shutdown interval (Low level interval of EN) must be set to 100 μ s or longer.

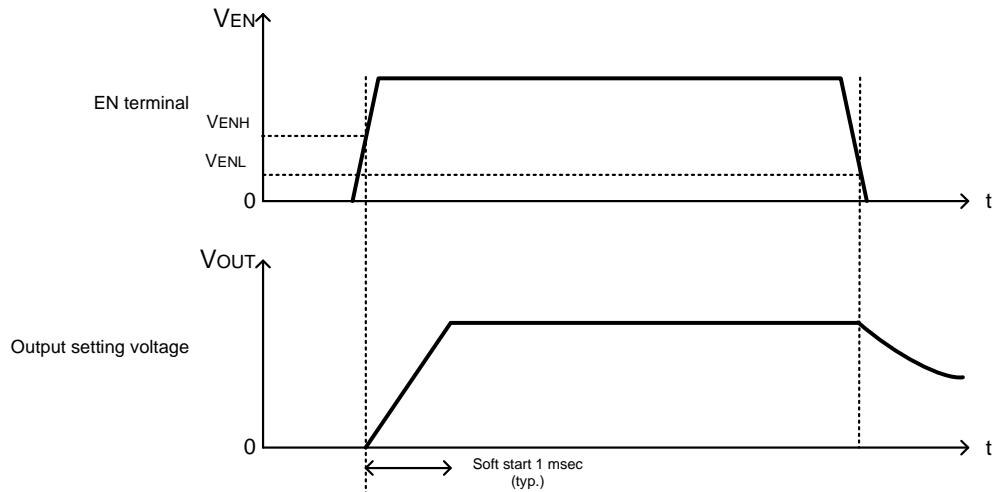


Figure 43. Start Up and Down with Enable

(3) Power Good

When the output voltage reaches more than 80% of the voltage setting, the open drain NMOSFET, internally connected to the PGD terminal, turns off and the PGD terminal turns to Hi-z condition. Also when the output voltage falls below 70% of voltage setting, the open drain NMOS FET turns on and PGD terminal pulls down with 100 Ω . Connecting a pull up resistor (10K Ω to 100K Ω) is recommended.

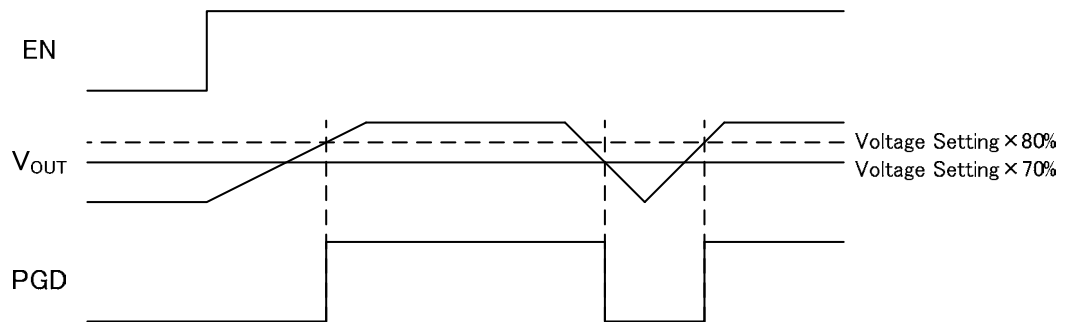


Figure 44. Power Good Timing Chart

(4) Soft Start

When EN terminal is turned High, Soft Start operates and output voltage gradually rises. With the Soft Start Function, over shoot of output voltage and rush current can be prevented. Rising time of output voltage when SS terminal is open is 1msec (typ.). Capacitor connected to SS terminal makes rising time more than 1msec. Please refer to page 23 for the method of setting rising time.

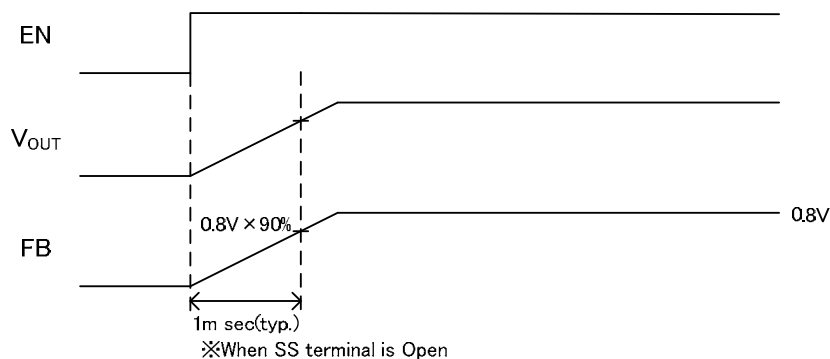


Figure 45. Soft Start Timing Chart

2. Protection

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Setting of Over current protection is 5.0A (typ.). When OCP is triggered, over current protection is realized by restricting On / Off Duty of current flowing in upper MOSFET by each switching cycle. Also, if Over current protection operates 1024 cycles in a condition where FB terminal voltage reaches below 70% of internal standard voltage, Short Circuit protection (SCP) operates and stops switching for 1msec (typ.) before it initiates restart. However, during startup, Short circuit protection will not operate even if the IC is still in the SCP condition.

Table 1. Over Current Protection / Short Circuit Protection Function

EN terminal	PGD	Startup	Over current protection	Short circuit protection
More than 2.0V	L	While start up	Valid	Invalid
		Startup completed	Valid	Valid
	H	*	Valid	Invalid
Less than 0.3V	*	*	Invalid	Invalid

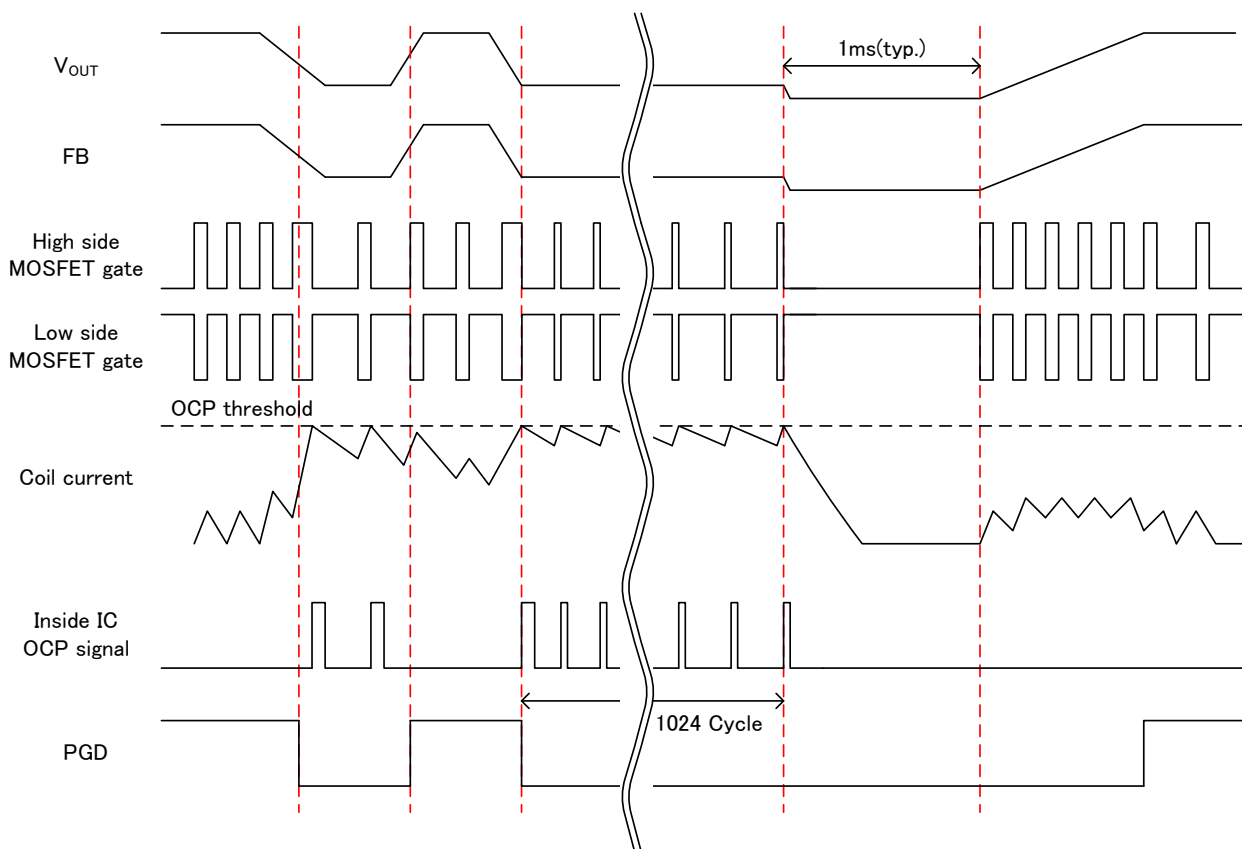


Figure 46. Short Circuit Protection (SCP) Timing Chart

(2) Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection circuit monitors the AVIN terminal voltage.

The operation enters standby when the AVIN terminal voltage is 2.45V (Typ) or lower.

The operation starts when the AVIN terminal voltage is 2.55V (Typ) or higher.

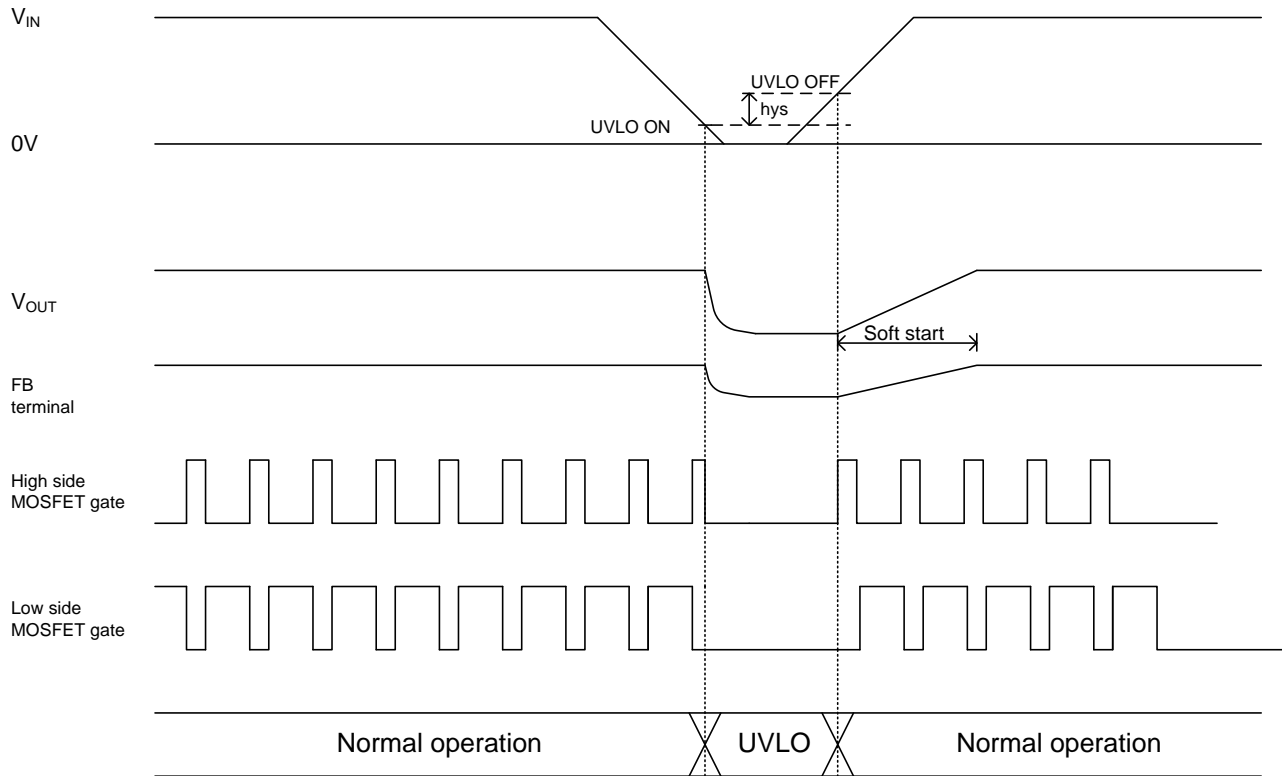


Figure 47. UVLO Timing Chart

(3) Thermal Shutdown

When the chip temperature exceeds $T_j=175^{\circ}\text{C}$, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding $T_{j\text{max}}=150^{\circ}\text{C}$. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

Application Example

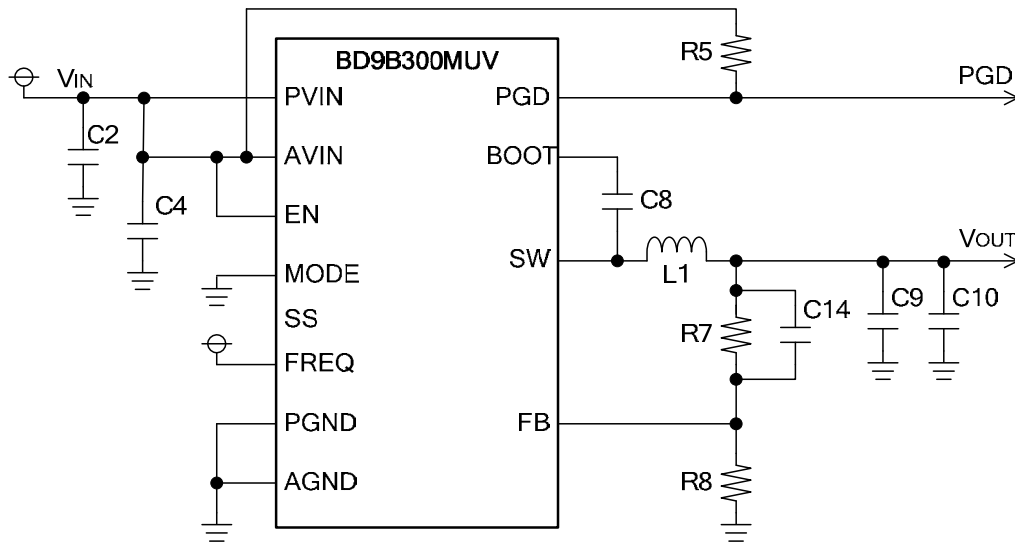


Figure 48. Application Circuit

Table 2. Recommended Component Values (VIN=5V, FREQ=H)

Reference Designator	VOUT					Description
	1.0V	1.2V	1.5V	1.8V	3.3V	
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	75kΩ	75kΩ	160kΩ	150kΩ	160kΩ	-
R8	300kΩ	150kΩ	180kΩ	120kΩ	51kΩ	-
C2	10μF	10μF	10μF	10μF	10μF	10V, X5R, 3216
C4	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	25V, X5R, 1608
C8	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	-
C9	22μF	22μF	22μF	22μF	22μF	6.3V, X5R, 3225
C10	22μF	22μF	22μF	22μF	22μF	6.3V, X5R, 3225
C14	120p	120pF	150pF	180pF	180pF	-
L1	1.5μH	1.5μH	1.5μH	1.5μH	1.5μH	TOKO, FDSD0630

Table 3. Recommended Component Values (VIN=5V, FREQ=L)

Reference Designator	VOUT					Description
	1.0V	1.2V	1.5V	1.8V	3.3V	
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	75kΩ	75kΩ	160kΩ	150kΩ	160kΩ	-
R8	300kΩ	150kΩ	180kΩ	120kΩ	51kΩ	-
C2	10μF	10μF	10μF	10μF	10μF	10V, X5R, 3216
C4	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	25V, X5R, 1608
C8	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	-
C9	22μF	22μF	22μF	22μF	22μF	6.3V, X5R, 3225
C10	22μF	22μF	22μF	22μF	22μF	6.3V, X5R, 3225
C14	100p	120pF	100pF	120pF	120pF	-
L1	1.0μH	1.0μH	1.0μH	1.0μH	1.0μH	TOKO, FDSD0630

Selection of Components Externally Connected

1. Output LC Filter Constant

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. It is recommended to use inductors of values 0.47μH to 1.0μH when FREQ=L or 1.0μH to 1.5μH at FREQ=H.

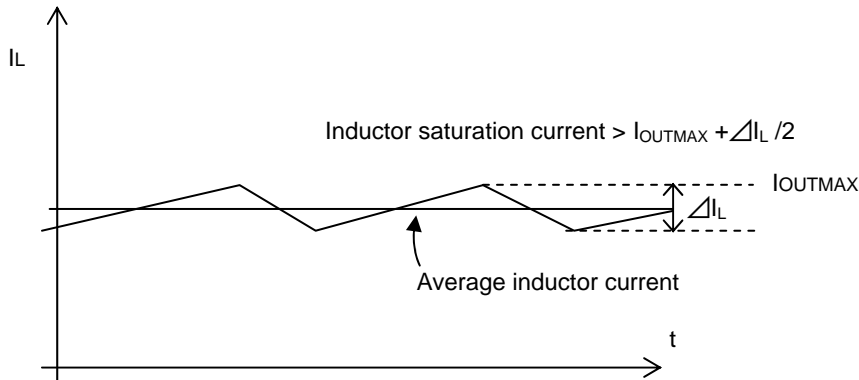


Figure 49. Waveform of current through inductor

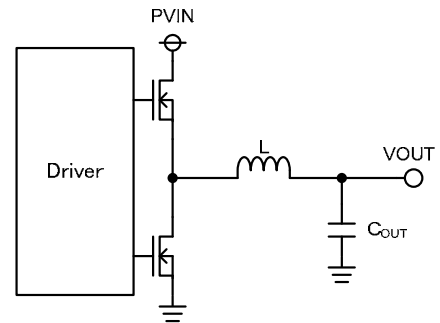


Figure 50. Output LC filter circuit

Inductor ripple current ΔI_L

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 608[\text{mA}]$$

Where:

VIN= 5V

VOUT= 1.2V

L=1.5μH

FOSC=1MHz (switching frequency)

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L .

The output capacitor COUT affects the output ripple voltage characteristics. The output capacitor COUT must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}})[V]$$

where RESR is the Equivalent Series Resistance (ESR) of the output capacitor.

* The capacitor rating must allow a sufficient margin with respect to the output voltage.

The output ripple voltage can be decreased with a smaller ESR.

A ceramic capacitor of about 22 μF to 47 μF is recommended.

*Be careful of total capacitance value, when additional capacitor C_{LOAD} is connected in addition to output capacitor C_{OUT}. Use maximum additional capacitor C_{LOAD} (Max) condition which satisfies the following condition.

$$\text{Maximum starting inductor ripple current } I_{LSTART} < \text{Over Current limit } 3.8A(\text{min})$$

Maximum starting inductor ripple current I_{LSTART} can be expressed using the following equation.

$$I_{LSTART} = \text{Maximum starting output current}(I_{OMAX}) + \text{Charge current to output capacitor}(I_{CAP}) + \frac{\Delta I_L}{2}$$

Charge current to output capacitor I_{CAP} can be expressed using the following equation.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} [A]$$

For example, given $V_{IN} = 5V$, $V_{OUT} = 3.3V$, $L = 1.5\mu H$, switching frequency $F_{OSC} = 800kHz$ (Min), Output capacitor $C_{OUT} = 44\mu F$, Soft Start time $T_{SS} = 0.5ms$ (Min), and load current during soft start $I_{OSS} = 3A$, maximum C_{LOAD} can be computed using the following equation.

$$C_{LOAD}(max) < \frac{(3.8 - I_{OSS} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 6.38 [\mu F]$$

If the value of C_{LOAD} is large, and cannot meet the above equation, adjust the value of the capacitor C_{SS} to meet the condition below.

$$C_{LOAD}(max) < \frac{(3.8 - I_{OSS} - \Delta I_L/2) \times V_{FB}}{V_{OUT} \times I_{SS}} \times C_{SS} - C_{OUT}$$

(Refer to the following items (3) Soft Start Setting equation of time T_{SS} and soft-start value of the capacitor to be connected to the C_{SS} .)

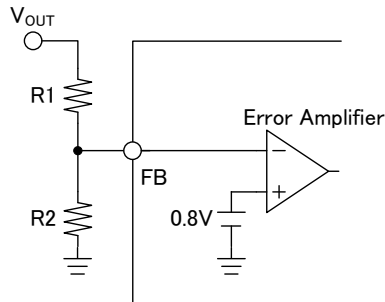
For example, given $V_{IN} = 5V$, $V_{OUT} = 3.3V$, $L = 1.5\mu H$, load current during soft start $I_{OSS} = 3A$, switching frequency $F_{OSC} = 800kHz$ (Min), Output capacitor $C_{OUT} = 44\mu F$, $V_{FB} = 0.792V$ (Max), $I_{SS} = 3.6\mu A$ (Max), with $C_{LOAD} = 220\mu F$, capacitor C_{SS} is computed as follows.

$$C_{SS} > \frac{V_{OUT} \times I_{SS}}{(3.8 - I_{OSS} - \Delta I_L/2) \times V_{FB}} \times (C_{LOAD} + C_{OUT}) = 6617 [pF]$$

2. Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio.

For stable operation, it is recommended to use feedback resistance R_1 of more than $20k\Omega$.



$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 0.8 [V]$$

$$R_2 = \frac{0.8}{V_{OUT} - 0.8} \times R_1 [\Omega]$$

Figure 51. Feedback Resistor Circuit

3. Soft Start Setting

Turning the EN terminal signal High activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$T_{SS} = (C_{SS} \times V_{FB}) / I_{SS}$$

$$C_{SS} = (I_{SS} \times T_{SS}) / V_{FB}$$

T_{SS} : Soft Start Time

C_{SS} : Capacitor connected to Soft Start Time Terminal

V_{FB} : FB Terminal Voltage (0.8V (Typ))

I_{SS} : Soft Start Terminal Source Current (1.0μA(Typ))

with $C_{SS} = 0.01\mu F$,

$$\begin{aligned} T_{SS} &= (0.01[\mu F] \times 0.8[V]) / 1.0[\mu A] \\ &= 8.0[\text{msec}] \end{aligned}$$

Turning the EN terminal signal High with the SS terminal open or with the terminal signal High (no capacitor connected) causes the output voltage to rise in 1msec (Typ).

4. FB Capacitor

Generally, in fixed ON time control (hysteresis control), sufficient ripple voltage in FB voltage is needed to operate comparator stably. Regarding this IC, by injecting ripple voltage to FB voltage inside IC it is designed to correspond to low ESR output capacitor. Please set the FB capacitor within the range of the following expression to inject an appropriate ripple.

$$\frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{f_{SW} \times 7.5 \times 10^3} < C_{FB} < \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})}{f_{SW} \times 3.6 \times 10^3}$$

V_{IN} : Input Voltage

V_{OUT} : Output Voltage

f_{SW} : Switching Frequency

PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the High-Side FET is turned ON. The flow starts from the input capacitor C_{IN} , runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT} . The second loop is the one into which the current flows when the Low-Side FET is turned on. The flow starts from the Low-Side FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the Low-Side FET via GND of C_{OUT} . Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

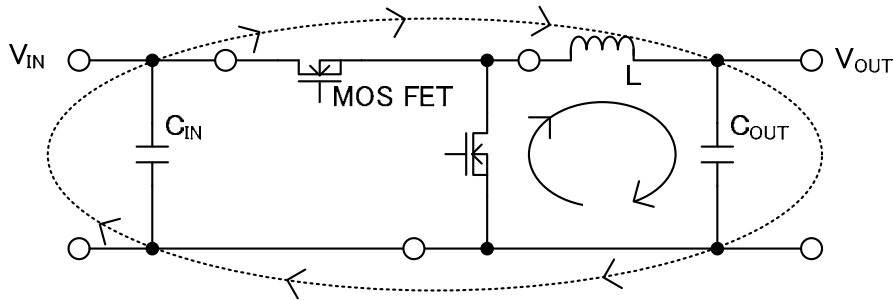


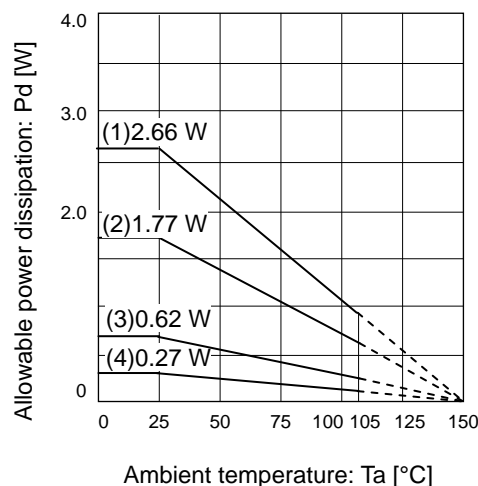
Figure 52. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.



- (1) 4-layer board (surface heat dissipation copper foil 5505 mm²)
(copper foil laminated on each layer)
 $\theta_{JA} = 47.0^{\circ}\text{C/W}$
- (2) 4-layer board (surface heat dissipation copper foil 6.28 mm²)
(copper foil laminated on each layer)
 $\theta_{JA} = 70.62^{\circ}\text{C/W}$
- (3) 1-layer board (surface heat dissipation copper foil 6.28 mm²)
 $\theta_{JA} = 201.6^{\circ}\text{C/W}$
- (4) IC only
 $\theta_{JA} = 462.9^{\circ}\text{C/W}$

Figure 53. Thermal Derating Characteristics
(VQFN016V3030)

I/O equivalence circuit(s)

<p>6. FB</p>	<p>7. FREQ</p>
<p>8. MODE</p>	<p>9. SS</p>
<p>10.11.12. SW</p>	<p>13. BOOT</p>
<p>14. PGD</p>	<p>15. EN</p>

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

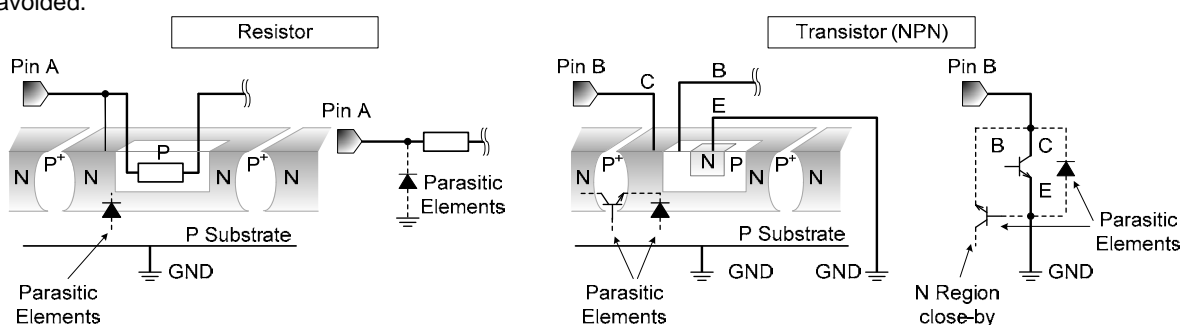


Figure 54. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

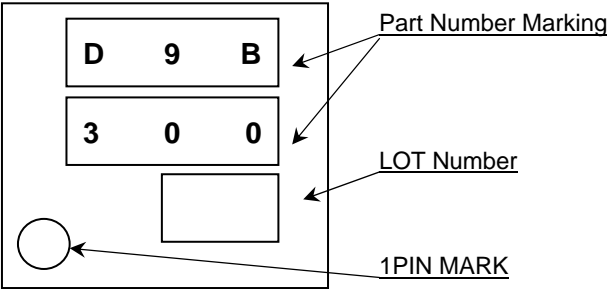
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B D 9 B 3 0 0 M U V										-	E 2	
Part Number										Package		Packaging and forming specification
										VQFN016N3030		E2: Embossed tape and reel

Marking Diagrams

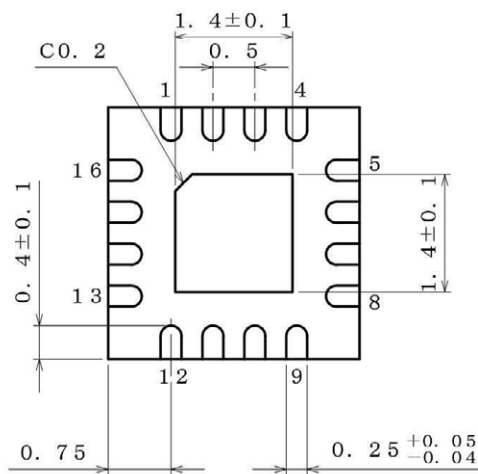
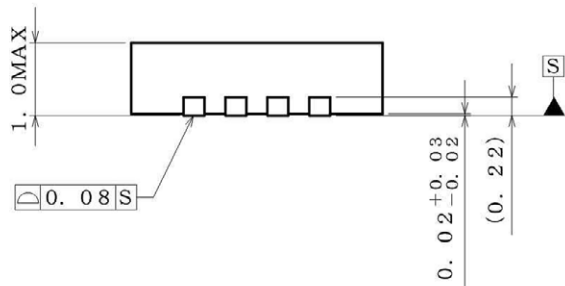
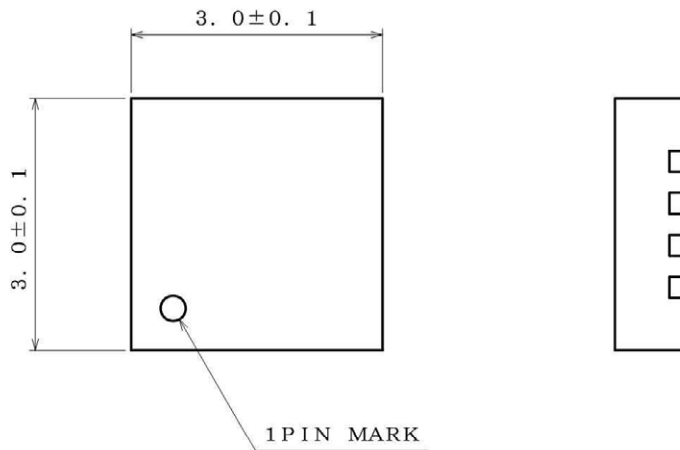
VQFN016V3030 (TOP VIEW)



Physical Dimension, Tape and Reel Information

Package Name

VQFN016V3030



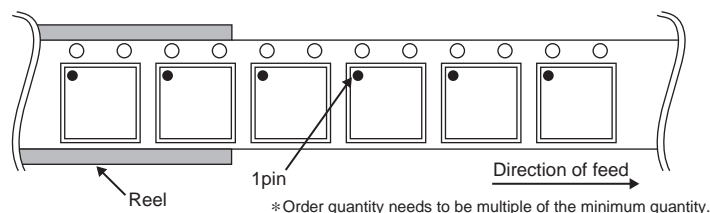
(UNIT : mm)

PKG : VQFN016V3030

Drawing No. EX460-5001-2

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
23.MAY.2014	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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