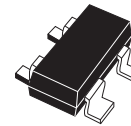


Open drain microprocessor reset

Features

- Low supply current of 1.5 μ A (typ)
- $\pm 1.8\%$ reset threshold accuracy (25 $^{\circ}$ C)
- Guaranteed $\overline{\text{RST}}$ assertion down to $V_{\text{CC}} = 1.0\text{V}$
- Open drain $\overline{\text{RST}}$ output can exceed V_{CC}
- Power supply transient immunity
- Operating temperature: -40 to $+125^{\circ}\text{C}$
- Available in SOT143-4 package.



SOT143-4 (W1)

Contents

| | | |
|----------|---|-----------|
| 1 | Summary description | 5 |
| 2 | Operation | 7 |
| 2.1 | Reset output | 7 |
| 2.2 | Manual reset input | 7 |
| 2.3 | Negative-going V_{CC} transients | 7 |
| 2.4 | Valid \overline{RST} output down to $V_{CC} = 0V$ | 8 |
| 3 | Typical operating characteristics | 9 |
| 4 | Maximum rating | 12 |
| 5 | DC and AC parameters | 13 |
| 6 | Package mechanical data | 16 |
| 7 | Part numbering | 18 |
| 8 | Revision history | 20 |

List of tables

| | | |
|----------|--|----|
| Table 1. | Signal names | 5 |
| Table 2. | Absolute maximum ratings | 12 |
| Table 3. | Operating and AC measurement conditions | 13 |
| Table 4. | DC and AC characteristics | 14 |
| Table 5. | SOT143-4 – 4-lead small outline transistor package mechanical data | 17 |
| Table 6. | Ordering information scheme | 18 |
| Table 7. | Marking description | 19 |
| Table 8. | Document revision history | 20 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Logic diagram | 5 |
| Figure 2. | SOT143-4 connections (top view) | 5 |
| Figure 3. | Block diagram | 6 |
| Figure 4. | Hardware hookup | 6 |
| Figure 5. | Reset timing diagram | 8 |
| Figure 6. | Manual reset timing diagram, switch bounce/debounce | 8 |
| Figure 7. | Supply current vs. supply voltage, $V_{RST} = 2.63V$ | 9 |
| Figure 8. | Supply current vs. temperature (no load), $V_{RST} = 2.63V$ | 9 |
| Figure 9. | \overline{RST} output voltage vs. output current, $V_{CC} = 4.25V$ | 10 |
| Figure 10. | Normalized reset time-out period vs. temperature | 10 |
| Figure 11. | Normalized reset threshold vs. temperature | 11 |
| Figure 12. | Max. transient duration not causing reset pulse vs. reset threshold Overdrive | 11 |
| Figure 13. | AC testing input/output waveforms | 13 |
| Figure 14. | SOT143-4 – 4-lead small outline transistor package outline | 17 |

1 Summary description

The STM6315 Microprocessor Reset Circuit is a low power supervisory device used to monitor power supplies. It performs a single function: asserting a reset signal whenever the V_{CC} supply voltage drops below a preset value and keeping it asserted until V_{CC} has risen above the preset threshold for a minimum period of time (t_{rec}). It also provides a manual reset input (\overline{MR}). The open drain \overline{RST} output can be pulled up to a voltage higher than V_{CC} , but less than 6V.

The STM6315 comes with standard factory-trimmed reset thresholds of 2.63V, 2.93V, 3.08V, 4.38V, and 4.63V. The STM6315 is available in the SOT143-4 package.

Figure 1. Logic diagram

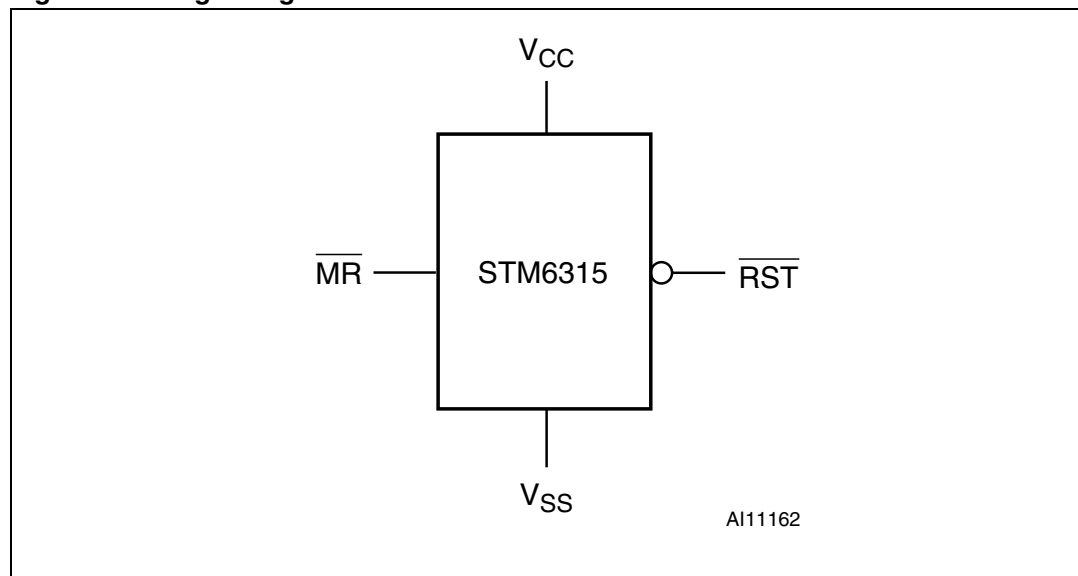


Table 1. Signal names

| Symbol | Description |
|------------------|------------------------------------|
| V_{CC} | Supply voltage |
| \overline{MR} | Manual reset input |
| \overline{RST} | Active-low open drain reset output |
| V_{SS} | Ground |

Figure 2. SOT143-4 connections (top view)

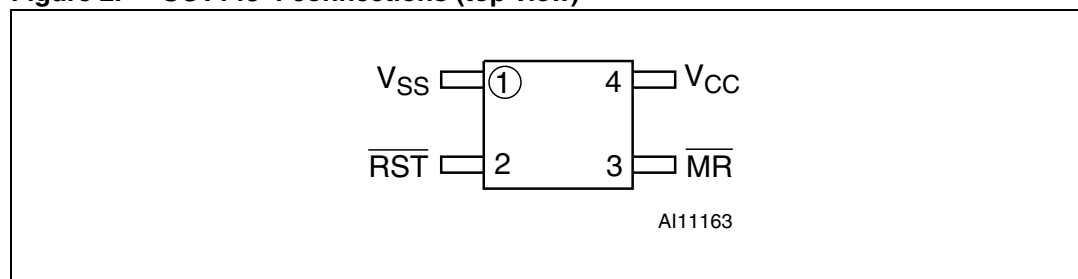


Figure 3. Block diagram

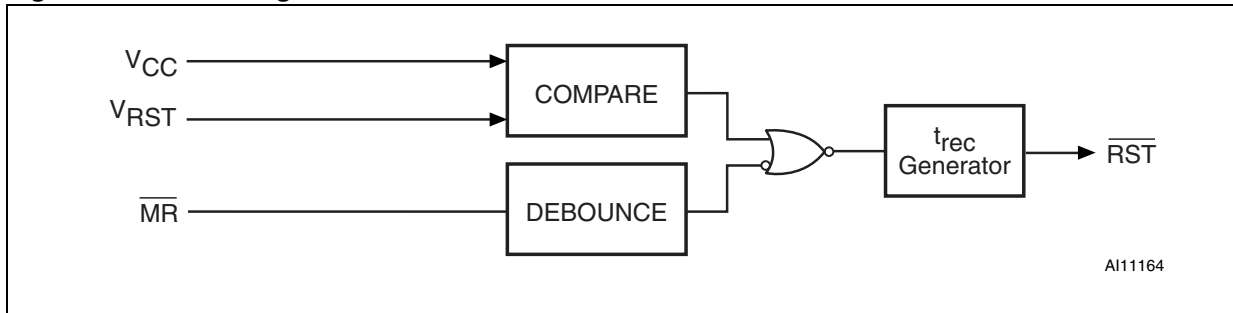
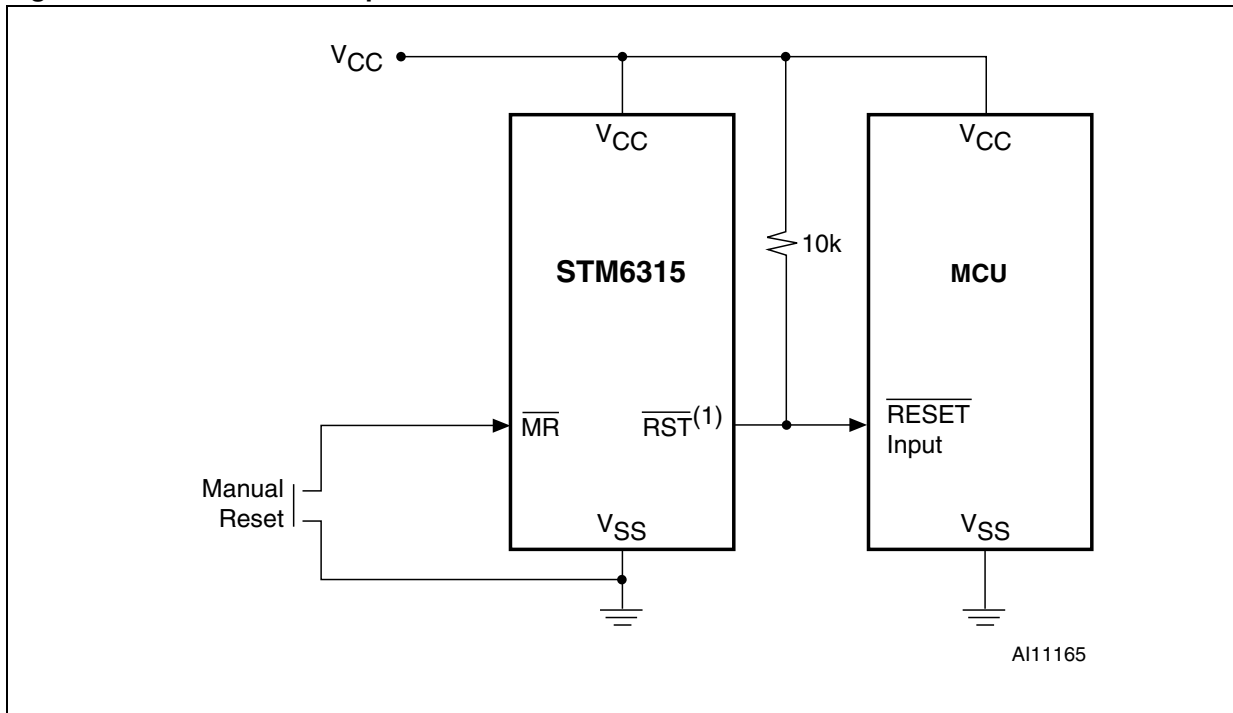


Figure 4. Hardware hookup



1. Open drain \overline{RST} output requires external pull-up resistor.

2 Operation

2.1 Reset output

The STM6315 Microprocessor Reset Circuit has an active-low, open drain reset output. This output structure will sink current when \overline{RST} is asserted. Connect a pull-up resistor from \overline{RST} to any supply voltage up to 6V (see [Figure 4 on page 6](#)). Select a resistor value large enough to register a logic low, and small enough to register a logic high while supplying all input current and leakage paths connected to the reset output line. A 10k pull-up is sufficient in most applications.

The STM6315 asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), or when the manual reset input (\overline{MR}) is taken low (see [Figure 5](#) and [Figure 6 on page 8](#)). \overline{RST} is guaranteed valid down to $V_{CC} = 1.0V$.

During power-up, (once V_{CC} exceeds the reset threshold) an internal timer keeps \overline{RST} low for the reset time-out period, t_{rec} . After this interval, \overline{RST} returns high.

If V_{CC} drops below the reset threshold, \overline{RST} goes low. Each time \overline{RST} is asserted, it stays low for at least the reset time-out period. Any time V_{CC} goes below the reset threshold, the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

2.2 Manual reset input

A logic low on \overline{MR} asserts \overline{RST} . \overline{RST} remains asserted while \overline{MR} is low, and for t_{rec} after it returns high. The \overline{MR} input has an internal pull-up resistor 63k Ω (typ), allowing it to be left open if not used.

This input can be driven with TTL/CMOS-logic levels or with open drain/collector outputs. Connect a standard open push-button switch from \overline{MR} to V_{SS} to create a manual reset function (see [Figure 4 on page 6](#)); external debounce circuitry is not required. If the device is used in a noisy environment, connect a 0.1 μ F capacitor from \overline{MR} to V_{SS} to provide additional noise immunity.

2.3 Negative-going V_{CC} transients

The STM6315 is relatively immune to negative-going V_{CC} transients (glitches). [Figure 12 on page 11](#) shows typical transient duration versus reset comparator overdrive (for which the STM6315 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to V_{CC} , starting at 0.5V above the actual reset threshold and ending below it by the magnitude indicated (Reset Threshold Overdrive). The graph indicates the maximum pulse width a negative V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal (see [Figure 12](#)). A 0.1 μ F bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

2.4 Valid $\overline{\text{RST}}$ output down to $V_{\text{CC}} = 0\text{V}$

When V_{CC} falls below 1V, the $\overline{\text{RST}}$ output no longer sinks current, but becomes an open circuit. In most systems this is not a problem, as most MCUs do not operate below 1V. However, in applications where $\overline{\text{RST}}$ output must be valid down to 0V, a pull-down resistor may be added to hold the $\overline{\text{RST}}$ output low. This resistor must be large enough to not load the $\overline{\text{RST}}$ output, and still be small enough to pull the output to Ground. A 100K Ω resistor is recommended.

Figure 5. Reset timing diagram

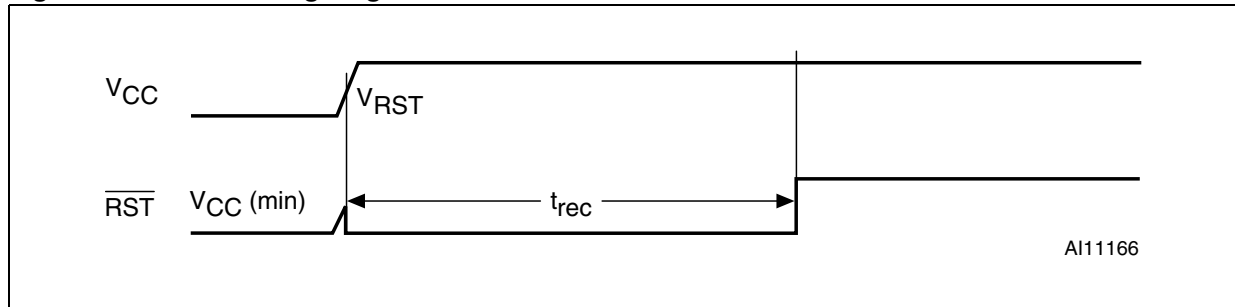
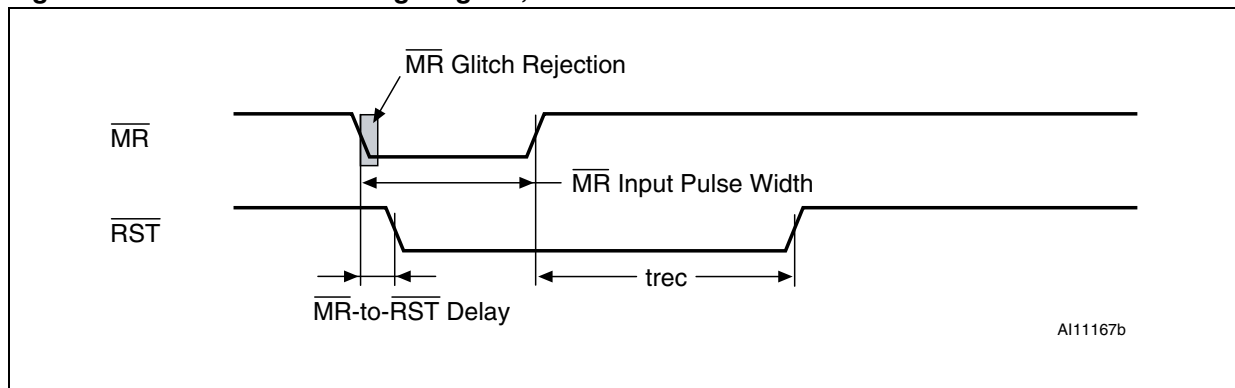


Figure 6. Manual reset timing diagram, switch bounce/debounce



3 Typical operating characteristics

Note: Typical values are at $T_A = 25^\circ\text{C}$.

Figure 7. Supply current vs. supply voltage, $V_{RST} = 2.63\text{V}$

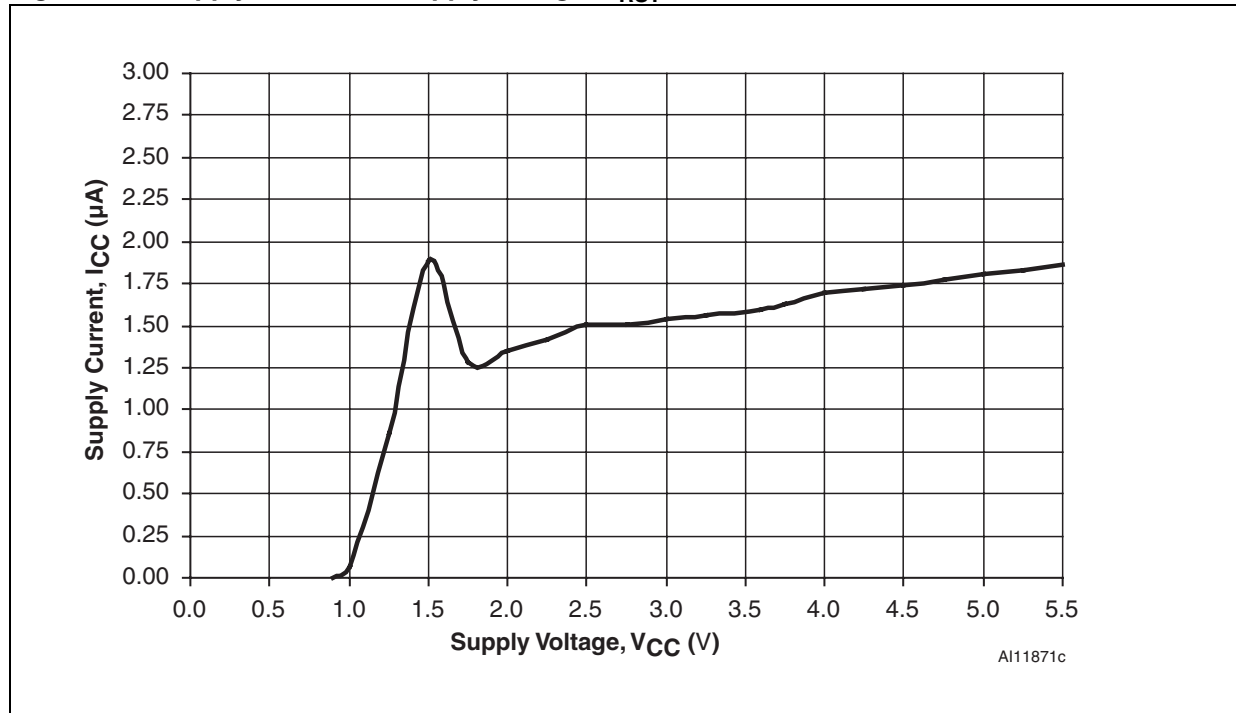


Figure 8. Supply current vs. temperature (no load), $V_{RST} = 2.63\text{V}$

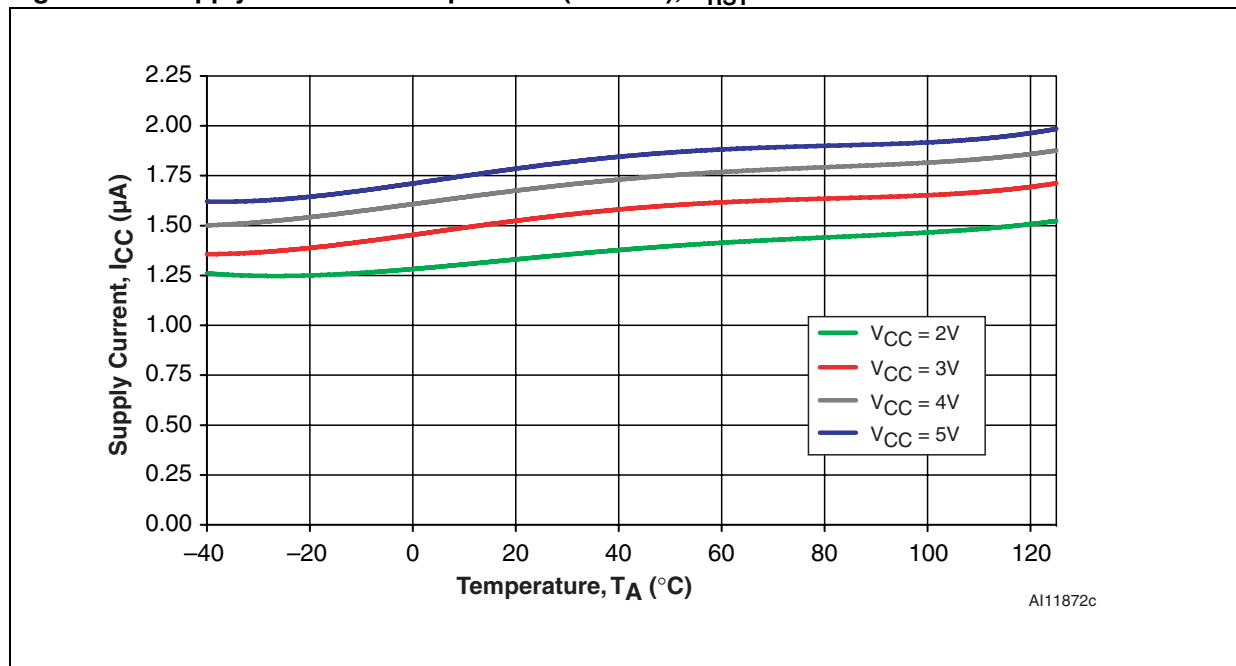


Figure 9. $\overline{\text{RST}}$ output voltage vs. output current, $V_{\text{CC}} = 4.25\text{V}$

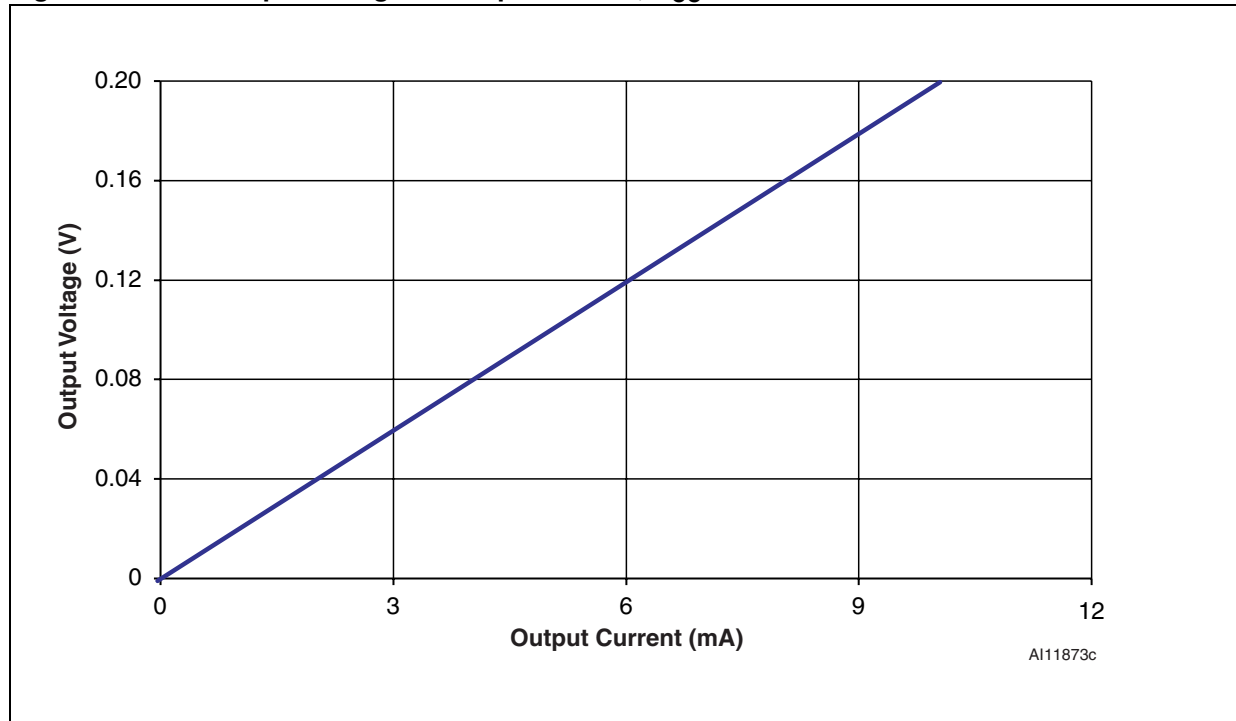


Figure 10. Normalized reset time-out period vs. temperature

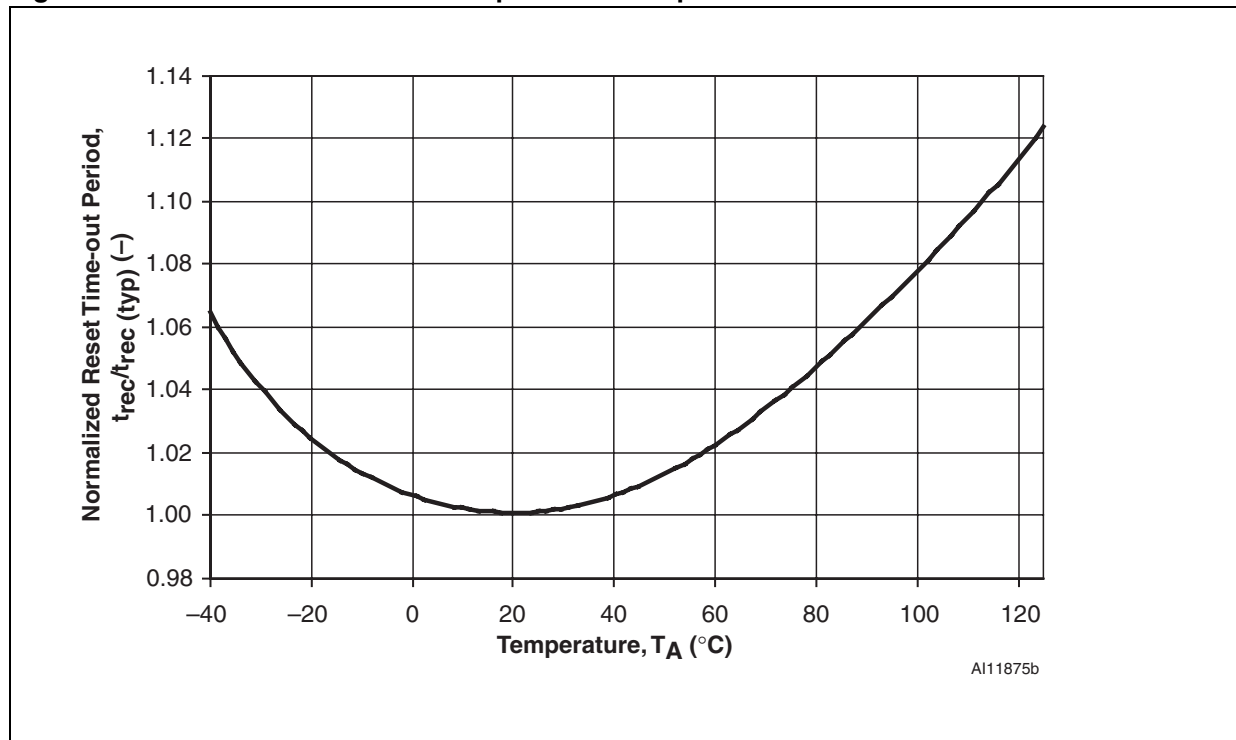


Figure 11. Normalized reset threshold vs. temperature

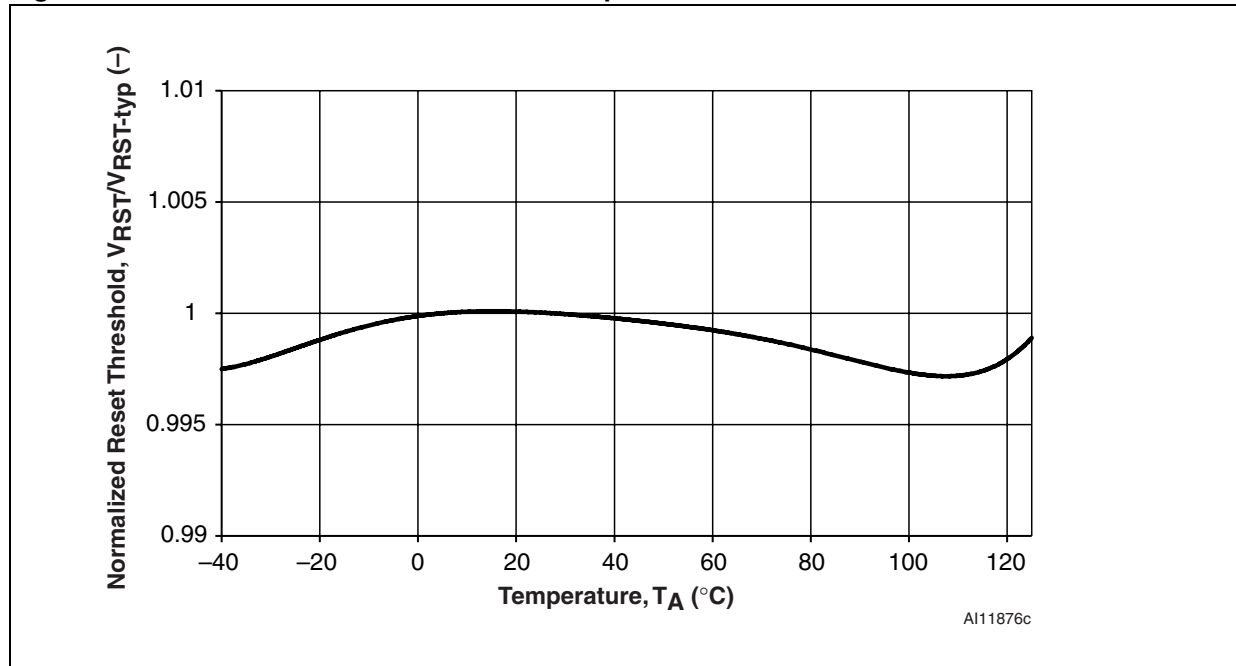
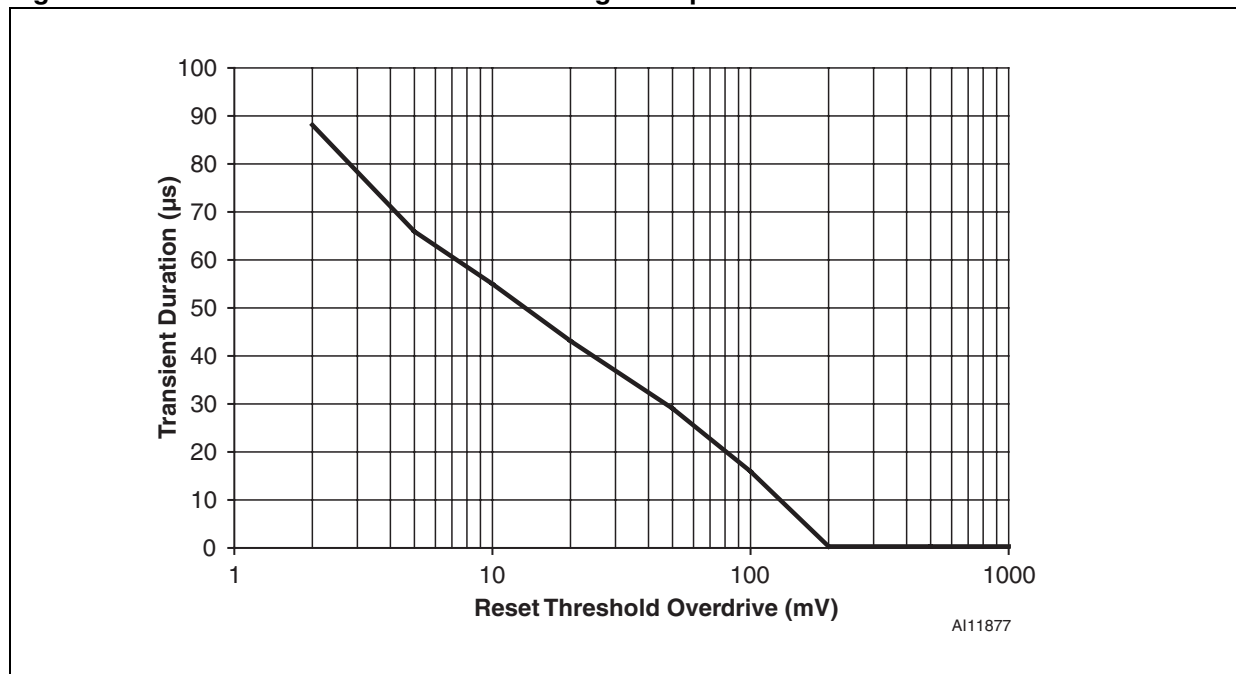


Figure 12. Max. transient duration not causing reset pulse vs. reset threshold Overdrive



Note: Reset occurs above the curve.

4 Maximum rating

Stressing the device above the rating listed in the [Table 2: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------------------------|---|-------------------------------|------|
| T _{STG} | Storage temperature (V _{CC} Off) | -55 to 150 | °C |
| T _{SLD} ⁽¹⁾ | Lead solder temperature for 10 seconds | 260 | °C |
| V _{IO} | Input or output voltage | -0.3 to V _{CC} + 0.3 | V |
| V _{CC} | Supply voltage | -0.3 to 7.0 | V |
| I _O | Output current | 20 | mA |
| P _D | Power dissipation | 320 | mW |

1. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow are derived from tests performed under the measurement conditions summarized in [Table 3: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and AC measurement conditions

| Parameter | STM6315 | Unit |
|--|--------------------|------|
| V_{CC} Supply Voltage | 1.0 to 5.5 | V |
| Ambient Operating Temperature (T_A) | -40 to +125 | °C |
| Input Rise and Fall Times | ~5 | ns |
| Input Pulse Voltages | 0.2 to $0.8V_{CC}$ | V |
| Input and Output Timing Reference Voltages | 0.3 to $0.7V_{CC}$ | V |

Figure 13. AC testing input/output waveforms

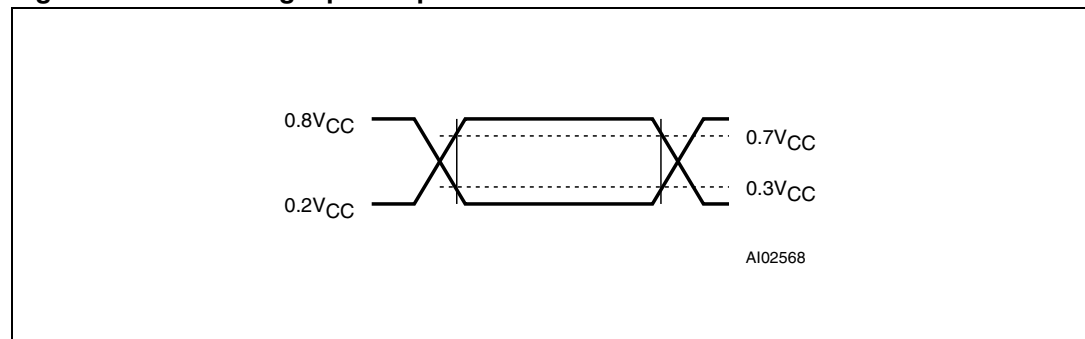


Table 4. DC and AC characteristics

| Sym | Description | Test Condition (1) | Min | Typ | Max | Unit | |
|-------------------------|--|---|--------------------------------|------------------|-------------------------|--------|----|
| V _{CC} | Operating voltage | | 1.0 | | 5.5 | V | |
| I _{CC} | V _{CC} supply current | V _{CC} = 5.5V, no load T _A = -40 to +85°C | | 2.0 | 12 | μA | |
| | | V _{CC} = 5.5V, no load T _A = -40 to +125°C | | | 15 | μA | |
| | | V _{CC} = 3.6V, no load T _A = -40 to +85°C | | 1.5 | 10 | μA | |
| | | V _{CC} = 3.6V, no load T _A = -40 to +125°C | | | 12 | μA | |
| V _{OL} | $\overline{\text{RST}}$ output voltage | V _{CC} > 4.25V, I _{SINK} = 3.2mA | | | 0.4 | V | |
| | | V _{CC} > 2.5V, I _{SINK} = 1.2mA | | | 0.3 | V | |
| | | V _{CC} > 1.0V, I _{SINK} = 80μA | | | 0.3 | V | |
| | $\overline{\text{RST}}$ output open drain Leakage Current | V _{CC} > V _{RST} , $\overline{\text{RST}}$ not asserted | | | 1 | μA | |
| Reset Thresholds | | | | | | | |
| V _{RST} | Reset threshold (2) (see Table 6 on page 18 for detailed listing) | V _{CC} falling; T _A = 25°C | V _{RST} - 1.8% | V _{RST} | V _{RST} + 1.8% | V | |
| | | V _{CC} falling; T _A = -40 to 85°C | V _{RST} - 2.5% | | V _{RST} + 2.5% | V | |
| | | V _{CC} falling; T _A = -40 to 125°C | V _{RST} - 3.5% | | V _{RST} + 3.5% | V | |
| t _{RD} | V _{CC} -to- $\overline{\text{RST}}$ delay | V _{CC} falling from (V _{RST} + 100mV) to (V _{RST} - 200mV) at 1mV/μs | | 35 | | μs | |
| t _{rec} | $\overline{\text{RST}}$ pulse width (2) | STM6315xAxxxx | T _A = -40 to +85°C | 1 | 1.5 | 2 | ms |
| | | | T _A = -40 to +125°C | 0.8 | | 2.4 | ms |
| | | STM6315xBxxxx | T _A = -40 to +85°C | 20 | 30 | 40 | ms |
| | | | T _A = -40 to +125°C | 16 | | 48 | ms |
| | | STM6315xDxxxx | T _A = -40 to +85°C | 140 | 210 | 280 | ms |
| | | | T _A = -40 to +125°C | 112 | | 336 | ms |
| STM6315xGxxxx | T _A = -40 to +85°C | 1120 | 1680 | 2240 | ms | | |
| | T _A = -40 to +125°C | 896 | | 2688 | ms | | |
| | Reset threshold temperature coefficient | | | 60 | | ppm/°C | |

Table 4. DC and AC characteristics (continued)

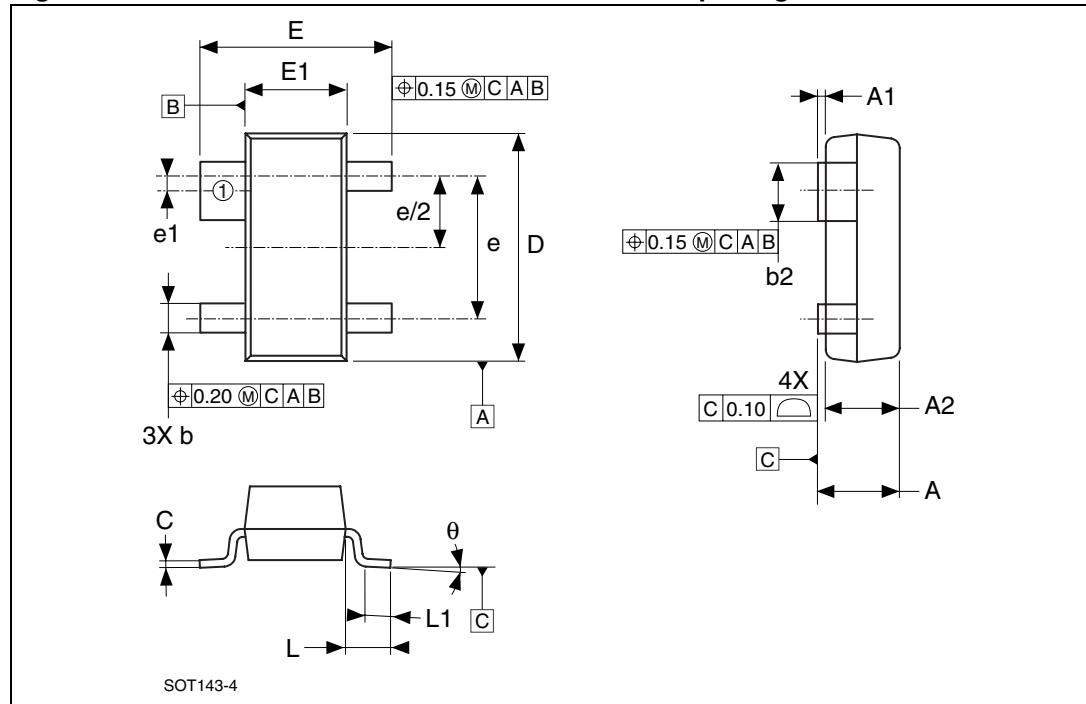
| Sym | Description | Test Condition ⁽¹⁾ | Min | Typ | Max | Unit |
|---------------------------|---|-------------------------------|--------------------|-----|--------------------|------|
| Manual Reset Input | | | | | | |
| V _{IL} | $\overline{\text{MR}}$ low input threshold | V _{RST} > 4.0V | 0.8 | | | V |
| | | V _{RST} < 4.0V | 0.3V _{CC} | | | V |
| V _{IH} | $\overline{\text{MR}}$ low input threshold | V _{RST} > 4.0V | | | 2.4 | V |
| | | V _{RST} < 4.0V | | | 0.7V _{CC} | V |
| | $\overline{\text{MR}}$ input pulse width | | 1 | | | μs |
| | $\overline{\text{MR}}$ glitch rejection | | | 100 | | ns |
| | $\overline{\text{MR}}$ -to- $\overline{\text{RST}}$ delay | | | 500 | | ns |
| | $\overline{\text{MR}}$ pull-up resistance | | 32 | 63 | 100 | kΩ |

- Valid for ambient operating temperature: T_A = -40 to 125°C; V_{CC} = 2.5 to 5.5V (except where noted).
- Other V_{RST} thresholds and t_{rec} timings are offered. Minimum order quantities may apply. Contact local sales office for availability.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. SOT143-4 – 4-lead small outline transistor package outline



Note: Drawing is not to scale.

Table 5. SOT143-4 – 4-lead small outline transistor package mechanical data

| Symbol | mm | | | inches | | |
|----------|------|------|------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | – | 0.89 | 1.12 | – | 0.035 | 0.044 |
| A1 | – | 0.01 | 0.10 | – | 0.001 | 0.004 |
| A2 | – | 0.88 | 1.02 | – | 0.035 | 0.042 |
| b | – | 0.37 | 0.51 | – | 0.015 | 0.020 |
| b2 | – | 0.76 | 0.94 | – | 0.030 | 0.037 |
| C | – | 0.09 | 0.18 | – | 0.004 | 0.007 |
| D | – | 2.80 | 3.04 | – | 0.110 | 0.120 |
| E | – | 2.10 | 2.64 | – | 0.083 | 0.104 |
| E1 | – | 1.20 | 1.40 | – | 0.047 | 0.055 |
| e | 1.92 | – | – | 0.076 | – | – |
| e1 | 0.20 | – | – | 0.008 | – | – |
| L | 0.55 | – | – | 0.022 | – | – |
| L1 | – | 0.40 | 0.60 | – | 0.016 | 0.024 |
| θ | | 0° | 10° | | 0° | 10° |
| N | | 4 | | | 4 | |

7 Part numbering

Table 6. Ordering information scheme

| Example: | STM6315 | R | D | W1 | 3 | F |
|---|---------|---|---|----|---|---|
| Device Type | | | | | | |
| STM6315 | | | | | | |
| Reset Threshold Voltage ⁽¹⁾ | | | | | | |
| L = $V_{RST} = 4.63V$ | | | | | | |
| M = $V_{RST} = 4.38V$ | | | | | | |
| S = $V_{RST} = 2.93V$ | | | | | | |
| R = $V_{RST} = 2.63V$ | | | | | | |
| \overline{RST} Pulse Width ⁽¹⁾ | | | | | | |
| A = $t_{rec} = 1.5ms$ | | | | | | |
| B = $t_{rec} = 30ms$ | | | | | | |
| D = $t_{rec} = 210ms$ | | | | | | |
| G = $t_{rec} = 1680ms$ | | | | | | |
| Package | | | | | | |
| W1 = SOT143-4 | | | | | | |
| Temperature Range | | | | | | |
| 3 = -40 to 125°C | | | | | | |
| Shipping Method | | | | | | |
| F = ECOPACK Package, Tape & Reel | | | | | | |

1. Other V_{RST} thresholds and t_{rec} timings are offered. Minimum order quantities may apply. Contact local sales office for availability.

Note: For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 7. Marking description

| Part Number | Reset Threshold ⁽¹⁾ (V) | RST Pulse Width ⁽¹⁾ (ms) | Output | Topside Marking ⁽²⁾ |
|-------------|---------------------------------------|--|------------------------------------|-----------------------------------|
| STM6315LB | 4.63 | 30 | Open drain $\overline{\text{RST}}$ | 9LBx |
| STM6315MD | 4.38 | 210 | Open drain $\overline{\text{RST}}$ | 9MDx |
| STM6315SD | 2.93 | 210 | Open drain $\overline{\text{RST}}$ | 9SDx |
| STM6315RA | 2.63 | 1.5 | Open drain $\overline{\text{RST}}$ | 9RAx |
| STM6315RB | 2.63 | 30 | Open drain $\overline{\text{RST}}$ | 9RBx |
| STM6315RD | 2.63 | 210 | Open drain $\overline{\text{RST}}$ | 9RDx |
| STM6315RG | 2.63 | 1680 | Open drain $\overline{\text{RST}}$ | 9RGx |

1. Other V_{RST} thresholds and t_{rec} timings are offered. Minimum order quantities may apply. Contact local sales office for availability.
2. Where "x" = Assembly Work Week (A to Z), such that "A" = WW01-02, "B" = WW03-04, and so forth.

8 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 14-Nov-2005 | 1.0 | First edition. |
| 08-Feb-2006 | 2.0 | Update template, characteristics, marking (Figure 7, 8, 9, 10, and 11; Table 4, 6, and 7). |
| 12-Apr-2006 | 3 | Updated characteristics (Figure 7, 8, and 11; Table 4, 6, and 7). |
| 27-Jul-2006 | 4 | Updated Table 3, 5 and 6. |
| 21-Mar-2007 | 5 | Updated Table 2, 6, and 7. |

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9